SWTW
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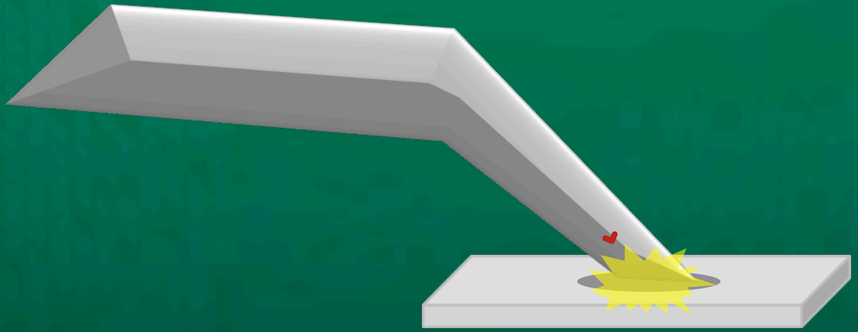
What Burns My Probes?



SanDisk®

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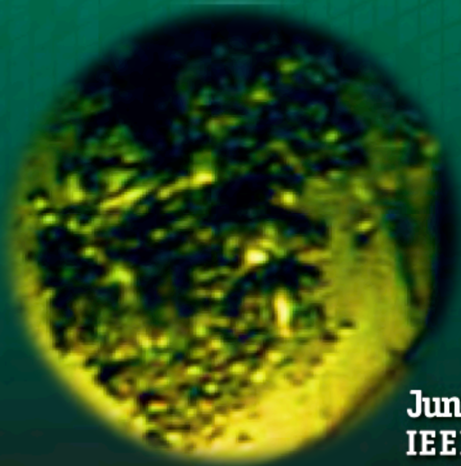
Background

- The ever growing need for a Known Good Die test dictates the execution of energy exhaustive tests at probe level.
- Normally, these energy exhaustive tests would be moved to the Final Test, which is less vulnerable to power stresses.
- Energies resulting from high currents may result in very high temperatures at the probe tip point and burn them.
- In this presentation, I would like to discuss arcing, the most influential source of the Burnt Tips problem . I will provide some insights on how it happens and guidelines on how to avoid it. I will try to answer the basic question:

What burns my probes?

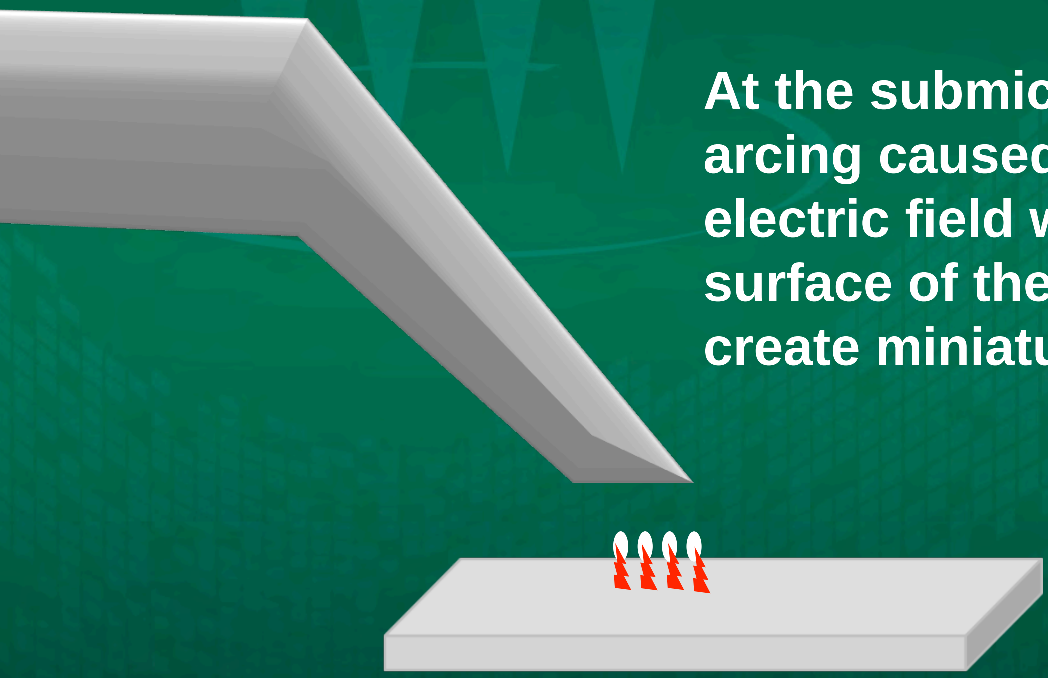


Agenda

- The Mechanism of the Probe Tip Contamination
- Increase in Temperature and Burning of the Tip
- Thermal Calculations of Burning Point of the Tip
- Empirical Experiment
- What Can Be Done?
- Conclusions
- Discussion

The Mechanism of the Probe Tip Contamination

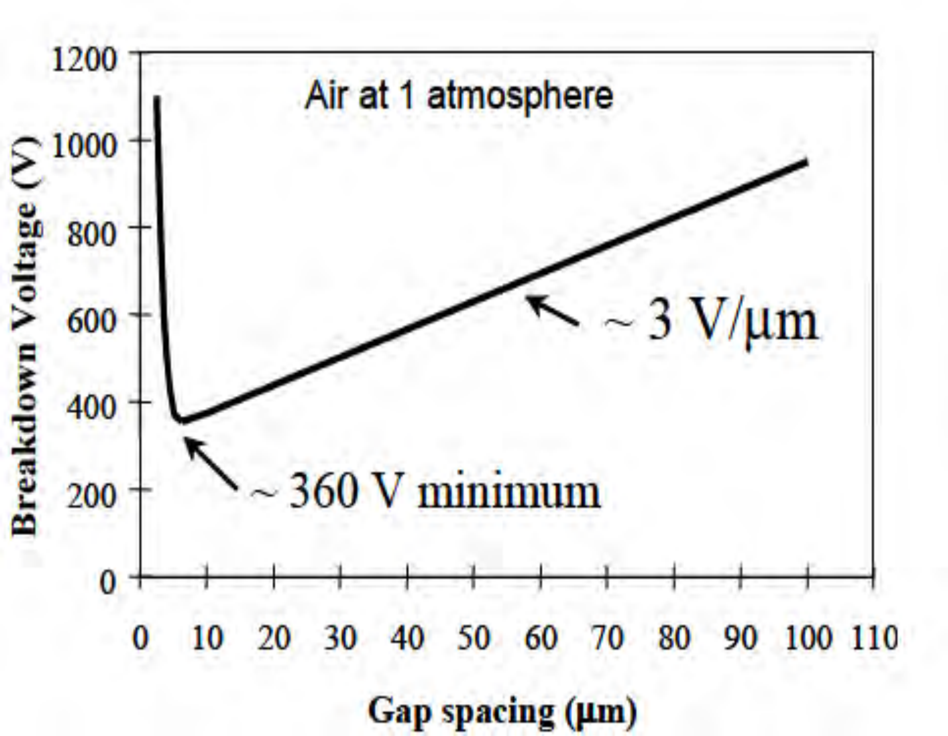
The following picture illustrates what is happening at the submicron gap between the probe and the pad, just before contact is made:



At the submicron gap, arcing caused by the electric field will melt the surface of the tip and will create miniature craters

What is arcing?

The Mechanism of the Probe Tip Contamination



Arcing is an electrical breakdown of gas which produces an ongoing plasma discharge and results in a current flow through normally nonconductive media such as air.

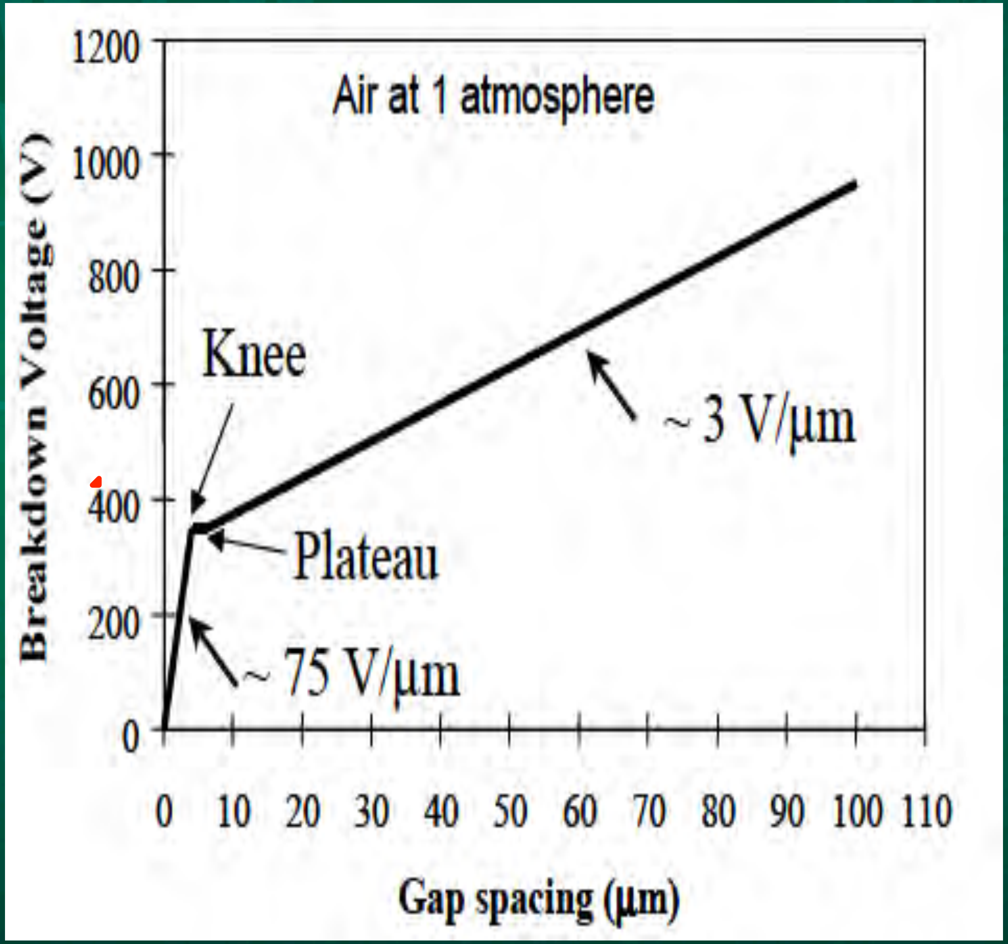
Paschen Curve represents breakdown voltage vs. gap between two conducting plates in the air.

Paschen Law states what one intuitively would say: that the higher the distance between two plates, the higher the voltage needed to cause a plasma discharge.

This however is not true for gaps lower than 5um. There, according to the law, voltage gaps higher than 360 V will cause arcing.

The Mechanism of the Probe Tip Contamination

However, at very small gaps, <5-7um, this rule does not apply. The breakdown here is caused by the field emission* and electrons tunneling** rather than the electrical breakdown of the gas.



Arcing caused by field emission and electron tunneling will happen at voltage differences below 1V at nm gaps.

The Mechanism of the Probe Tip Contamination

*Field emission:

….Field emission (FE) is the emission of electrons induced by an electrostatic field…. …FE can take place from solid or liquid surfaces, into vacuum, air, a fluid….it is most commonly an undesirable primary source of vacuum breakdown and electrical discharge phenomena, which engineers work to prevent. ….The theory of field emission from bulk metals was proposed by Ralph H. Fowler and Lothar Wolfgang Nordheim.[1] A family of approximate equations, "Fowler–Nordheim equations", is named after them. Strictly, Fowler-Nordheim equations apply only to field emission from bulk metals and (with suitable modification) to other bulk crystalline solids, but they are often used – as a rough approximation – to describe field emission from other materials….

** Tunnel Junction:

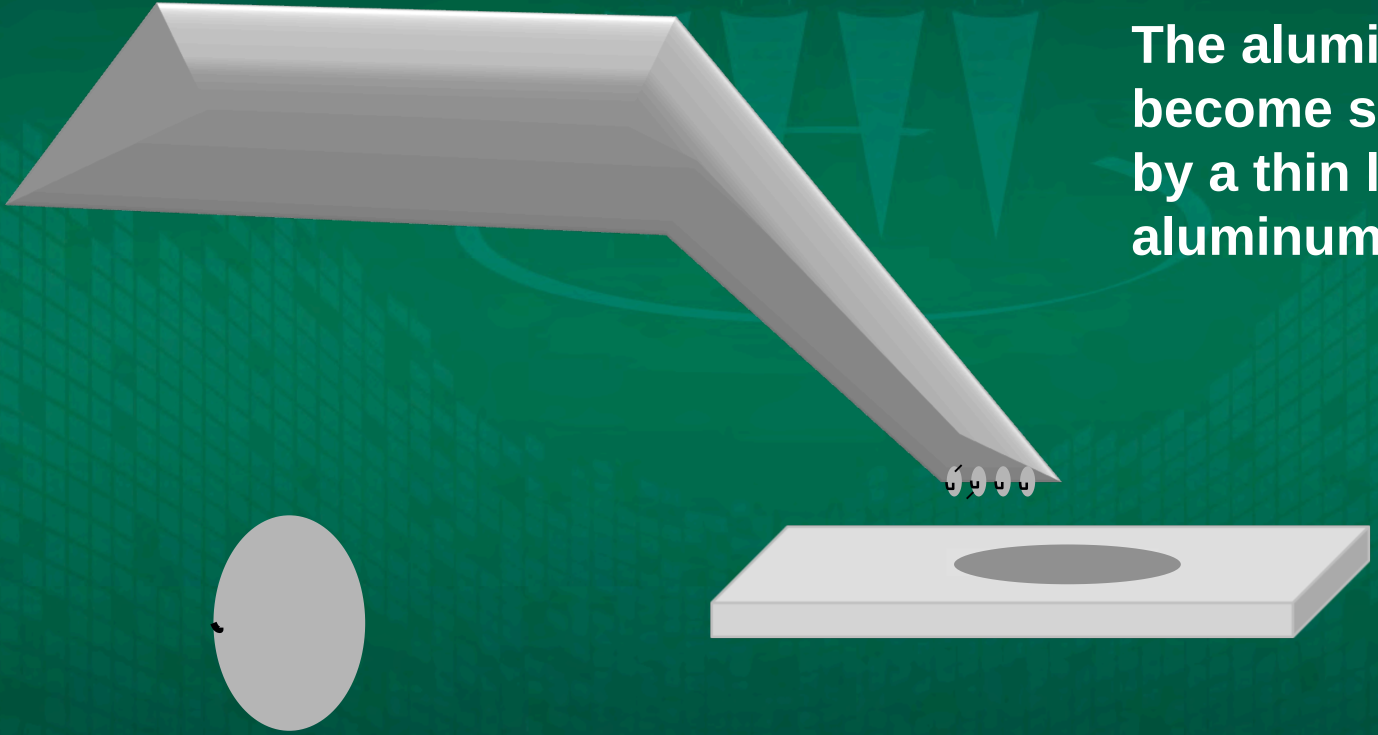
…..A tunnel junction is a barrier, such as a thin insulating layer or electric potential, between two electrically conducting materials. Electrons (or quasiparticles) pass through the barrier by the process of quantum tunneling. Classically, the electron has zero probability of passing through the barrier. However, according to quantum mechanics, the electron has a non-zero wave amplitude in the barrier, and hence it has some probability of passing through the barrier…..

The Mechanism of the Probe Tip Contamination

What happens?

Small particles of aluminum (Al) fill up the craters and stay stuck there after the probe disconnects from the pad

The Mechanism of the Probe Tip Contamination



The aluminum particles become soon covered by a thin layer of aluminum oxide (Al_2O_3)

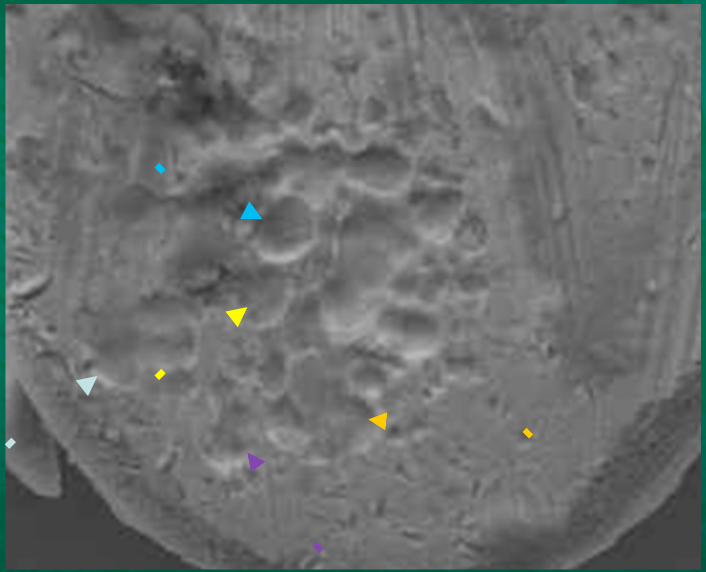
The Mechanism of the Probe Tip Contamination

This is how the probe tips look in reality under the optical microscope with magnification of X250

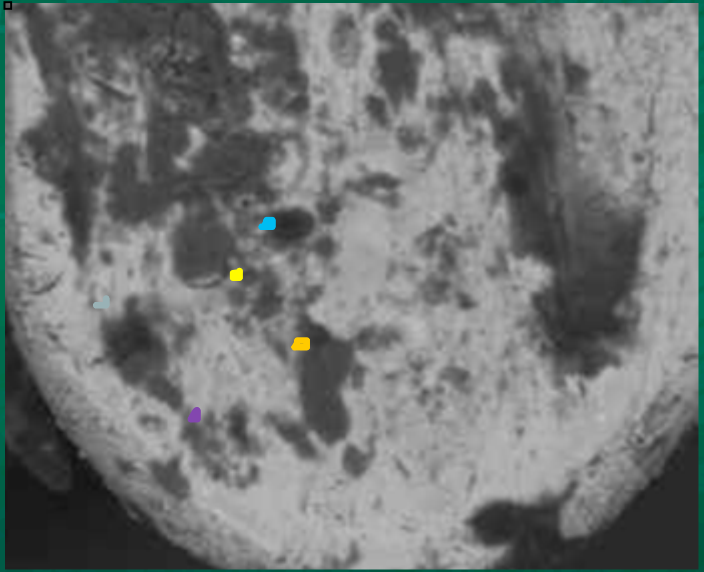
The Mechanism of the Probe Tip Contamination

Although it may look like it, this is not a picture of the Moon!

This is how the probe tip looks under the Scanning Electron Microscope.



SEM image showing small craters caused by micro-arcing on the probe tip.



Back scatter image showing aluminum debris filling into the same small craters.

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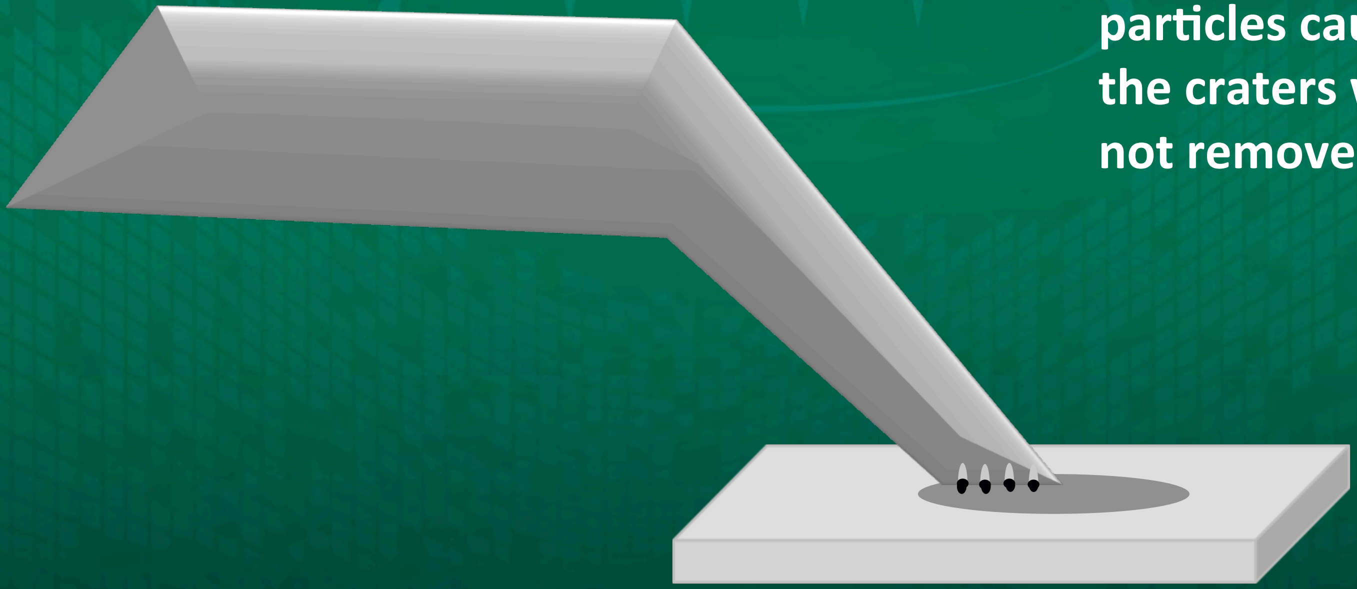
Increase in Temperature and Burning of the Tip

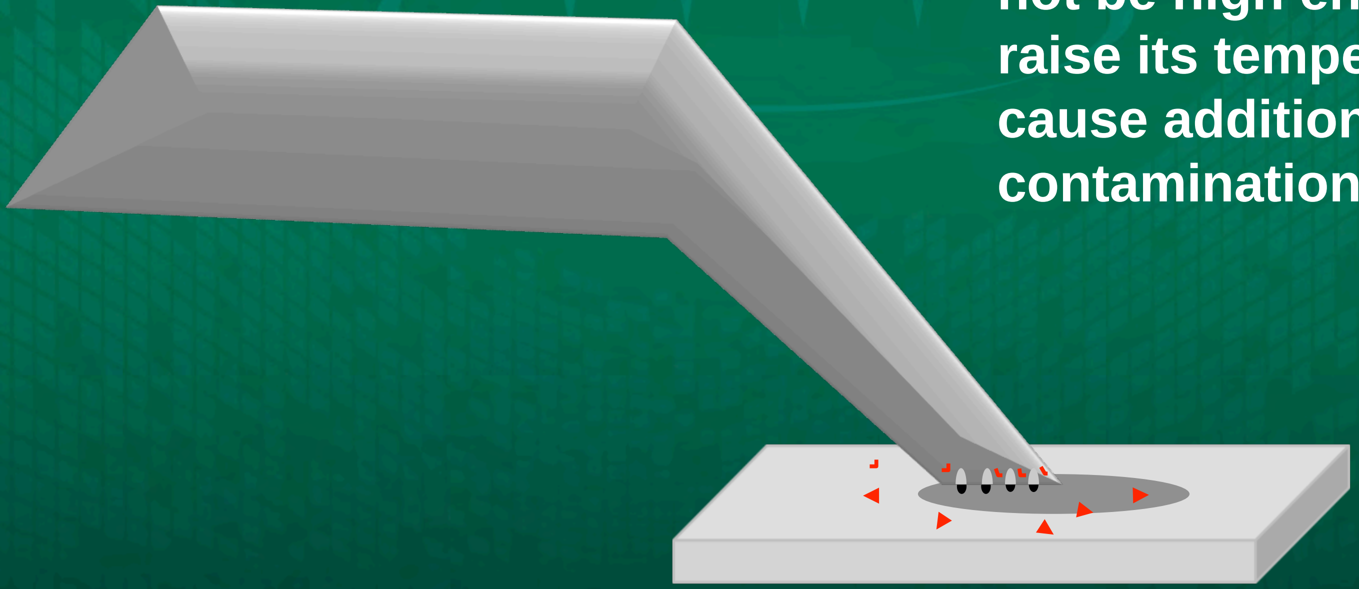
Normally, most of the accumulated debris will be cleaned out when the probe penetrates the thin and hard aluminum oxide layer. This is also called a self -cleaning effect.



However, oxidized particles caught in the craters will be not removed

Increase in Temperature and Burning of the Tip

Small currents will flow "easily" through the regions where the contact is still good and clean.

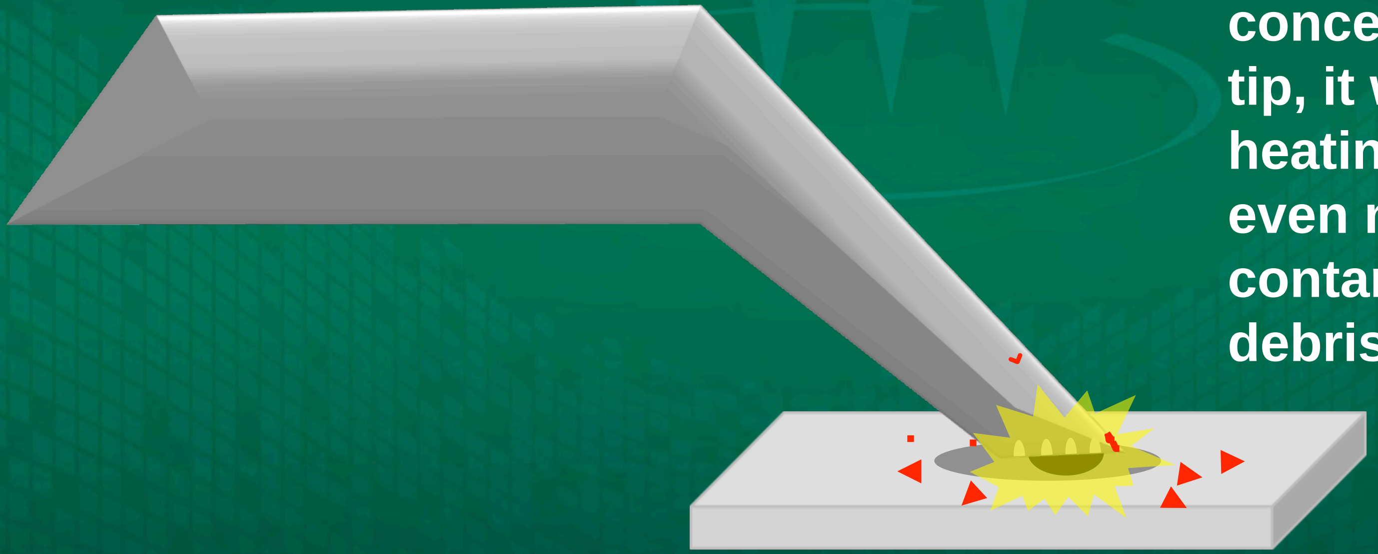


The power at the tip will not be high enough to raise its temperature and cause additional contamination or melting.

The probe will remain operational until it is permanently cleaned up by standard cleaning methods.

Increase in Temperature and Burning of the Tip

However, this is not the case with probes through which higher currents flow during the test. Since the effective (well conducting) tip area decreases due to accumulated nonconductive debris, current density and power at the tip point will increase.

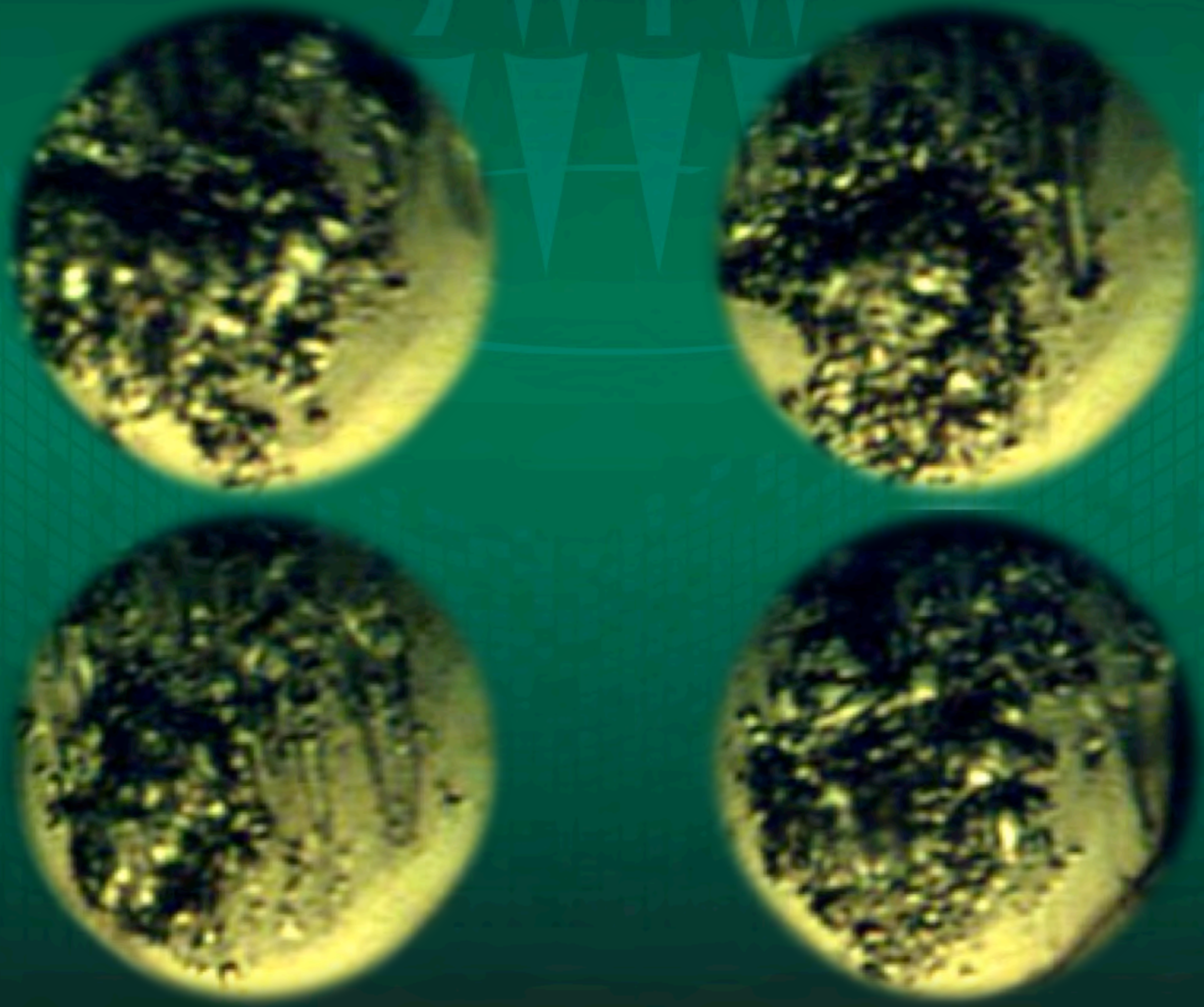


With high power concentration at the tip, it will start heating up causing even more contamination and debris.

This process will repeat and intensify with each landing until the entire tip is covered with nonconductive debris.

Increase in Temperature and Burning of the Tip

This is what may often happen to the tip through which high currents are forced:



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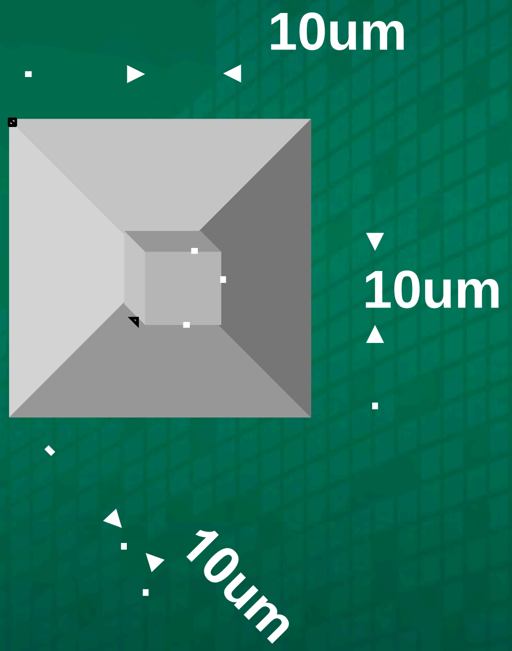
Thermal Calculations of Burning Point of the Tip

Let's try to quantify the problem…

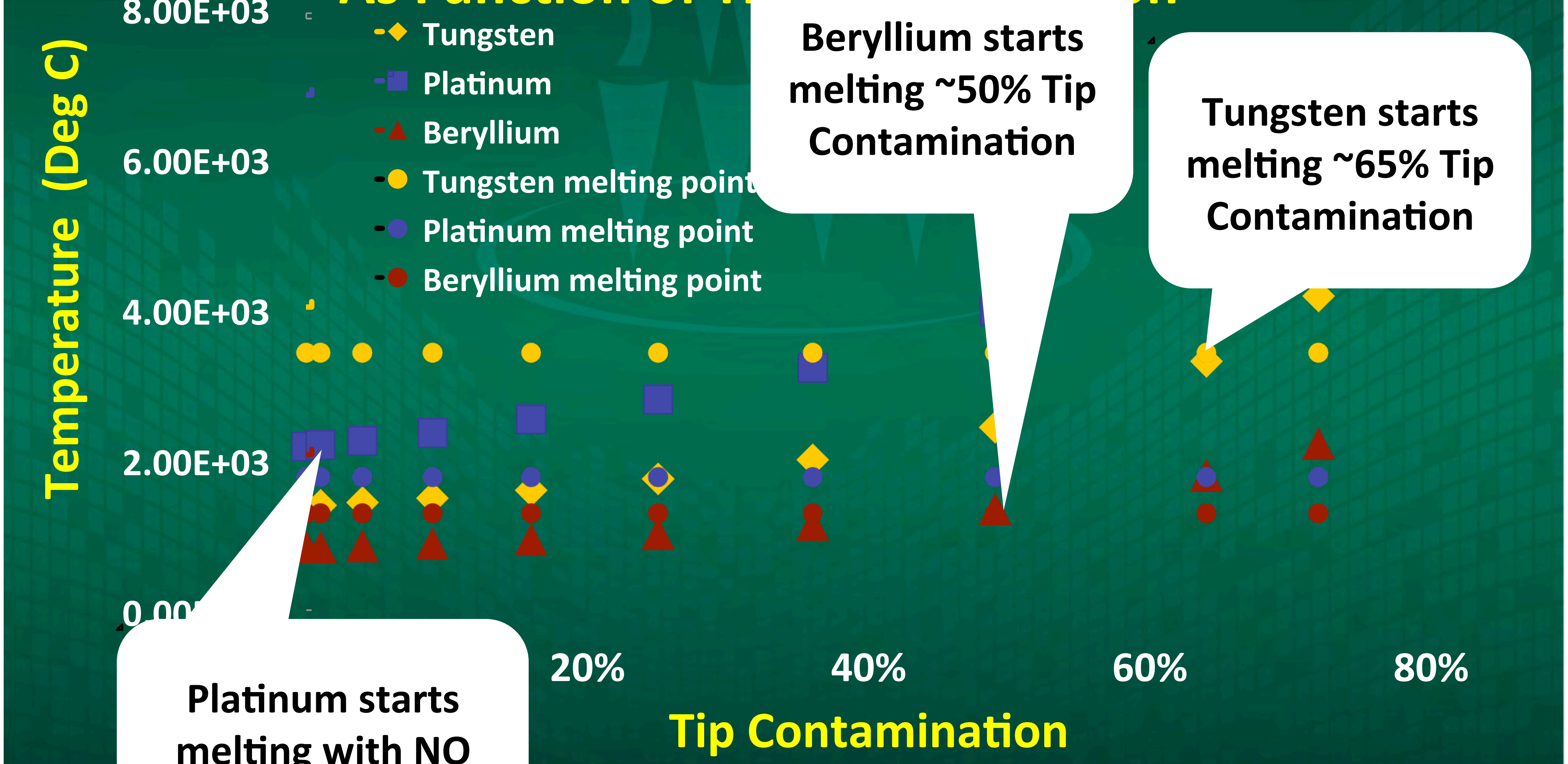
Assume a probe tip with the following properties:

1. The tip surface is 100um^2
2. The effective volume of the tip is 1000um^3
3. The tip contamination ranges between 0% and 100%
4. We have three tips made of; platinum (Pt), Beryllium (Be) and Tungsten (W)
5. The graph on the next slide shows to what temperature the tip will raise if a current of 100mA were driven through it for a period of 50msec



Tip Temperature Under the Stress of 0.1A/ 50ms

As Function of Ti on



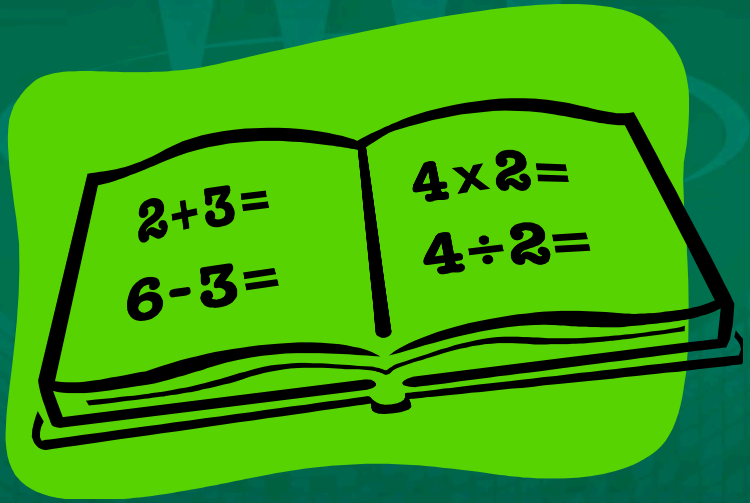
Beryllium starts melting ~50% Tip Contamination

Tungsten starts melting ~65% Tip Contamination

Platinum starts melting with NO Tip Contamination

Thermal Calculations of Burning Point of the Tip

The calculations are presented on the following two hidden slides:



Thermal Calculations of Burning Point of the Tip

The probe tip temperature calculation is based on three basic equations:

Eq1. $Q = P * t$,

Eq2. $Q = M * C * deltaT$,

Eq3. $P = I^2 * R$

Q – energy	[Joule]
P – Power	[Watt]
t – time	[sec]
M – mass	[gr]
C – heat capacity	[Joul/(gr*Kelvin)]
T – Temperature	[Kelvin]
R – Resistance	[ohms]

By substitution we will find that:

Eq4. $T(deg\ C) = 300 + ((P * t) / (M * C))$

Thermal Calculations of Burning Point of the Tip

The following are basic properties of the relevant materials, either calculated or taken from the tables:

Property	name	Tungsten	Platinum	Beryllium	units
resistivity		5.59E-08	1.06E-07	3.60E-08	ohm meter
R	resistance	5.59E-03	1.06E-02	3.60E-03	ohm
P	Power	5.59E-05	1.06E-04	3.60E-05	w
D	Density	1.93E+07	2.15E+07	1.85E+06	gr/m cube
M	mass	1.93E-08	2.15E-08	1.85E-09	gr
C	heat capacity	0.134	0.132	1.82	Joul/(gr*Kelvin)
melting point		3422	1768	1287	DegC

Note: It is important to remember that in reality, due to power dissipation to the air and to the probe, the temperatures will not raise that fast. Nevertheless, the graph is believed to be very close to reality.

Using Eq4, a tip temperature was calculated as function of changing percentage of tip contamination (x axis) while driving through it 100mA for the period of 50ms.

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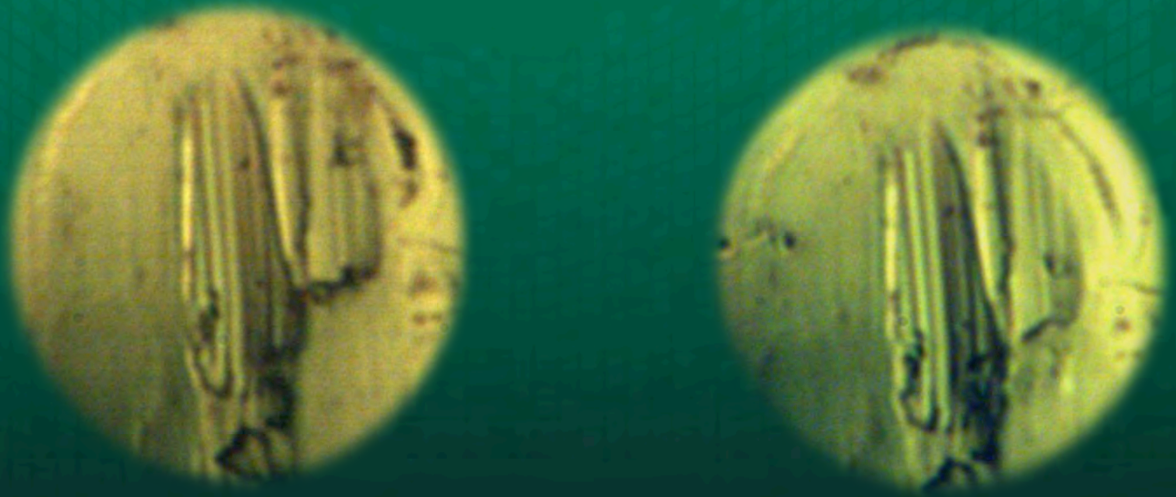
Empirical Experiment

An empirical experiment was performed to prove the theory and to show how the contamination increases when the probes step over the wafer and high currents flow over them during the test. In this experiment, after each step 200mA current was sourced through the probe for a period of 100 msec.

Initially, the probe tips were cleaned and the test was executed 1740 times <u>without</u> any stepping. The probe tip was examined before the first test and after the test 1740.

No contamination was observed as shown below:



Before

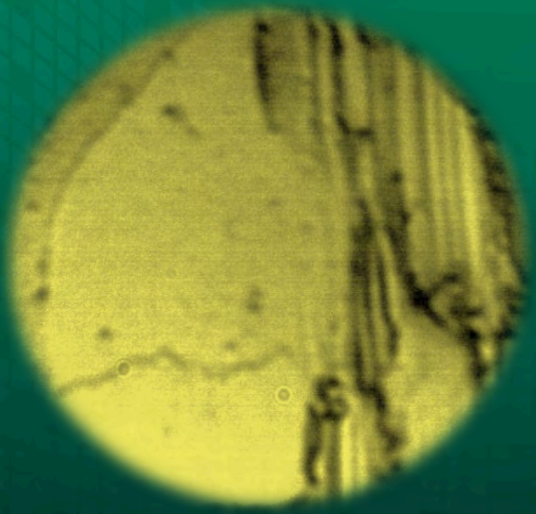
After

Empirical Experiment

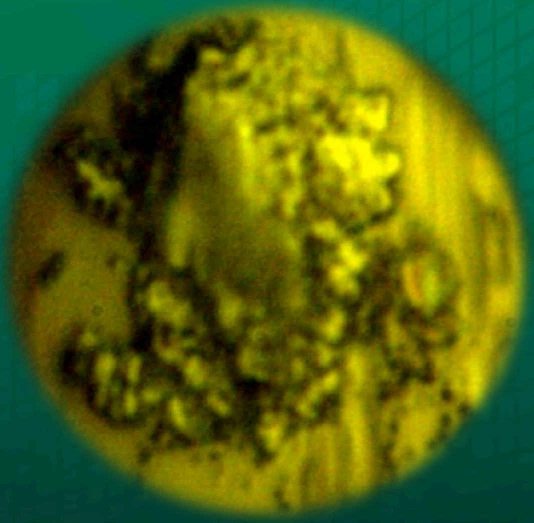
Then we stepped 1740 times over the wafer while sourcing 200mA of current per each step for a period of 100 msec. The probe tip was examined before the first test and after the test 1740.

Severe contamination was observed as shown below:

Before

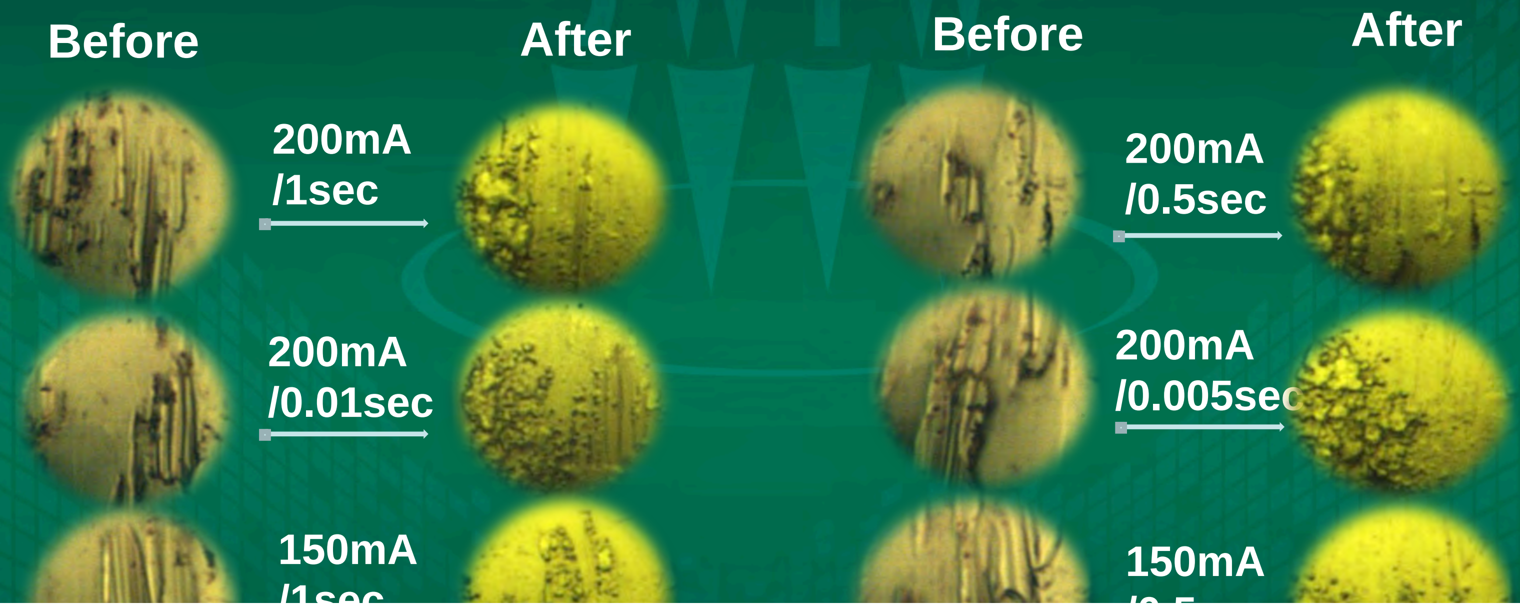


After



Empirical Experiment

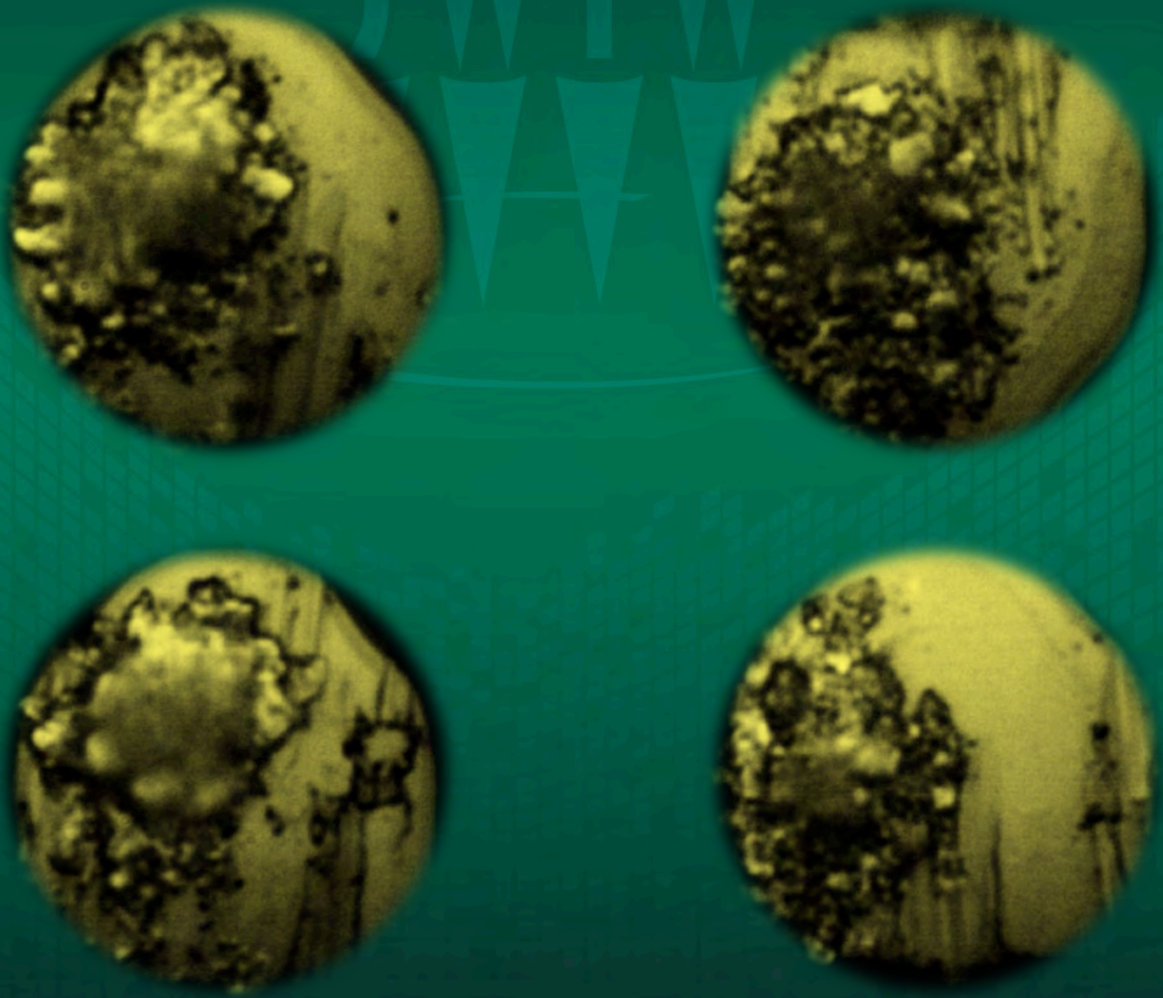
Images of different probes were taken before and after stepping over the full wafer, while imposing a different current stress per each step :



Note that no particular correlation exists between the level of contamination and the level of energy applied to the probe during the test. The source of the contamination is arcing, which is independent of the test. Because there was still enough "good" contact, current density was not high enough to raise the temperature and burn the probes.

Empirical Experiment

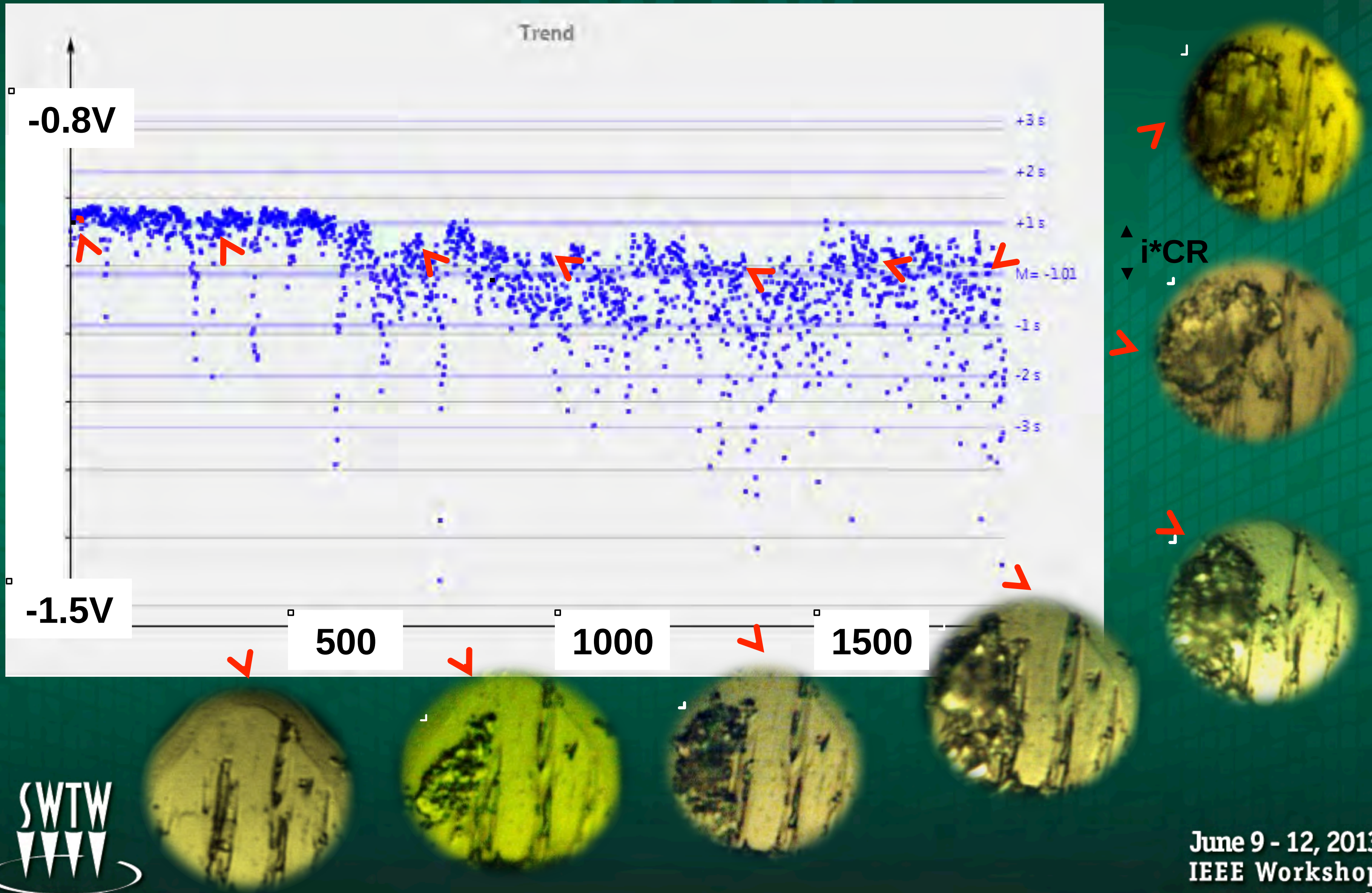
Yet, not all probes were that “lucky”, some of them started melting..:



Empirical Experiment

- **Let's now observe what happens to the probe tip when we step over the wafer, execute the test per every step and monitor tip contamination per every 290 steps**
- **Increase in CR is represented by the increase in the voltage drop**
- **1740 steps on the wafer were executed while sourcing 200mA through the probe per every step for 1 sec**
- **Observations (next slide):**
    - Cr increased by ~0.4ohm in average after 1740 landings
    - Because of the degrading contact quality, in some landings the increase in CR is as much as 1-1.5ohm

Empirical Experiment



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What Can Be Done?

- **The following list summarizes some recommendations presented in detail on the next hidden slides (due to time constraints)**
- **Execution of these recommendations will contain, if not eliminate, the problem of burnt probe tips:**

1. Lowering current by distribution via multiple pads

   As a common practice, the current flowing through one probe should never exceed 100mA whether DC, AC or momentary

2. Discharging all capacitors on the board at the end of the Test Program Flow

3. Eliminating high current sources on the DIB

   Currents that flow through the probe tip can be in magnitude higher than those that the Power Supplies can provide

What Can Be Done?

4. Monitoring and eliminating current spikes
   - Support infrastructure should be prepared up-front

6. Reduction of the impact of other sources of currents:

   - Power ON/OFF sequences,
   - Power Contentions between the DUT outputs and the Tester resources,
   - Tester resources changing ranges,
   - Hot switching,
   - Oscillations,
   - Current loads during test,
   - Other

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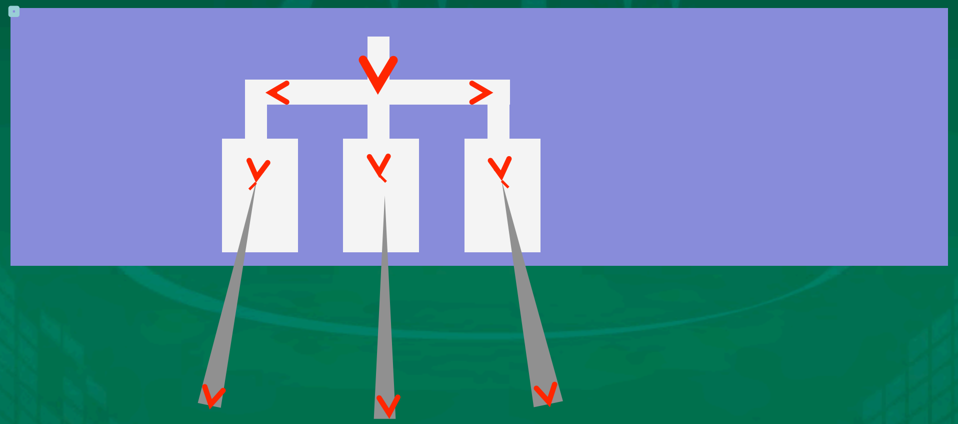
What Can Be Done?

Lowering current by distribution via multiple pads:



Comments:

- Negotiations with the Design Teams may be required
- The cost of the final product may increase
- As a common practice, the current flowing through one probe should not exceed 100mA whether DC, AC or momentary

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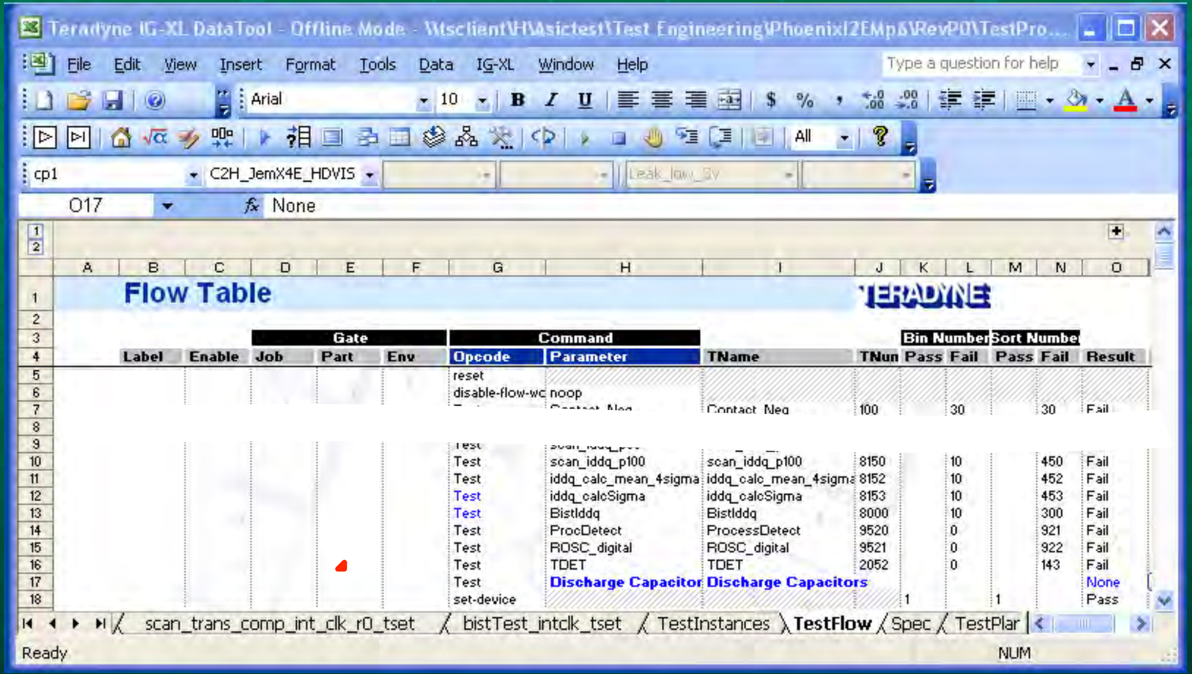
What Can Be Done?

Discharging capacitors at the end of the Test Program Flow

Tips:

- Avoid landing on the pads of the next die with probes connected to charged capacitors
- Make sure all capacitors are discharged to 0V
- Use FVMI modes
- Make sure the routine is also executed on sites that failed



Flow Table

		Gate			Command				Bin Number		Sort Number		
Label	Enable	Job	Part	Env	Opcode	Parameter	TName	TNum	Pass	Fail	Pass	Fail	Result
					reset								
					disable-flow-wc	noop							
					Test	Contact_Neg	Contact_Neg	100		30		30	Fail
					Test	[illegible]							
					Test	scan_iddq_p100	scan_iddq_p100	8150		10		450	Fail
					Test	iddq_calc_mean_4sigma	iddq_calc_mean_4sigma	8152		10		452	Fail
					Test	iddq_calcSigma	iddq_calcSigma	8153		10		453	Fail
					Test	BistIddq	BistIddq	8000		10		300	Fail
					Test	ProcDetect	ProcessDetect	9520		0		921	Fail
					Test	ROSC_digital	ROSC_digital	9521		0		922	Fail
					Test	TDET	TDET	2052		0		143	Fail
					Test	**Discharge Capacitor**	**Discharge Capacitors**						None
					set-device				1		1		Pass

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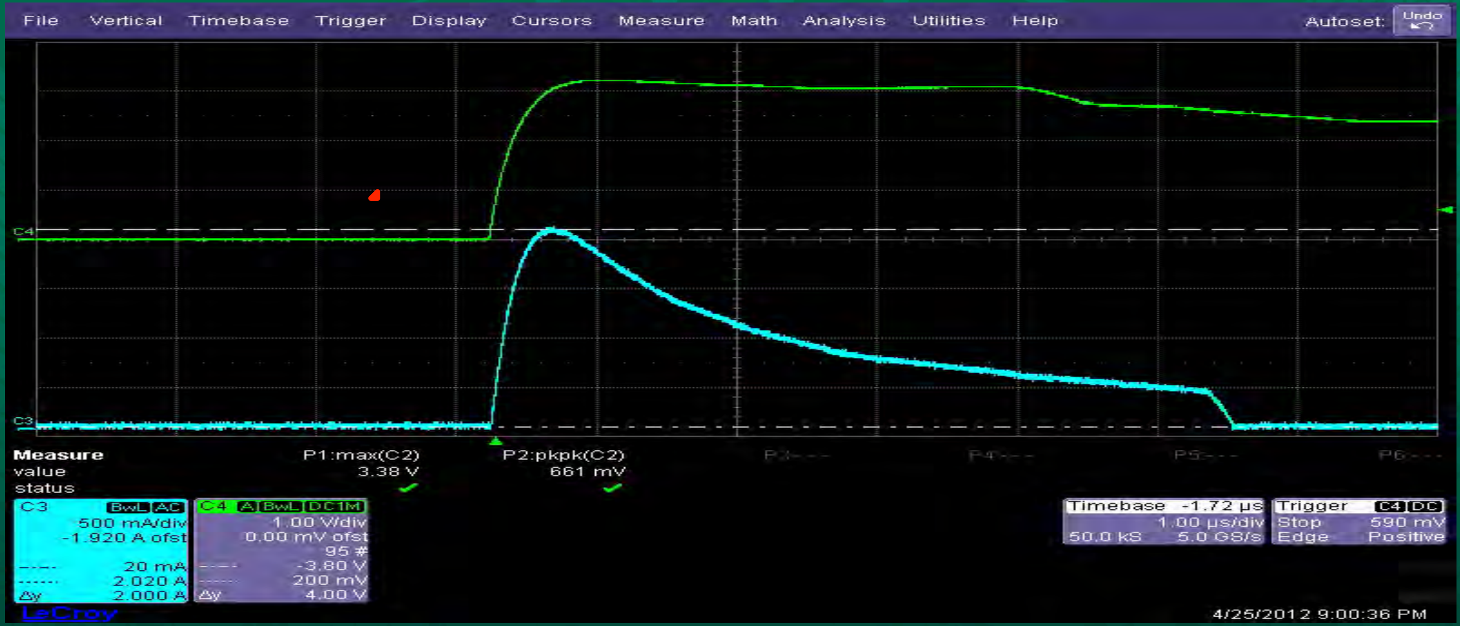
What Can Be Done?

Eliminating high current sources on the DIB

Bear in mind that currents that flow through the probe tip can be higher than those that your Power Supplies can provide

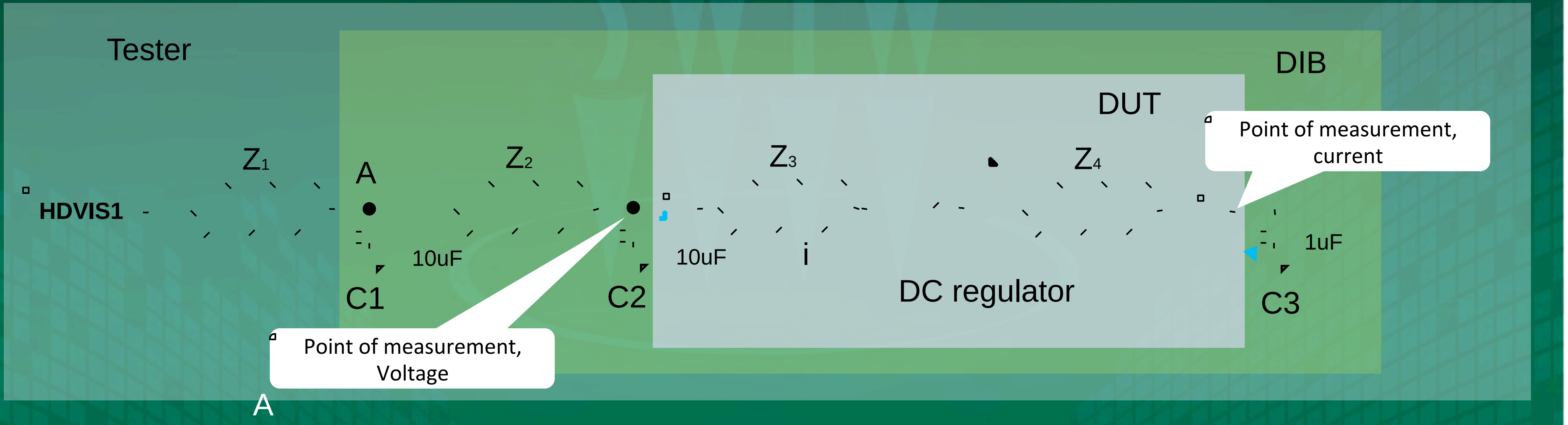
Example: the following was observed on the J750, HDVIS based system, (max current is 200mA):



A current of 2A was read on the Power Supply output pads. How is it possible?

What Can Be Done?

Eliminating high current sources on the DIB - explanation:



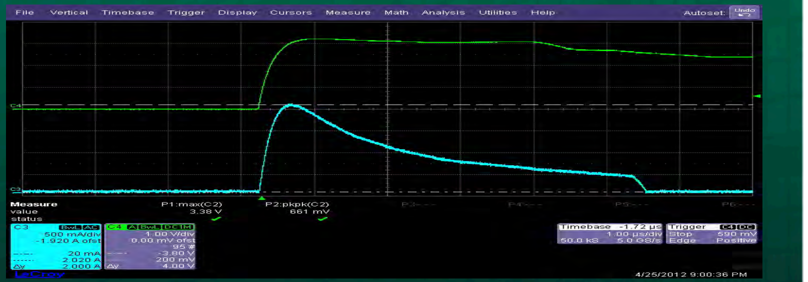
Initially HDVIS1 turns ON and charges capacitors C1 and C2. DC regulator is in a high Z state. C3 is not charged.

At a certain threshold level the DC Regulator turns into a bypass mode state:

Since:

$Z_{1,} Z_2 >> Z_{3,} Z_4$

Capacitor C3 is loaded from capacitor C2: the current i is very high since Z_3 and Z_4 are very small and $C_3 << C_2$.



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  - Lowering Current by distribution via multiple pads
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  - **Monitoring and eliminating Current spikes**
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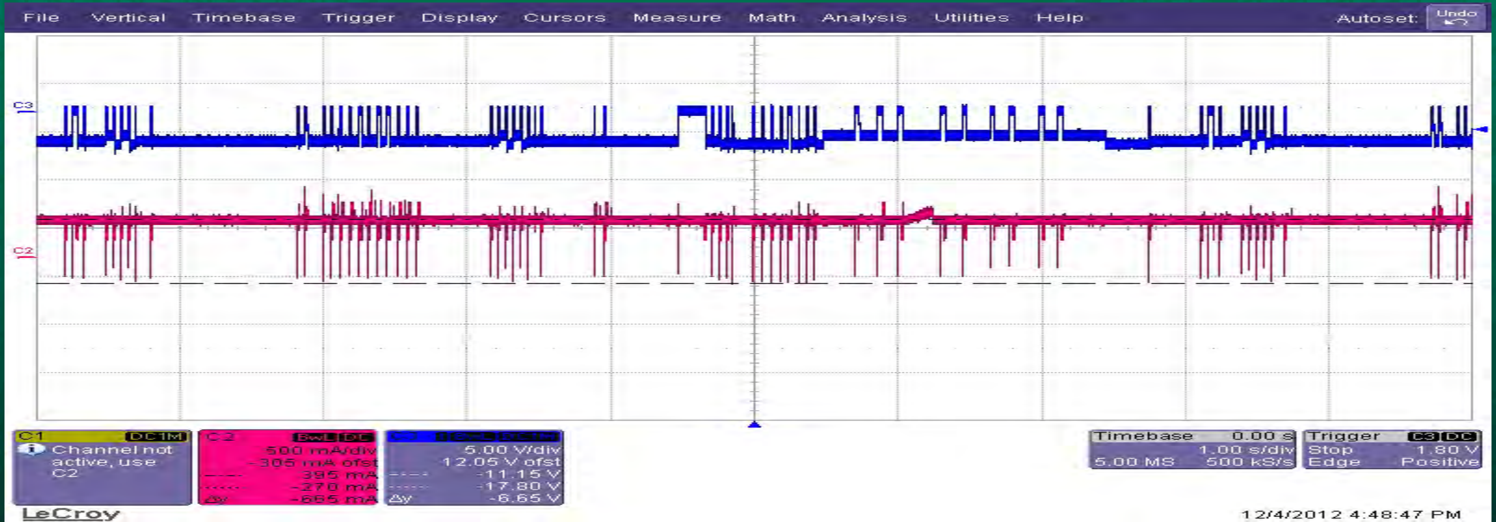
What Can Be Done?

Monitoring and eliminating current spikes

Other sources of current spikes might be:

- **Power ON/OFF sequences,**
- **Power Contentions between the DUT outputs and the Tester resources,**
- **Tester resources changing ranges,**
- **Hot switching,**
- **Oscillations,**
- **Current loads during test,**
- **Other**

There will be many current spikes during the Test flow execution:



C1 DC1M
Channel not active, use C2

C2 BwL DC
500 mA/div
-305 mA ofst
395 mA
-270 mA
Δy -665 mA

5.00 V/div
12.05 V ofst
-11.15 V
-17.80 V
Δy -6.65 V

Timebase 0.00 s
1.00 s/div
5.00 MS 500 kS/s

Trigger C3 DC
Stop 1.80 V
Edge Positive

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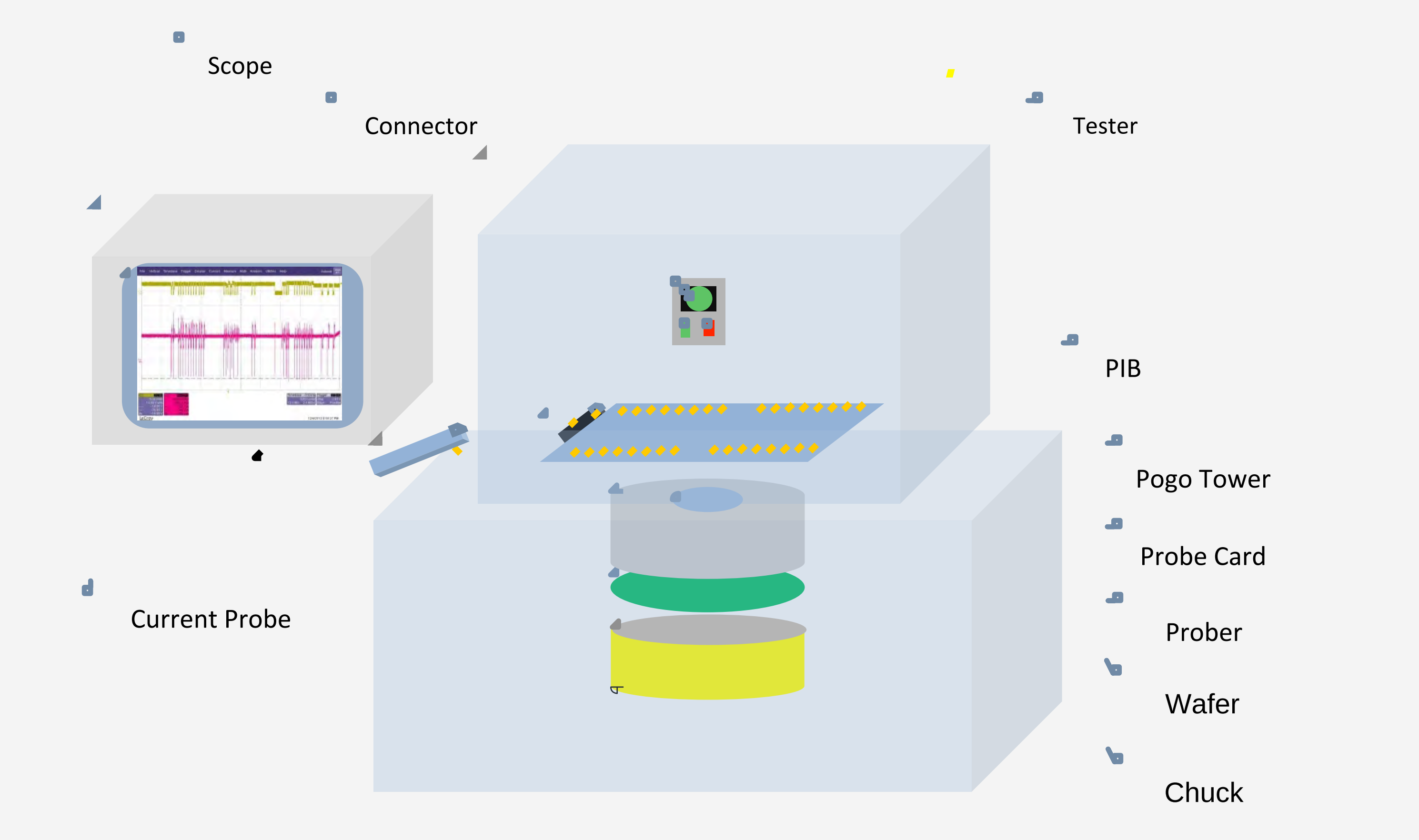
What Can Be Done?

Have your Test Infrastructure ready to monitor current spikes and eliminate them



What Can Be Done?

After getting the infrastructure in place, strive to eliminate current spikes

C1 DC1M
5.00 V/div
11.30 V ofst
-8.70 V
-20.20 V
Δy -11.50 V

C2 BwL DC
200 mA/div
-900.0 mA
1.004 A
544 mA
Δy -460 mA

Timebase -310 ms
500 ms/div
12.5 MS 2.5 MS/s

Trigger C1 DC
Stop 4.15 V
Edge Positive

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C1 DC1M
5.00 V/div
11.30 V ofst
-20.20 V
-17.45 V
Δy 2.75 V

C2 BwL DC
200 mA/div
-900.0 mA
544 mA
654 mA
Δy 110 mA

Timebase -310 ms
500 ms/div
12.5 MS 2.5 MS/s

Trigger C1 DC
Stop 4.15 V
Edge Positive

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It can be done!!

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Conclusions

- Probe Tips contamination cannot be avoided as it is caused by submicron arcing and non conductive debris buried in the craters.

- Currents smaller than 200mA, can melt contaminated probe tips easily because of high current density at the probe tip.

- By implementing of proper precautions the problem can be contained and minimized.

Discussion

Thank you!