



IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

June 9 - 12, 2013 | San Diego, California

Analyzing probe card scrub margin

or

“Are all of these probes really going to hit all of these pads?”



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FormFactor, Inc.

Analyzing/Predicting Scrub Margin

- What is scrub margin?
- How is scrub capability determined?
- What parameters determine scrub capability?
- Why not simply specify the key parameters?
- What types of analysis methods or tools are appropriate?
- How can I best use my existing tools?
- Summary

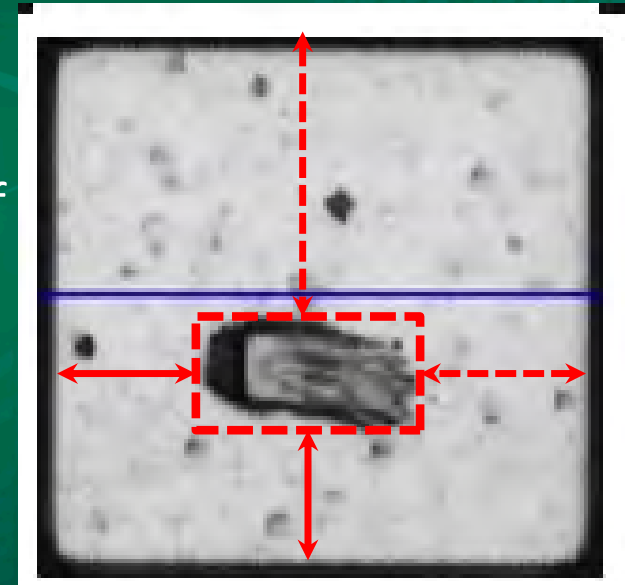


Scrub Margin

- **Start simple**

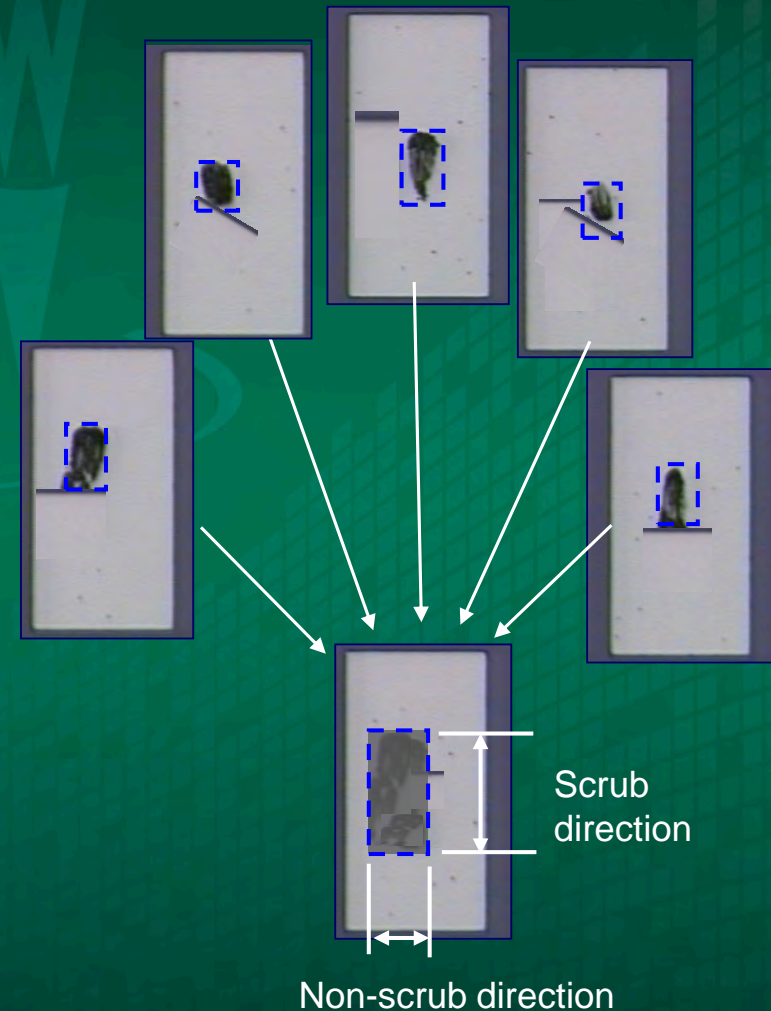
- Bond pad and a scrub mark
 - Include “prow” pushed to front and “furrow” pushed to side
 - Bounding box around the overall mark
 - Distance from left, right, top, and bottom of bounding box to left, right, top, and bottom edge of pad respectively
 - Capture and quantify the scrub mark size and position for aggregate analysis

Scrub margin is minimum distance in scrub and non-scrub directions to pad edge



Super Position of Scrub Marks

- **Collective measurement and consolidation of scrub marks**
 - Capture and quantify scrub size and position on all marks
 - Superimpose those marks onto a single virtual pad
 - Bounding box around superimposed scrub marks



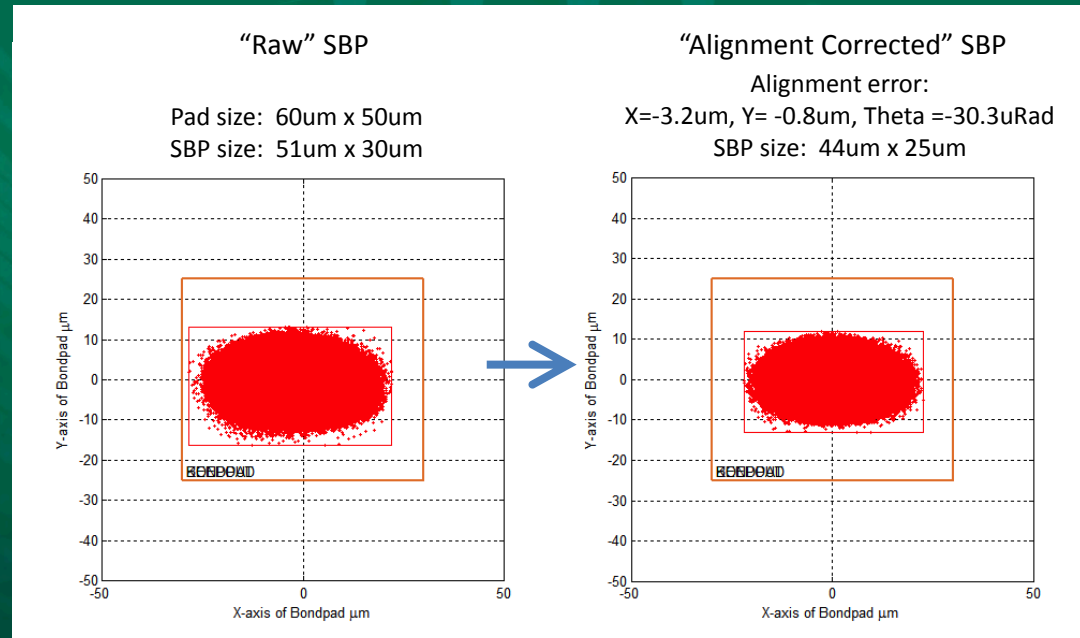
“Super Bond Pad”

Separating Probe Card from Prober

- Quantify and remove probe card to wafer alignment error
 - Have a “raw” SBP at this point
 - Need to mathematically compute the average X, Y, and Theta error and recalculate each mark to determine probe card capability

Graphical representation and superposition of each mark as an oval

- Major axis = Scrub Length
- Minor axis = Scrub Width



Scrub margin impact of 3-4um due to theta error

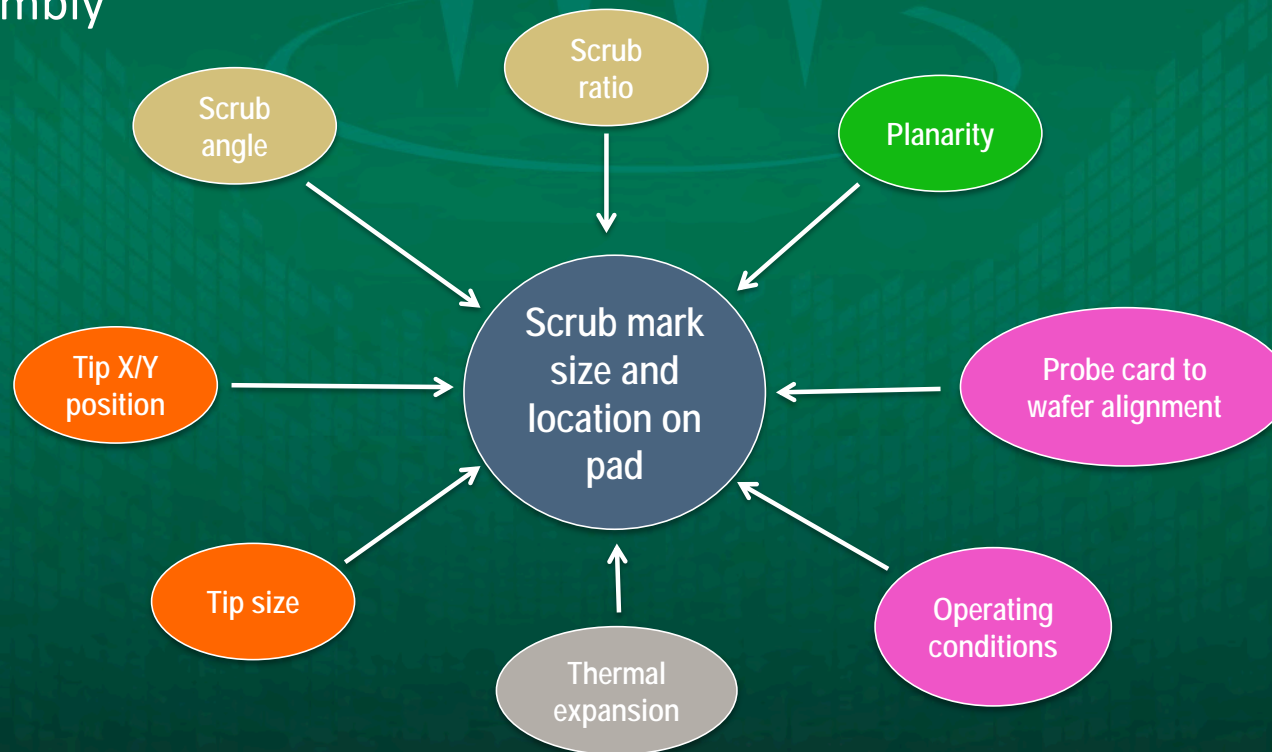
If operating conditions are correct, the alignment corrected SBP is an accurate measure of *probe card scrub capability*



Key Parameters

Scrub Mark Size and Location

- **Critical factors in determining where the probe mark is on the pad, how long, and how wide**
 - Grouped by application, design, intrinsic properties, manufacturing and assembly



Probe Card Allowances (or Allocation)

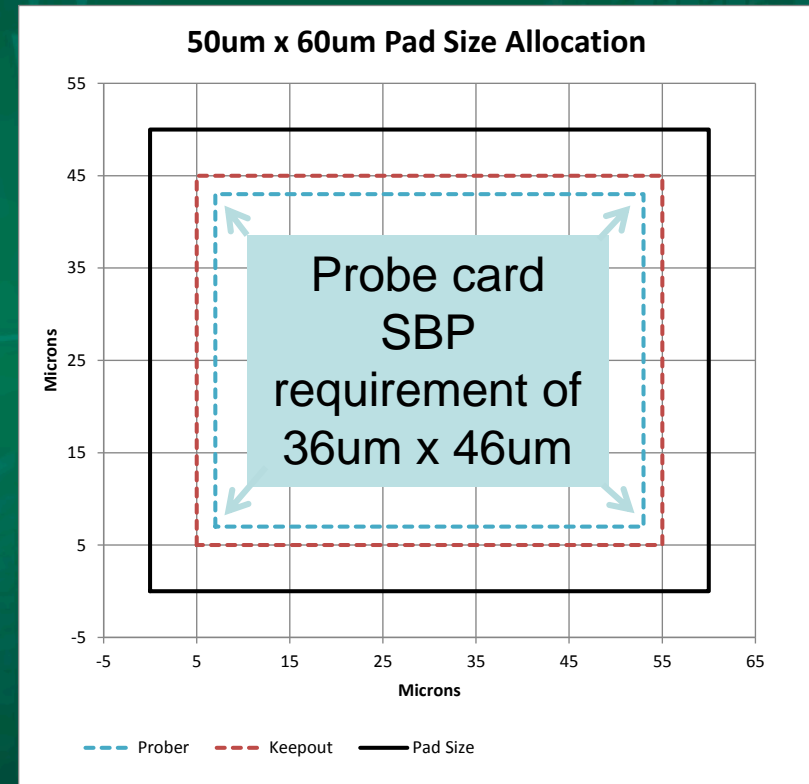
50 x 60um pad size example

- **Keepout**

- Defines portion of the pad available for scrub mark
 - Scrub marks should be contained within the keepout boundary

- **Prober Alignment**

- Budget for prober alignment tolerance
 - Should be sufficient such that the “as probed” wafer does not have scrub marks within the keepout area



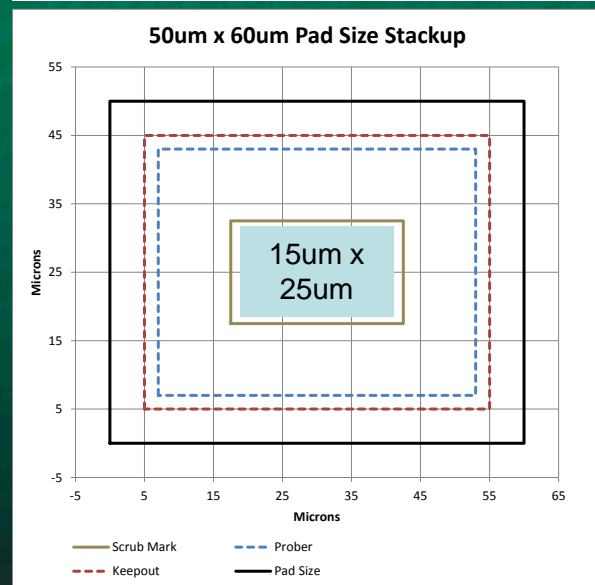
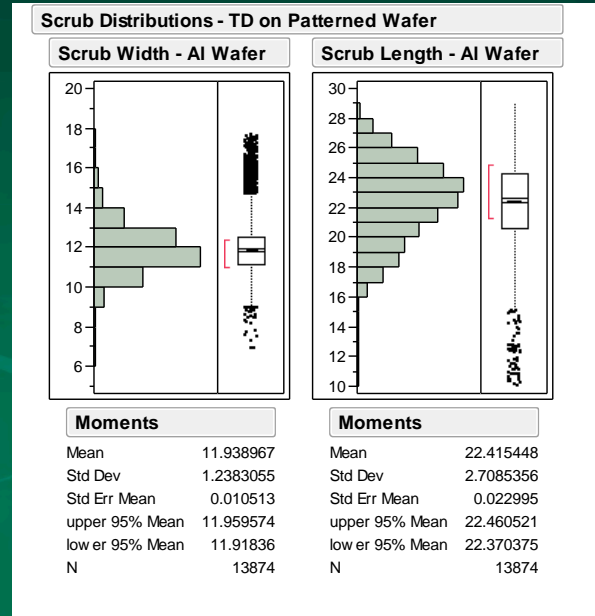
Tolerance Stack Up Approach

- **Scrub mark width**

- Composite spec of tip size and nominal over travel/scrub length
- For simplification, will use:
 - Scrub mark width of 15um

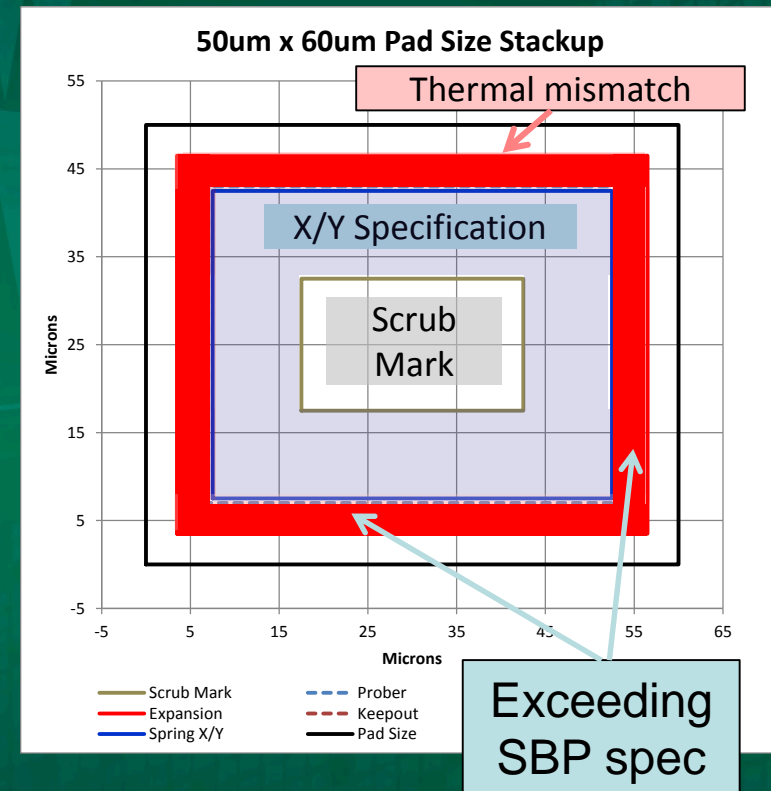
- **Scrub mark length**

- Based on expected scrub length, scrub ratio, over travel
- For simplification, will use:
 - Scrub mark length of 25um
 - 80um OT x scrub ratio + ½ of planarity spec equals 22um



Tolerance Stack Up Approach

- **Scrub mark X/Y position**
 - Composite of tip position, scrub ratio, planarity, and other factors
 - For simplification, will use:
 - X/Y alignment specification of +/-10um
- **Thermal expansion/contraction**
 - X/Y position measurements generally taken at room temperature conditions
 - Actual operating conditions have some thermal mismatch
 - Use +/-25ppm or ~ 4um in this case



Tolerance stack up exceeds SBP requirement by 7um

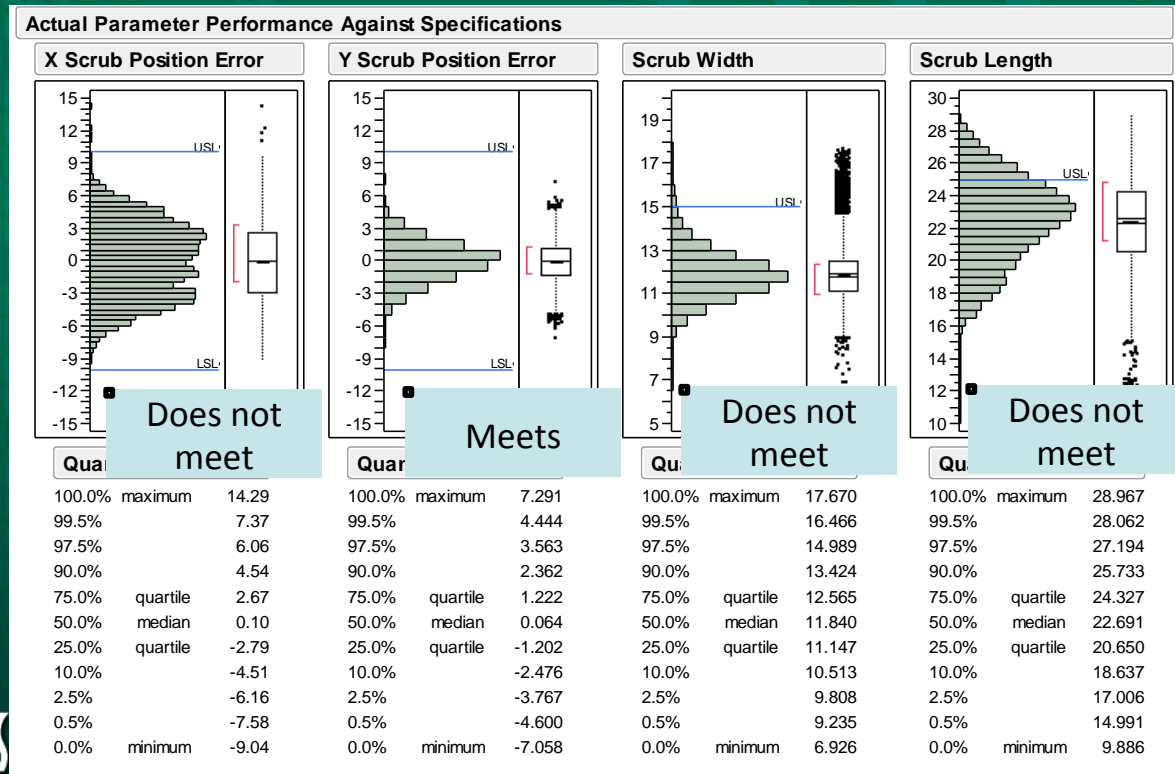
43 x 53um against 36 x 46um requirement



Tolerance Stack Up vs. Actual

- **Distributions vs. specifications**

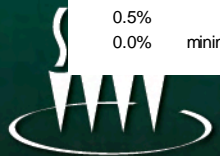
- First pass assessment of actual positional data for selected key parameters against specifications



- Three of four key parameter distributions not meeting tolerance stack up specifications
- Can choose to drive improvement efforts on individual specifications

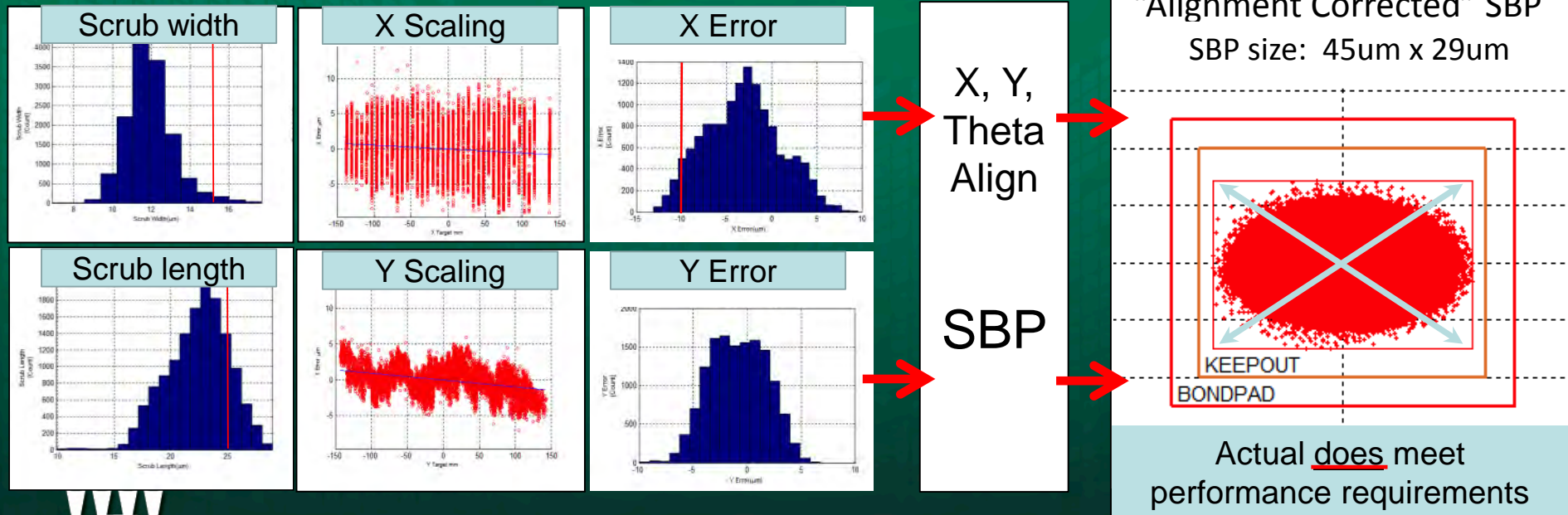
Or

- Can assess aggregate product performance and requirements through an SBP approach



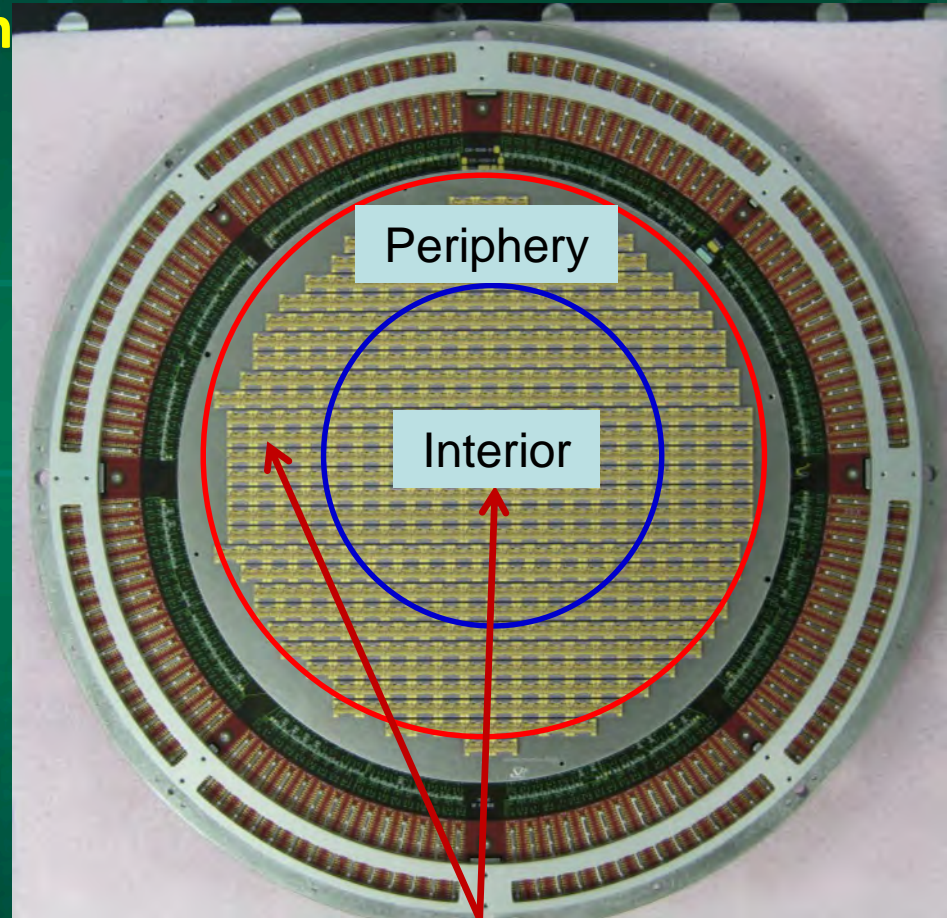
Scrub Capability Approach

- **Integrated assessment of scrub capability**
 - Assess *actual* scrub margin performance
 - Alignment corrected SBP from aggregate parameter data
 - Actual performance meets requirements
 - 8 -14um different than tolerance approach



Issues with Tolerance Stack Up Approach

- **Uniform specification approach is not appropriate**
 - Not all probe card areas are equal
 - Interior array performance requirements are less stringent than periphery
 - Over spec/under spec risk and cost implications with uniform specification approach
 - Worst case performance on multiple parameters is unlikely
- **SBP approach integrates all of the critical requirements and assures against worst case**



Different requirements for the probe card depending on location in the array



– *Why over spec?*

– *Why double spec?*

Methods and Approaches

- **Probe card measurement tooling considerations**

- What if I don't have a wafer and/or prober?
- Multiple types of probe card metrology tools can be used
 - Key is to understand probe card metrology measurement mechanism and determine correlation to actual scrub mark size and location

- **Correlation considerations for probe card metrology**

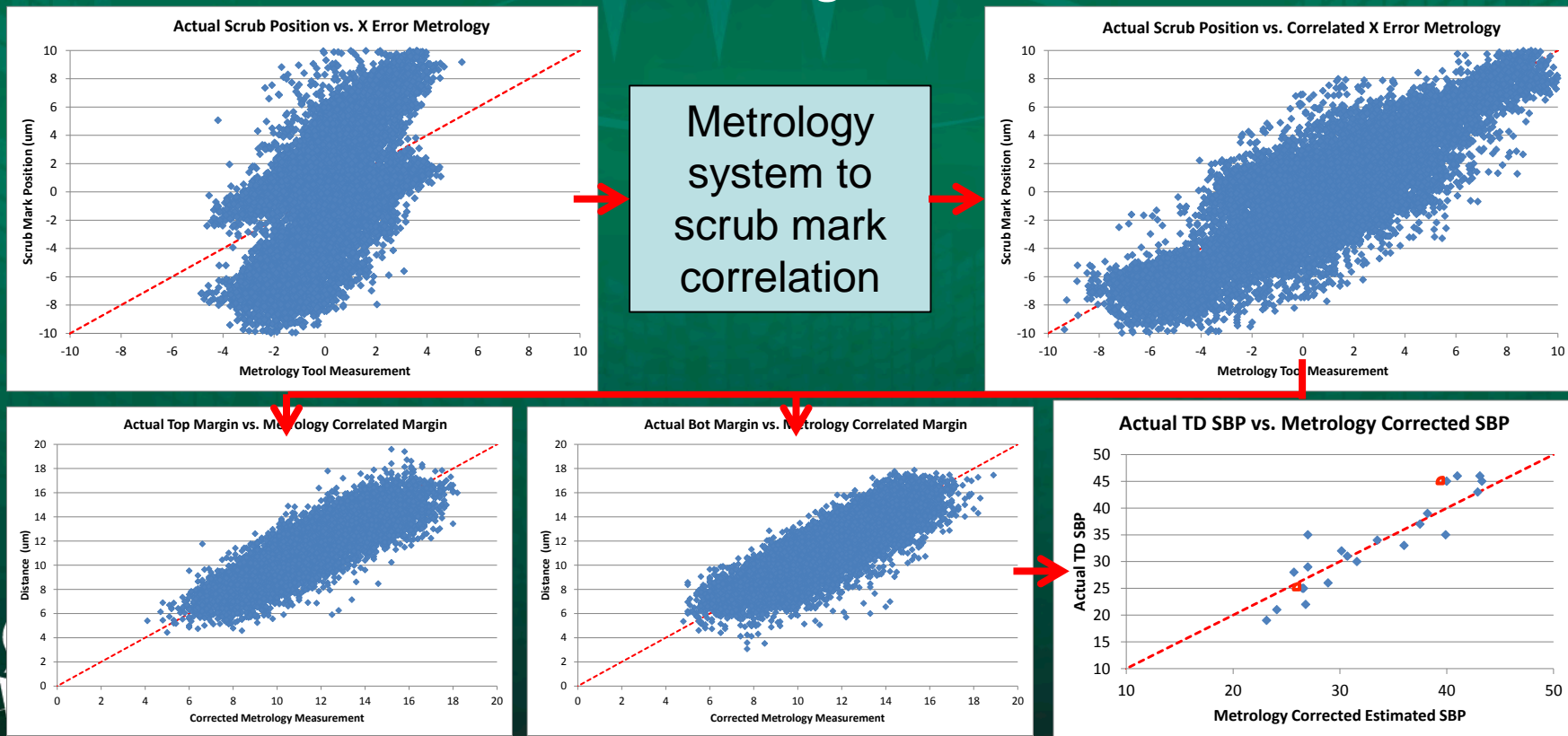
- Virtual scrub
- Tip position start/end of scrub
- Tips up (uncompressed)
- Tip size/morphology vs. scrub dynamics and mark formation
- Effective over travel on metrology tool vs. prober/test system
- Thermal compensation/correction

Differences among metrology tools means the SBP approach is more of an “apples to apples” analysis in determining scrub capability



Metrology Tool Analysis and Prediction

- **Applying correction methods to metrology data**
 - Need to develop correlation of measured values adjusted for actual OT, thermal, and scrub performance differences between measurement tooling and actual scrub marks



Probe Card Scrub Capability Summary

- **Probe card scrub capability**

- Determined by aggregate, collective assessment of all scrub marks produced by the card
 - Confirm operating condition of system and probe card
 - Remove (mathematically) probe card to wafer misalignment (X, Y, Theta)
 - Compute the bounding box “Super Bond Pad” of all marks and compare against the bond pad/footprint size requirements
- Cost effective/efficient method that determines capability more effectively than an individual parameter specification process

- **Measurement considerations**

- Actual wafer scrub mark measurement is the true arbiter
 - Probe card metrology tools can and should be used, but correlation of measured parameters to actual scrub mark performance is key to a successful process



Acknowledgements

- **FormFactor**
 - Mickey Lee
 - Yue Yang

