

IEEE SW Test Workshop Semiconductor Wafer Test Workshop

June 8 - 11, 2014 | San Diego, California

Thermal Analysis of Wafer Level Probes for Final Test

Johns<u>tech</u>®

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Computational Modeling With

 In this tutorial you will learn how to setup up and run a computational thermal analysis

ANSYS ICEPAK

Electronics thermal management

Joule Heating / Resistive Heating
Computational Fluid Dynamics

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Assumptions

400 micron Pitch Probe Geometry
Generic Probe Design
Joule Heating Along One Axis
Heat Sinks have constant temperature

50°C DUT temp
20°C LBD temp

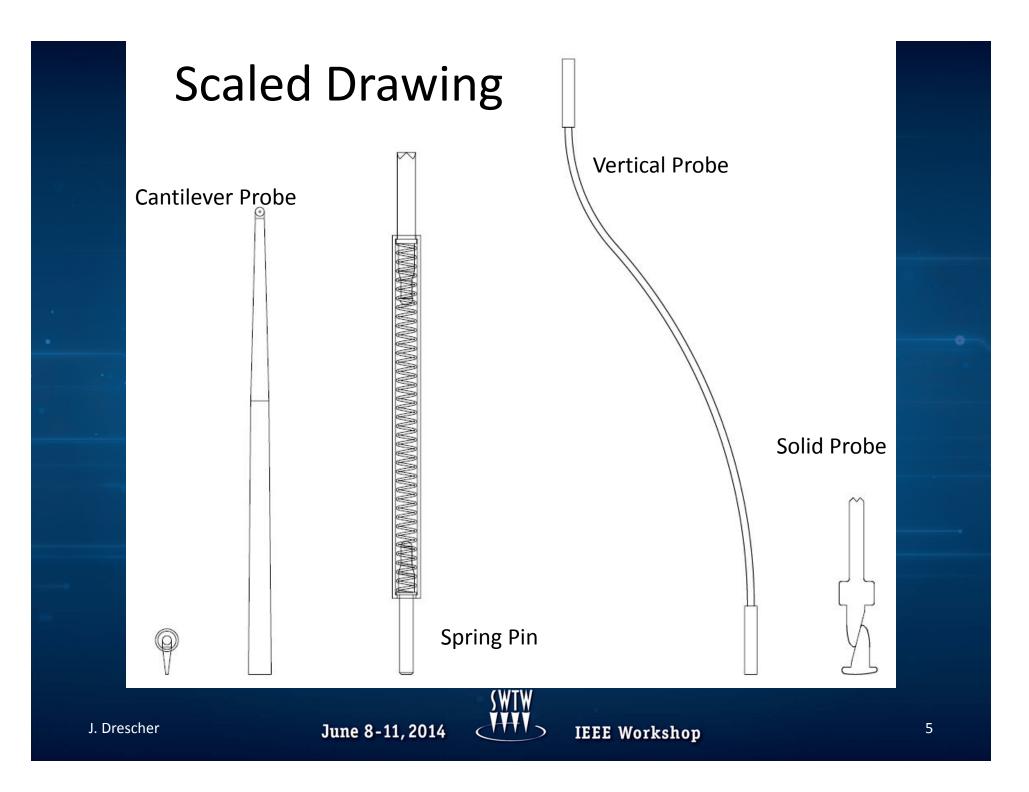
Material is Beryllium Copper

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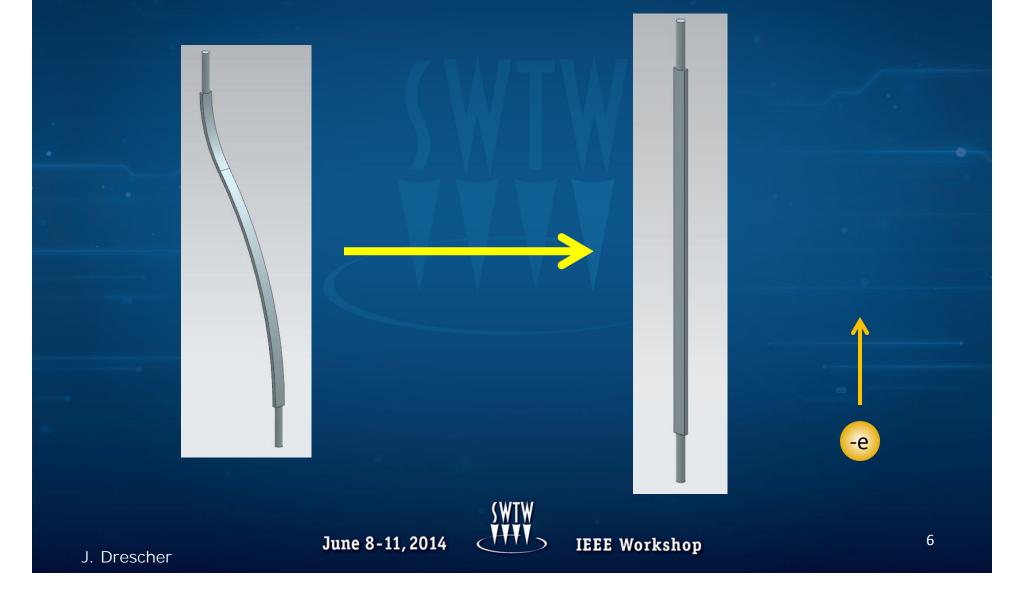
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Probe Types

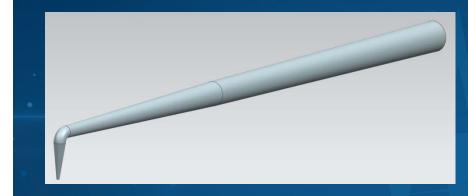




Real Geometry vs. Physics Geometry



Real Geometry vs. Computational Geometry



Real Geometry

Computational Geometry



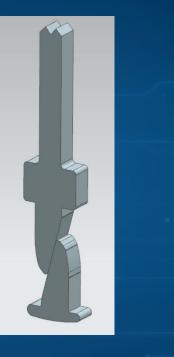


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Real Geometry vs. Computational Geometry





Spring pins and solid probes all have electrons traveling in one axis and no changes are required for the computational model

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Mesh Settings

Mesh control		
Num elements: not loaded Num nodes: not loaded		
Settings Display Quality		
瞤 Load 🛛 🎟 Generate 📄 Terminate		
Mesh type: Mesher-HD 🚽 Mesh units mm 🚽		
Max element size Minimum gap I → Y 50.0 × 0.0025 m ▼ I → Y 50.0 Y 0.0002 m ▼ I → Z 50.0 Z 0.002 m ▼		
Image: Point Stress		
Close Help		

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Mesh Type

– Mesher-HD → CAD Geometry

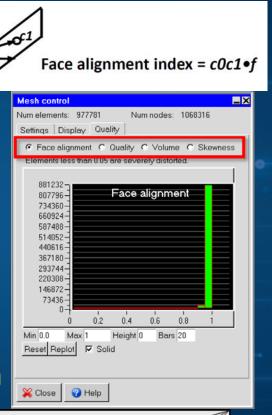
- Max element size
 - X,Y, and Z directional sizes of the background mesh
 - Balance between accuracy and runtime
 - Minimum Gap
 - All geometries below this tolerance will be ignored by the mesher

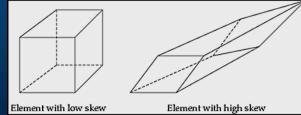


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Meshing Verification

- Face Alignment
 - Range from 0 (bad) to 1 (good)
 - Face alignment must be greater than 0.05
 - Best results above 0.15
- Volume
 - Determines if you use double or single precision solver (1e-13)
- Skewness
 - Skewness determines how close to ideal a face or cell is
 - Should be above 0.02

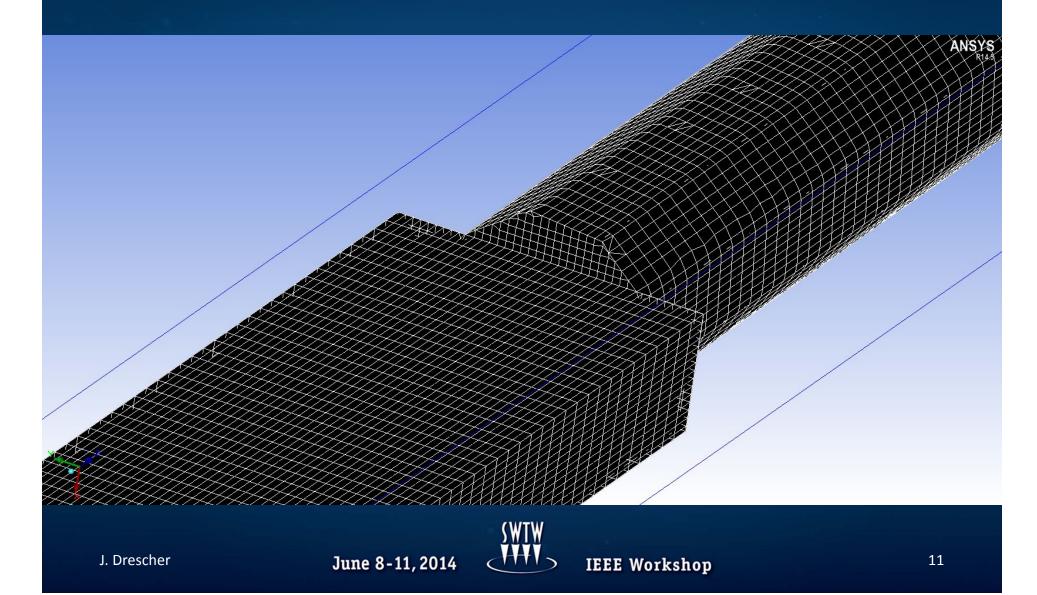




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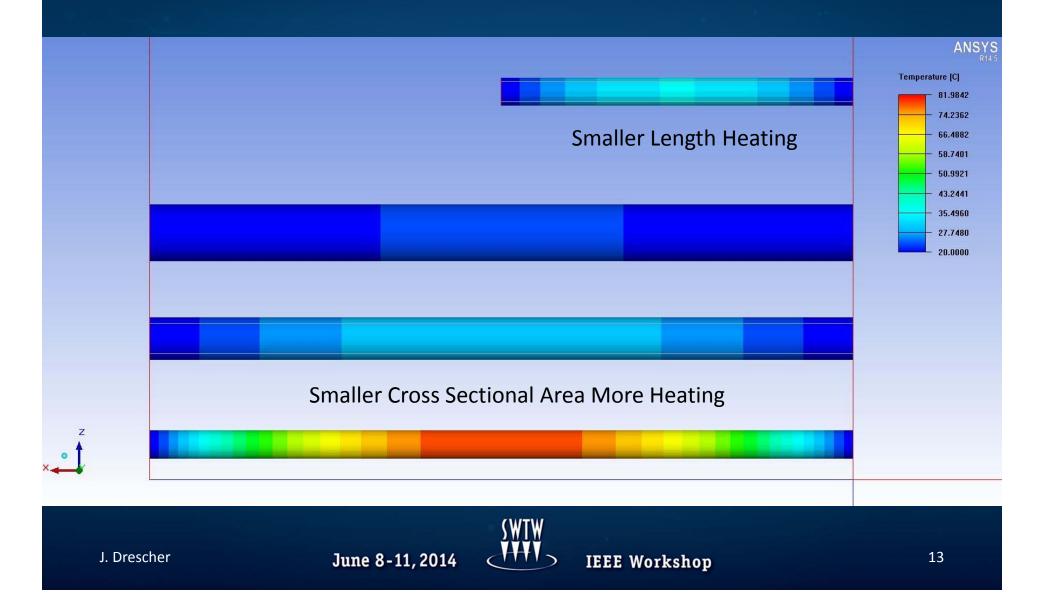
Visual Inspection of the Mesh



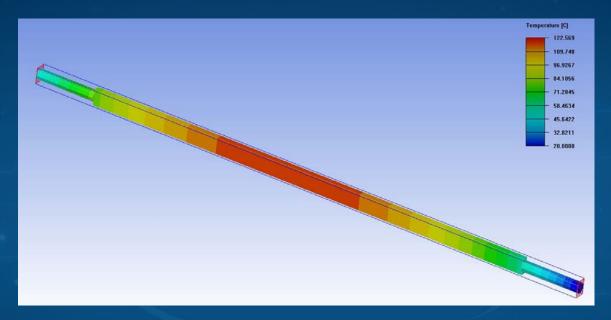
Material Properties and Joule Heating

	Blocks [Buckling Beam Flat]	
	Info Geometry Properties Notes	
	Block type: Solid O Hollow O Fluid C Network Surface specification	
Joule heating power	Surface material default	
Power type: Constant C Varying	Area multiplier 1.0	
P = Current²(ρL/A) ρ = Resistivity(1+C(T-Tref))	Radiation Edit	
Current 3.0 Amp - Transient 🚺 Edit	🗖 Individual sides 🧾 Edit	
L Zlength	Thermal specification	
Resistivity 7.68e-008 Ohm-m 🔻	Solid material Beryllium Copper	
C 1.0	Total power 0.0 W 🚽 Joule heating 🚽 🚺 Edit	
Tref ambient C	Rotation 0 RPM	
Low temperatureambient C	External conditions Edit	
High temperature ambient		
Density = 8321.0 kg/m3 Specific heat = 419.0 J/kg-K Conductivity type = Isotropic Conductivity = 95.0 W/m-K	☐ Temperature limit default ☐ Fix values	
	🗸 Update 🛛 🙀 New 🛛 🏂 Reset 🛛 🙆 Delete	
Vpdate 🖇 Reset 🕢 Done 💥 Cancel 💡 Help	☐ Copy from	

Joule Heating of a Physics Rod



Adding Heat Sinks

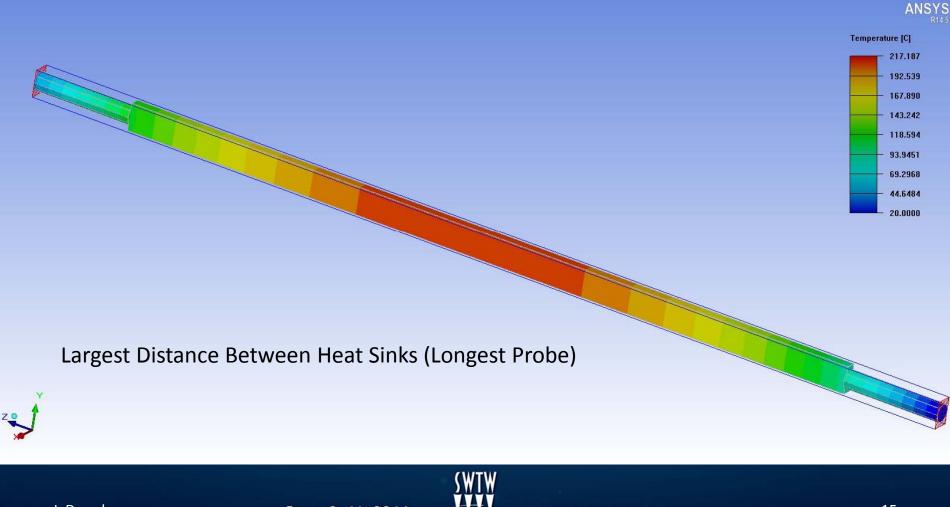


Heat sinks being applied – 50°C DUT temperature – 20 °C Load board trace temperature

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Vertical Probe

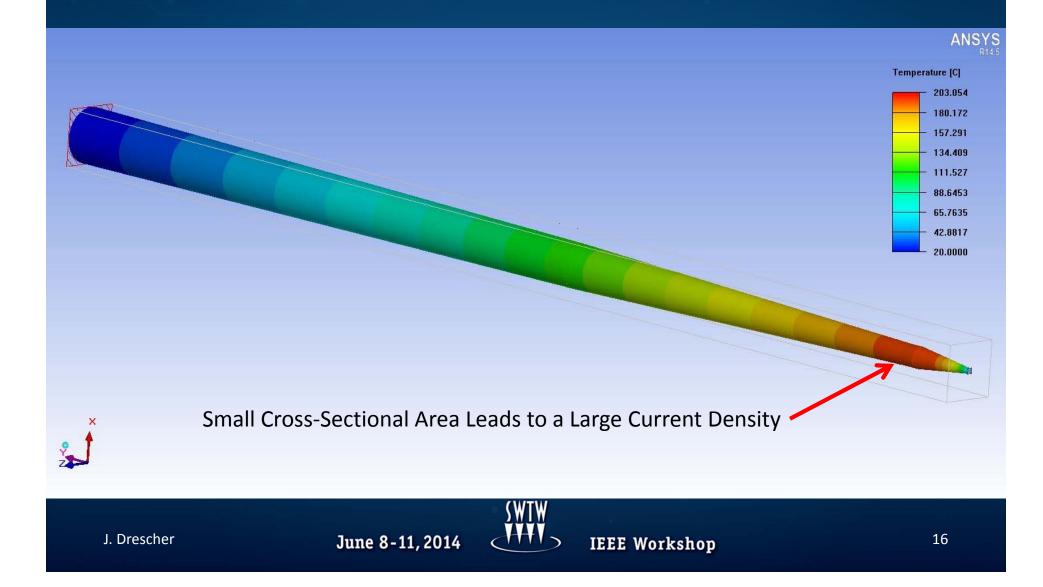


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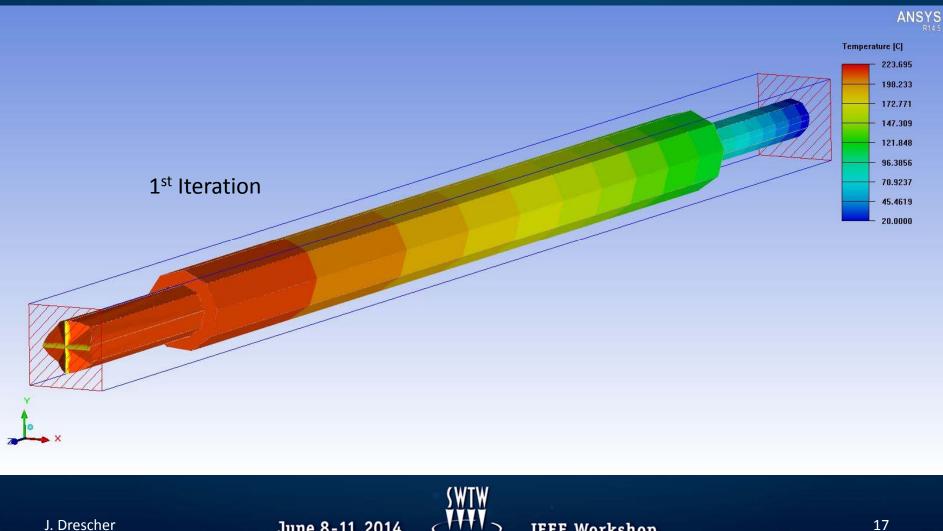
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Cantilever Probe



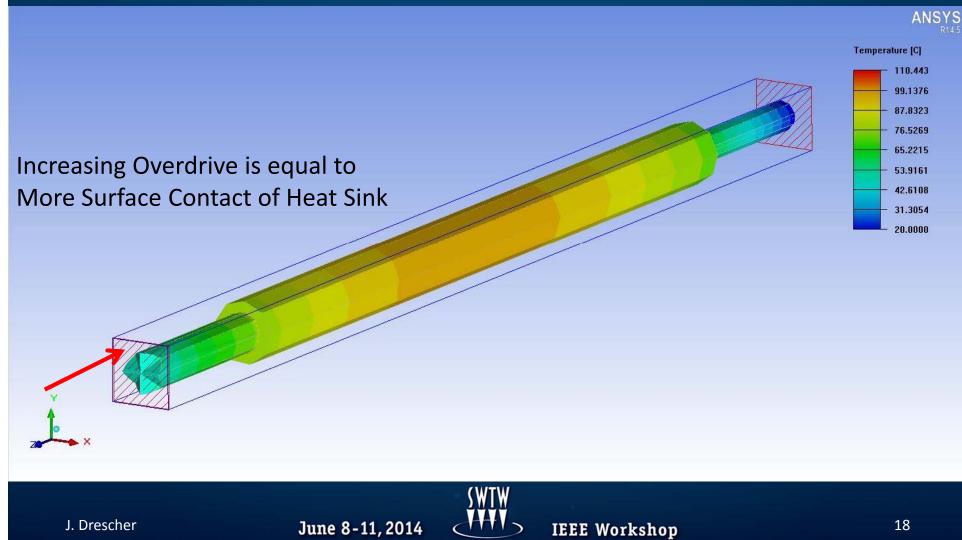
Spring Pin



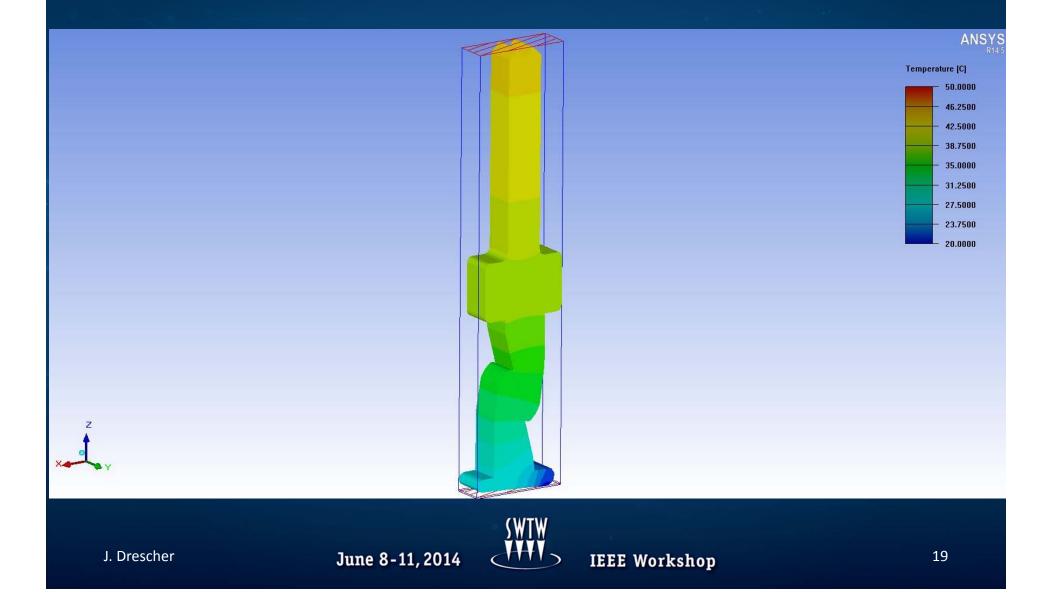
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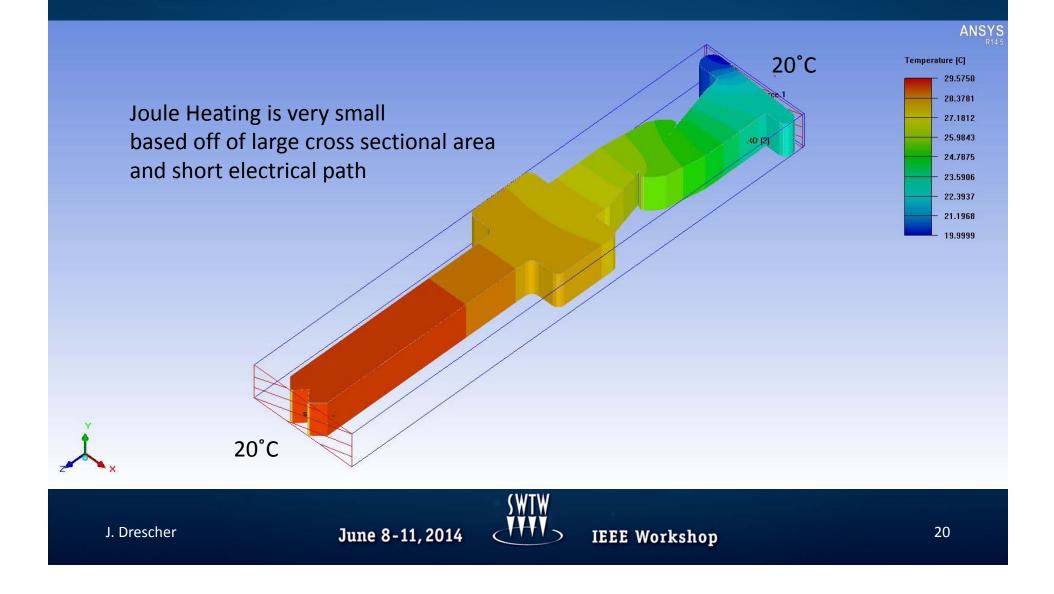
Improved Accuracy



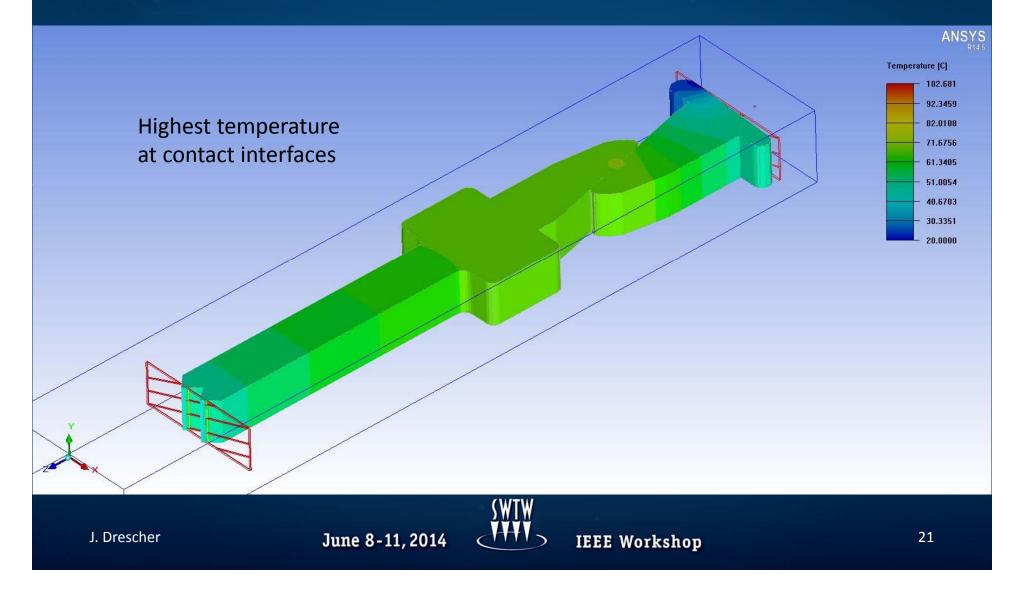
Solid Probe



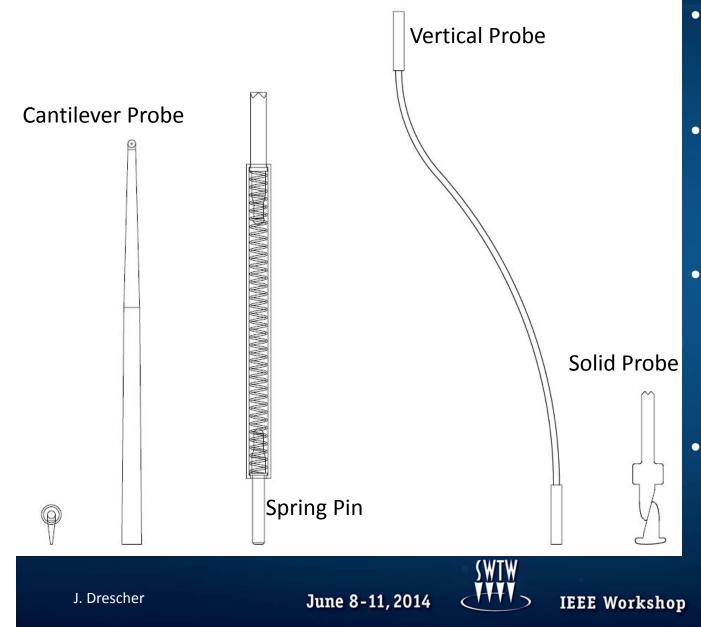
2nd Iteration



Adding Contact Resistance and Natural Convection



Probe Type Conclusions



- Vertical Probe has a the longest length leading to higher temperatures
- The cantilever probe has a small cross sectional area leading to high current density
- The Spring Pin has a contact resistance between the tips and the barrel leading to increased heating
- Solid Probe has the lowest Joule heating effect, but has internal contact resistances

Increasing Accuracy

- Adding Real Heat Sinks
 - Active DUT Heating
 - Conduction to Retaining Features
 - Natural Convection
 - Contact Resistance
 - Load Board Trace Cooling

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Computational Conclusion

- Generate physical geometry for computational requirements
- Conduct accurate meshing and validate
- Review results and iterate with increasing complexity for best correlation to reality



Why Should You Care?

- Tomorrows devices will have higher transistor density and run hotter. We must address that today.
- Leveraging computational thermal analysis at the wafer scale will create better and faster designs pushing innovative solutions



Questions?



