



IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

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Conductive Paste-Based Interconnection Technology for High Performance Probe Card



TSE

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TSE Co., Ltd.

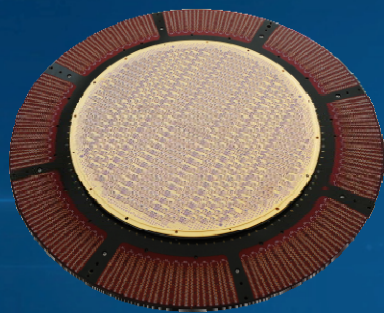
Overview

- **Introduction of TABP Technology**
- **Key Technology of Core to Core Interconnection**
- **Test Results & Application Examples**
 - ✓ **Electrical & Thermal Reliability of Core to Core Interconnection PCB by Actual Application**
- **Probe Card Application by Design Rules**
- **Conclusions**

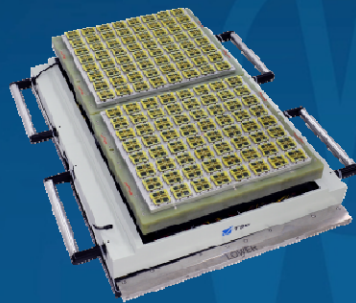


TSE Who we are

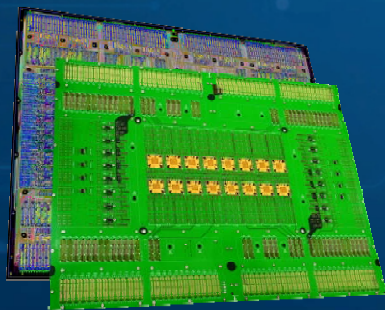
TSE Co., Ltd.



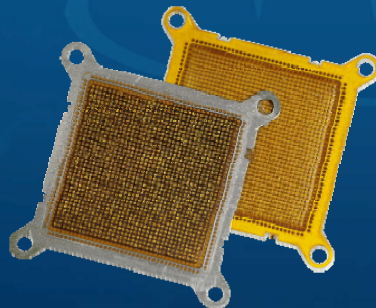
Probe Card



Memory Test Board



Load Board

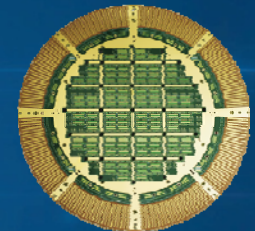
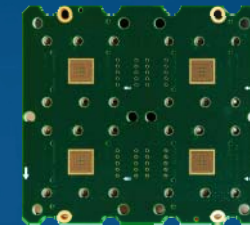
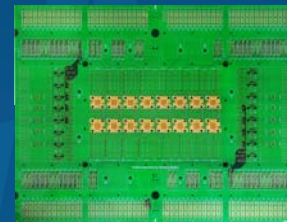


Test Socket

Affiliated Companies



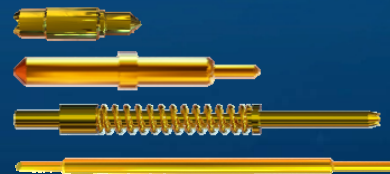
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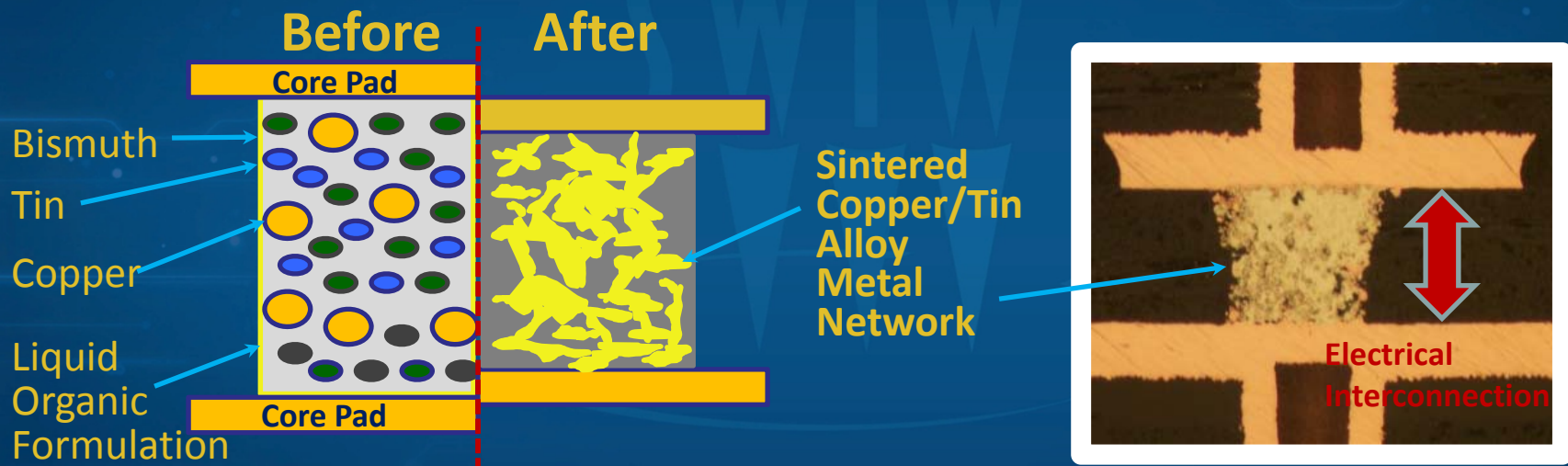


GMTEST



What is TABP?

- TABP = “TSE Advanced Bump PCB”
→ Core to core interconnection PCB



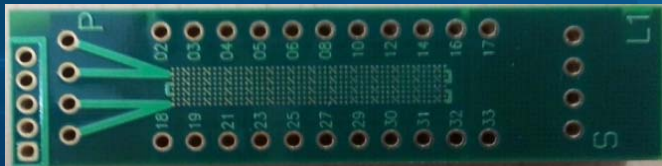
<Structural Change of Conductive Paste by Sintering>

<Section View>

Advantages of TABP

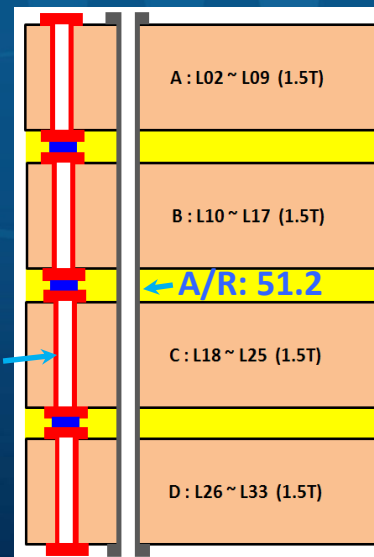
- Free of Thick Board Drilling
- Free of High Aspect Ratio Via Hole Plating
- Reducing Complexity of Back Drilling
- Enhance Fabrication Capability for Fine Pitch HDI PCBs

IST Coupon

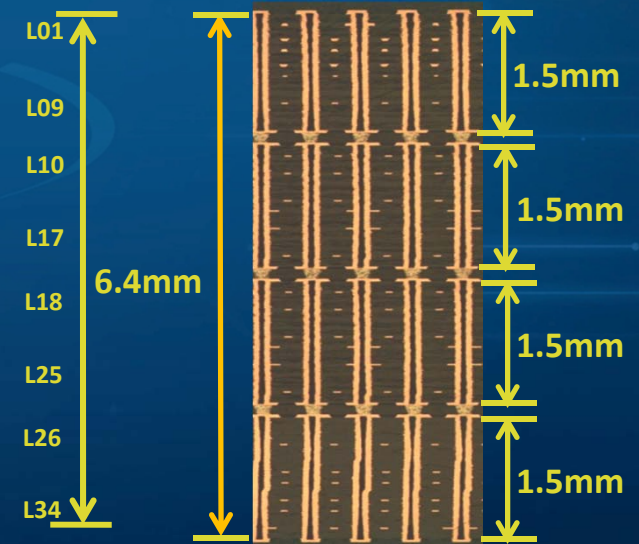


- Min. Pitch : 0.4mm
- Layer Count : 34
- Thickness : 6.4mm
- Aspect Ratio : 51.2
- Via Size : 0.125mm Φ
- PCB Size : 12.7mm x 50.8mm

Layup Structure

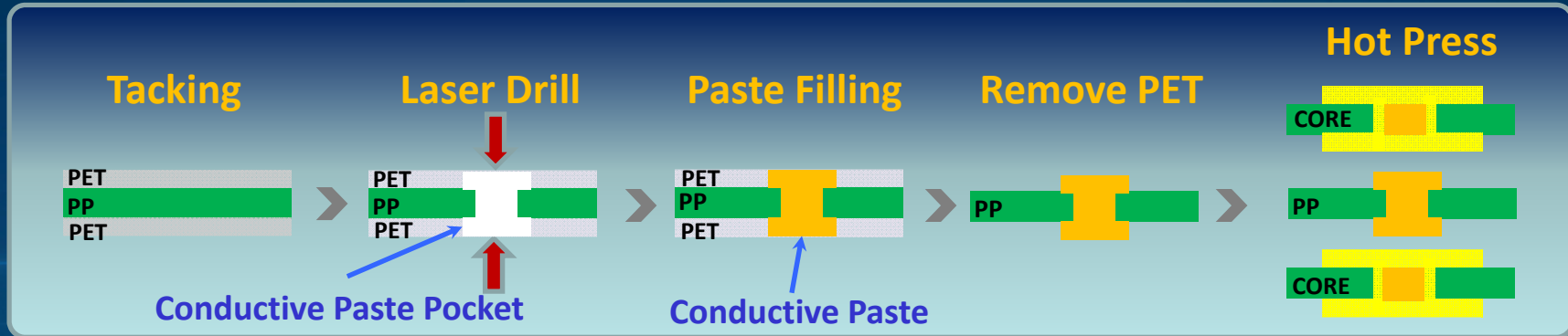


Cross Section

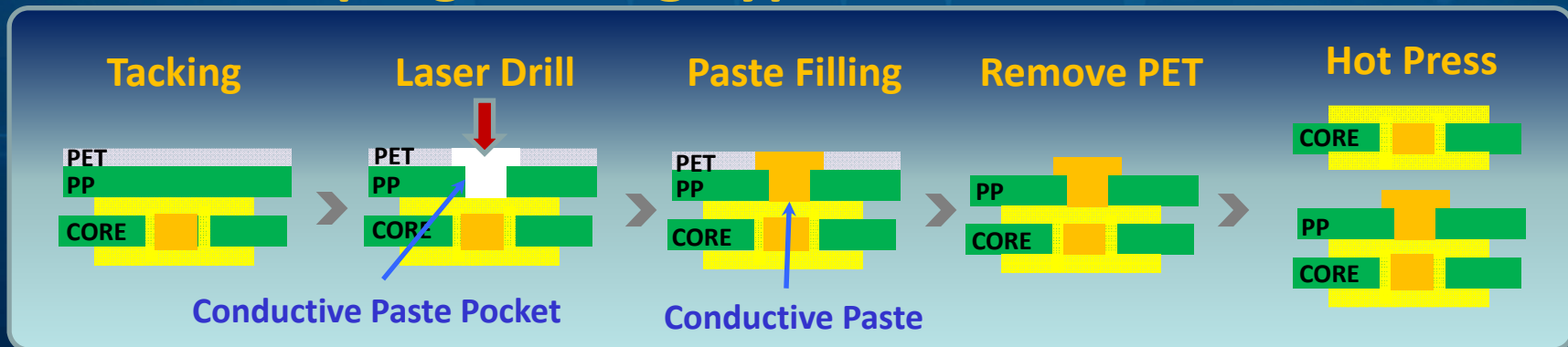


TABP Fabrication Process Flow

• Prepreg Tacking Type



• Core & Prepreg Tacking Type



Key Technology

TABP

(TSE Advanced
Bump PCB)

Electrical Conductivity

- Perfect Sintered Alloy Structure
- Sufficient Amount of Paste Fill
- Optimized Forming of Conductive Paste Pocket

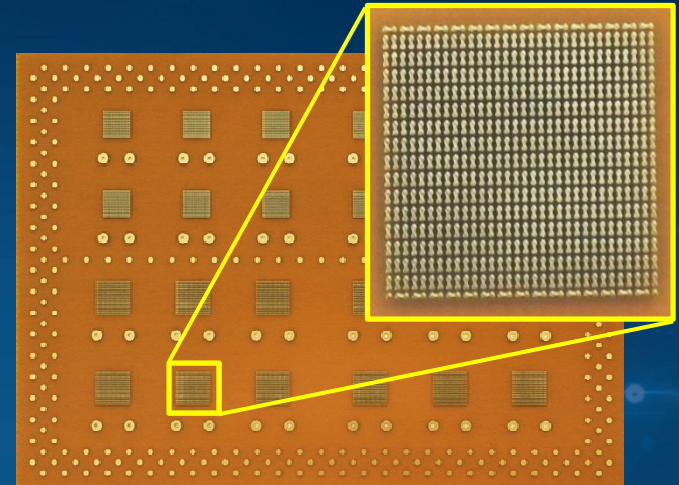
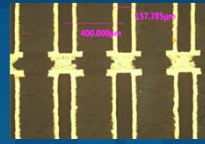
Thermal Reliability

- Withstanding Thermal Stress
 - ✓ Sintered Alloy
 - ✓ Bonding Layer
- Sufficient Resin at Bonding Layer
- Optimized Material, Layup & Design

Electrical Conductivity

- **Coupon Board**

- 0.5mm Pitch 12DUTs & 0.4mm Pitch 12DUTs
- Each Via has 1 TABP interconnection.
- BGA Count of Each DUT = 1,024
- Each Via in Same DUT connected by Daisy Chain
- PCB Thickness = 1.2mm



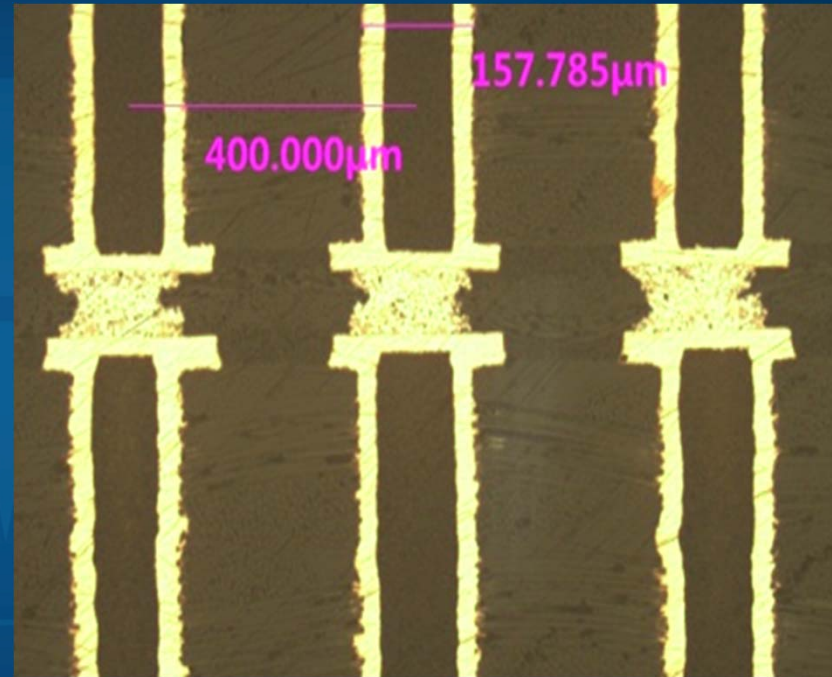
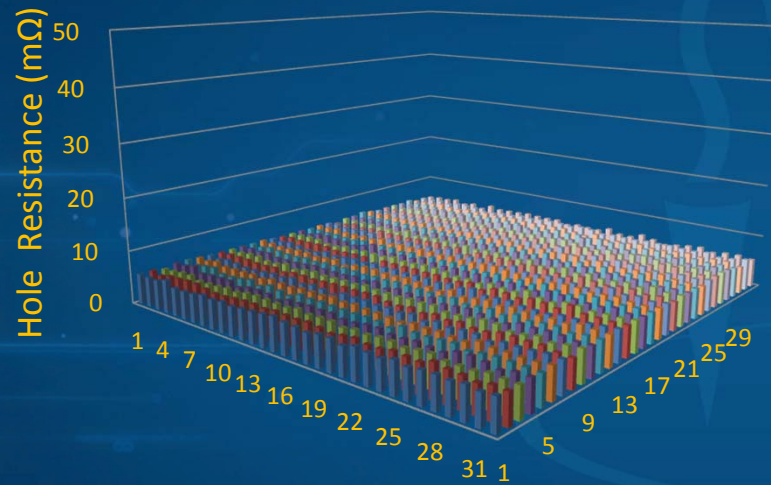
- **DC Interconnection Resistance Values**

BGA Pitch		Daisy Chained DUT (1,024 BGA 24DUTs)	Each BGA Via (Total Count=24,576Ea)
0.5mm (12DUTs)	Max.	6.0Ω	6.65mΩ
	Min.	5.64Ω	4.64mΩ
0.4mm (12DUTs)	Max.	7.63Ω	7.05mΩ
	Min.	7.25Ω	4.81mΩ

Measured by DVM, Microcraft EMX6151

Electrical Conductivity

- Via Holes Resistance of 1 DUT
- Cross Section of Test Coupon

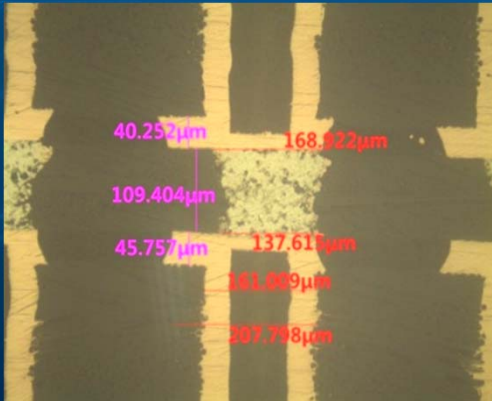
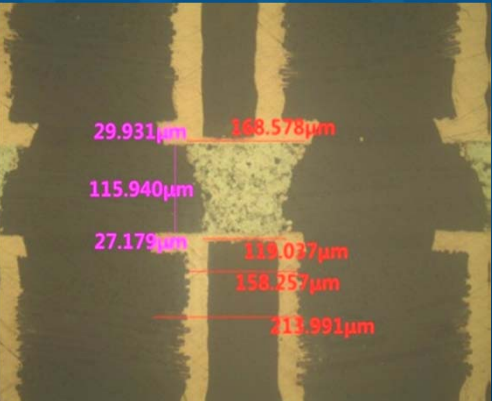
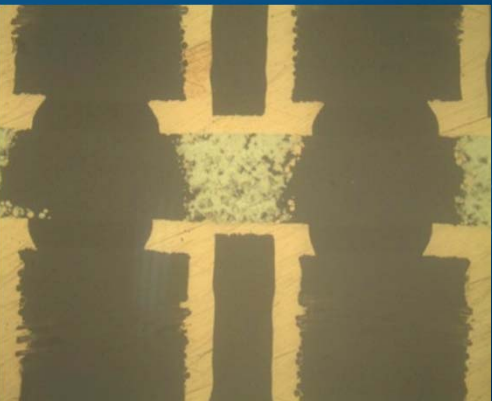


- BGA Pitch : 0.4mm
- 1,024 TABP Vias in 1DUT
- Max Via Hole resistance : 7.05mΩ
- Laser Drill Diameter : 150μm
- Prepreg Thickness : 110μm

<Stable Sintered Alloy Structure>

Thermal Reliability

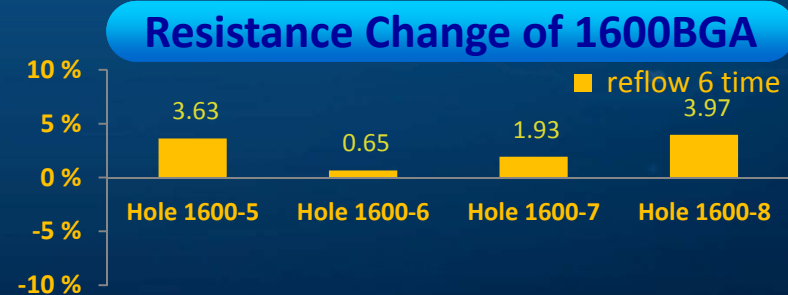
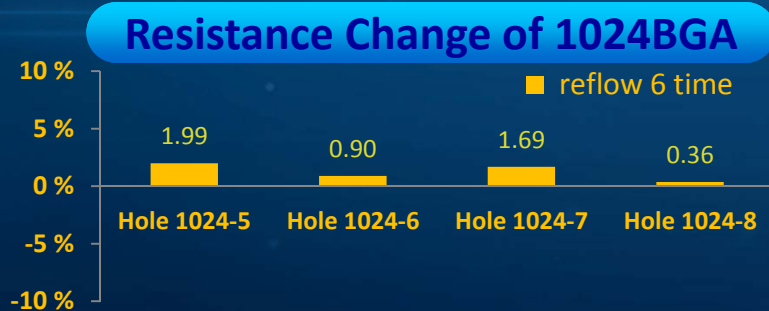
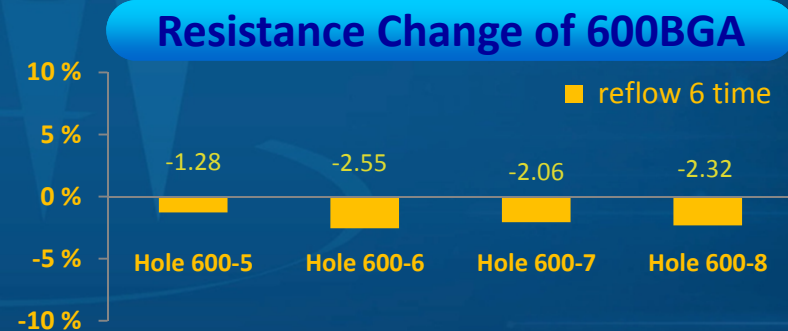
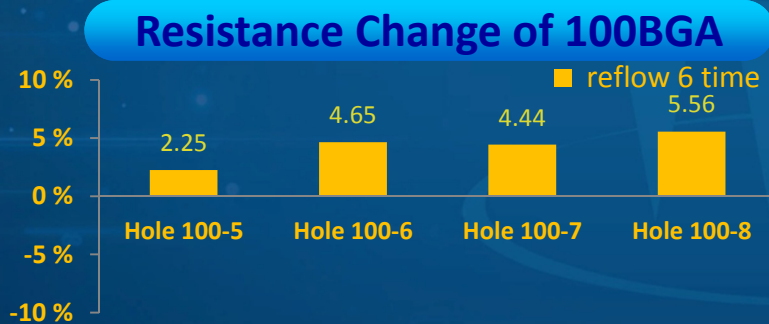
- **Cross Section Analysis after Solder Pot Floating Test**
 - Thermal Impact Condition : 3 Times, 288°C Solder Pot Floating 10sec
 - BGA Count per Each DUT : 100, 600, 1024 & 1600 Ea
 - Each Via in Same DUT connected by Daisy Chain
 - All BGA Interconnection Test was passed.
 - TABP can withstand Thermal Impact of Solder Floating Test.

After Lamination	After Out Layer Formation	After Printing
		
All passed after 3X T/I	All passed after 3X T/I	All passed after 3X T/I

Thermal Reliability

- Resistance Changes after Solder Reflow Exposures

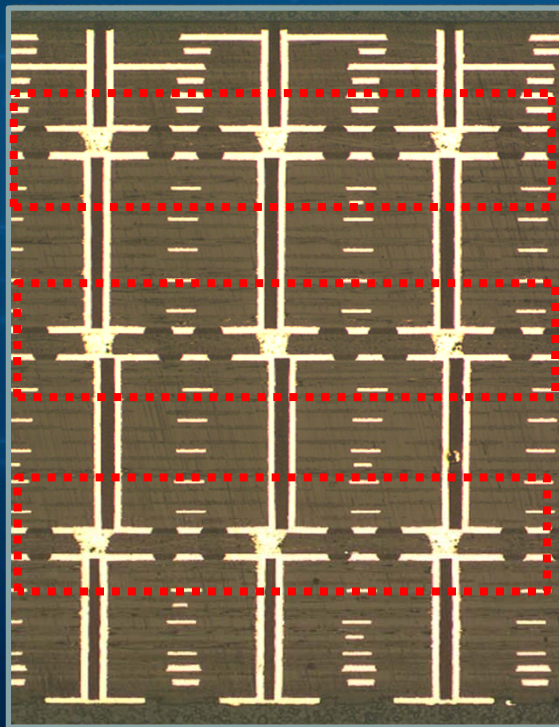
- Reflow Condition : 6 Times Reflow @260°C
- BGA Count per Each DUT : 100, 600, 1024 & 1600 Ea
- Each Via in Same DUT connected by Daisy Chain
- All BGA Interconnection Test was passed.
- IPC Standards for DC Resistance Change after Reflow : Max 10%



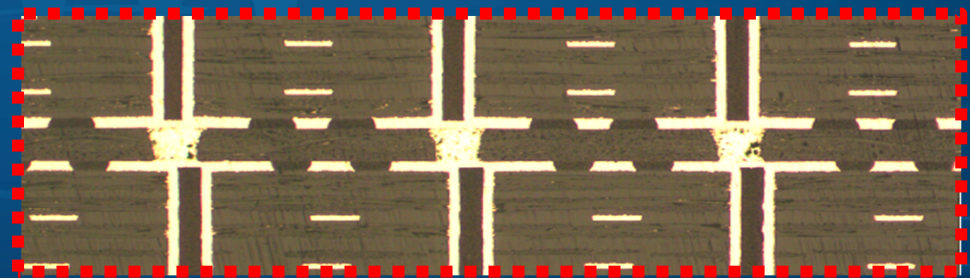
Thermal Reliability

- **Cross Section Analysis after 6x Reflow Exposure**

- Board Profile : 296FBGA, 0.35mm Pitch, 4mmT, 3 TABP, 0.15mm Φ Laser Drill
- Applied Thermal Impact Condition : 6 Times Reflow @260°C
- TABP's Structural Stability can withstand 6 times of Reflow Condition.



< Cross Section after Thermal Impact >



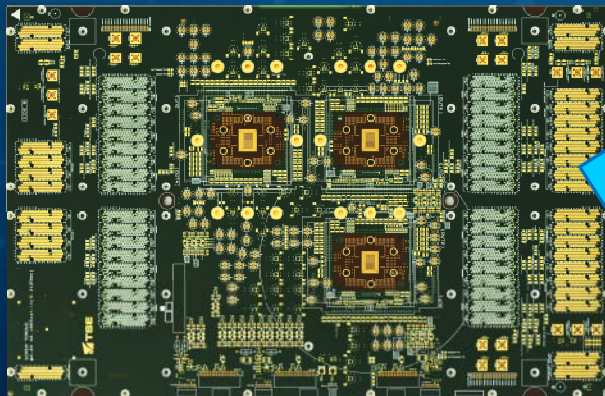
Stable Paste Structure & Bonding Condition

TABP Application Examples

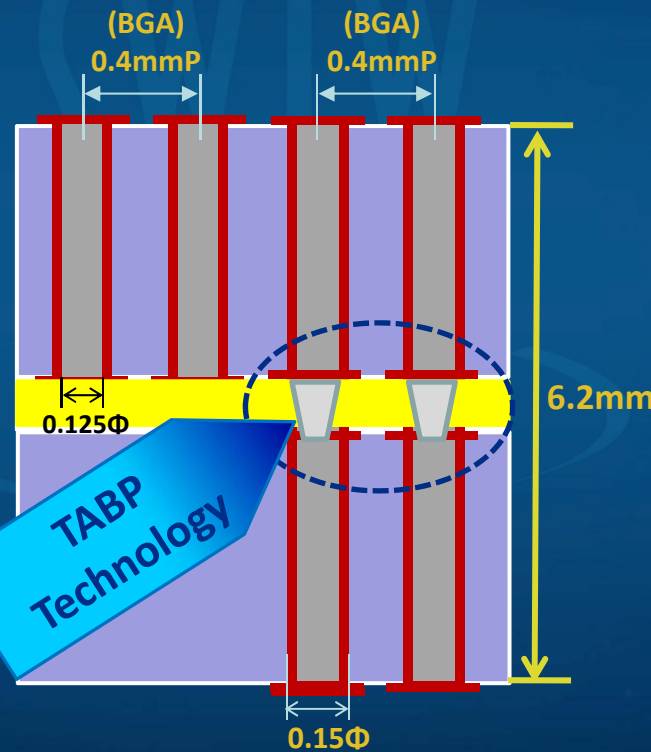
- Load Board – 0.4mm Pitch, Aspect Ratio 41.3

Board Profiles

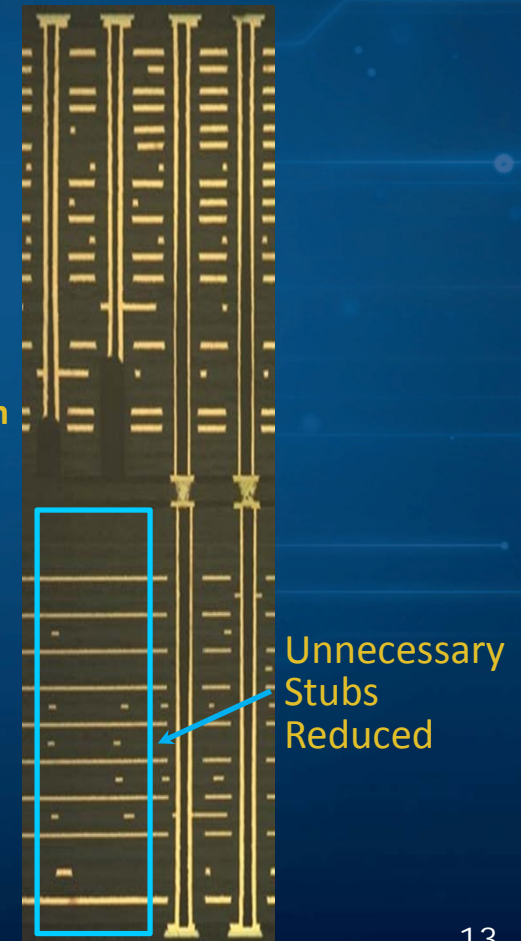
- BGA Pitch : 0.4mm Pitch
- Layer Count : 38L
- Thickness : 6.2mm
- Via Size : 0.15mm Φ
- Aspect Ratio : 41.3
- PCB Size : 340mm x 520mm
- Option : TABP + HPL + Back Drill



Structure



Cross Section

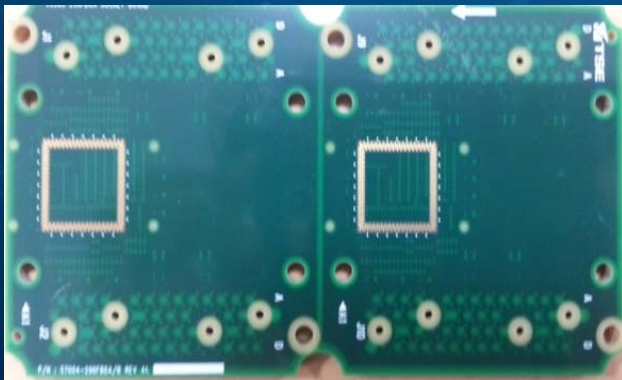


TABP Application Examples

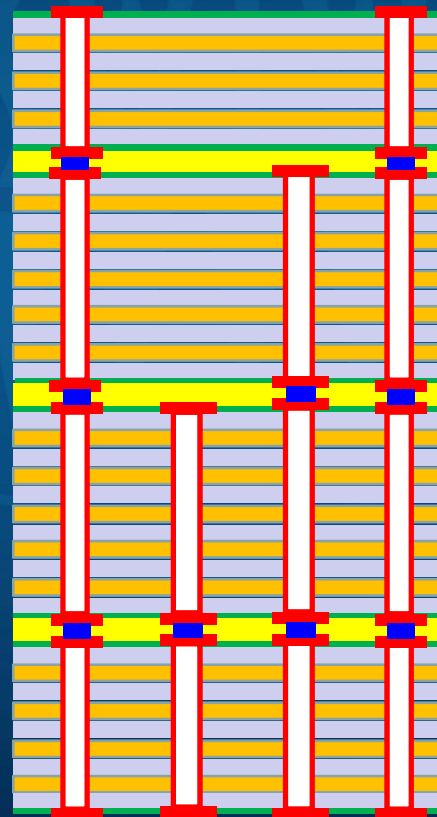
- Memory Test Board – 0.35mm Pitch, Aspect Ratio 28

Board Profiles

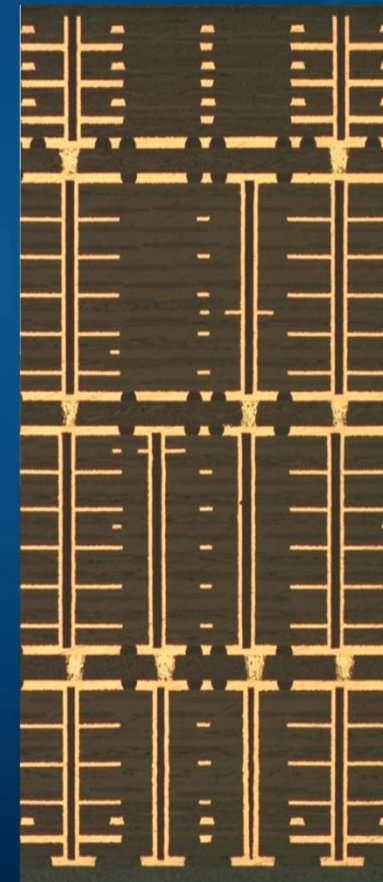
- BGA Pitch : 0.35mm
- Layer count : 38
- Thickness : 3.5mm
- Via Size : 0.125mm Φ
- Aspect Ratio : 28
- PCB Size : 59mm x 109 mm
- Option : TABP + HPL + Back Drill



Structure



Cross Section

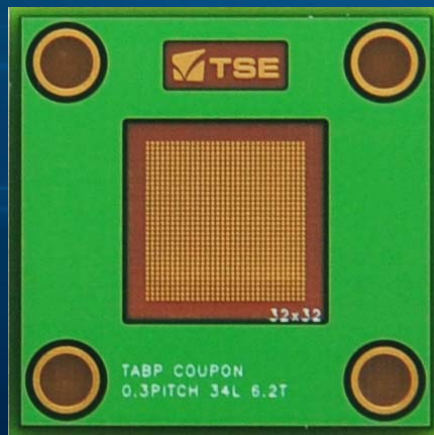


TABP Application Examples

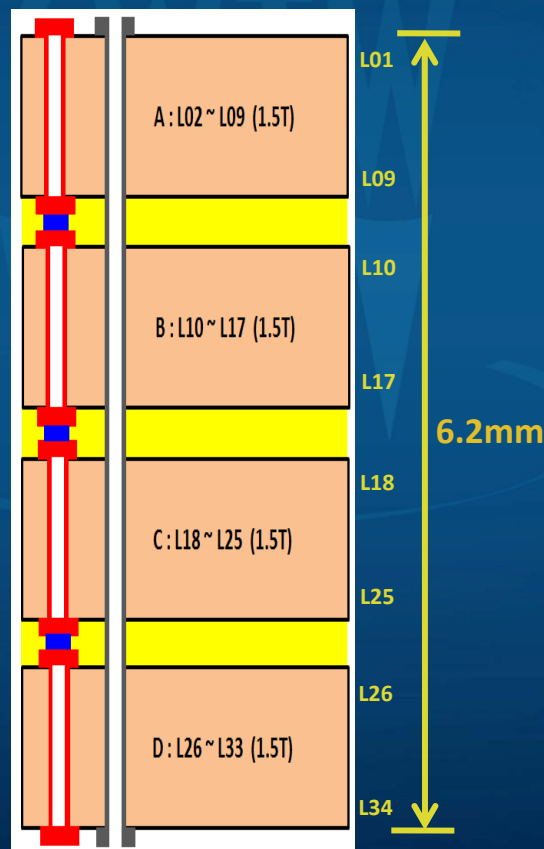
- Pretest Coupon - 0.3mm Pitch, Aspect Ratio 62

Board Profiles

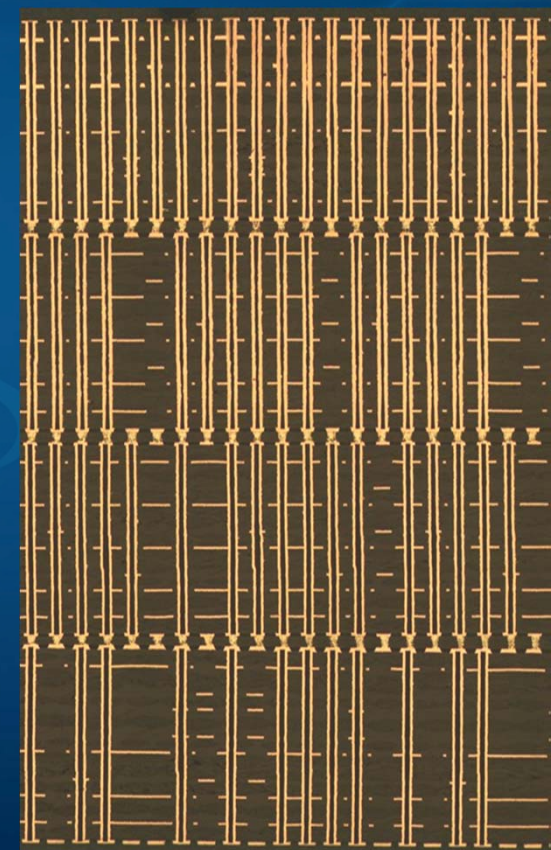
- BGA Pitch : 0.3mm
- Layer Count : 34
- Thickness : 6.2mm
- Via Size : 0.1mm Φ
- Aspect Ratio : 62
- PCB Size : 26mm x 26mm
- Option : TABP + HPL + Back Drill



Structure



Cross Section



Challenges for Probe Card PCB

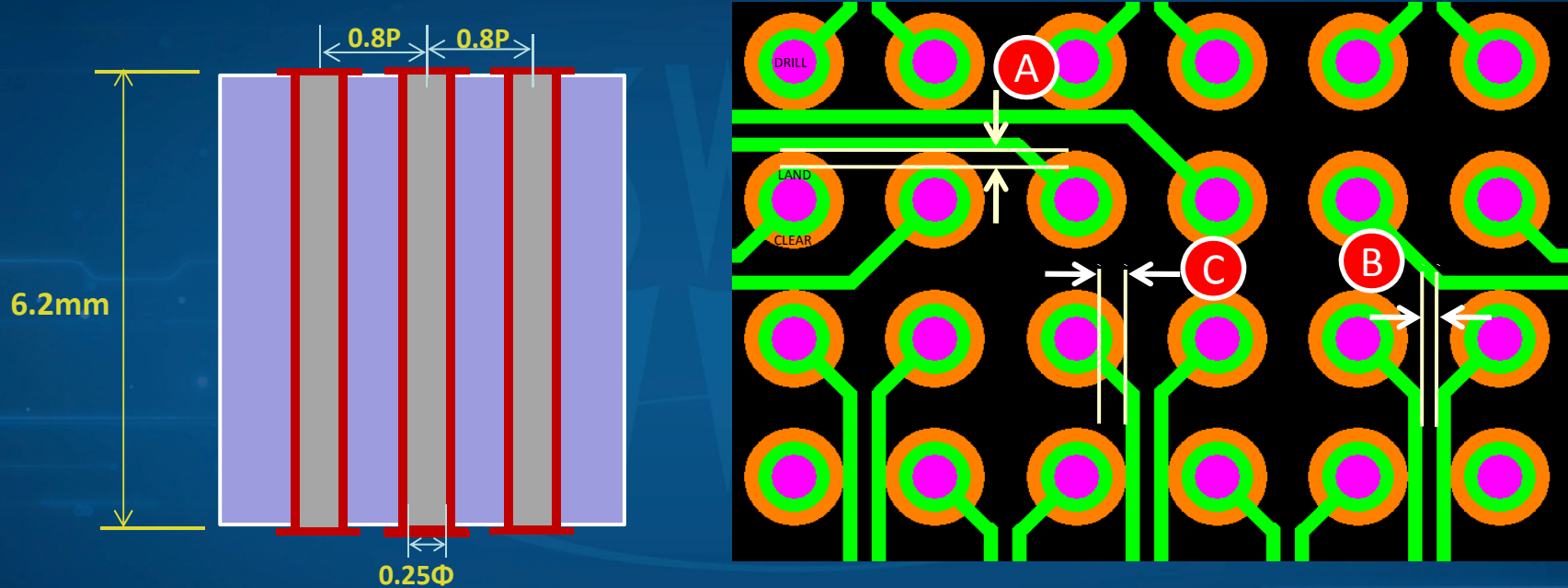
- High Layer Count / High Aspect Ratio
- SI Performance for High Speed Application
- Design/Fabricate PCB at Competitive Conditions

TABP is a Solution for Advanced Probe Card PCB.

- by Eliminating of Thick Board Drilling
- by Eliminating of High Aspect Ratio Via Plating
- by Reducing Drilling Complexity & Improving Yield

Design Rule for 0.8mm Pitch P/C PCB in Double Line Array

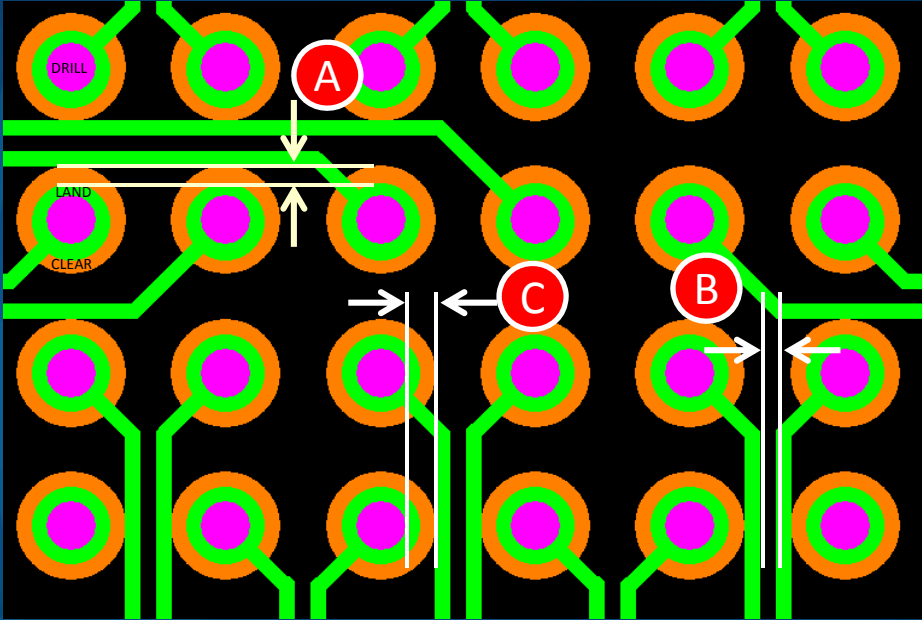
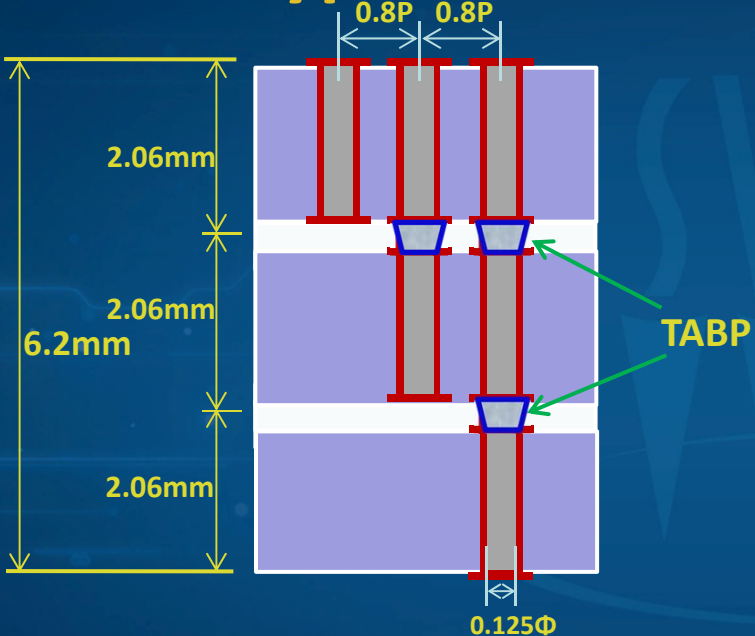
- Plating Through Hole Type



Drill Dia.	A/R	Line Width	A Land to Line	B Line to Line	C Drill to Metal
250 μ m Φ	24.8	80 μ m	80 μ m	80 μ m	155 μ m

Design Rule for 0.8mm Pitch P/C PCB in Double Line Array

- TABP Type**



Drill Dia.	A/R	Line Width	A Land to Line	B Line to Line	C Drill to Metal
125μmΦ	49.6 (16.5)	80μm	90μm	160μm	177μm

Conclusions

- **Conductive Paste Based Core to Core Interconnection Technology at PCB was realized. Especially excellent core to core conductivity and thermal reliability were proved. Therefore, we hope the TABP technology would pave the way for fine pitch and high aspect ratio PCB fabrication.**
- **0.4mm Pitch, Aspect Ratio 41.3 Load Board & 0.3mm Pitch, Aspect Ratio 62 Board were possible to fabricated with TABP Technology.**
- **Test boards for wafer test also need TABP technology to respond for the requirement of multi sites, fine pitch and high frequency performance.**

Thank you very much.

Questions?