SWTW

IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

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Design For Probe:

Probe Card Selection Process

Texas Instruments

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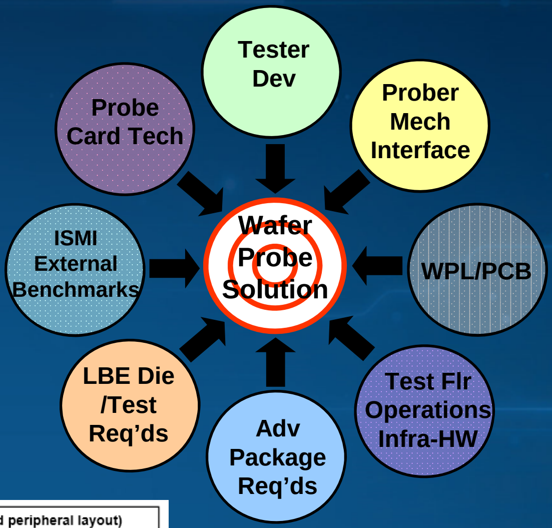
Agenda

- DFP Overview
- TI Qualified Vendors
- Qualification Process
- Probe Technologies
- Specifications / Documentation
- Benefits of DFP Process
- Questions / Discussion

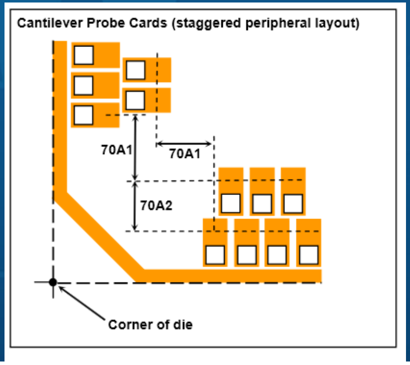
Design For Probe Overview

DFP-Design For Probe is a risk-review process involving a cross functional team of experienced probe test members whose objective is to target probe solutions that are aligned to TI's Roadmap and Best Practices.

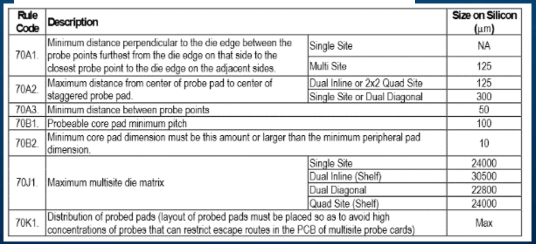


Benefits

- **Optimize the Probe Card technology selection!**
  - Build the right Probe Card for your device.
  - Take advantage of the latest qualifications
  - Understand each test floor's strengths for smooth offload.
- **Maintain Probe Card Build Spec**
  - Monitor vendor compliance to avoid probe card mis-builds and lost cycle time
- **WPL assists with RFQ to ensure best pricing!**
- **Design Rules for various silicon technologies.**
- **Help to provide robust solutions that can easily be transferred across various TI sites worldwide.**



Ex:
Cantilever design rules below for pad layout.



Rule Code	Description		Size on Silicon (µm)
70A1.	Minimum distance perpendicular to the die edge between the probe points furthest from the die edge on that side to the closest probe point to the die edge on the adjacent sides.	Single Site	NA
		Multi Site	125
70A2.	Maximum distance from center of probe pad to center of staggered probe pad.	Dual Inline or 2x2 Quad Site	125
		Single Site or Dual Diagonal	300
70A3.	Minimum distance between probe points		50
70B1.	Probeable core pad minimum pitch		100
70B2.	Minimum core pad dimension must be this amount or larger than the minimum peripheral pad dimension.		10
70J1.	Maximum multisite die matrix	Single Site	24000
		Dual Inline (Shelf)	30500
		Dual Diagonal	22800
		Quad Site (Shelf)	24000
70K1.	Distribution of probed pads (layout of probed pads must be placed so as to avoid high concentrations of probes that can restrict escape routes in the PCB of multisite probe cards)		Max

Design For Probe Organization

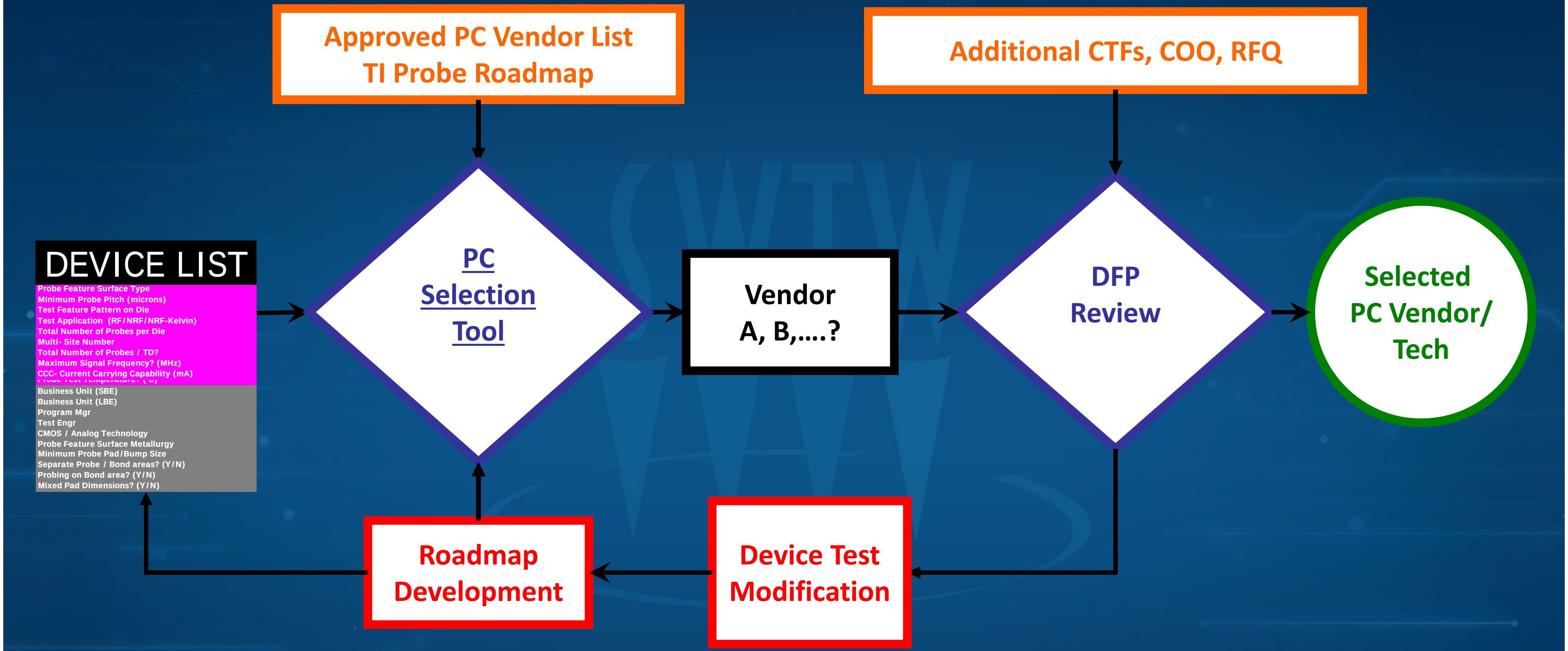
Brandon Mair
DFP Team Lead

Test Sites

Probe Test Solutions

Business Units

Design for Probe Process Flow



DEVICE LIST

Probe Feature Surface Type
Minimum Probe Pitch (microns)
Test Feature Pattern on Die
Test Application (RF/NRF/NRF-Kelvin)
Total Number of Probes per Die
Multi- Site Number
Total Number of Probes / TD?
Maximum Signal Frequency? (MHz)
CCC- Current Carrying Capability (mA)
Probe Test Temperature? (C)
Business Unit (SBE)
Business Unit (LBE)
Program Mgr
Test Engr
CMOS / Analog Technology
Probe Feature Surface Metallurgy
Minimum Probe Pad/Bump Size
Separate Probe / Bond areas? (Y/N)
Probing on Bond area? (Y/N)
Mixed Pad Dimensions? (Y/N)

Approved PC Vendor List
TI Probe Roadmap

PC
Selection
Tool

Vendor
A, B,….?

Additional CTFs, COO, RFQ

DFP
Review

Selected
PC Vendor/
Tech

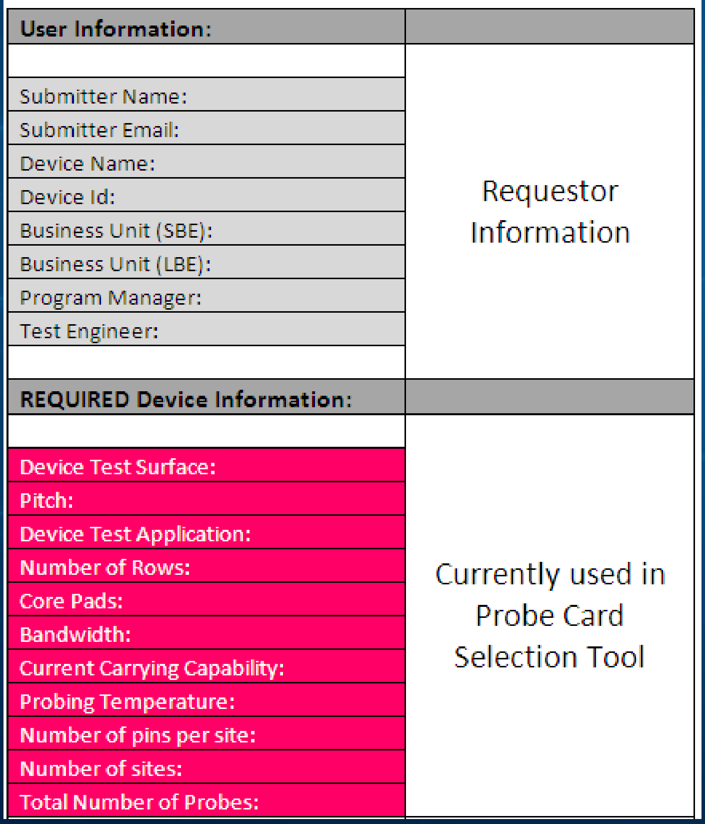
Device Test
Modification

Roadmap
Development

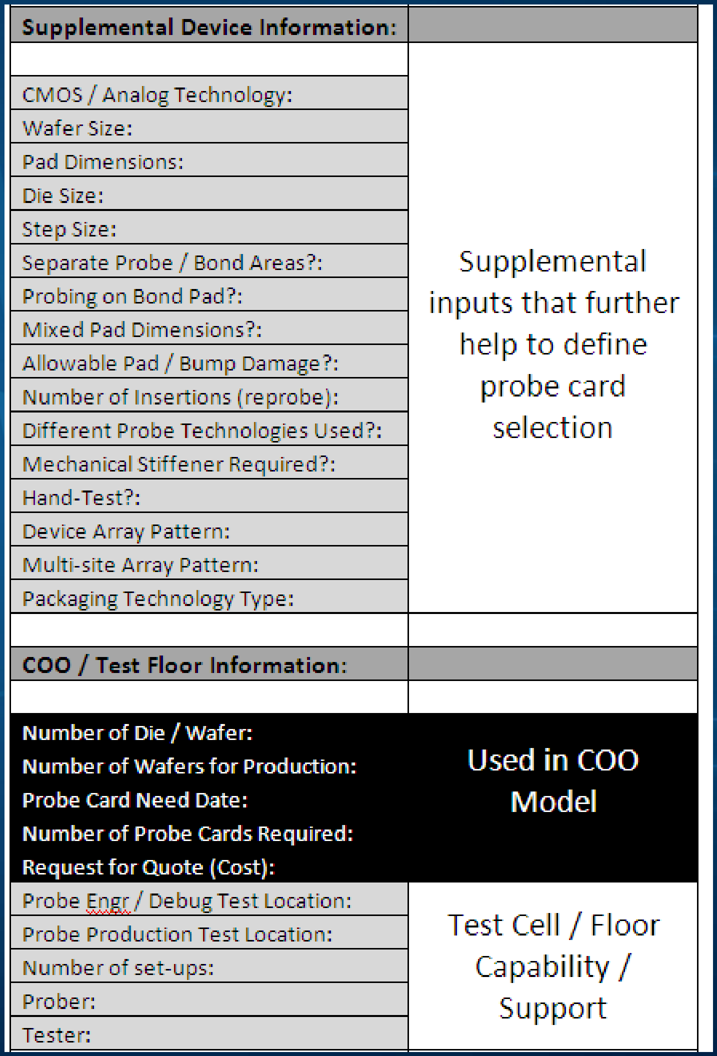
- The Design for Probe Team utilizes the Business Unit’s device input to determine the best probe card technology and vendor. The recommendations are based on cost of ownership models for pricing and lifetime performance.

Device Input for the Selection Process

- **Device Input list requests relevant information about the device.**
- **All parameters are input into the Probe Card Selection Tool to select qualified probe card vendors and technologies.**



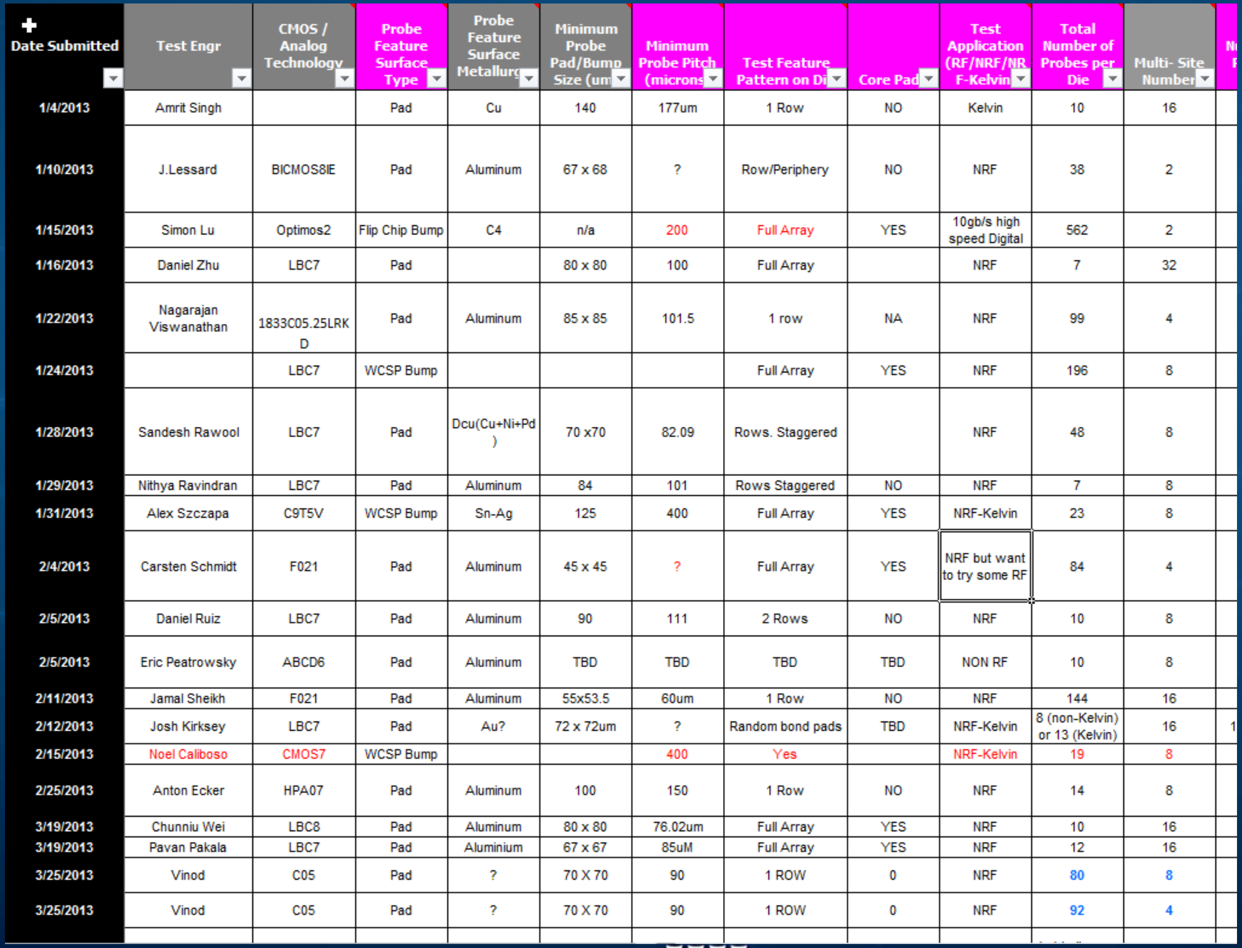
User Information:	
Submitter Name:	Requestor Information
Submitter Email:	
Device Name:	
Device Id:	
Business Unit (SBE):	
Business Unit (LBE):	
Program Manager:	
Test Engineer:	
REQUIRED Device Information:	
Device Test Surface:	Currently used in Probe Card Selection Tool
Pitch:	
Device Test Application:	
Number of Rows:	
Core Pads:	
Bandwidth:	
Current Carrying Capability:	
Probing Temperature:	
Number of pins per site:	
Number of sites:	
Total Number of Probes:	



Supplemental Device Information:	
CMOS / Analog Technology:	Supplemental inputs that further help to define probe card selection
Wafer Size:	
Pad Dimensions:	
Die Size:	
Step Size:	
Separate Probe / Bond Areas?:	
Probing on Bond Pad?:	
Mixed Pad Dimensions?:	
Allowable Pad / Bump Damage?:	
Number of Insertions (reprobe):	
Different Probe Technologies Used?:	
Mechanical Stiffener Required?:	
Hand-Test?:	
Device Array Pattern:	
Multi-site Array Pattern:	
Packaging Technology Type:	
COO / Test Floor Information:	
Number of Die / Wafer:	Used in COO Model
Number of Wafers for Production:	
Probe Card Need Date:	
Number of Probe Cards Required:	
Request for Quote (Cost):	
Probe Engr / Debug Test Location:	Test Cell / Floor Capability / Support
Probe Production Test Location:	
Number of set-ups:	
Prober:	
Tester:	

DFP – Device Spreadsheet Data

- **Sample from Device List.**
- **Collecting different data from each device to allow for easy tracking / review of data.**



Date Submitted	Test Engr	CMOS / Analog Technology	Probe Feature Surface Type	Probe Feature Surface Metallurg	Minimum Probe Pad/Bump Size (um	Minimum Probe Pitch (microns	Test Feature Pattern on Di	Core Pad	Test Application (RF/NRF/NR F-Kelvin	Total Number of Probes per Die	Multi- Site Number	N F
1/4/2013	Amrit Singh		Pad	Cu	140	177um	1 Row	NO	Kelvin	10	16	
1/10/2013	J.Lessard	BICMOS8IE	Pad	Aluminum	67 x 68	?	Row/Periphery	NO	NRF	38	2	
1/15/2013	Simon Lu	Optimos2	Flip Chip Bump	C4	n/a	200	Full Array	YES	10gb/s high speed Digital	562	2	
1/16/2013	Daniel Zhu	LBC7	Pad		80 x 80	100	Full Array		NRF	7	32	
1/22/2013	Nagarajan Viswanathan	1833C05.25LRKD	Pad	Aluminum	85 x 85	101.5	1 row	NA	NRF	99	4	
1/24/2013		LBC7	WCSP Bump				Full Array	YES	NRF	196	8	
1/28/2013	Sandesh Rawool	LBC7	Pad	Dcu(Cu+Ni+Pd)	70 x70	82.09	Rows. Staggered		NRF	48	8	
1/29/2013	Nithya Ravindran	LBC7	Pad	Aluminum	84	101	Rows Staggered	NO	NRF	7	8	
1/31/2013	Alex Szczapa	C9T5V	WCSP Bump	Sn-Ag	125	400	Full Array	YES	NRF-Kelvin	23	8	
2/4/2013	Carsten Schmidt	F021	Pad	Aluminum	45 x 45	?	Full Array	YES	NRF but want to try some RF	84	4	
2/5/2013	Daniel Ruiz	LBC7	Pad	Aluminum	90	111	2 Rows	NO	NRF	10	8	
2/5/2013	Eric Peatrowsky	ABCD6	Pad	Aluminum	TBD	TBD	TBD	TBD	NON RF	10	8	
2/11/2013	Jamal Sheikh	F021	Pad	Aluminum	55x53.5	60um	1 Row	NO	NRF	144	16	
2/12/2013	Josh Kirksey	LBC7	Pad	Au?	72 x 72um	?	Random bond pads	TBD	NRF-Kelvin	8 (non-Kelvin) or 13 (Kelvin)	16	1
2/15/2013	Noel Caliboso	CMOS7	WCSP Bump			400	Yes		NRF-Kelvin	19	8	
2/25/2013	Anton Ecker	HPA07	Pad	Aluminum	100	150	1 Row	NO	NRF	14	8	
3/19/2013	Chunniu Wei	LBC8	Pad	Aluminum	80 x 80	76.02um	Full Array	YES	NRF	10	16	
3/19/2013	Pavan Pakala	LBC7	Pad	Aluminium	67 x 67	85uM	Full Array	YES	NRF	12	16	
3/25/2013	Vinod	C05	Pad	?	70 X 70	90	1 ROW	0	NRF	80	8	
3/25/2013	Vinod	C05	Pad	?	70 X 70	90	1 ROW	0	NRF	92	4	

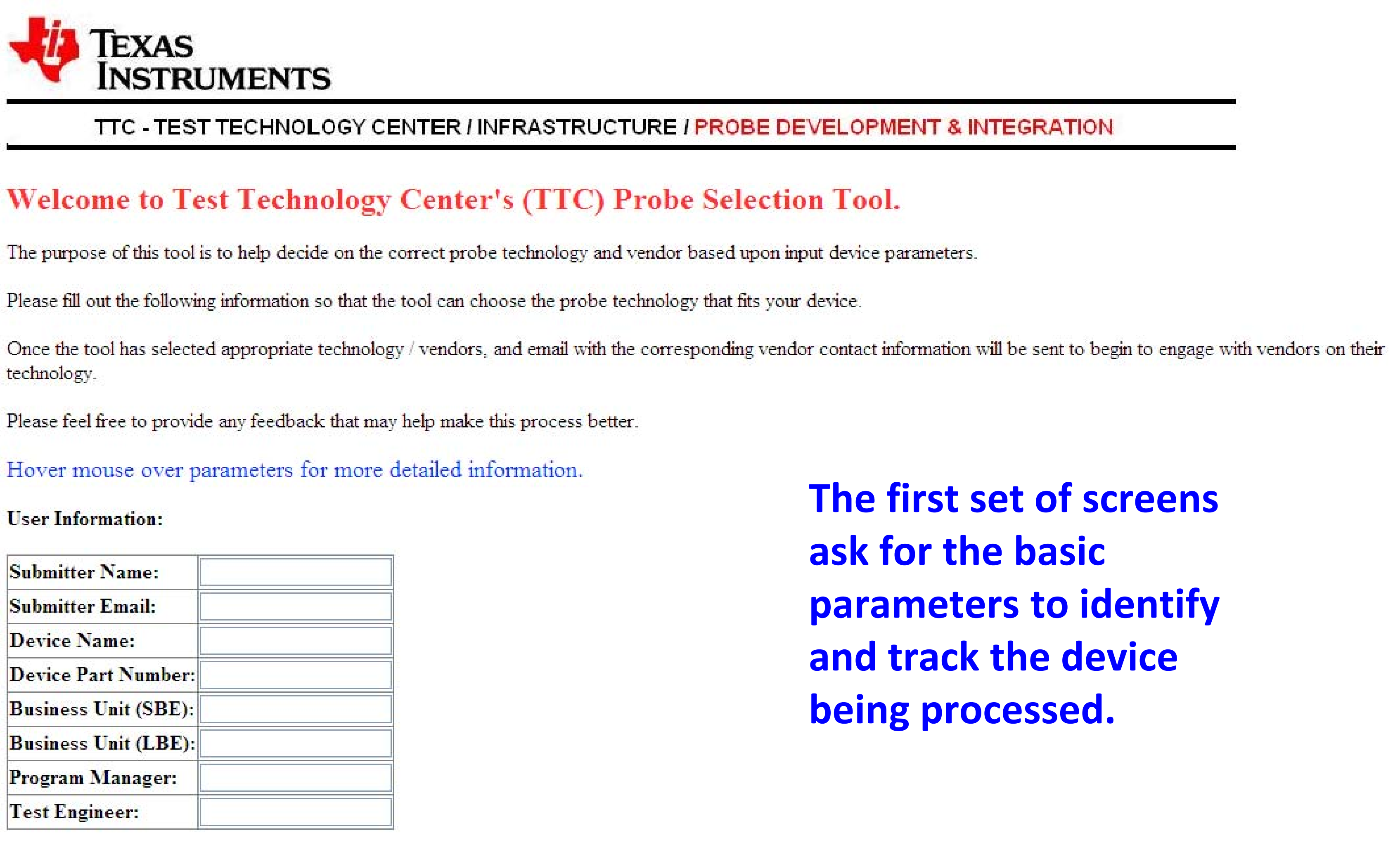
Probe Card Selection Tool: Objective:

- In the past, DFP has relied on manual inputs and “tribal” knowledge of DFP members or TI test community to select an appropriate probe card technology and vendor.

- As a result, the **Probe Card Selection Tool** was developed to automate / capture the probe CTFs-critical to function parameters, to make better and more consistent decisions in a timely and cost-effective manner for TI WW.

- PTS used third party software from Logicnets to aid in automation of the probe card technology decision process in a systematic manner.

Probe Card Selection Tool



TTC - TEST TECHNOLOGY CENTER / INFRASTRUCTURE / PROBE DEVELOPMENT & INTEGRATION

Welcome to Test Technology Center's (TTC) Probe Selection Tool.

The purpose of this tool is to help decide on the correct probe technology and vendor based upon input device parameters.

Please fill out the following information so that the tool can choose the probe technology that fits your device.

Once the tool has selected appropriate technology / vendors, and email with the corresponding vendor contact information will be sent to begin to engage with vendors on their technology.

Please feel free to provide any feedback that may help make this process better.

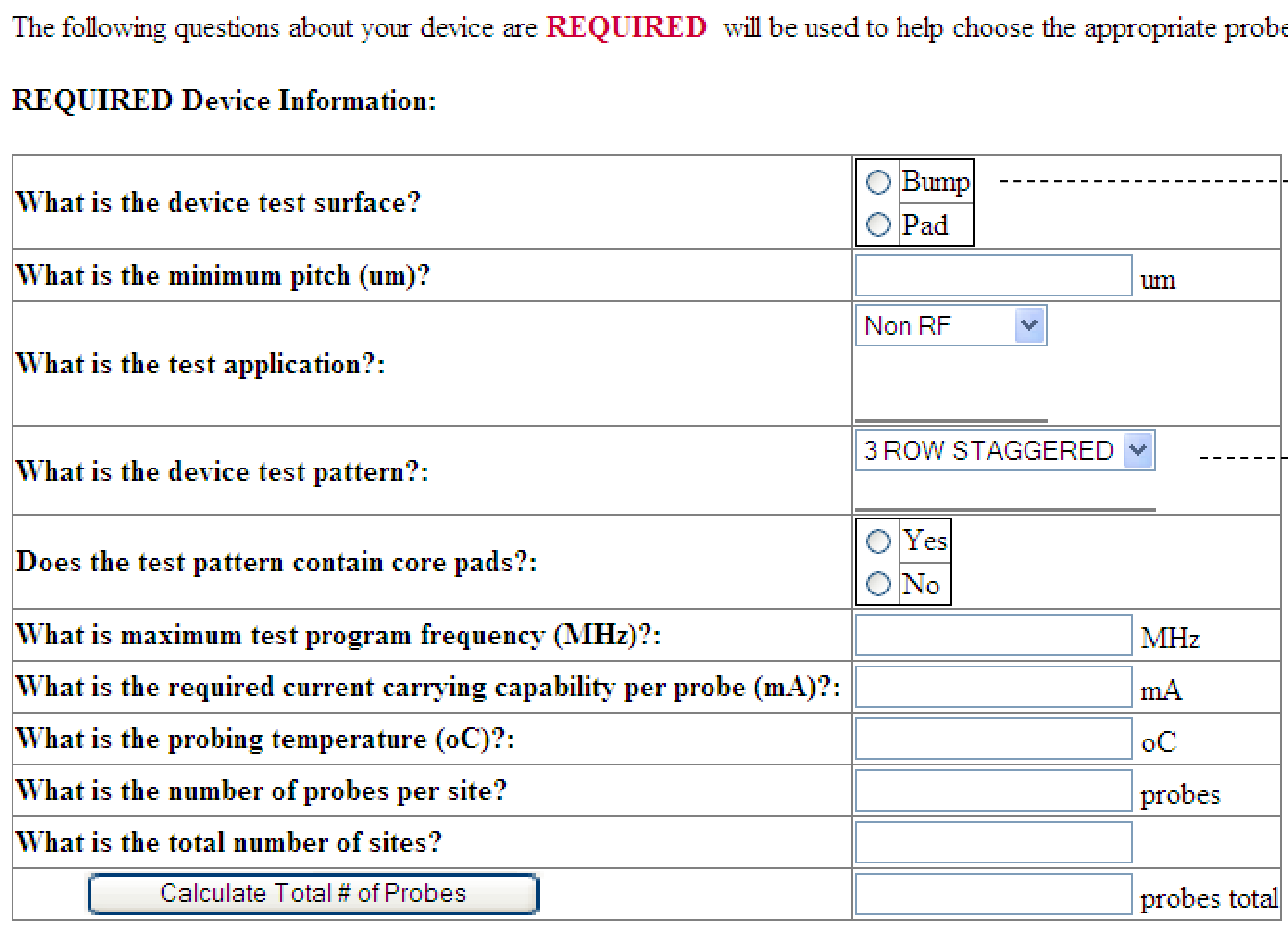
Hover mouse over parameters for more detailed information.

User Information:

Submitter Name:	
Submitter Email:	
Device Name:	
Device Part Number:	
Business Unit (SBE):	
Business Unit (LBE):	
Program Manager:	
Test Engineer:	

The first set of screens ask for the basic parameters to identify and track the device being processed.

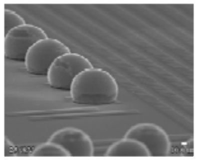
Probe Card Selection Tool: Required Inputs

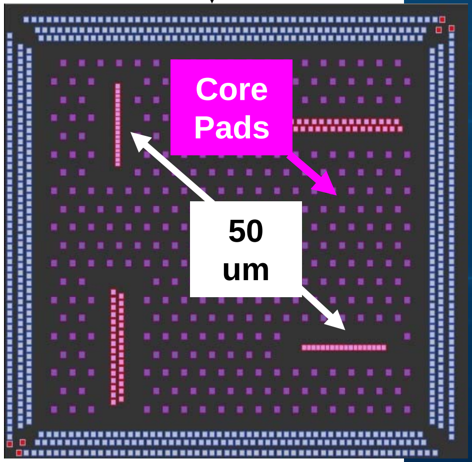


The following questions about your device are **REQUIRED** will be used to help choose the appropriate probe card technology for your device:

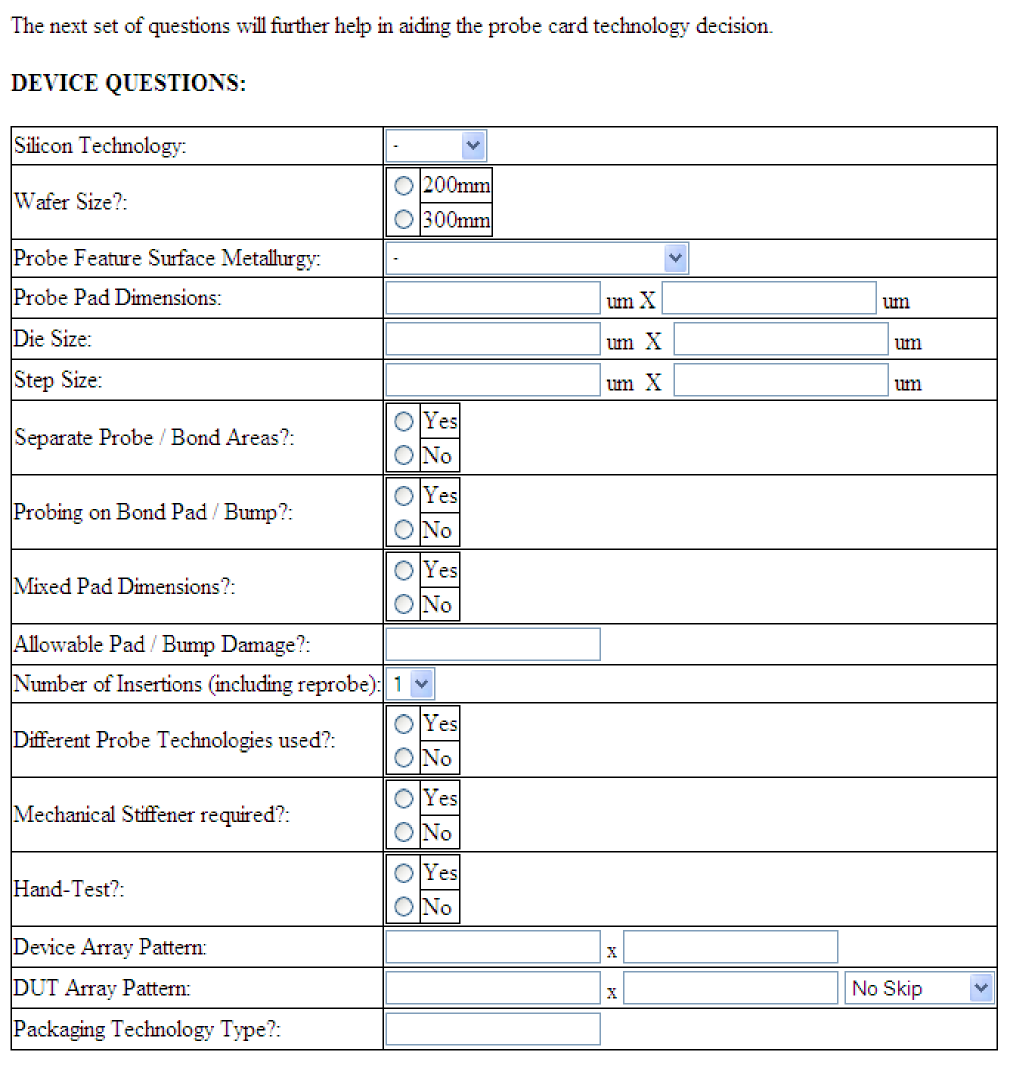
REQUIRED Device Information:

What is the device test surface?	○ Bump ○ Pad	
What is the minimum pitch (um)?		um
What is the test application?:	Non RF	
What is the device test pattern?:	3 ROW STAGGERED	
Does the test pattern contain core pads?:	○ Yes ○ No	
What is maximum test program frequency (MHz)?:		MHz
What is the required current carrying capability per probe (mA)?:		mA
What is the probing temperature (oC)?:		oC
What is the number of probes per site?		probes
What is the total number of sites?		
Calculate Total # of Probes		probes total





Probe Card Selection Tool: Supplemental Device Inputs



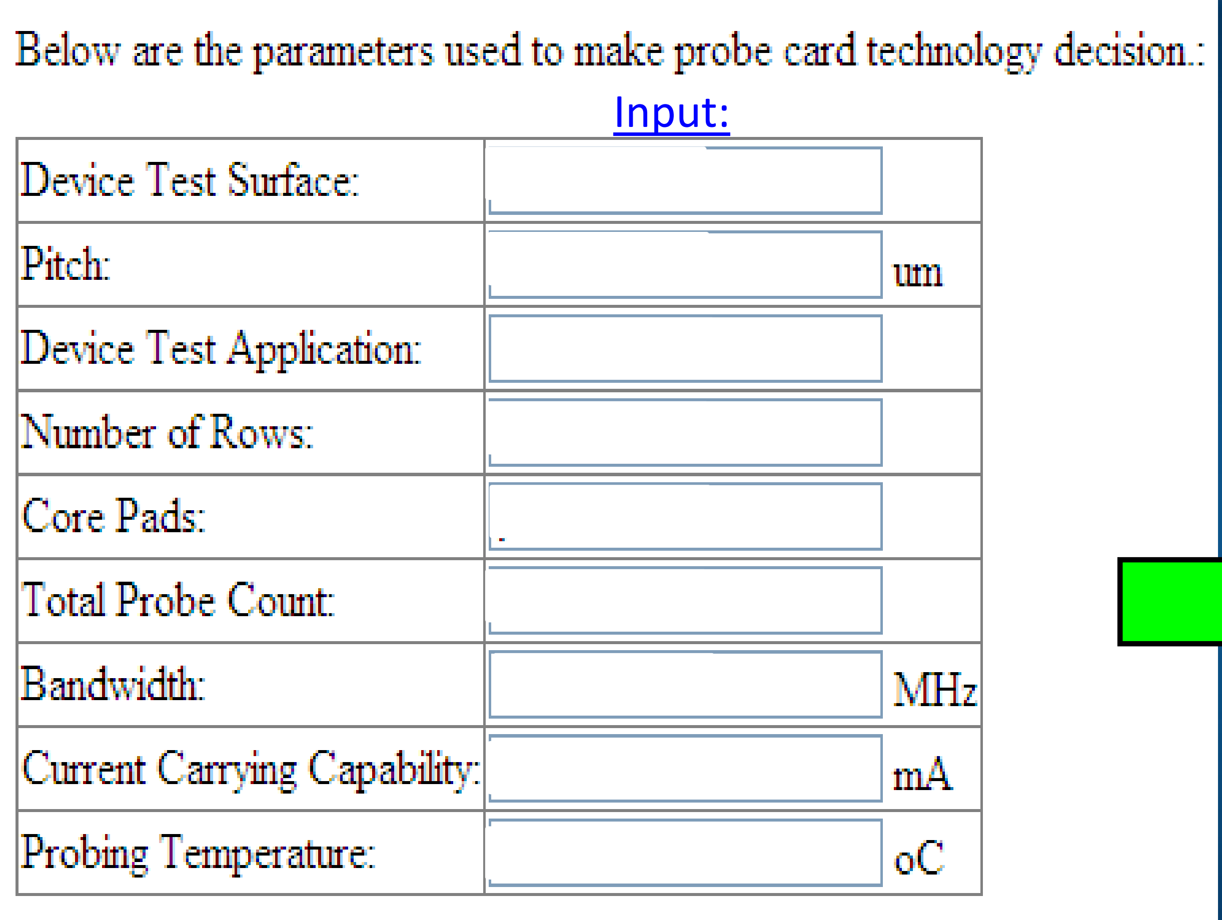
The next set of questions will further help in aiding the probe card technology decision.

DEVICE QUESTIONS:

Silicon Technology:	-
Wafer Size?:	○ 200mm ○ 300mm
Probe Feature Surface Metallurgy:	-
Probe Pad Dimensions:	um X um
Die Size:	um X um
Step Size:	um X um
Separate Probe / Bond Areas?:	○ Yes ○ No
Probing on Bond Pad / Bump?:	○ Yes ○ No
Mixed Pad Dimensions?:	○ Yes ○ No
Allowable Pad / Bump Damage?:	
Number of Insertions (including reprobe):	1
Different Probe Technologies used?:	○ Yes ○ No
Mechanical Stiffener required?:	○ Yes ○ No
Hand-Test?:	○ Yes ○ No
Device Array Pattern:	x
DUT Array Pattern:	x No Skip
Packaging Technology Type?:	

Supplemental information helps to further narrow down vendor / technology decision.

Probe Card Selection Tool: Input and Output



Below are the parameters used to make probe card technology decision.:

Input:

Device Test Surface:		
Pitch:		um
Device Test Application:		
Number of Rows:		
Core Pads:		
Total Probe Count:		
Bandwidth:		MHz
Current Carrying Capability:		mA
Probing Temperature:		oC

EXAMPLE Device

Output:

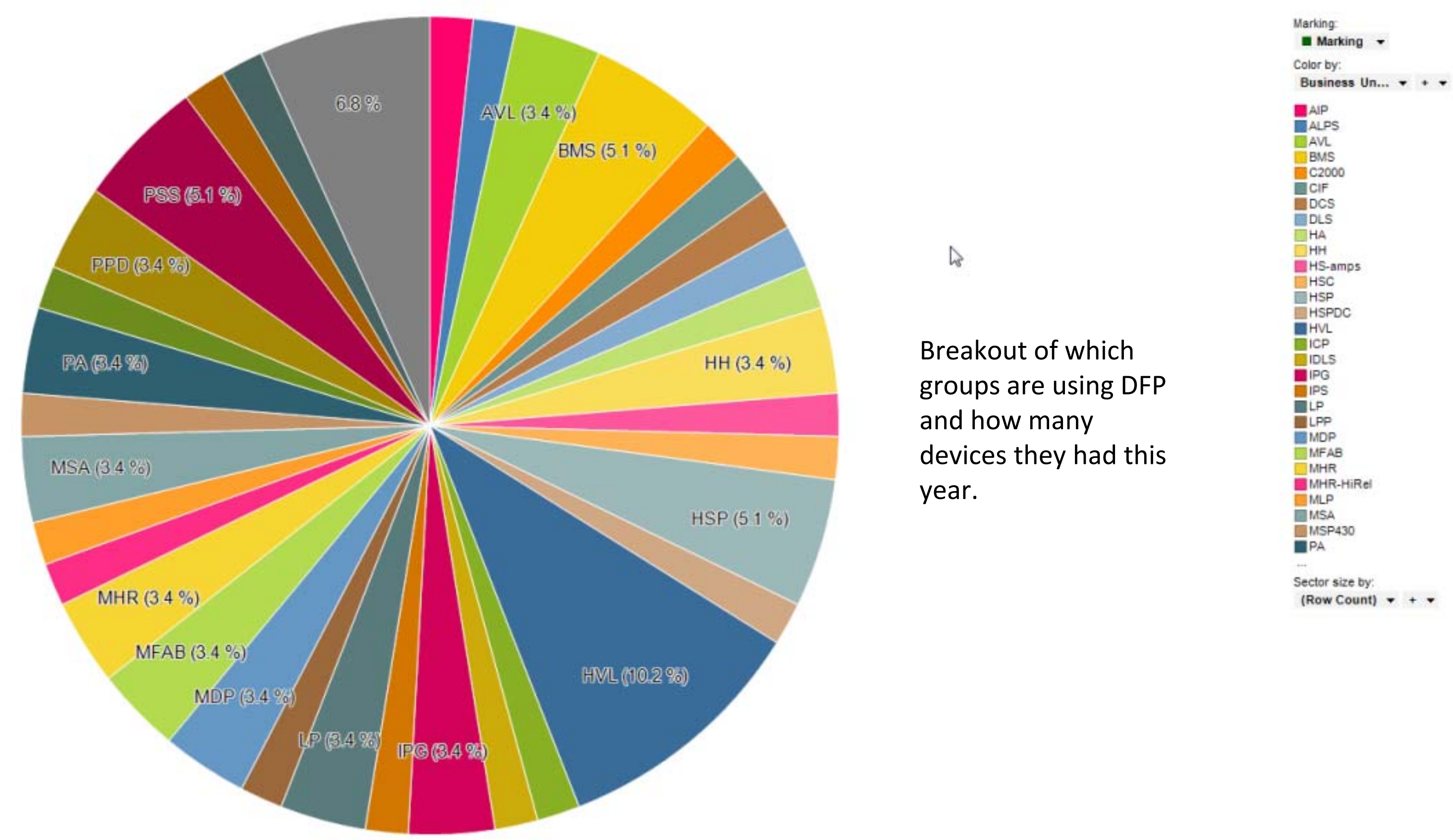
2 Qualified PC Vendors / technologies.

WPL Submits RFQ for LBE review and selection.

Output:

Vendor	Technology	Technology Name	Vendor Contact	Vendor Email	Vendor Website
Superman Inc	Vertical	Kryptonite	Clark Kent	clarkkent@superman.com	www.superman.com
Batman Technologies	Vertical	Crusader	Bruce Wayne	bwayne@batman.com	www.batman.com

2013 DFP Results

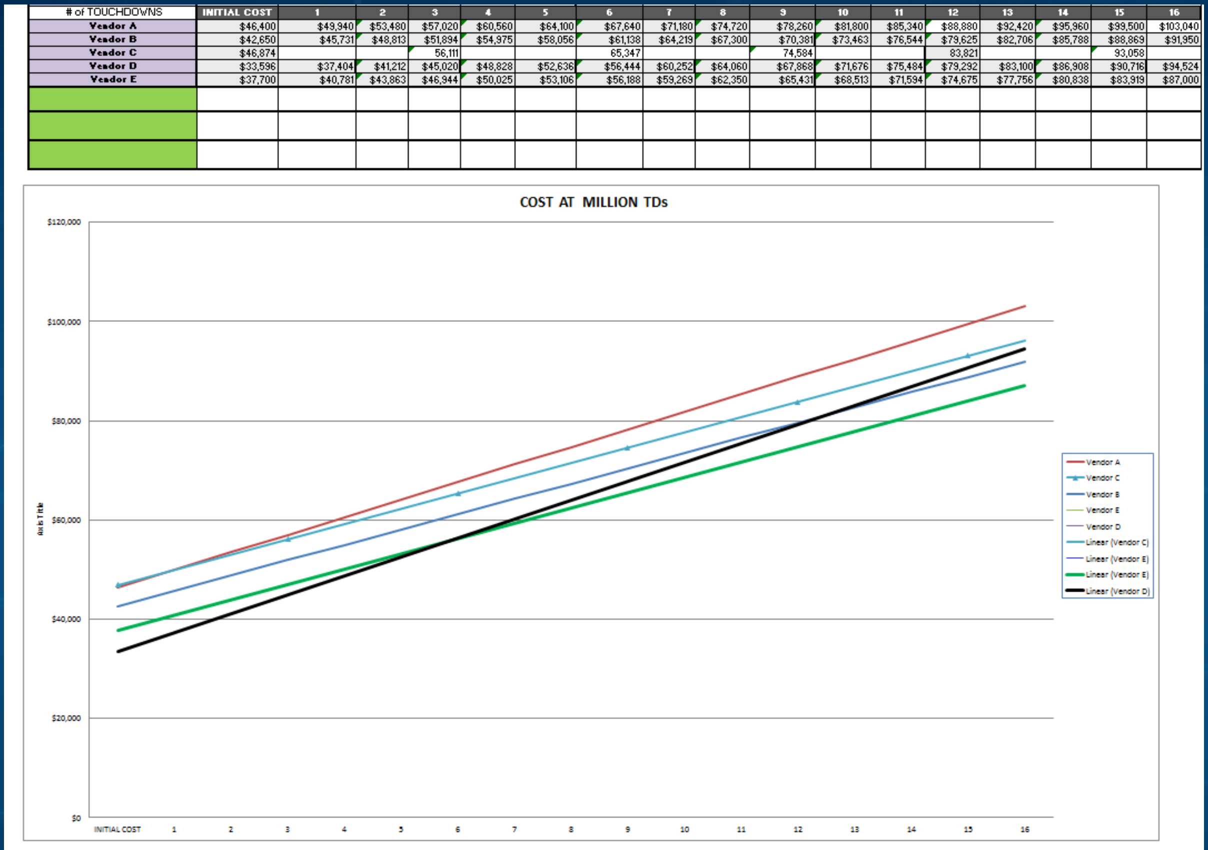


Breakout of which groups are using DFP and how many devices they had this year.

Devices run through DFP this year

- 66% Pad devices
- 33% Bump devices

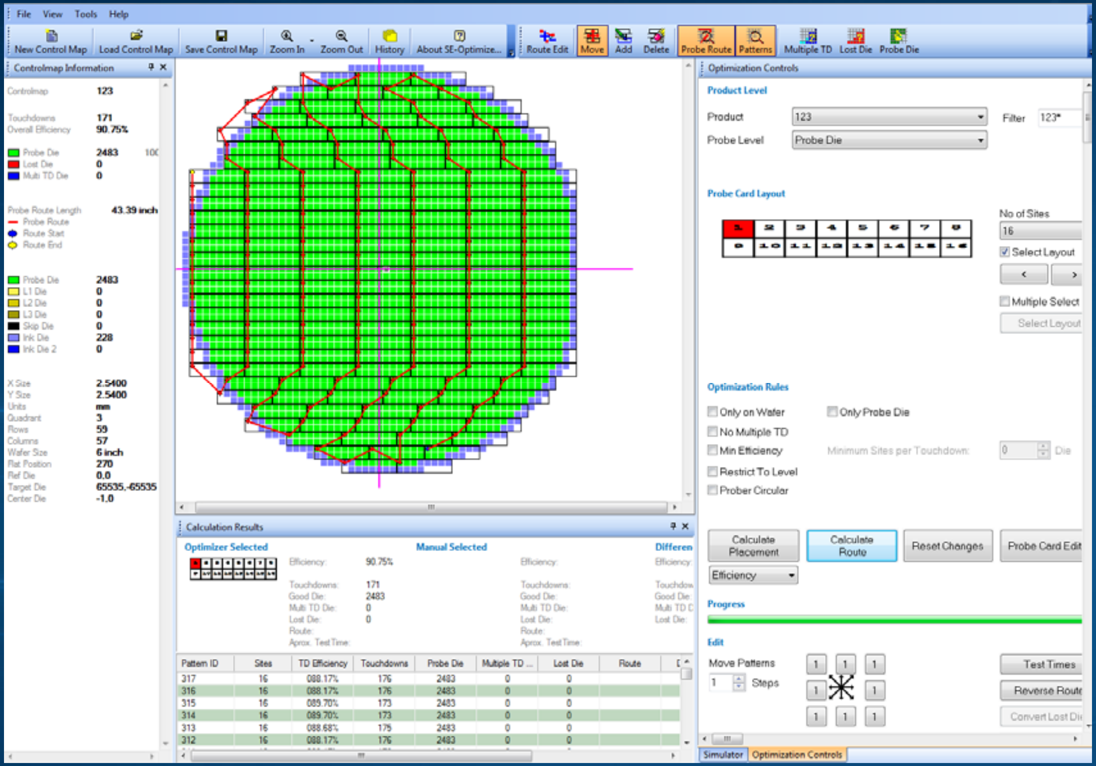
WPL Quoting Process



# of TOUCHDOWNS	INITIAL COST	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Vendor A	$46,400	$49,940	$53,480	$57,020	$60,560	$64,100	$67,640	$71,180	$74,720	$78,260	$81,800	$85,340	$88,880	$92,420	$95,960	$99,500	$103,040
Vendor B	$42,650	$45,731	$48,813	$51,894	$54,975	$58,056	$61,138	$64,219	$67,300	$70,381	$73,463	$76,544	$79,625	$82,706	$85,788	$88,869	$91,950
Vendor C	$46,874			56,111			65,347			74,584			83,821			93,058	
Vendor D	$33,596	$37,404	$41,212	$45,020	$48,828	$52,636	$56,444	$60,252	$64,060	$67,868	$71,676	$75,484	$79,292	$83,100	$86,908	$90,716	$94,524
Vendor E	$37,700	$40,781	$43,863	$46,944	$50,025	$53,106	$56,188	$59,269	$62,350	$65,431	$68,513	$71,594	$74,675	$77,756	$80,838	$83,919	$87,000

- **WPL helps to provide cost analysis between available technologies for each device.**
- **Rebuild cost is also a factor considered when comparing the various vendors.**

Stepping Efficiency



Controlmap 123

Touchdowns 171
Overall Efficiency 90.75%

🟩 Probe Die 2483
🟥 Lost Die 0
🟦 Multi TD Die 0

Probe Route Length 43.39 inch
Probe Route
Route Start
Route End

🟩 Probe Die 2483
🟨 L1 Die 0
🟨 L2 Die 0
🟫 L3 Die 0
⬛ Skip Die 0
🟪 Ink Die 228
🟦 Ink Die 2 0

X Size 2.5400
Y Size 2.5400
Units mm
Quadrant 3
Rows 59
Columns 57
Wafer Size 6 inch
Flat Position 270
Ref Die 0,0
Target Die 65535,-65535
Center Die -1,0

Optimizer Selected
Efficiency: 90.75%
Touchdowns: 171
Good Die: 2483
Multi TD Die: 0
Lost Die: 0
Route:
Aprox. Test Time:

Manual Selected
Efficiency:
Touchdowns:
Good Die:
Multi TD Die:
Lost Die:
Route:
Aprox. Test Time:

Pattern ID	Sites	TD Efficiency	Touchdowns	Probe Die	Multiple TD ...	Lost Die	Route
317	16	088.17%	176	2483	0	0	
316	16	088.17%	176	2483	0	0	
315	16	089.70%	173	2483	0	0	
314	16	089.70%	173	2483	0	0	
313	16	088.68%	175	2483	0	0	
312	16	088.17%	176	2483	0	0	

Product Level
Product 123
Filter 123*
Probe Level Probe Die

Probe Card Layout
No of Sites 16
☑ Select Layout
☐ Multiple Select

Optimization Rules
☐ Only on Wafer
☐ Only Probe Die
☐ No Multiple TD
☐ Min Efficiency
Minimum Sites per Touchdown: 0 Die
☐ Restrict To Level
☐ Prober Circular

Efficiency

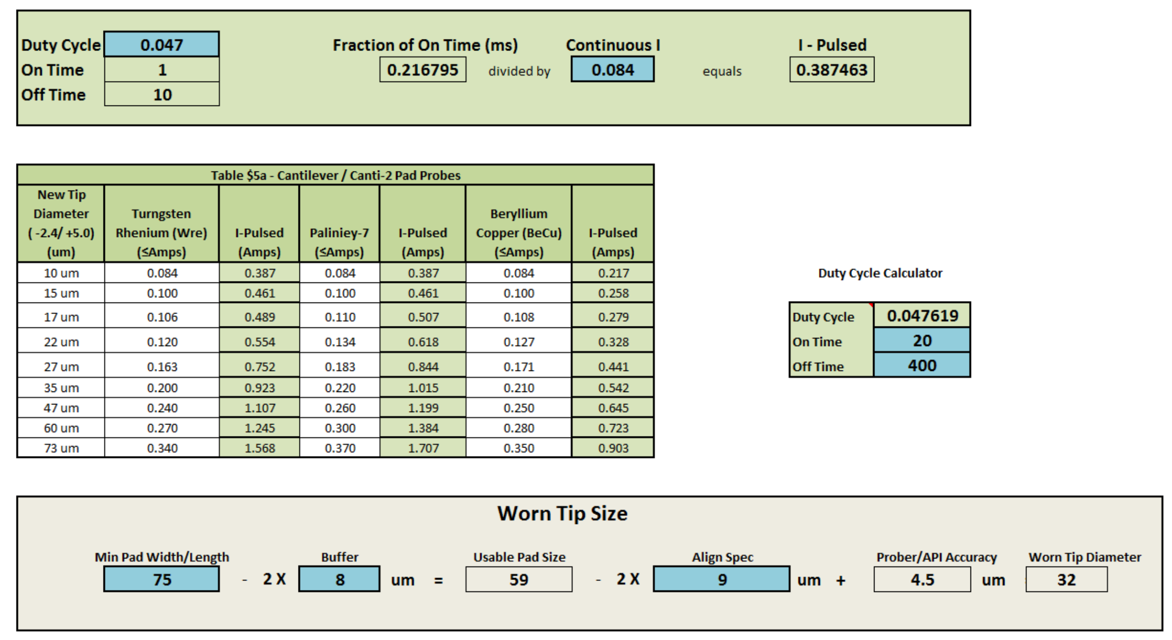
Progress

Edit
Move Patterns 1 Steps

Tool can go through multiple designs in a matter of minutes to find most optimal design based upon wafer layout.

- **Stepping Efficiency Tool can help to quickly determine most optimal stepping efficiency pattern as well as stepping pattern across the wafer.**

Current Modeling Tool



Duty Cycle	0.047	Fraction of On Time (ms)	Continuous I		I - Pulsed
On Time	1	0.216795 divided by	0.084	equals	0.387463
Off Time	10				

Table $5a - Cantilever / Canti-2 Pad Probes

New Tip Diameter (-2.4/ +5.0) (um)	Turngsten Rhenium (Wre) (≤Amps)	I-Pulsed (Amps)	Paliniey-7 (≤Amps)	I-Pulsed (Amps)	Beryllium Copper (BeCu) (≤Amps)	I-Pulsed (Amps)
10 um	0.084	0.387	0.084	0.387	0.084	0.217
15 um	0.100	0.461	0.100	0.461	0.100	0.258
17 um	0.106	0.489	0.110	0.507	0.108	0.279
22 um	0.120	0.554	0.134	0.618	0.127	0.328
27 um	0.163	0.752	0.183	0.844	0.171	0.441
35 um	0.200	0.923	0.220	1.015	0.210	0.542
47 um	0.240	1.107	0.260	1.199	0.250	0.645
60 um	0.270	1.245	0.300	1.384	0.280	0.723
73 um	0.340	1.568	0.370	1.707	0.350	0.903

Duty Cycle Calculator

Duty Cycle	0.047619
On Time	20
Off Time	400

Worn Tip Size

Min Pad Width/Length		Buffer		Usable Pad Size		Align Spec		Prober/API Accuracy		Worn Tip Diameter
75	- 2 X	8	um =	59	- 2 X	9	um +	4.5	um	32

- Developed a tool to help provide guidelines on which technologies / vendors can handle device required current.
- Tool available to use in DFP process so that we can make sure technology chosen can handle required current.

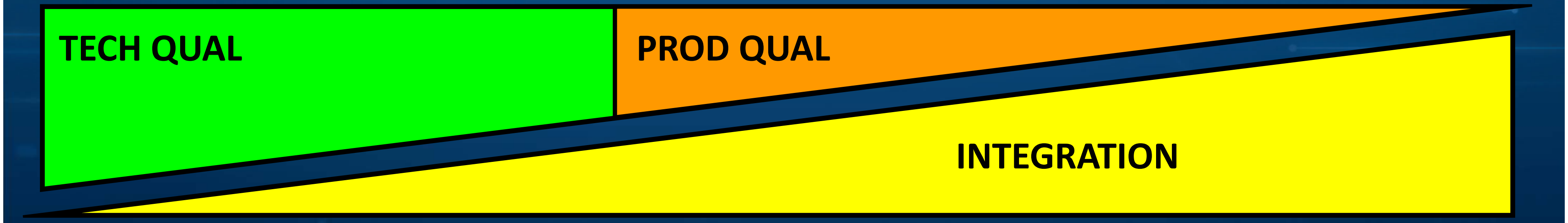
TI Qualified Vendors

TI Qualified Vendors

- For each vendor used, an extensive qualification process is used to ensure that the vendor / technology performs up to standard mechanically and electrically over time.
- Part of this qualification is also a cleaning evaluation to ensure that cleaning procedures / cleaning media are optimal.

Qualification Process

Technology - Production QUALIFICATION	
PASSES Category	Meets required CTF-Critical To Function parameters. Passes qualification category for the particular probe requirements envelope or node intended. e.g. 70 um, x32/x64 multi-site enablement
PASSES Category	Meets most CTF-Critical To Function parameters. Passes qualification step. However, contingent on additional data, data analysis either on-line or off-line to resolve.
DOES NOT QUALIFY	Does not meet most CTF-critical to function parameters. Does not pass qualification category. Not considered a show-stopper; however, ARs required to be resolved
DOES NOT QUALIFY	Does not meet required CTF-critical to function parameters. Does not pass qualification category. Considered a show-stopper, significant work required to resolve.



Qualification Worksheet

Test	Requirement	Total Qual	Cleaning Qual	Results	Data	Pass/Fail
bin to bin correlation	98% bin to bin from baseline card to new probe technology or LBE/PDE acceptance	X		94% bin to bin correlation approved by the LBE Yvonne So	Bin2Bin	Pass
Dielectric cracking	Dielectric cracking study Automotive requirement 9x TD in the same location and max production probing OT) –	X		No dielectric cracking report needed for Bump Material		NA
Punch through	No under layer metal exposure on automotive products QSS states for Al technologies "shall not expose underlying passivation or underlying metal equal to or greater than 25% of the pad width adjacent to the edge of the pad or exceeds 1.0mil2 near the center of the bond pad.	X		No punch through report need for bump material		NA
Cres over time	3 Ohms Standard deviation 100k TD and a minimum 100 wafers Probed	X	X	Cleaning Media 1um Grit ProbeLapp Cleaning Settign 25 wafer TD 10 Cres across 9k dies 0.15Ω Stdev	Cres Data	Pass
Cleaning rotation as it relates to Cres and contact related bin fails	How many rotations of the cleaning material?	X	X	Cleaning Media 1um Grit ProbeLapp Cleaning Settign 25 wafer TD 10 Cres across 9k dies 0.15Ω Stdev	Cres Data	Pass
New material has a requirement of a MSDS, no polyethylene allowed, high temp transfer study is needed		X	X	ProbeLap is currently used in production at -40 - 200C	MSDS	Pass
Life time study	**100k TD and a minimum 100 wafers Probed** in production or accelerated probing and cleaning wear study to show the TD vs. Tip length as it relates to probe card end of life. (life expected must be (>750K TD)	X	X	Card Life Data shows TD production probing	Life Time Data	Pass
Prober device file set up needle tip alignment settings		X		Needle tip Algorithm 0 Standard size		Pass
AVI fail rate	fail rate must be less the 0.25% across 20 EWR lots at all temperatures.	X		No AVI data for Bump probing		NA
Bump Damage	Damage must meet all packaging requirments	X		Mushroom probing showed no damage Reflow bumps require packaging sample eval YIELD: FT1- 98.94% PB2- 97.96% PB3- 99.66%	Bump Damage	Pass
Thermal agility	X, Y, Z correction across a wafer must be lest the 30um min to max without dramatic swings not including stops to the prober with in a wafer once the card gets to temps	X		Bump devices do not probe at high temp no optical alignment data needed		NA

- PHYSICAL
- DESIGN PROCESS
- MANUFACTURING
- SUSTAINABILITY
- TEST PERFORMANCE
- RELIABILITY
- TEST OPERATIONS
- FUTURE APPLICABLITY
- COST OF OWNERSHIP
- OVERALL ASSESSMENT

Probe Card Technology

Probe Card Technologies Categories vs. TI Device Node/Test Feature Probe Requirements RM:

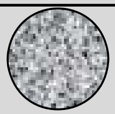
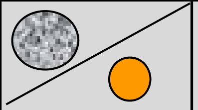
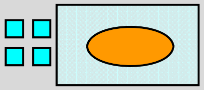
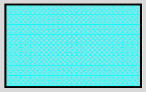
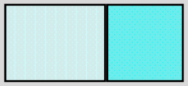
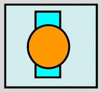
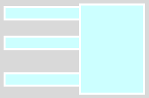
WSP Wafer Socket Probe (Pogo-Pin)	AFC Advanced Flip Chip	C-VPC Conventional Vertical	A-VPC Advanced Vertical	Cantilever / Canti-2

WCSP Balls………………………. FC / Cu Bumps

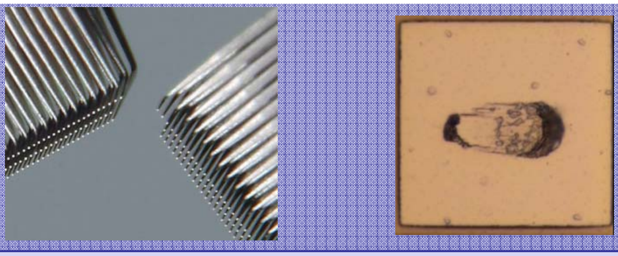
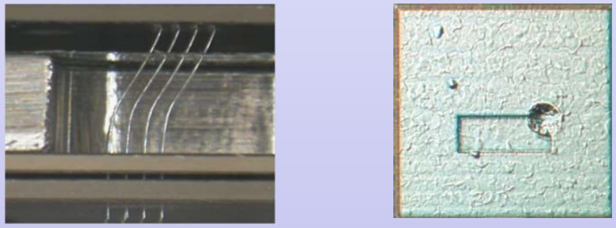
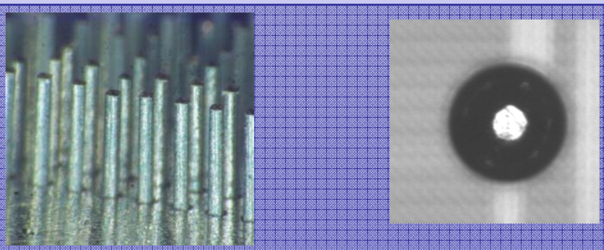
Min Pitch 400…300……….150um

Al Pads…………… (BOAC)NiPd Pads

400…………………..50um

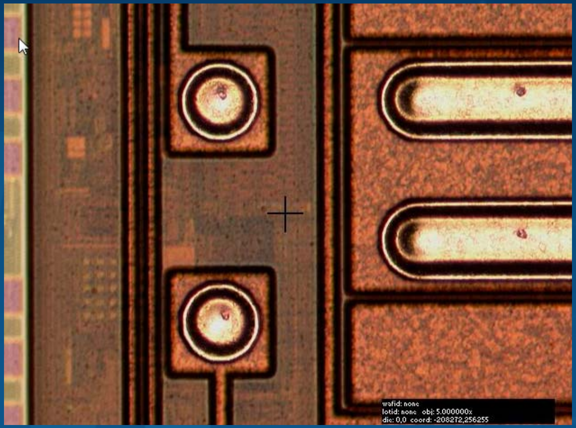
	TI-Node RM >>	WCSP	FC / Cu Pillar	C28	C027	C021	C014	LBCX / HPA07
TI Probe RM / CTFs	Pitch um	400	150	40/80/100	60	50	30/60	NA
	Size um	200	75	45x75	55x65	45x63.5	45x45	NA
	Feature Shape							
	Rows / Array	Full Array / 1500 pins	Full Array / 20000+ pins	3 Rows Cores 8000pins	1 Row 2000pins	1 Row Cores 3000 pins	2 Rows Cores 4000pins	Full Array / 1600 pins
	% Max Scrub Area	<33%	<33%	*<10%	<25%	<75%	*<10%	TBD

Probe Card Technologies

Technology	Example Probe Mark
Cantilever	
Vertical	
Conventional VPC	
WSP – Pogo Pin	

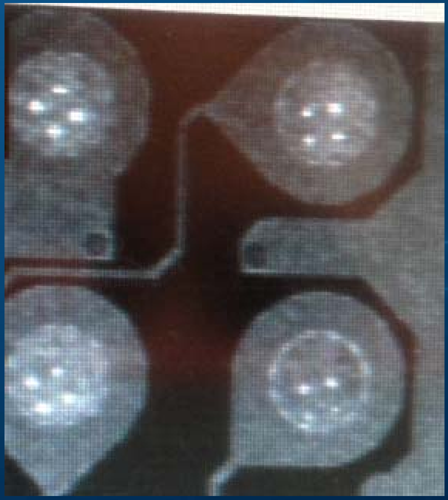
Recent Quals

- Ultra High Temp
- Cu Pillar Probing
- High Voltage (>1KV)
- High RF



Example of Cu pillar structures.

Example of Cu Pads probed with a WSP technology.

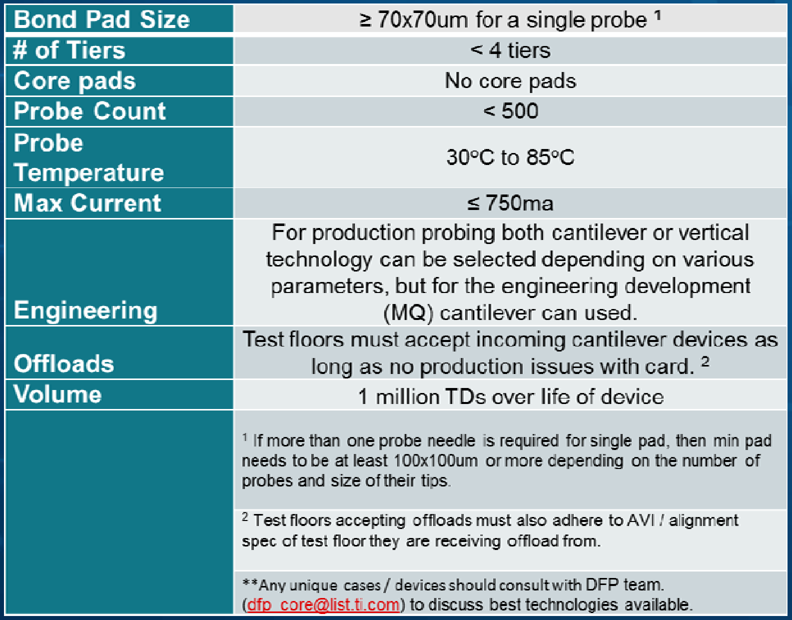


Probe Test Solution
Specifications / Documentation

Probe Card Build Spec

- **Released Probe Card Build Spec**
  - This document is to provide guidelines for probe card vendors on specifications to build probe cards

Example Info from Spec:



Bond Pad Size	≥ 70x70um for a single probe [1]
# of Tiers	< 4 tiers
Core pads	No core pads
Probe Count	< 500
Probe Temperature	30°C to 85°C
Max Current	≤ 750ma
Engineering	For production probing both cantilever or vertical technology can be selected depending on various parameters, but for the engineering development (MQ) cantilever can used.
Offloads	Test floors must accept incoming cantilever devices as long as no production issues with card. [2]
Volume	1 million TDs over life of device
	[1] If more than one probe needle is required for single pad, then min pad needs to be at least 100x100um or more depending on the number of probes and size of their tips.
	[2] Test floors accepting offloads must also adhere to AVI / alignment spec of test floor they are receiving offload from.
	**Any unique cases / devices should consult with DFP team. (dfp_core@list.ti.com) to discuss best technologies available.

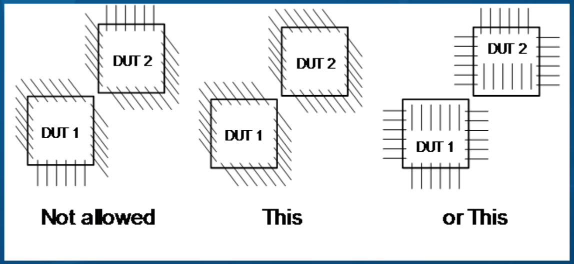
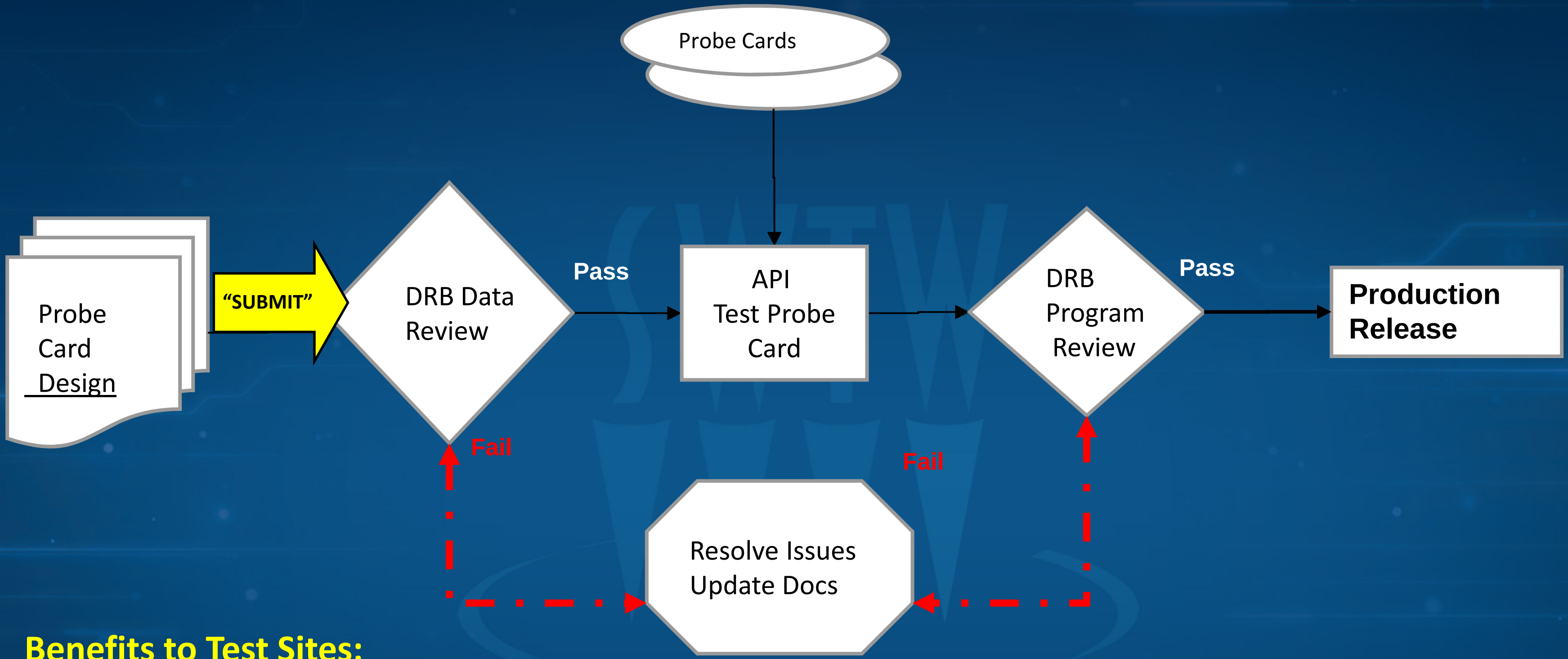


Diagram shows that the build direction of the probes for cantilever cards must either be straight or all diagonal. No mixing of straight and diagonal builds.

Cantilever Acceptance Guidelines recently added to place some general guidelines when cantilever versus vertical technology makes sense.

Design Review Process Flow



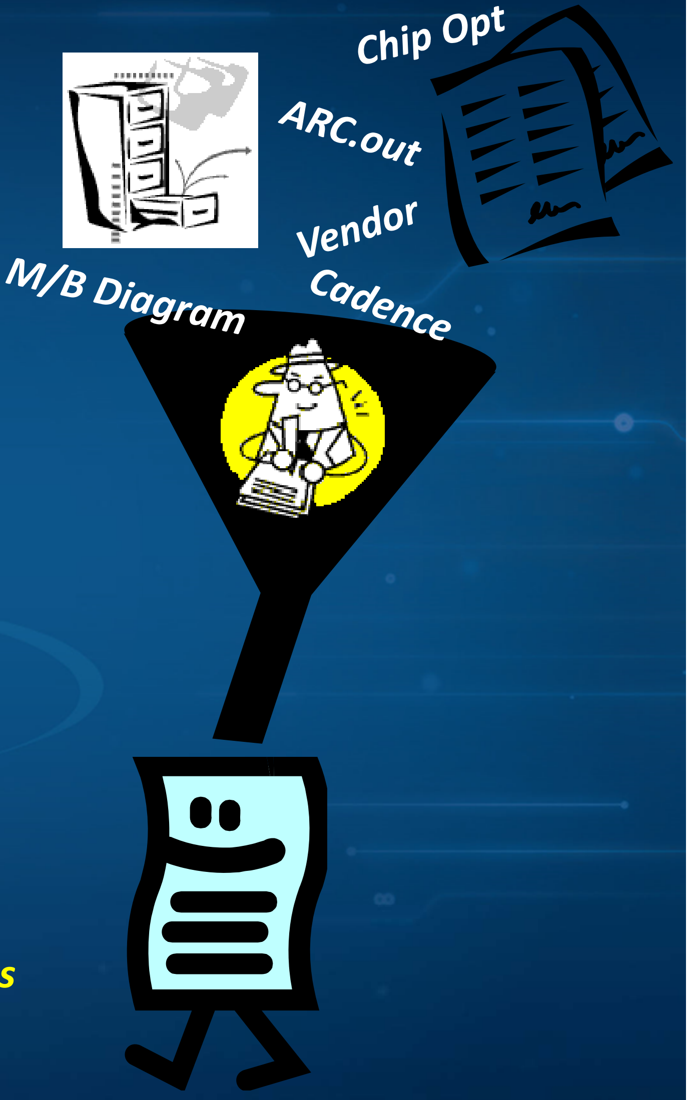
- **Benefits to Test Sites:**
  - The PBD provides TI Test Groups with the documentation needed to repair, maintain, and order new builds for production probe cards
    - Onsite repair reduces tester downtime and offsite repair time
    - Dual sourcing of New Orders and Rebuilds help control cycle time and cost.
- **Benefits to TI:**
  - All probe card documentation resides in TI systems
  - Accurate build data reduces build errors and avoids reverse engineering.
  - Having the information needed to complete the order helps vendors control their cycle times.

PBD Sources and Benefits

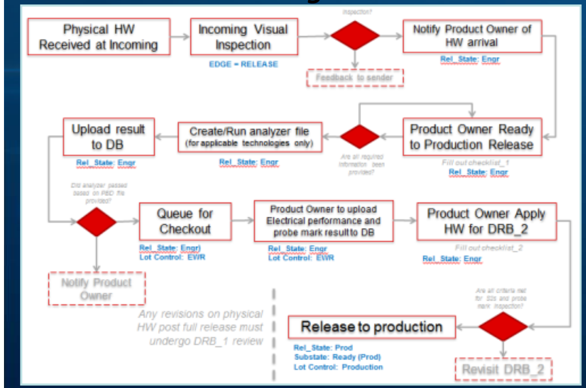
Probe Card Build Data

- The Probe Build Document (PBD) provides the details required to build TI's Probe Cards
- Today Probe Card build data is scattered across multiple documents until combined in the PBD.
  - PBD Sources:

    Arc, ChipOpt, Cadence, M/B diagram; Vendor; etc
- Once Completed and released on EDGE, it is ready for review by a TI test site



Test Site Design Review



PBD Benefits:

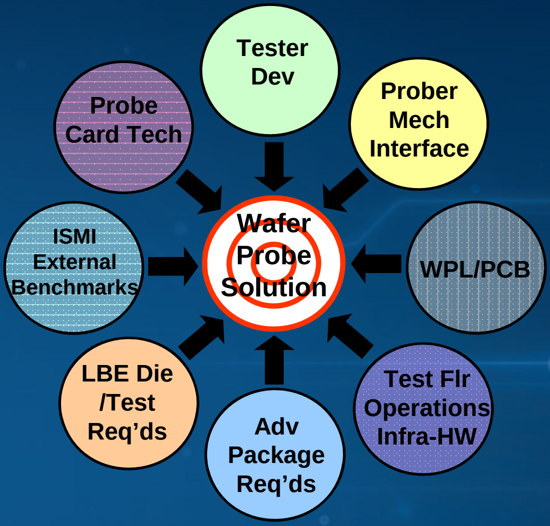
- ***Design For Probe***
- ***Support Multiple Suppliers***
- ***Design data for new technology***
- ***Repair/Maint support at test sites***

EDGE Release Complete

PBD Finalized

What are the benefits of Design For Probe Process???

- We are a support organization that has constant communication with the various pieces required for probe card solution.
- Meet on a weekly basis with test floors to get feedback and discuss any issues that have surfaced as well as any new qualifications / optimizations that are taking place.
- We maintain many specifications that help to provide the outline for how probe card should be designed.
- Interface with WPL and PC vendors so can help work through issues where cards not performing as should and make sure communicated back to vendors
- Utilizing the DFP team and its resources helps to provide <u>the most optimal robust probe solutions for TI!</u>



Wafer Probe Solution

Tester Dev

Prober Mech Interface

WPL/PCB

Test Flr Operations Infra-HW

Adv Package Req’ds

LBE Die /Test Req’ds

ISMI External Benchmarks

Probe Card Tech

Questions

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Thanks!

- **DFP Team**
  - Dawn Copeland
  - Al Wegleitner
  - Piper Oostdyk
  - Dale Anderson
  - Harry Singh
  - Walt Edmonds
- **TI BUs**
- **TI Test Floors**
- **The many probe card vendors we interface with!**