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Advance Low Force Probe cards Used on Solder Flip Chip Devices

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Overview

- **Probe Solution Requirements**
- **Material Properties and Performance**
- **Production Results**
  - Probe Card Planarity
  - Bin to Bin Correlation
  - Bump Damage
  - Cres Over Time
  - Life Time Data
  - Interposer Longevity
  - Burnt Probes
  - Production Up time MTdBF

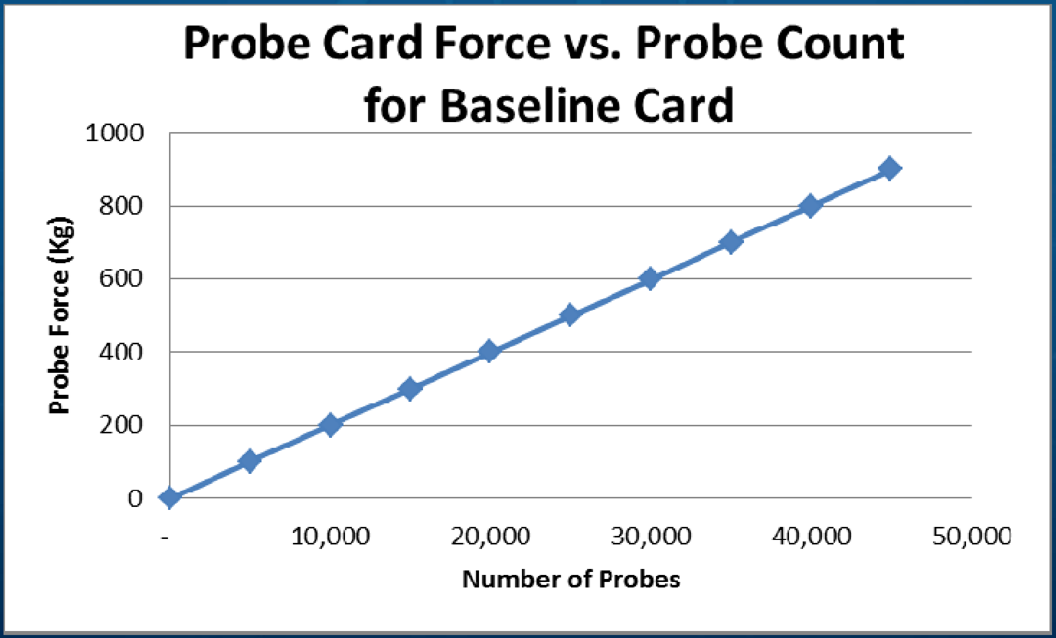
The Probe Solution Must Meet These Requirements

1. Handle high probe count cards
    - Increased solder flip chip die size and performance is pushing the need for more bumps to be tested
    - Reduction in test cost along with faster test time is pushing for higher parallelism at test this is forcing the demand to have greater then 20,000 probes per card
2. Have controlled Cres (Contact resistance)
    - Cres is a key factor on probe card performance
    - Without stable Cres, the overall wafer yield will drop
    - Burnt probes on power supplies will increase
3. On-site probe Re-placement
    - Less down time for damaged and burnt probes

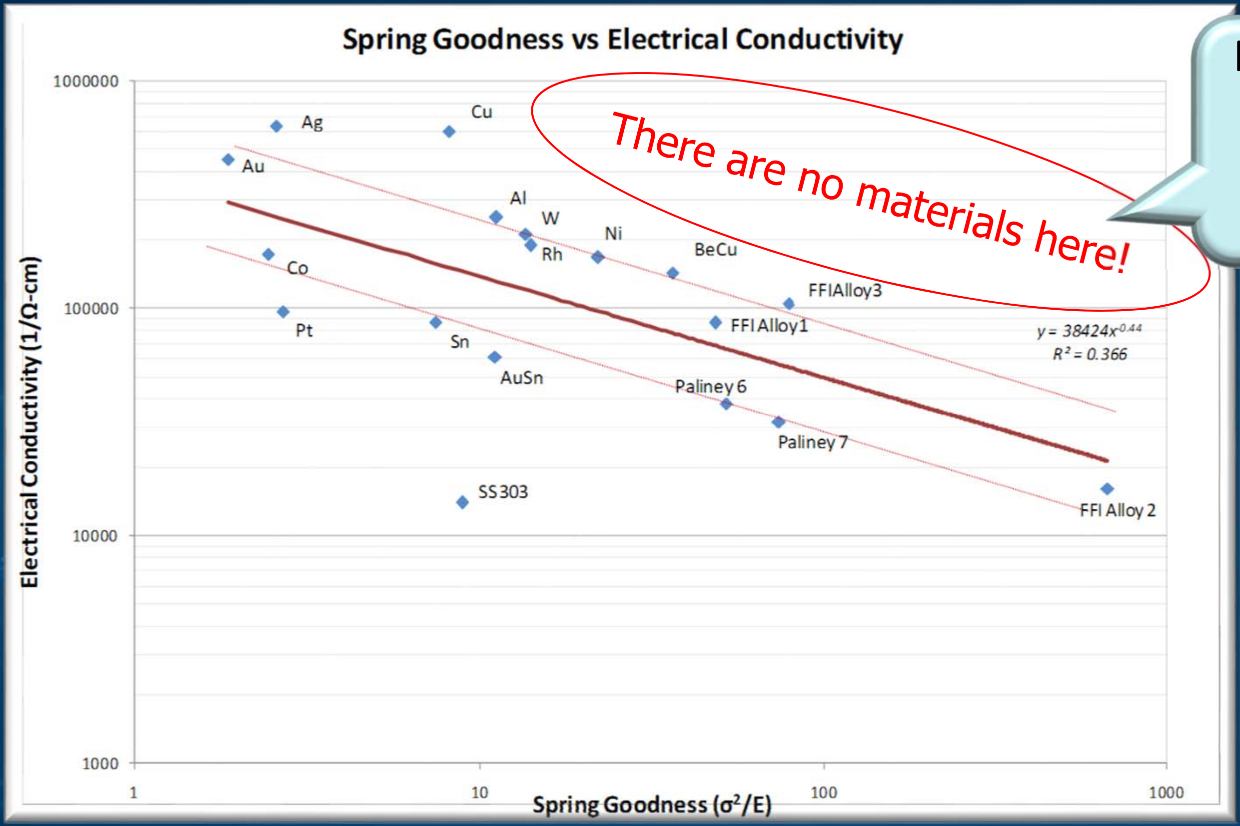
4. Long probe card life greater then 2M touch downs

3. Low probe pin force

- Higher the spring count on a card increases the spring force
- Depending on the prober model the amount of force can limit the prober chuck from moving the programmed over travel
- If total force is too high, PCB and MLC deflection could occur
- Probe Force x Number of Probes x Probing Over Travel = Probe Force



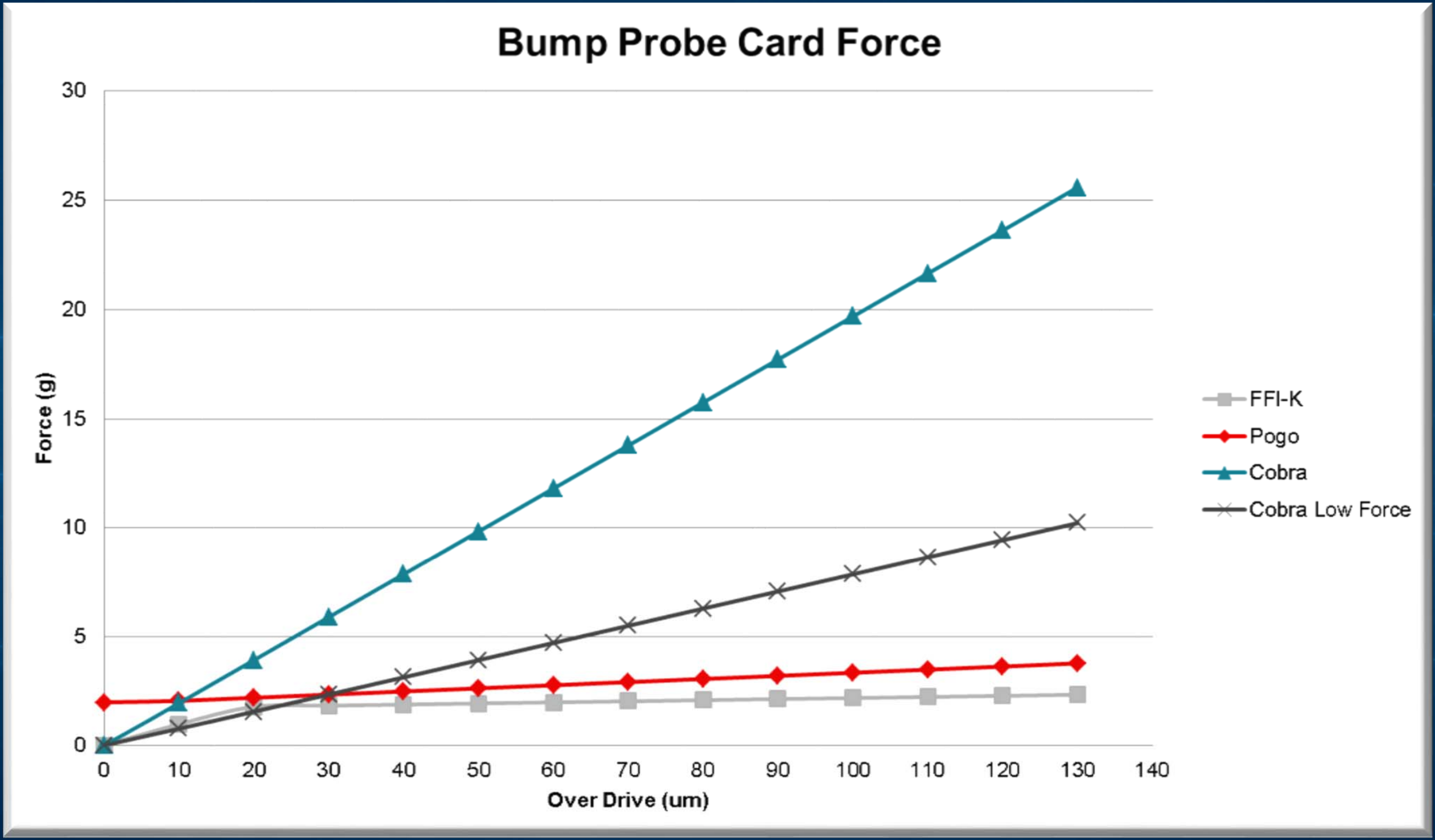
Electrical vs. Mechanical Material Properties



MEMS gives us the ability to build a spring that meets good conductivity and spring force

- Materials that exhibit good electrical conductivity are generally pure metals and have low yield strengths - they make poor springs
- Materials that exhibit good spring characteristics have high yield strengths and low modulus - they make poor electrical conductors.

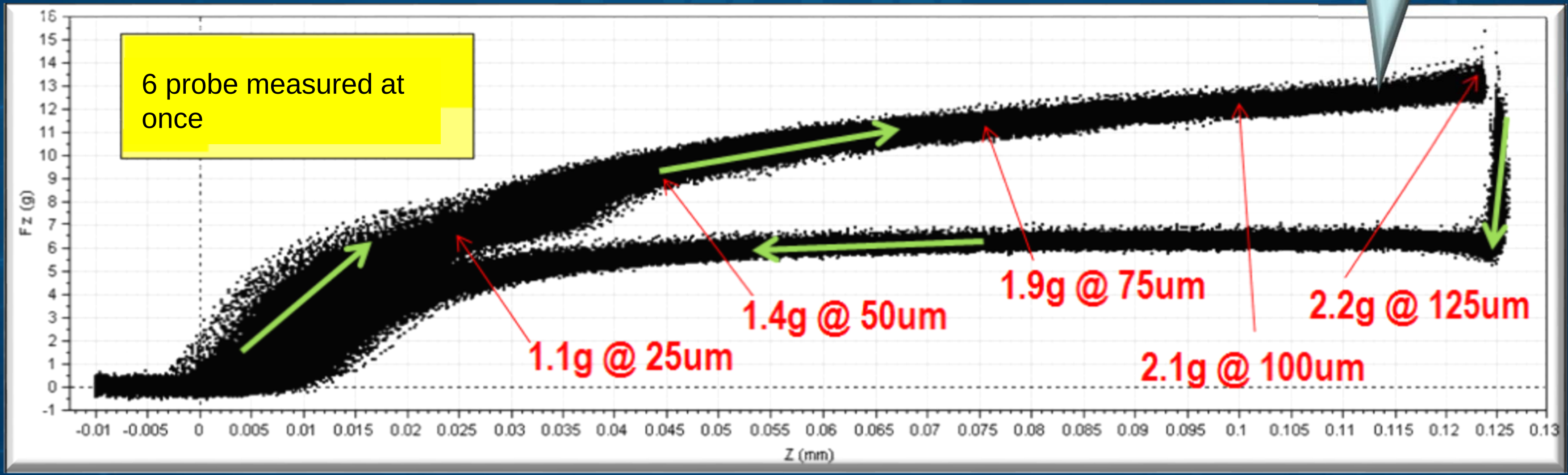
Probe Card Force



FFI Spring Performance

Full Probe cycle of being compressed and released

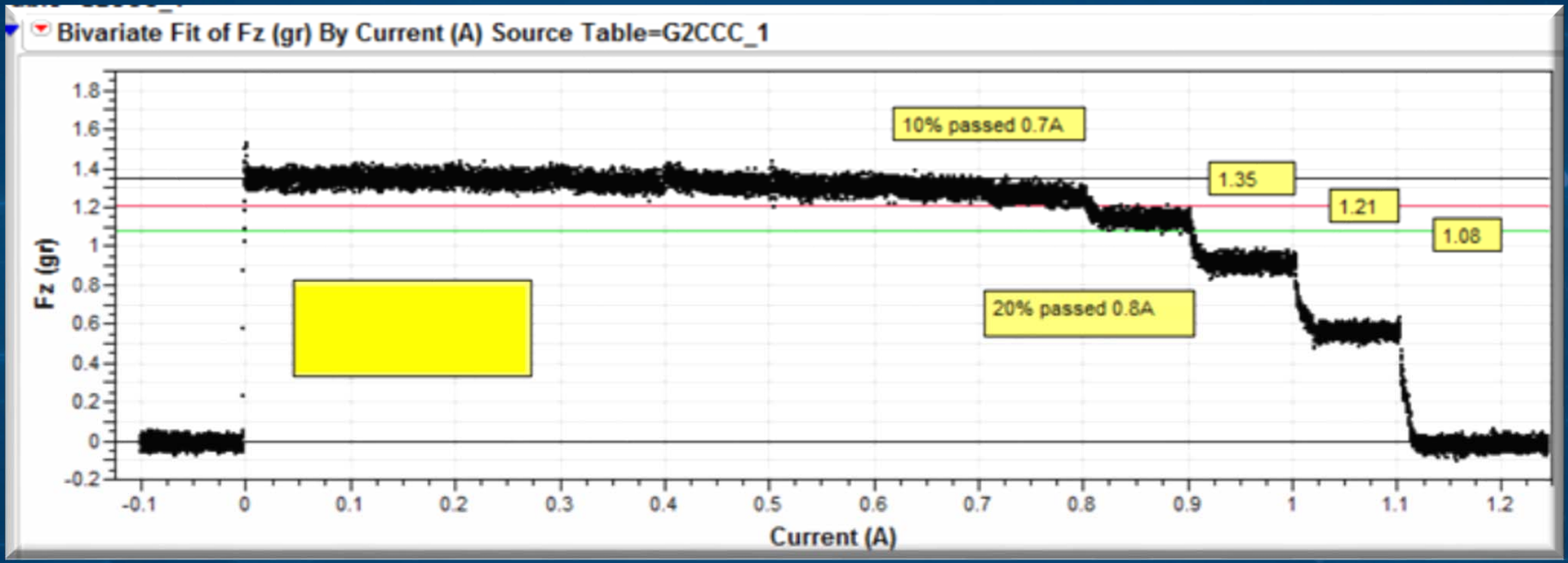
Probe Force vs. Over Travel



Data after 1.5M cycles

FFI Spring Performance

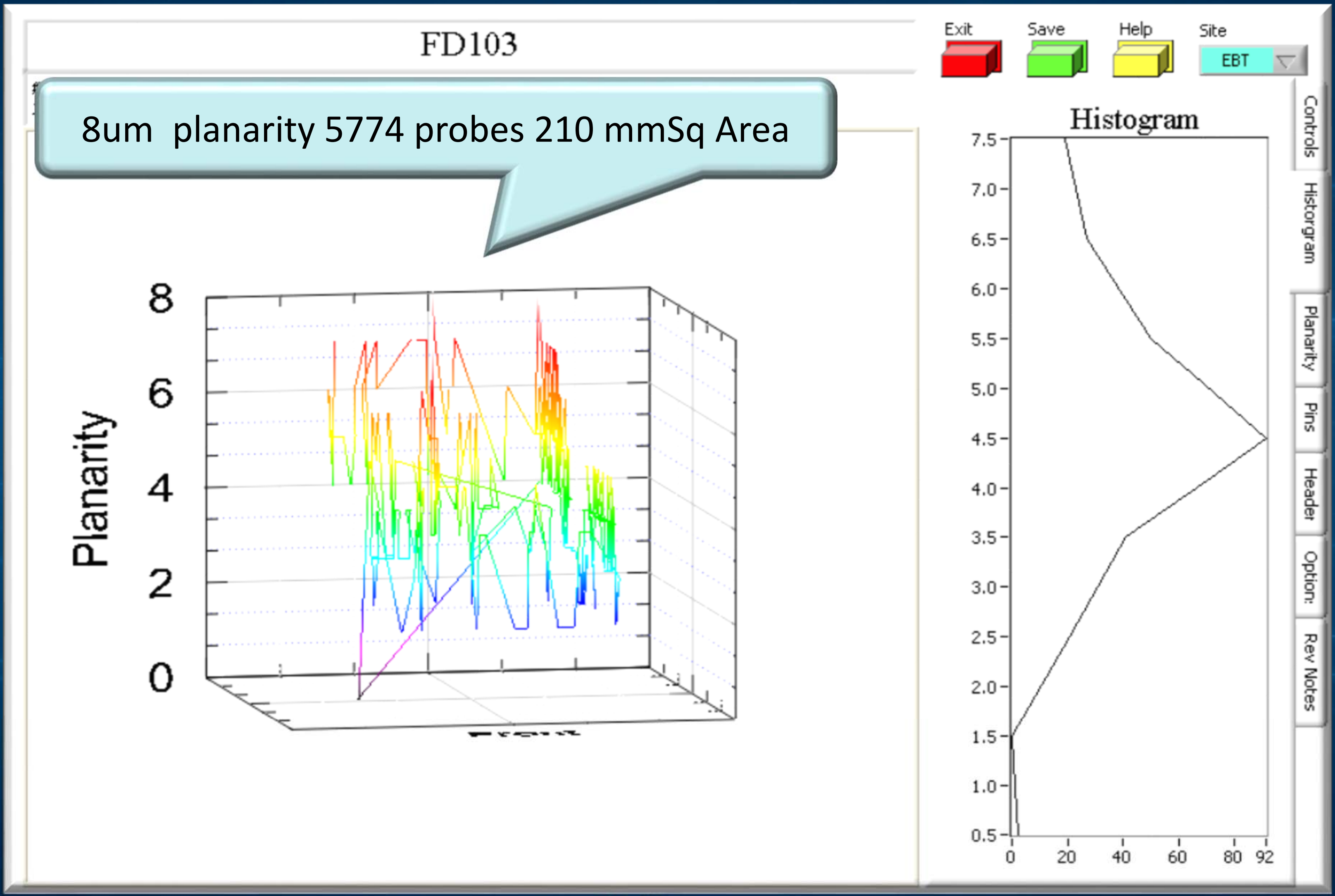
ISMI Current carrying capacity criteria



Data after 1.5M cycles

Probe Solutions In Production

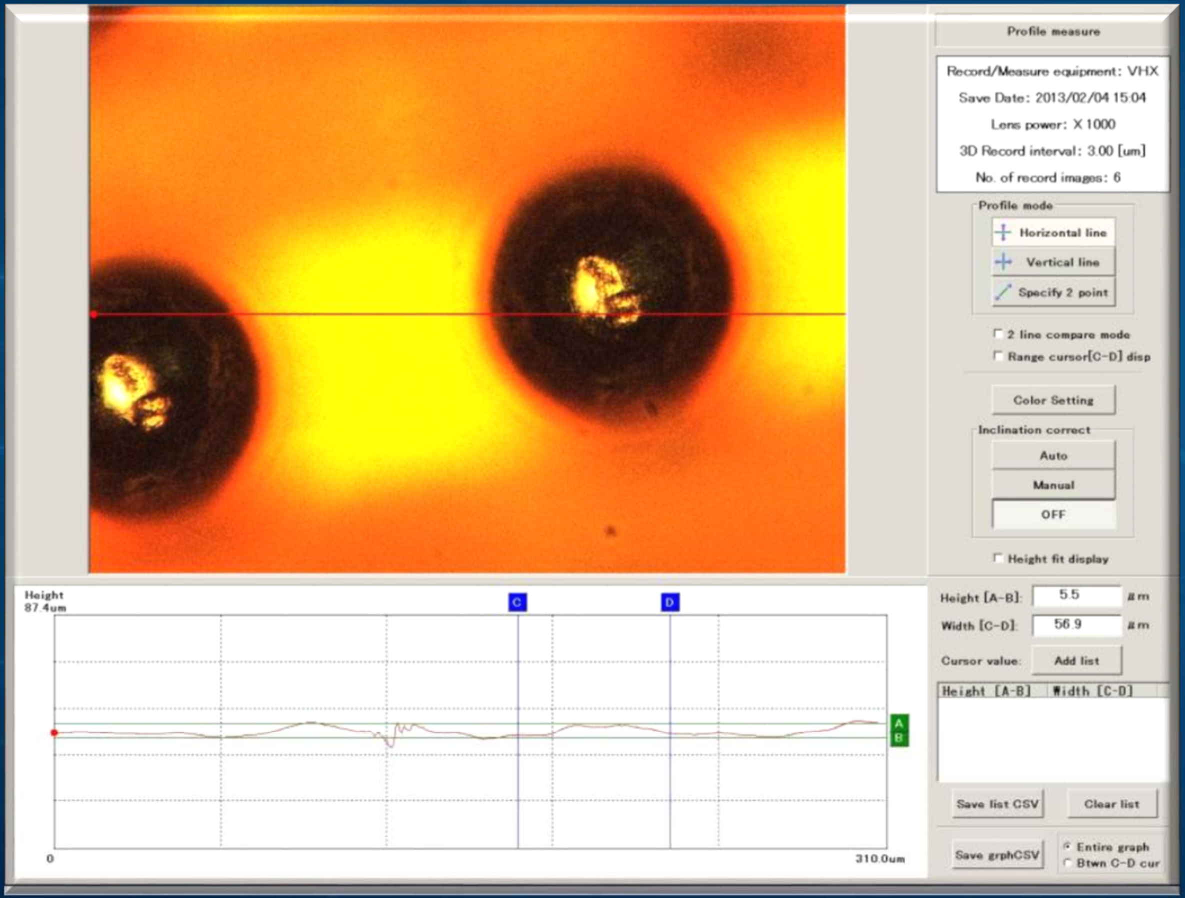
Probe Card Electrical Planarity



8um planarity 5774 probes 210 mmSq Area

Bump Damage

FFI K-probe on Reflow bump



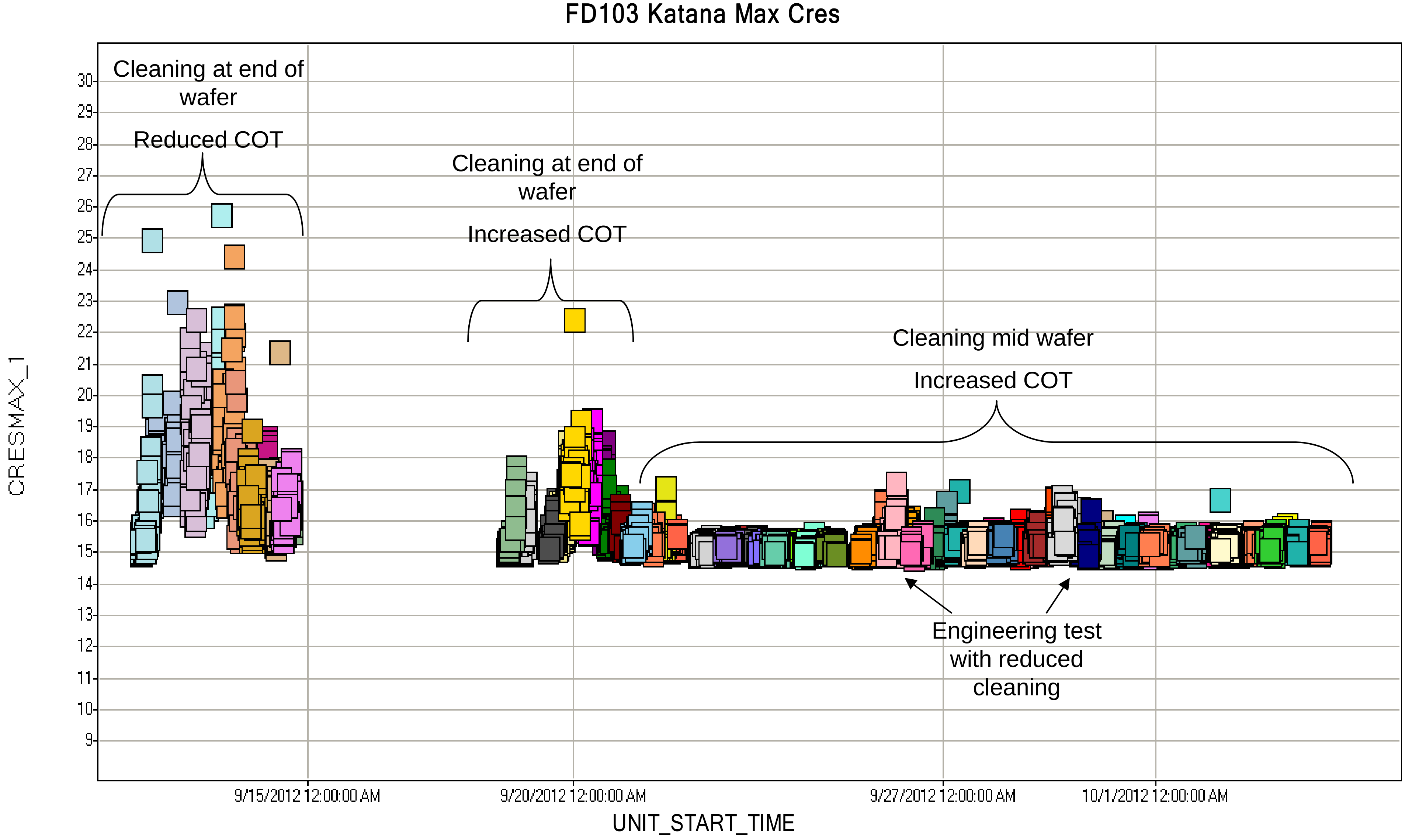
Profile measure

Record/Measure equipment: VHX
Save Date: 2013/02/04 15:04
Lens power: X 1000
3D Record interval: 3.00 [um]
No. of record images: 6

Height [A-B]: 5.5 µm
Width [C-D]: 56.9 µm

Cobra probe on Reflow bump

Max Cres at Installation



FD103 Katana Max Cres

Cleaning at end of wafer

Reduced COT

Cleaning at end of wafer

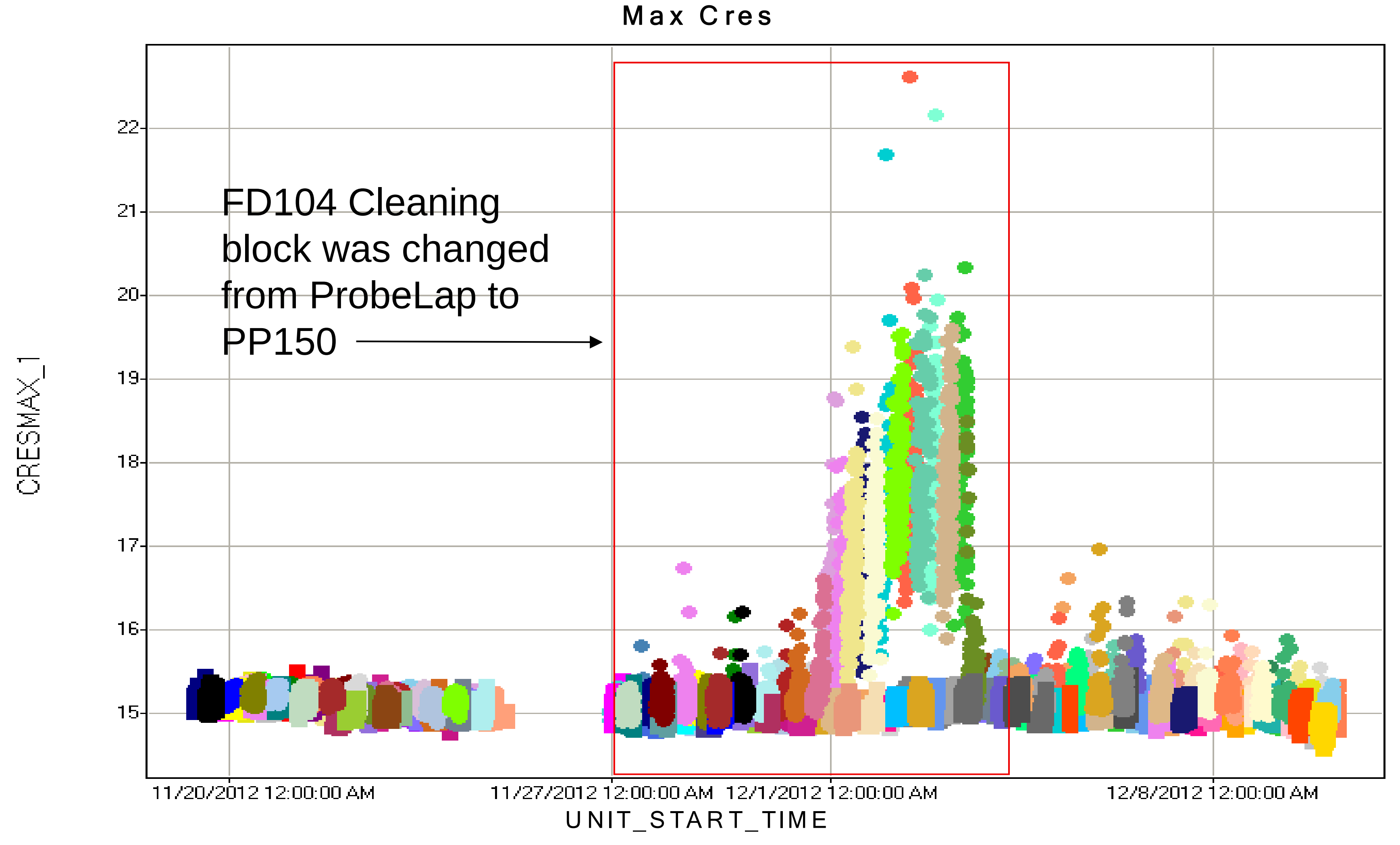
Increased COT

Cleaning mid wafer

Increased COT

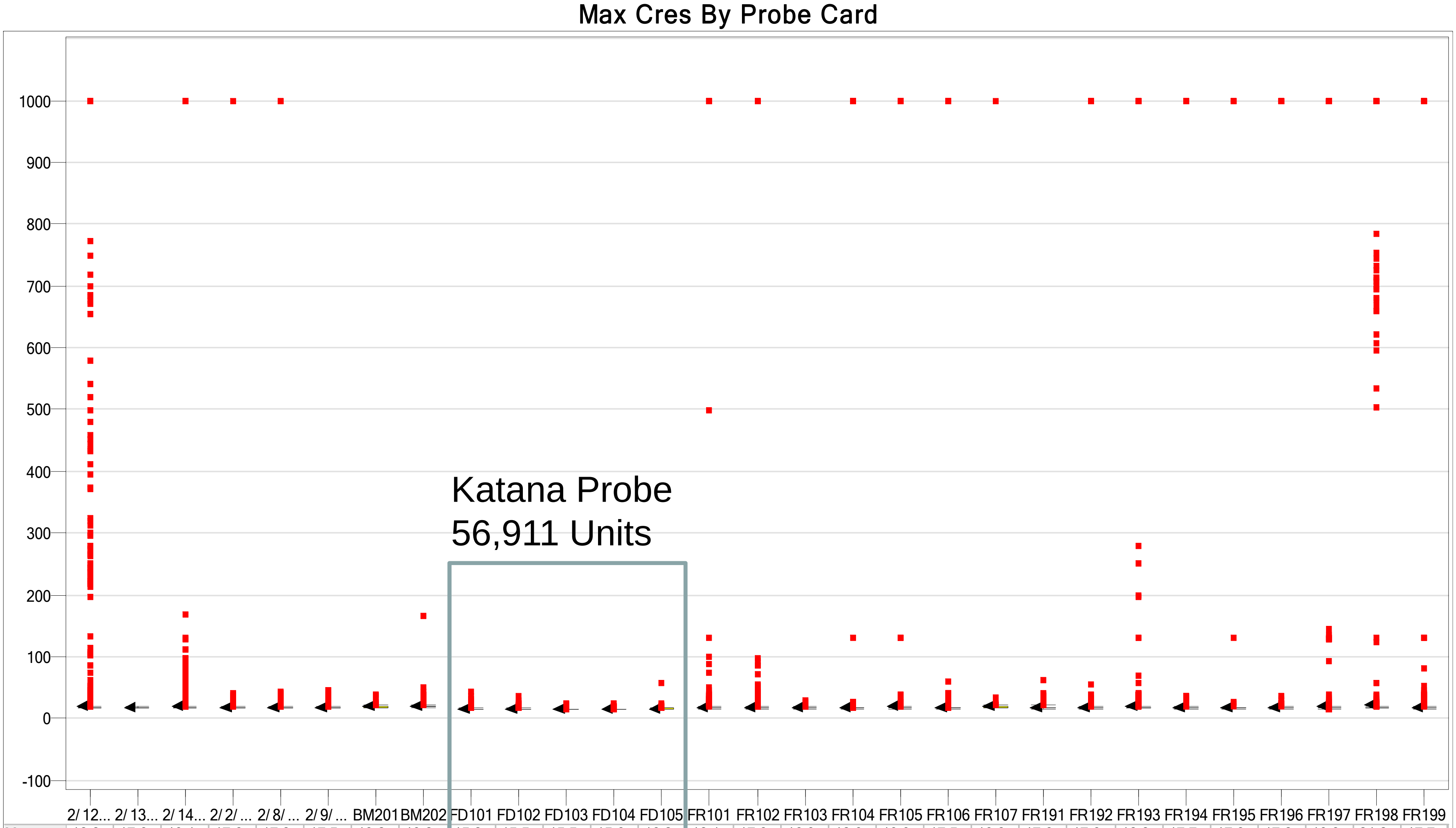
Engineering test with reduced cleaning

Production Max Cres



FD104 Cleaning block was changed from ProbeLap to PP150 →

Probe Card Max Cres Katana vs. Cobra and Pogo

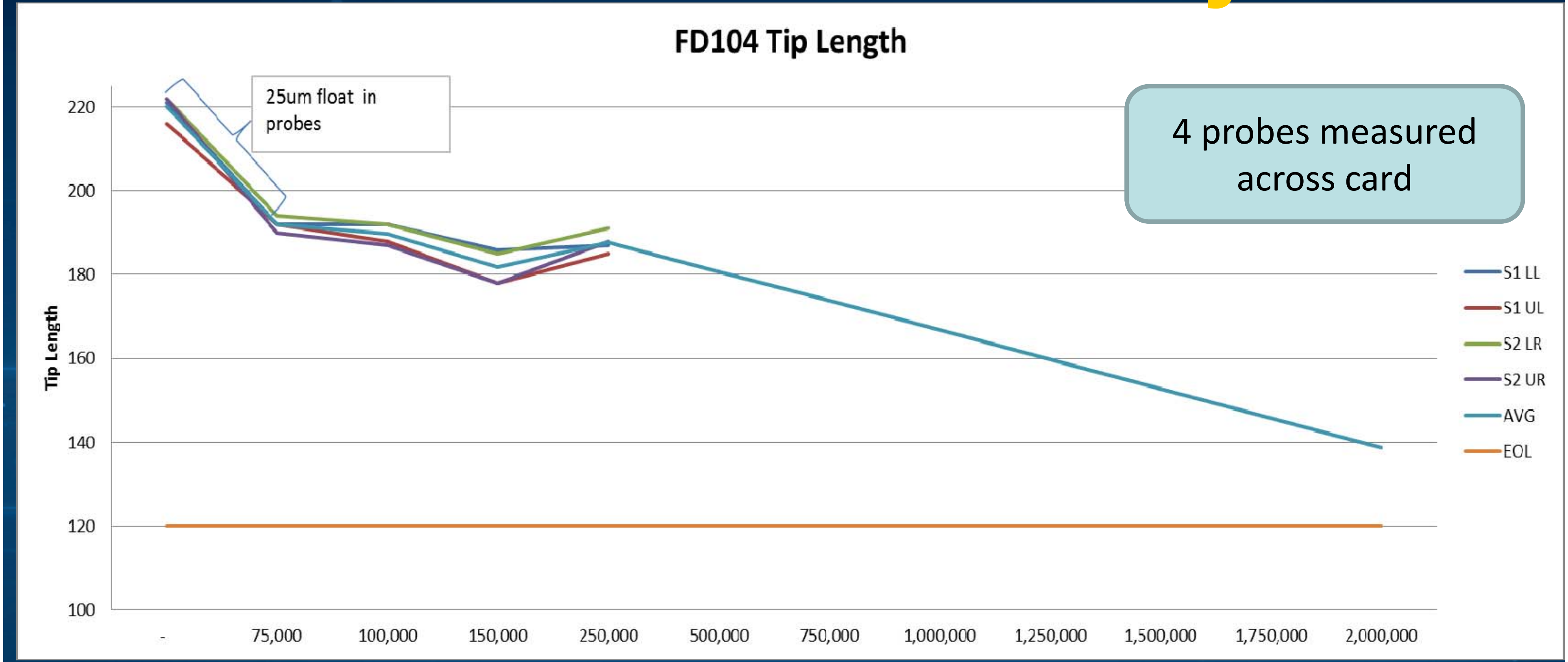

Max Cres By Probe Card

Katana Probe
56,911 Units

	2/ 12...	2/ 13...	2/ 14...	2/ 2/ ...	2/ 8/ ...	2/ 9/ ...	BM201	BM202	FD101	FD102	FD103	FD104	FD105	FR101
Mean	18.8...	17.6...	19.1...	17.6...	17.8...	17.5...	19.2...	19.8...	15.8...	15.5...	15.5...	15.6...	16.2...	18.1...
StdDev	27.4...	0.54...	23.7...	6.79...	7.77...	0.95...	1.10...	2.09...	1.05...	0.87...	0.74...	0.80...	0.98...	23.0...

	FR102	FR103	FR104	FR105	FR106	FR107	FR191	FR192	FR193	FR194	FR195	FR196	FR197	FR198	FR199
Mean	17.3...	16.9...	18.0...	19.9...	17.5...	19.3...	17.6...	17.6...	18.8...	17.7...	17.3...	17.8...	19.3...	21.2...	17.7...
StdDev	13.6...	0.54...	33.6...	49.5...	20.1...	35.1...	1.47...	18.8...	21.8...	18.7...	12.7...	22.1...	45.2...	57.1...	19.4...

Life Time Data Study



25um float in probes

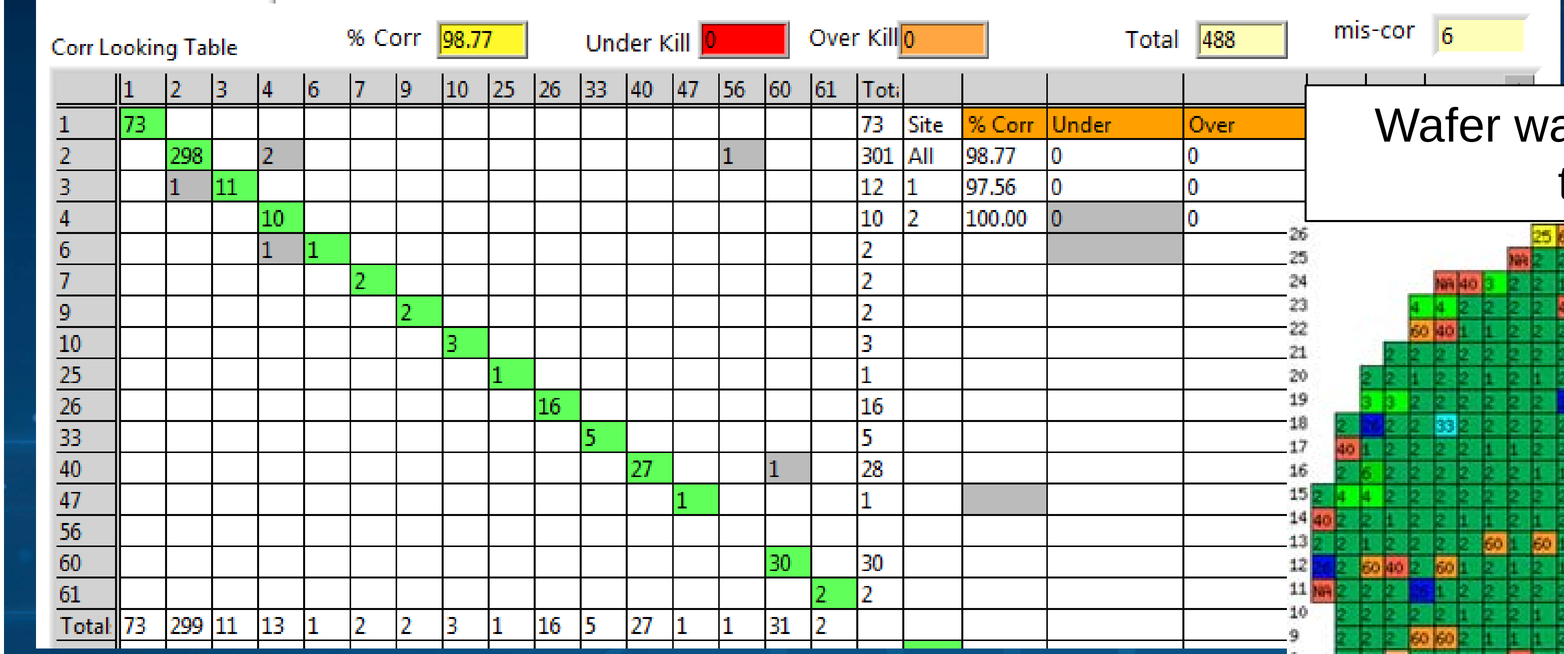
4 probes measured across card

Probe Settings:
Production wafer in demo
Production cleaning and over travel

Number of TD	175,000.00
Tip Length Loss (um)	5.00
Tip loss for 500k (um)	14.29
Usable Tip Length (um)	70.00
Projected TD Life	2,450,000.00

Post Life Time Data

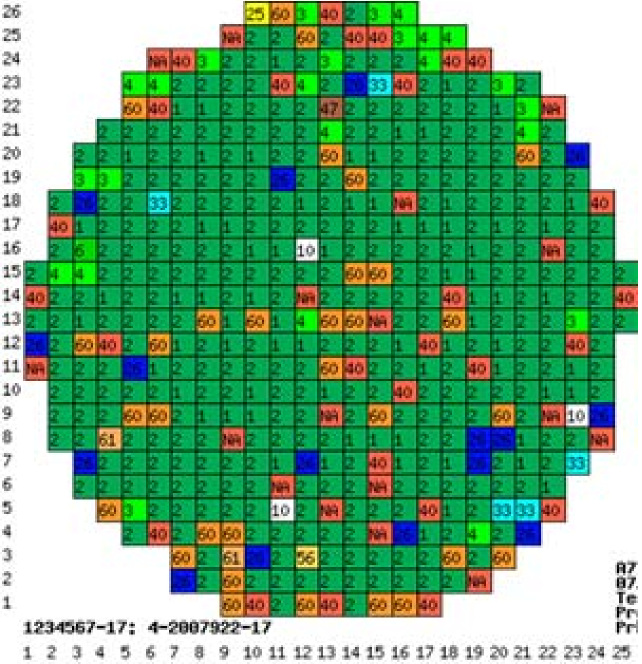
Demo probe had 250k TD

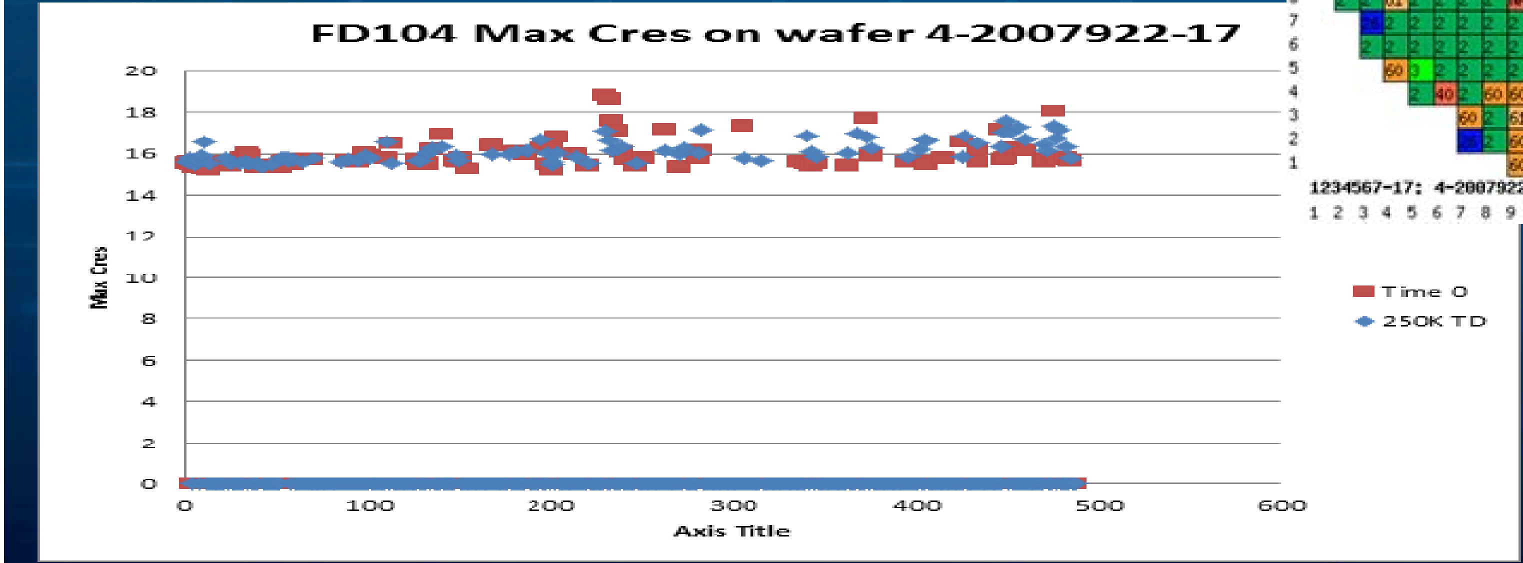


Corr Looking Table % Corr 98.77 Under Kill 0 Over Kill 0 Total 488 mis-cor 6

	1	2	3	4	6	7	9	10	25	26	33	40	47	56	60	61	Tot:				
1	73																73	Site	% Corr	Under	Over
2		298		2										1			301	All	98.77	0	0
3		1	11														12	1	97.56	0	0
4				10													10	2	100.00	0	0
6				1	1												2				
7						2											2				
9							2										2				
10								3									3				
25									1								1				
26										16							16				
33											5						5				
40												27			1		28				
47													1				1				
56																					
60															30		30				
61																2	2				
Total	73	299	11	13	1	2	2	3	1	16	5	27	1	1	31	2					

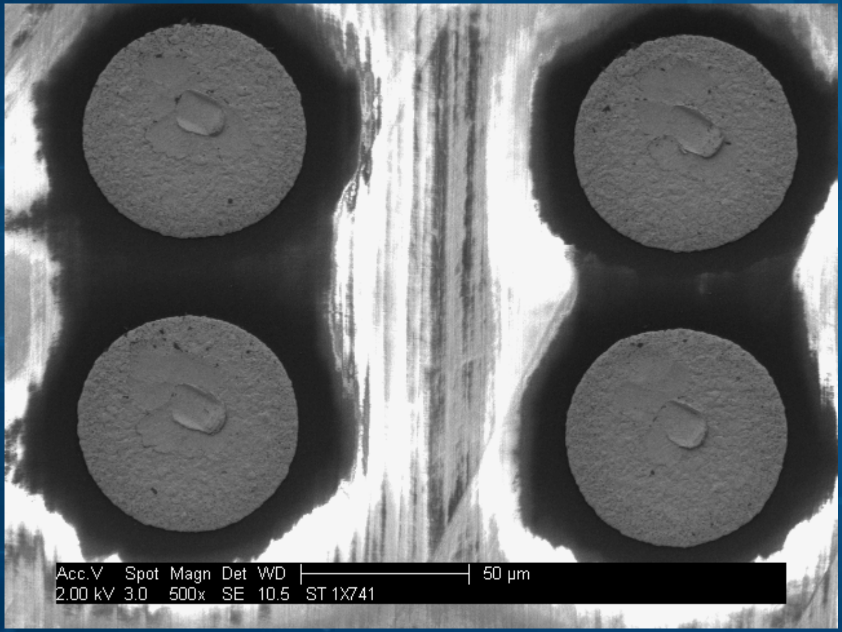
Wafer was probed 947 times

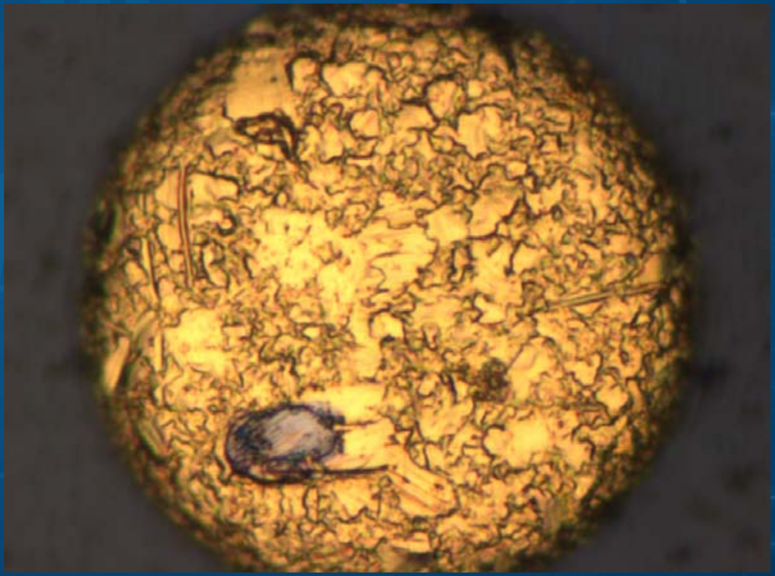




Low Substrate Pad Wear

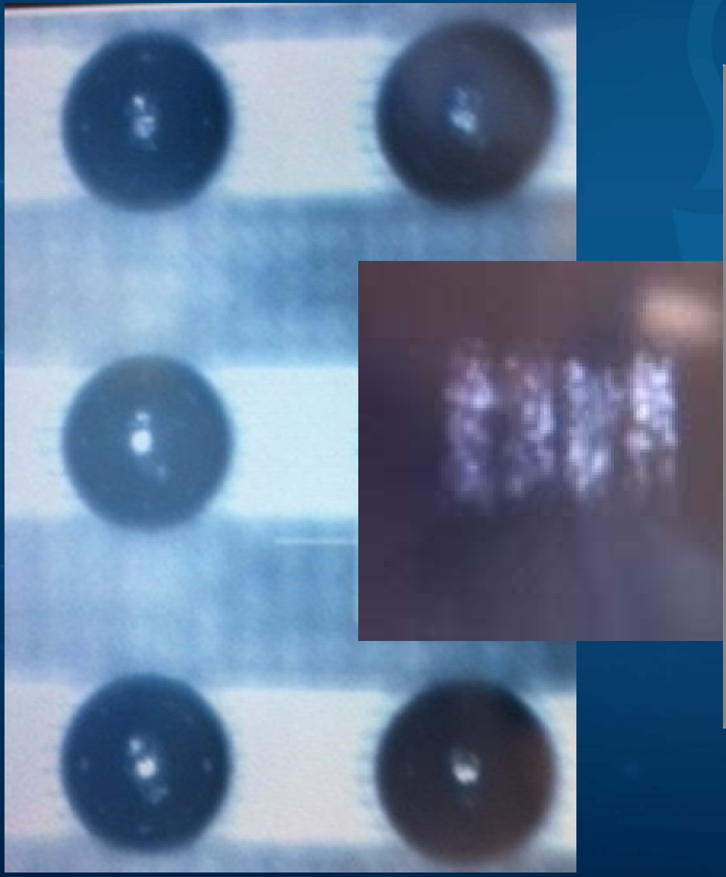
1.5M cycles

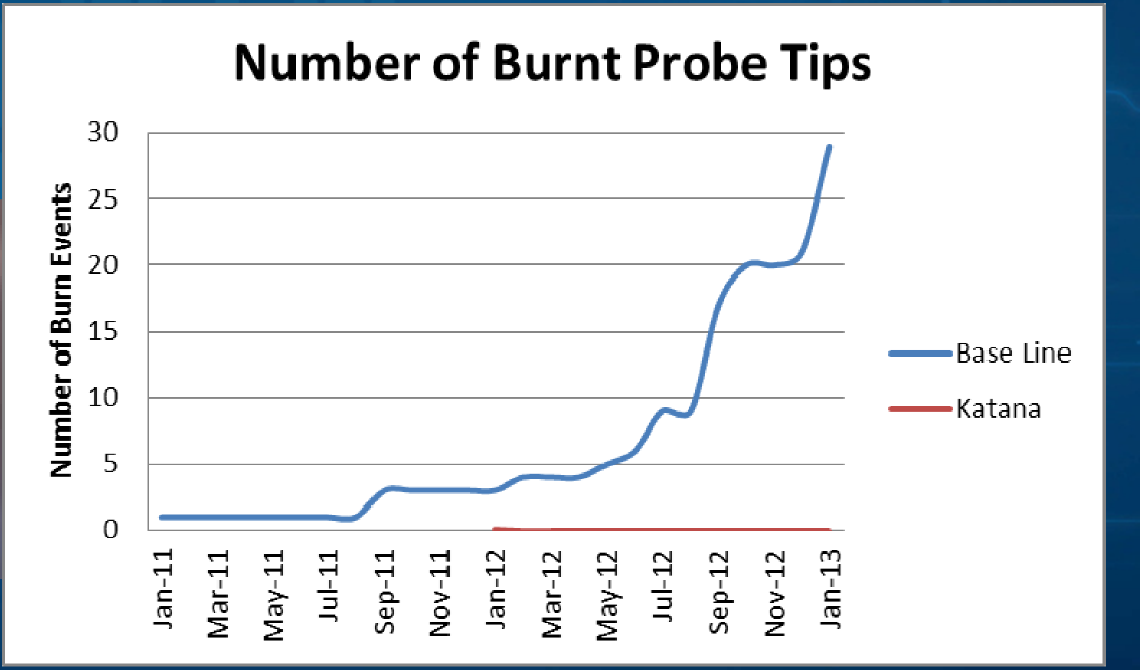




Burning Probes

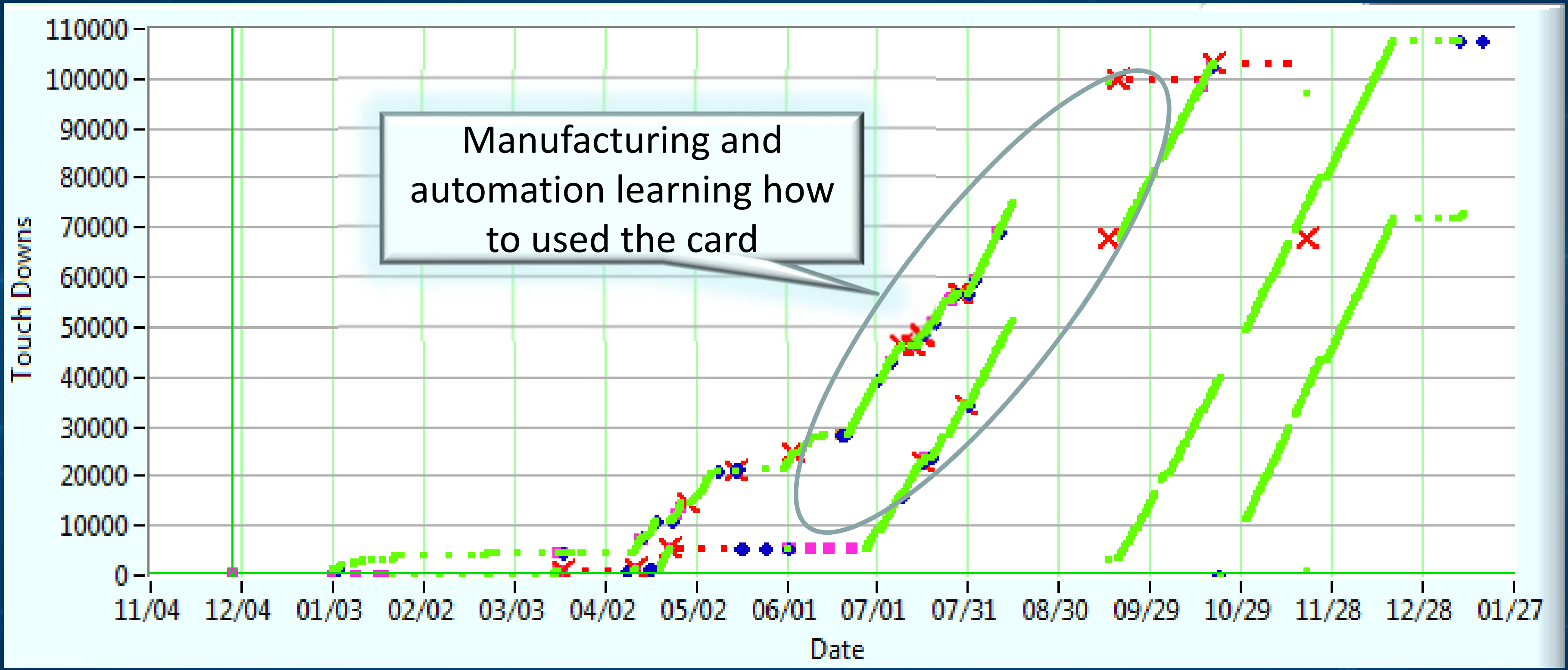
- **No burn events on four FFI K-Probe cards with greater than 100k touchdowns each**
  - Baseline probe card had 26 burn events in the same time frame





Production Performance

Mean Touchdowns Between Failures: 50,241



Manufacturing and automation learning how to used the card

X: Card put in a down state.
Note: none of the down states required the card to be tested on an probe card analyzer or repaired

Conclusion

- **Low-force MEMS Probe Card Technology, such as FormFactor's K-Probe, demonstrated several advantages for solder flip-chip probing in high-volume production**
  - Production stability for high pin counts, > 20,000 pins
  - Scalability for multi-DUTs probing, >= 8 DUTs
  - Long life-time, >2M touchdowns demonstrated
  - Controlled Cres in production
- **As flip-chip pitch continues to shrink, requiring finer vertical probes, MEMS probe technology is proven to be a viable path to continue lowering cost of test**

Acknowledgments

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- Doug Shuey, FormFactor