



IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

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Novel Precision Probe Array for Wafer Level Final Test of WLCSP

Johnstech[®]

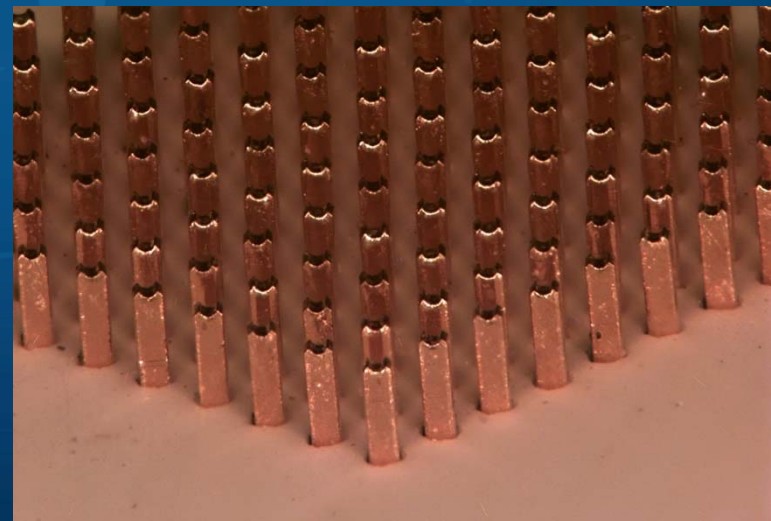
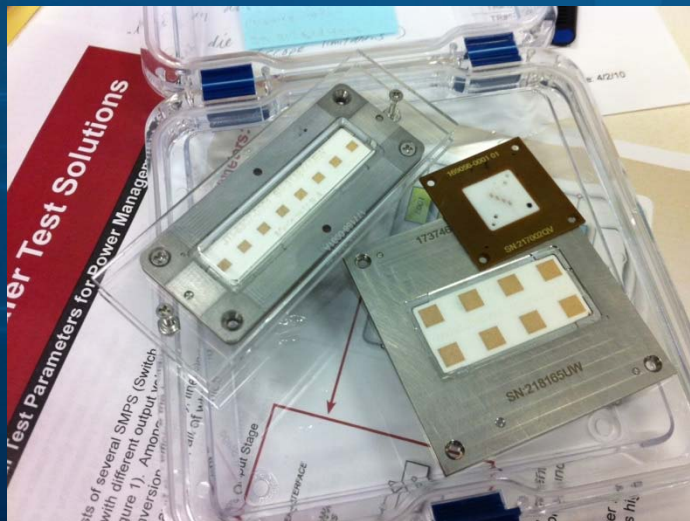
Jathan Edwards
Johnstech International

Presentation Outline

- Introduction to IQtouch™ Micro - Final Test Probe Arrays for 300-500 micron pitch WLCSP
- Compare/contrast with existing technology
- Probe Array and Probing characteristics
- Performance data examples
- Summary and Acknowledgements

IQtouch™ Micro Background

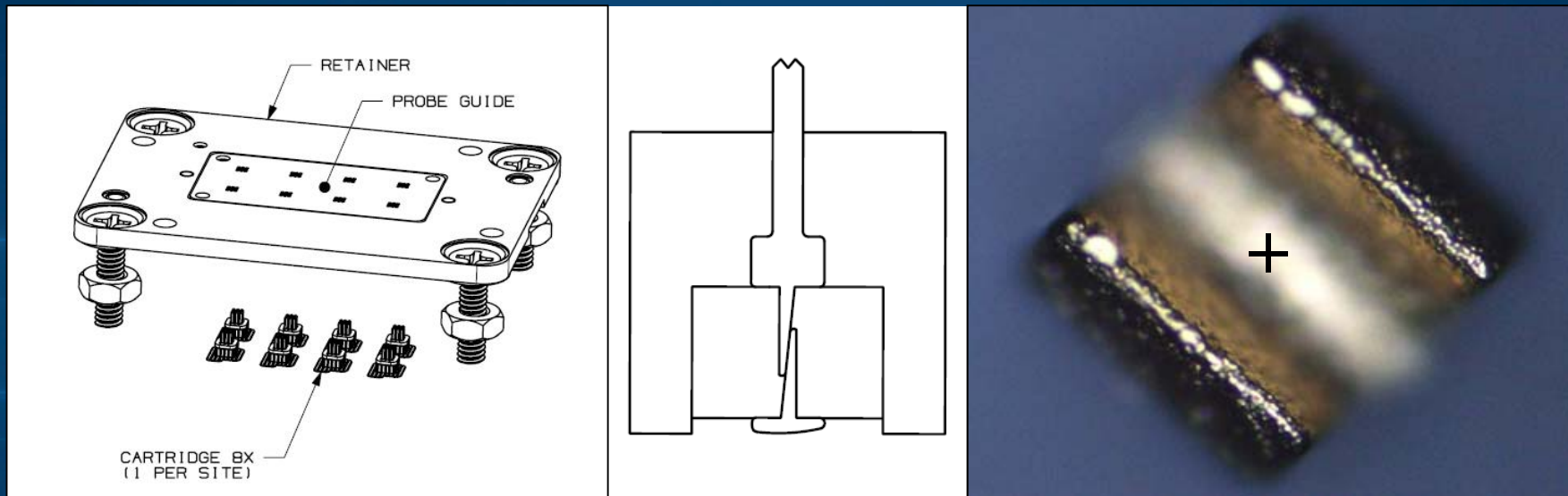
- Johnstech International - well established in final package test
- IQtouch™ Micro is initial offering into WLCSP final test.
- 300, 350, 400 and 500 micron pitch available



IQtouch™ Micro General Product Scope

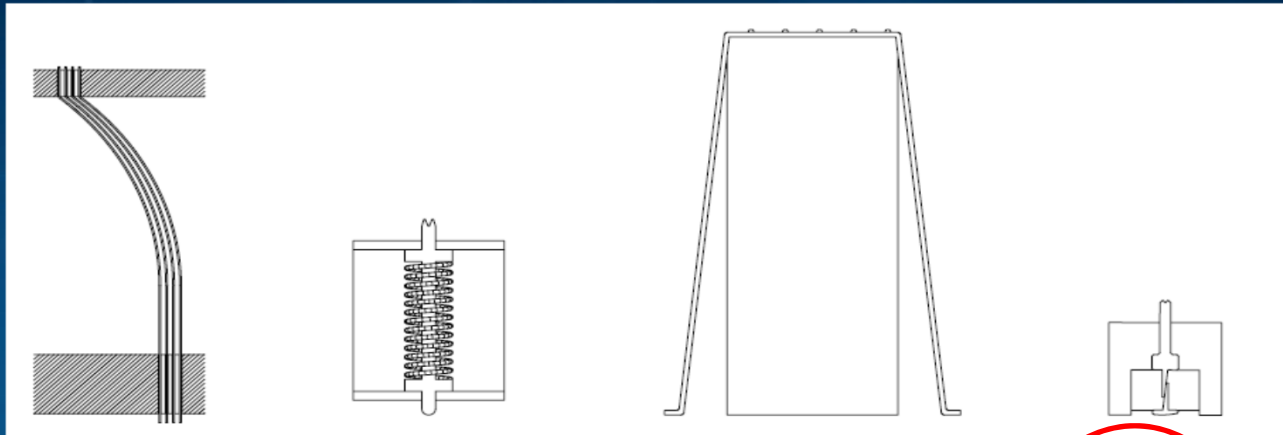
- Ball Count: ≤ 144 Balls / site
- Package Size: $\leq 10 \times 10$ mm
- Ball Material: SAC 405, 305, 105, 266, SnAg
- Ball Diameter: 0.15 - 0.3mm (400/500),
0.15 - 0.21mm (300/350)
- Site configurations: Up to 32x and up to 50mm total span
- Spec Sheet and application notes posted at <http://www.johnstech.com/iqtouch/>

IQtouch™ Micro Product Configuration



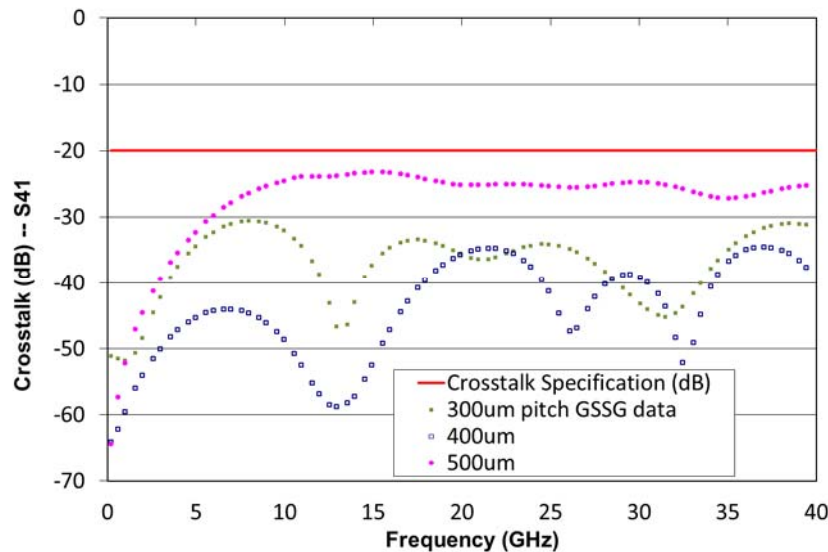
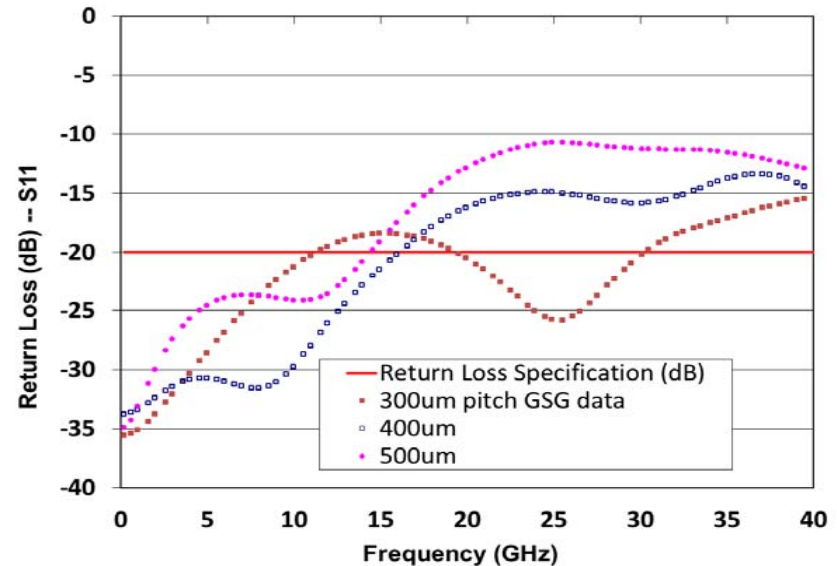
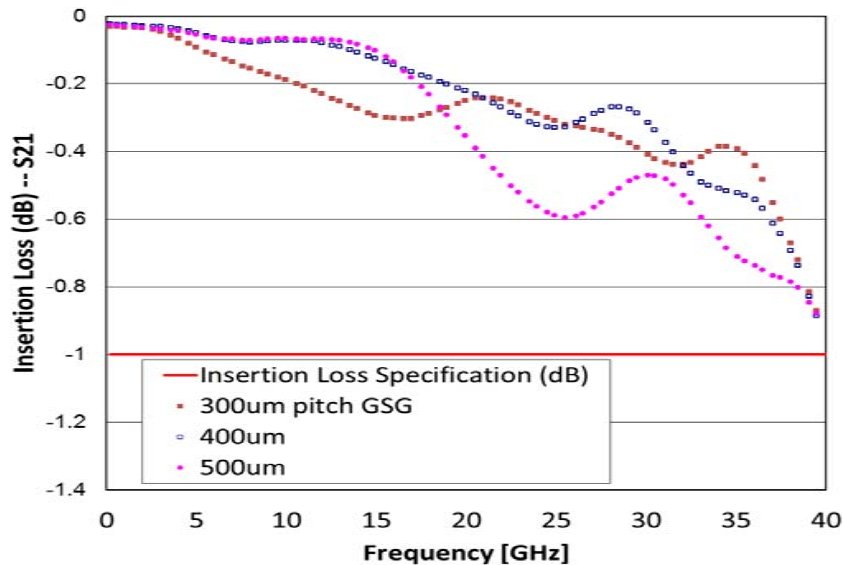
- Site replaceable elastomeric cartridges for quicker MTTR
- The elastomeric web is designed to provide controlled probe force to DUT and between two rigid probes
- Sharp probe tip knife edges for high piercing stress are keyed at 45° to array axis
- Probe alignment teaching centered to focus in valley

IQtouch™ Micro Comparison



Performance	Vertical Probes	Spring Pins	Membrane Probes	iQtouch™ Micro
Inductance	2 nH	1nH	0.2nH	.3nH
Bandwidth	1.3 GHz	8 GHz	5-70GHz	20-40 GHz
CRES	1 Ω	80-200mΩ	300-500mΩ	< 50mΩ
Cleaning Interval [TD]	100-1,000	100-10,000	100-1,000	3,000- 100,000
Cont. Current (20°C)	500mA	1.5A	< 500 mA	2A
Free height [mm]	~ 6mm	3.3mm	~6mm [pedestal]	1.9mm

Measured RF Characteristics¹



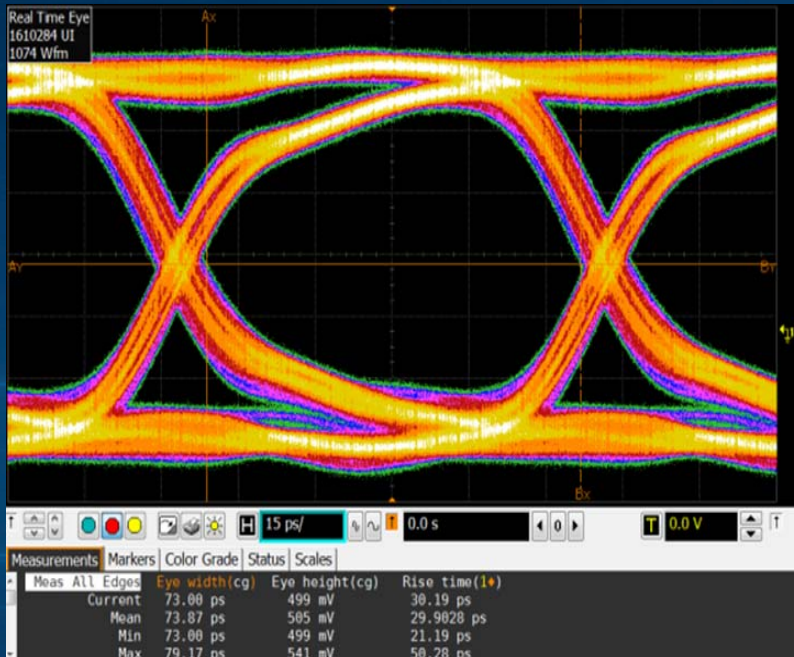
SPICE models are fitted to measured data to generate equivalent circuit parameters (e.g. 400 micron pitch):

Inductance: 0.285 nH Self
 0.104 nH Mutual

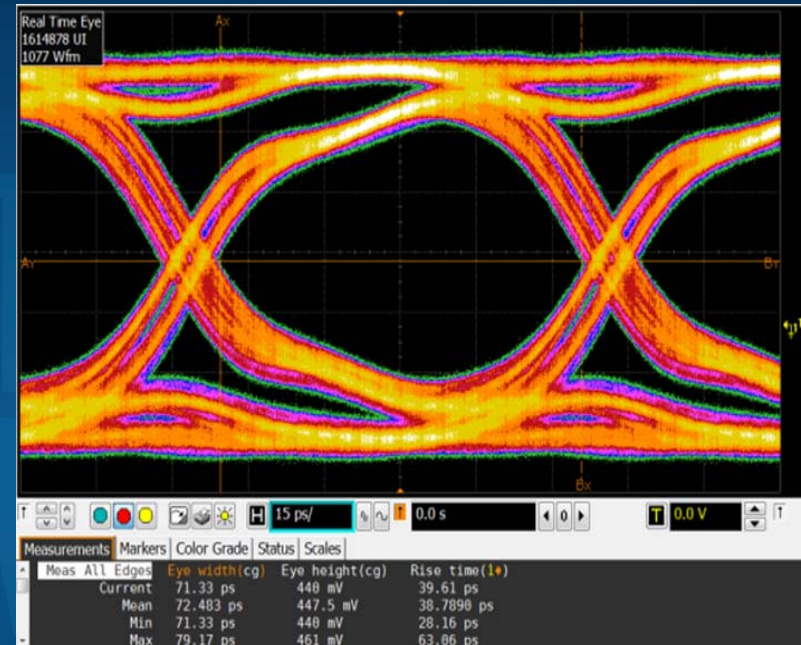
Capacitance: 0.045 pF Ground
 0.038 pF Mutual

Measured Digital Signal Characteristics

(33 GHz, 10 ps Edge Rate PRBS 2⁷-1 Signal)



Input Signal

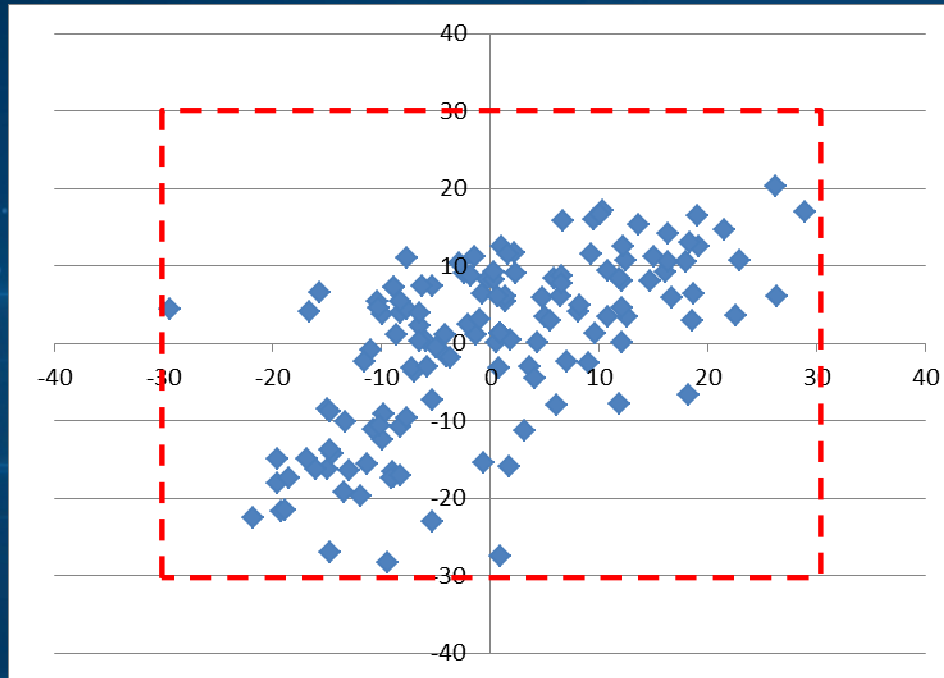


Transmitted Signal through Probe pairs and sample / DUT.

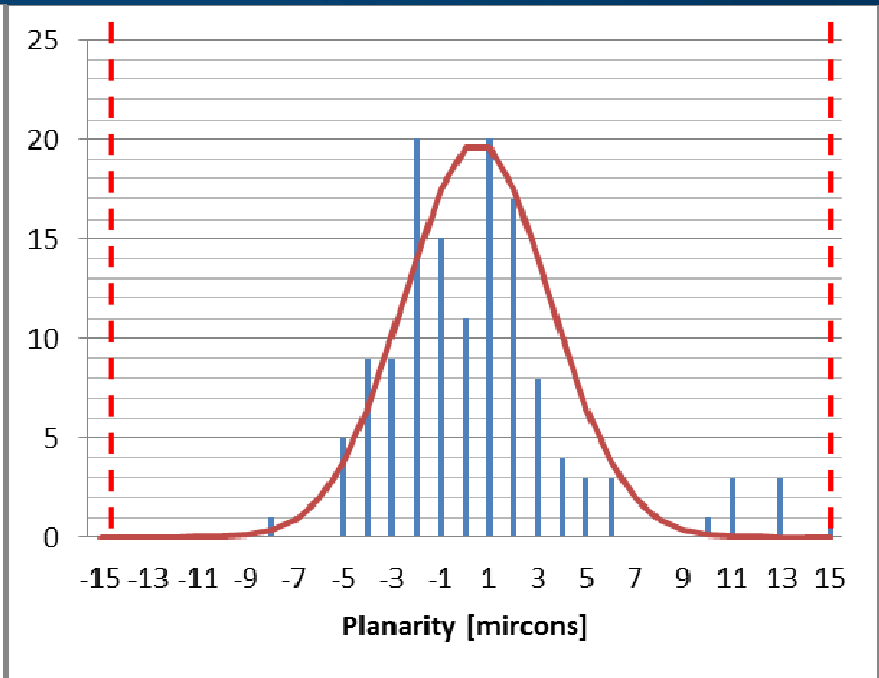
Description			
RF BD #1	Eye Width	Eye Height	Rise Time
Cal Path	73.87 ps	505 mV	29.903 ps
Path Plus Device and Probes	72.48 ps	447.5 mV	38.789 ps
Device and Probes Degradation	1.39 ps	57.5 mV	8.886 ps

Probe Array Precision X,Y,Z

X/Y probe position scatter plot

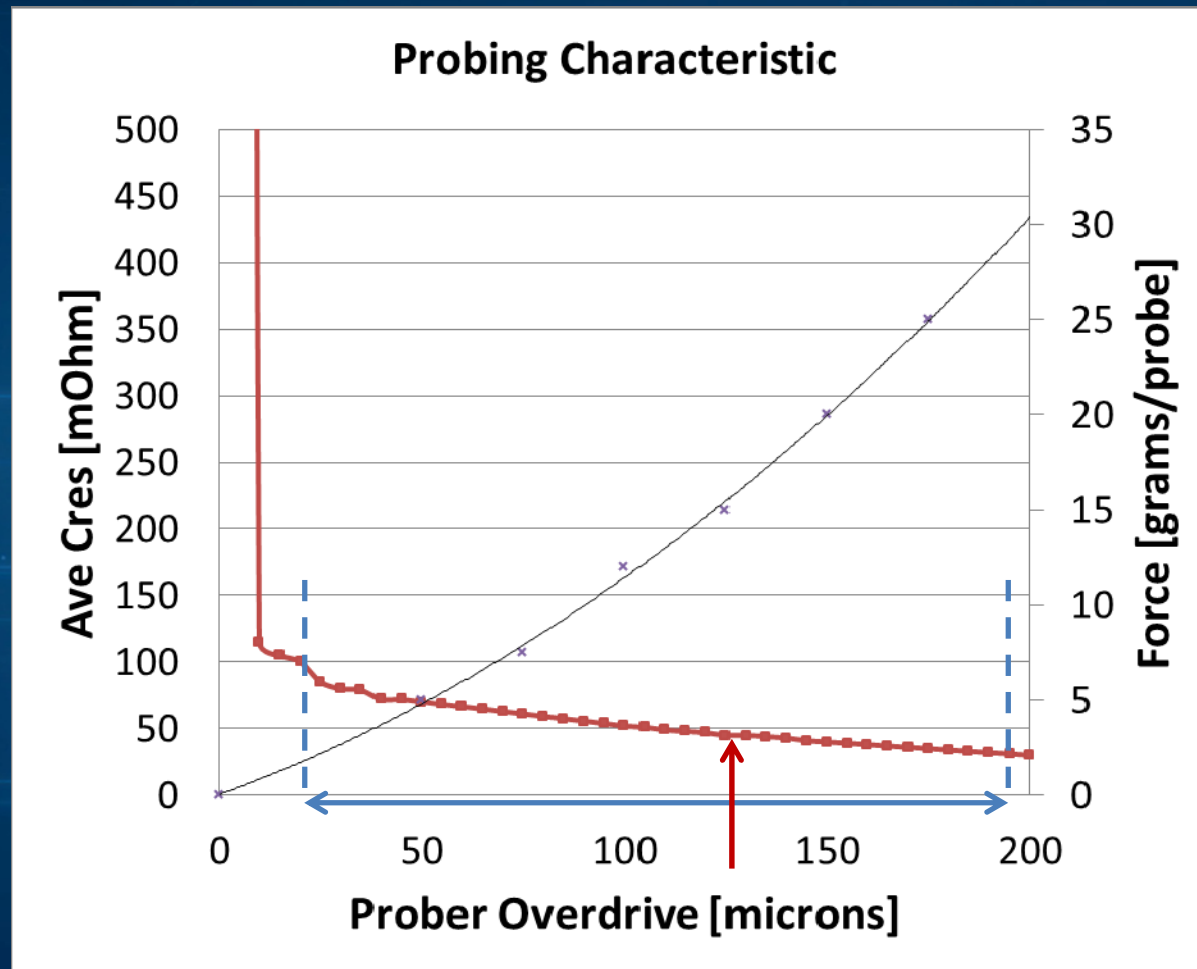


Probe Z-height histogram



Standard automated checkout of each probe array via ITC Probilt 3500 Probe Card Analyzer; automated probe capture camera isn't quite as precise as prober, but provides quick validation for each probe's XY Err, planarity, Cres and Force prior to shipment.

Probing FDR Characteristics



- “Good” Cres range (< 100 mΩ) for ~ 175 microns on SAC ball materials
- Recommended starting OD at 125 microns
- 195 microns max (cartridge limit)

Probing Characteristics: Sample Off-Apex Ball Marks



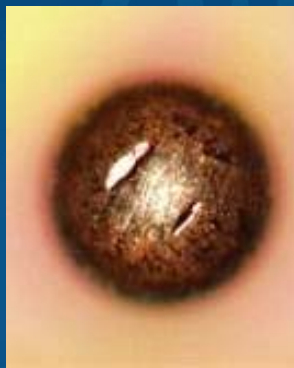
OD: 50um

5 gpp



75um

7.5 gpp



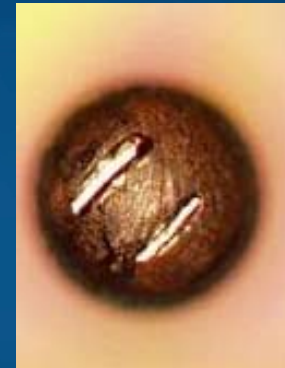
100um

12 gpp



125um

15 gpp



150 um

20 gpp

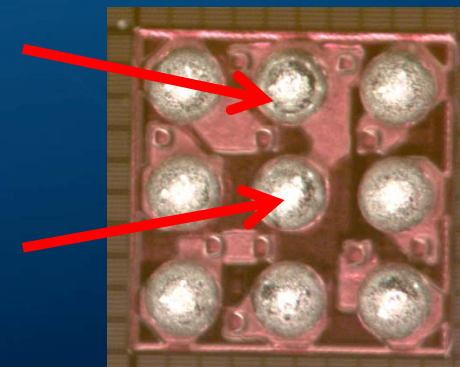
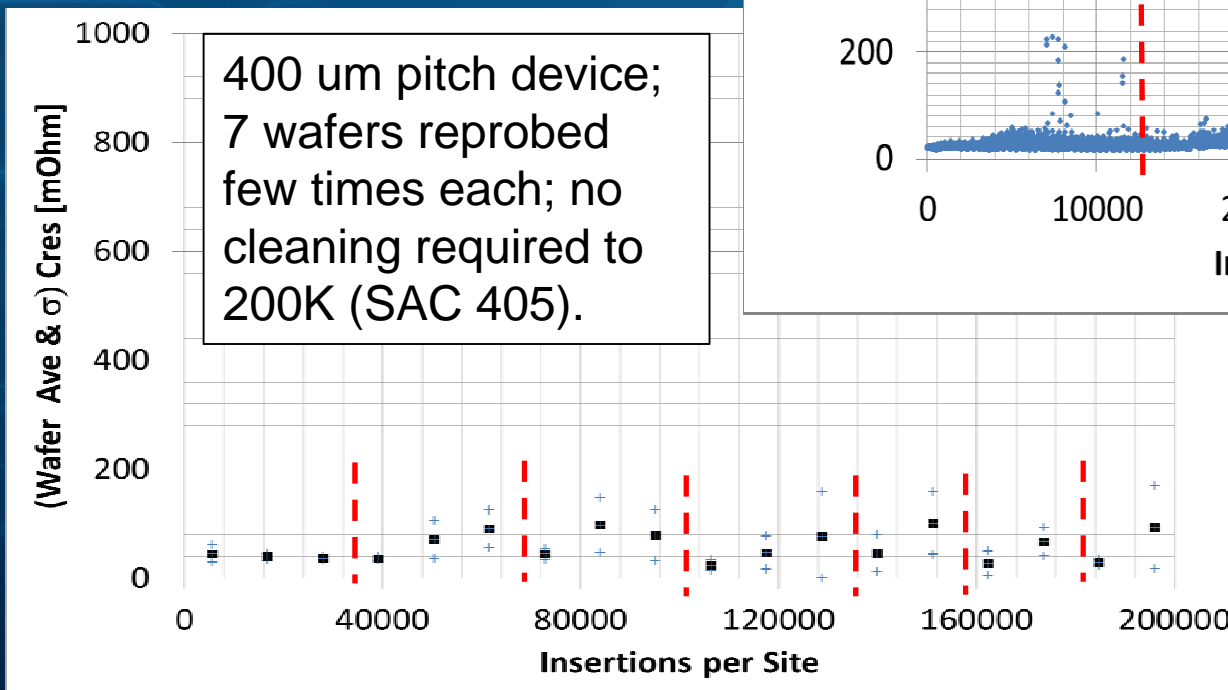
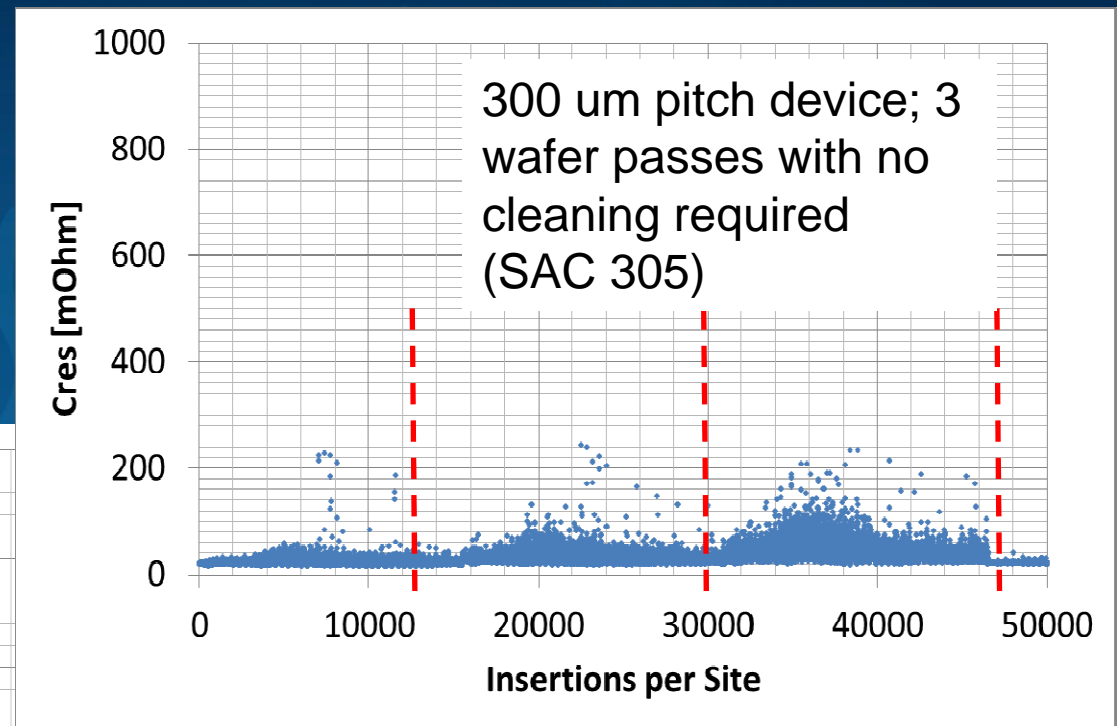


175 um

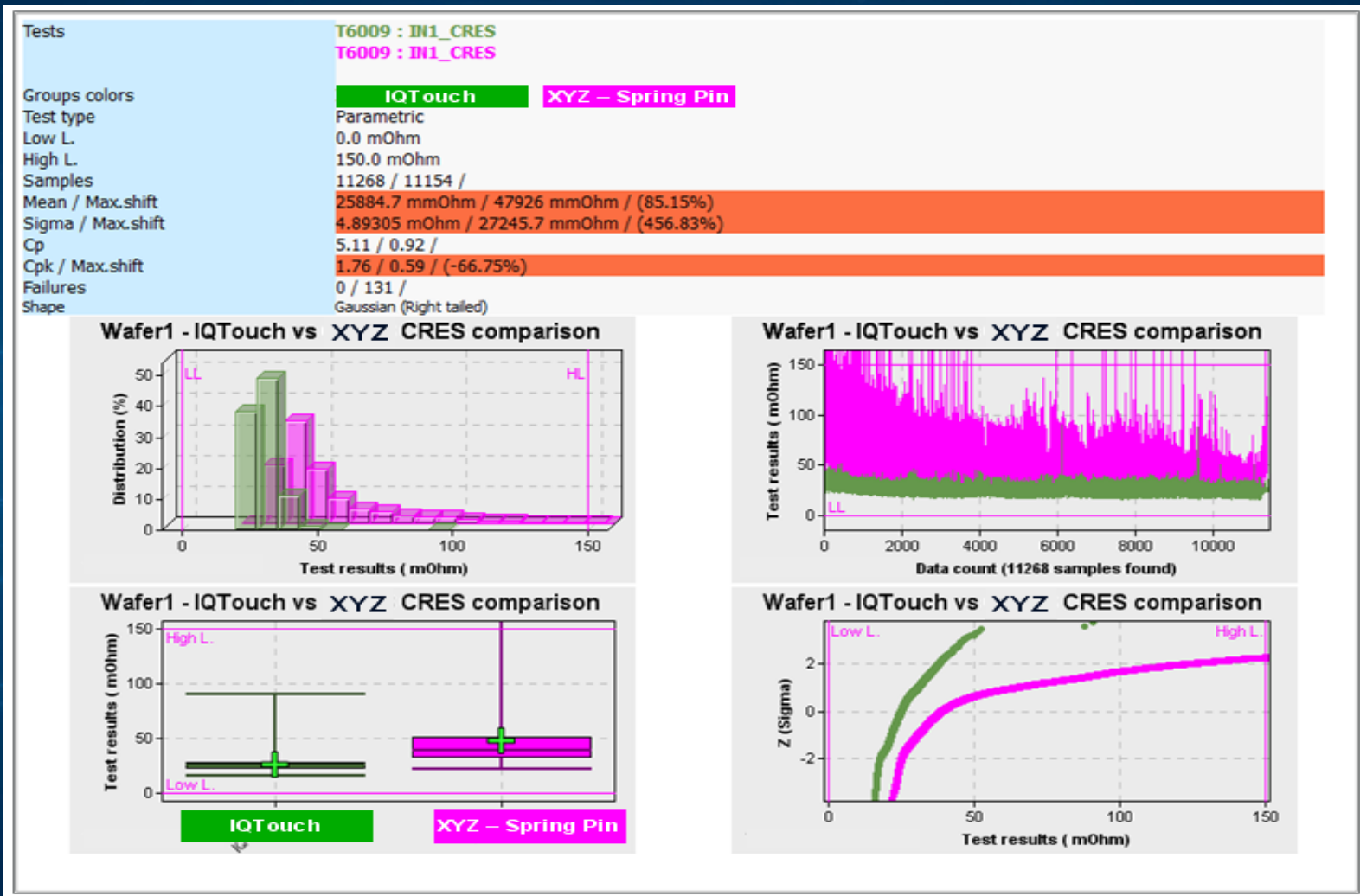
25 gpp

Method to Measure Cres directly from Customer Wafers

Customers supplied wafers for 300 & 400 micron pitch. We used the common bussed device grounds of the devices to make Cres measurements through I/O pairs.



Customer Performance Data Sample



Cleaning Interval effect on OEE

- Cleaning intervals typically depend on WLCSP ball material and the sensitivity of the customer tests (Cpk within test parameter limits).
- Beta Phase evaluations were “drop-in” comparisons against competing probe array technologies (VPC and Pogo) where the customer cleaning intervals were often set for 50-100 touchdowns.
- In some cases, customers time studies show that up to 10% of total wafer test time is devoted to cleaning stops (i.e. 4 minutes of cleaning and 40 minutes of actual device testing). In one case, we were able to demonstrate extending cleaning interval from 10X per wafer to once per 10 wafers to provide significant Overall Equipment Efficiency (OEE) improvement of the test cell.

Technical Challenges

- The higher performance probes require shorter free height than what docking hardware has been designed for in some cases. Usually, this has been accommodated simply with changing prober software z-height limit. In some cases, we have had to supply interposer to increase height to bring probe operating range into prober acceptance range.
- For “drop-in” replacement applications, the lower impedance and higher frequency response for *IQtouch*[™] Micro sometimes require retuning of test programs and/or probe card matching components to be compatible for functional tests.
- Probe tip recognition for *IQtouch*[™] Micro in TEL/ TSK prober systems works robustly with some algorithms but not all of them; we are compiling list for recommendations from customer experience.

Summary and Acknowledgements

- A brief introduction of the novel precise probe array technology we call IQ*touch*™ Micro. This new probe array has the potential to enable new devices types to be final tested at wafer level package.
 - ❑ RF performance to enable applications in 5-40 GHz
 - ❑ Lower and more stable Cres for improved Cpk and
 - ❑ Enhanced cleaning intervals in production environments for improved OEE

Thanks to my colleagues at Johnstech with special recognition to:
Brian Halvorson, Charles Marks, Jeff Sherry, and Ron Gelbmann

(1) "Effects of device configuration", Jeff Sherry (Johnstech), Chip Scale Review, May/June 2014 gives a more thorough comparisons of differing ground configurations.

jdedwards@johnstech.com