

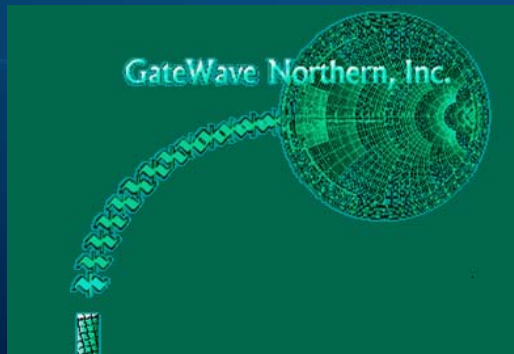


IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

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Measuring Probe, Socket and Device Capacitance and Inductance Through a Probe Card



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Problem

- **Measurements from perimeter of probe card contain information about entire connection**
- **Removal of non-essential information is required to extract pure device or probe parameters**
- **Process is referred to as 'de-embedding'**
- **Generally requires understanding of RF and circuit principles in conjunction with suitable algorithms**

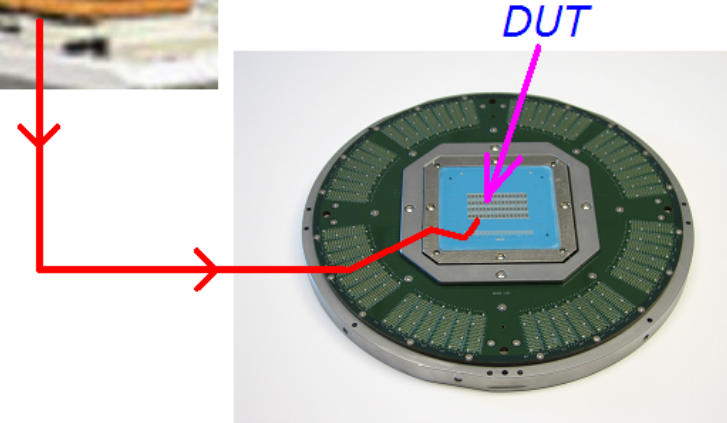
Approach

- Provide overview of problem set
- Briefly illuminate general techniques
- Define challenges unique to the probe card industry
- Examples and custom solutions

How do we measure probe or DUT ?

- Connect meter or other measuring device at the tester resource connections
- Measurement includes
 - Cables
 - Probe card connections
 - Probes
 - Device under test

Instrument, analyser or tester



Probe card

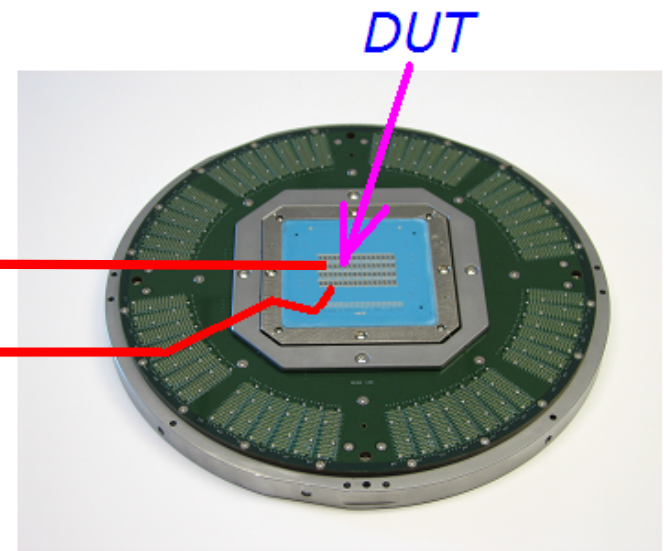
Getting to the point

- **Decide type of measurement**
- **Calibrate to the point of interest, i.e. probes, DUT**
- **Measure part of the chain that is not of interest and remove**
- **Select removal method**
- **'De-embed' the unwanted constituents**

What is de-embedding ?

- De-embedding can be viewed as mathematical removal of measurement contributions stemming from the signal path to the device-under-test (DUT) with the intent of obtaining only the DUT specific parameters.

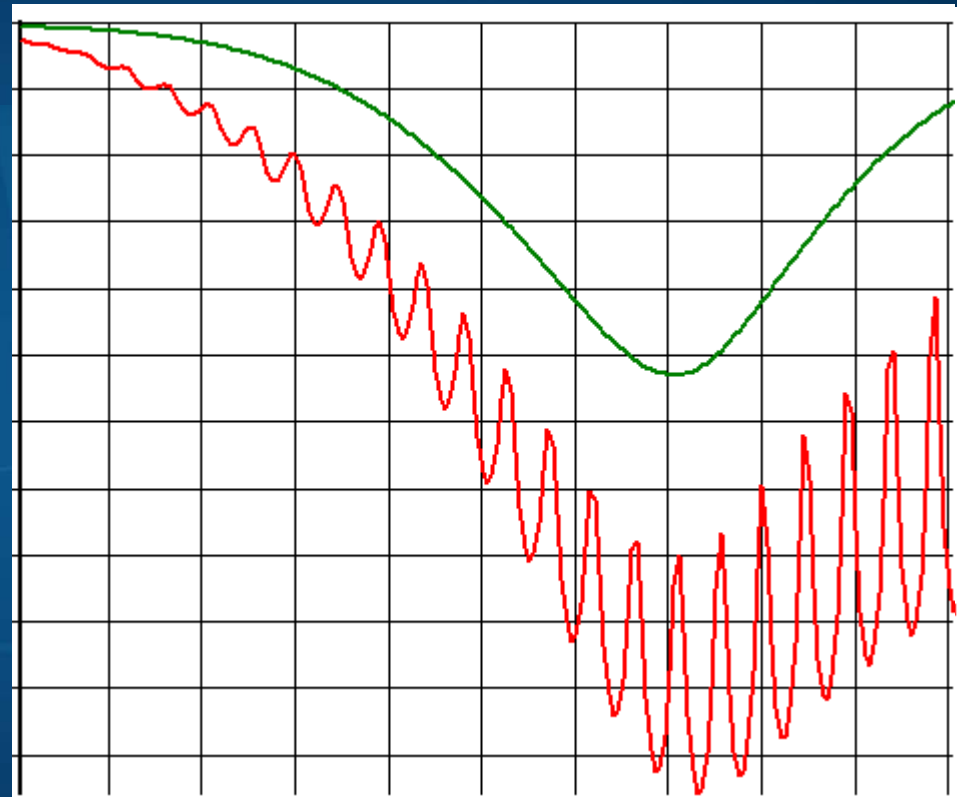
*Testhead w.
electronics*



Probe card

Why is it needed ?

- Example – signal loss as a function of frequency
- (red = probe card plus DUT)
- Contributions from connections can overwhelm the DUT only parameters (green curve)



Situations where de-embedding is required

- **When is de-embedding needed**

- Examples of parameters to be de-embedded
 - Device input capacitance, inductance and resistance
 - Probe capacitance, inductance and resistance
 - S-parameters such as insertion loss and return loss
 - Eye diagrams

- **Example methods of de-embedding**

- Subtraction
- SOLT, SOL
- TRL
- 1-port AFR
- Custom

Environment

- **Instruments**

- Meters
- VNA
- TDR



- **Tester**

- Time domain only
- with S-parameter capabilities



De-embedding with a meter

- Determine path contributions without device of interest (calibrate)
- Determine capacitance, inductance or resistance with relevant device connected
- Subtract

Calibration at the business end

- If probe characteristics are the desired outcome, it is necessary to calibrate to the top of the probe card PCB or interposer:

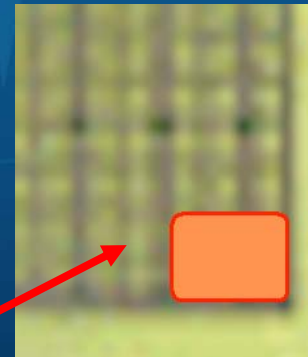
OPEN

(for shunt resistance, capacitance)



SHORT

(for series resistance, inductance)



The short must cover as many grounds as possible

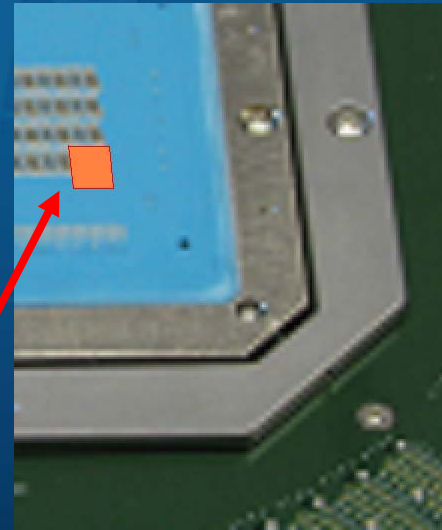
Calibration at the business end

- If DUT characteristics are desired the calibration must be to the tip of the probes

OPEN



SHORT



The short must cover as many grounds as possible

Resistance

- **Meter**

- DC measurement possible only if no blocking caps in measurement path
- Measure with open or short depending on whether series or shunt resistance is to be measured
- AC measurement necessary with blocking caps
 - Change of frequency requires a new calibration because of frequency dependent blocking capacitor resistance
 - AC measurement is often not readily possible on power lines because of bypass caps that shunt too much signal away

Capacitance, Inductance

- **Meter**

- ‘Calibrate’ with open (C) or short (L) at probes
- AC measurement necessary
 - Change of frequency requires a new calibration because of frequency dependent capacitor and inductor resistance
- Mutual parameters ?

Meter Example

- Capacitance (open cal):

| | DUT+card | card | DUT | DUT subtract | |
|--------|--------------|--------------|-------------|--------------|----|
| 50 MHz | 28.77 | 26.34 | 2.50 | 2.43 | pF |

DUT=direct measurement of sample, DUT subtract=de-embedded

- Inductance (short cal):

| | DUT+card | card | DUT | DUT subtract | |
|--------|--------------|--------------|-------------|--------------|----|
| 50 MHz | 52.49 | 50.90 | 1.54 | 1.60 | nH |

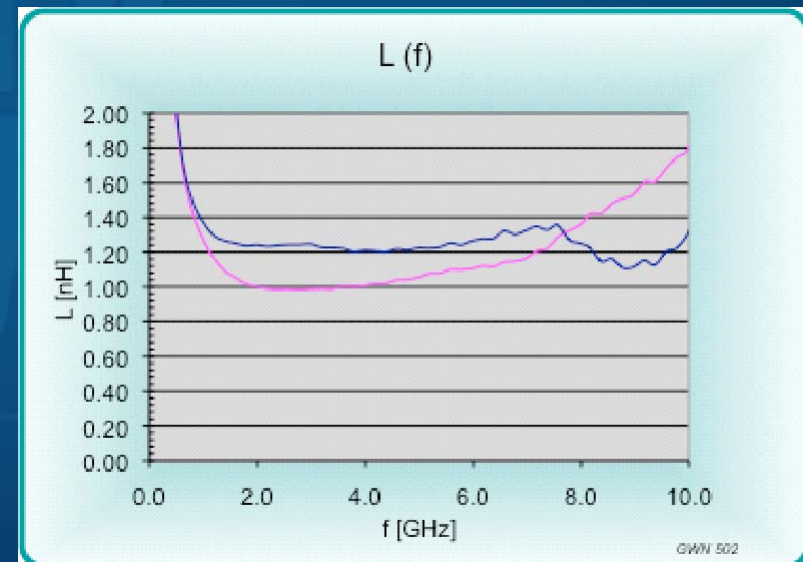
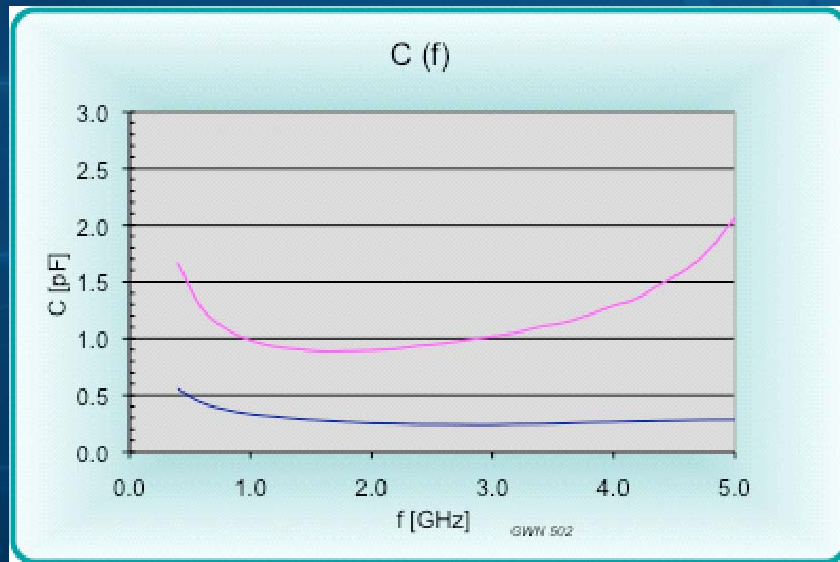
❖ But.....there is a small warning flag.....

Frequency dependence

- **Examine frequency dependence of results with a network analyzer based technique**
 - Calibrate as previously (open/short) at location of probes or probe tips
 - Measure return loss phase
 - Add probes or DUT
 - Measure return loss phase again
 - Subtract

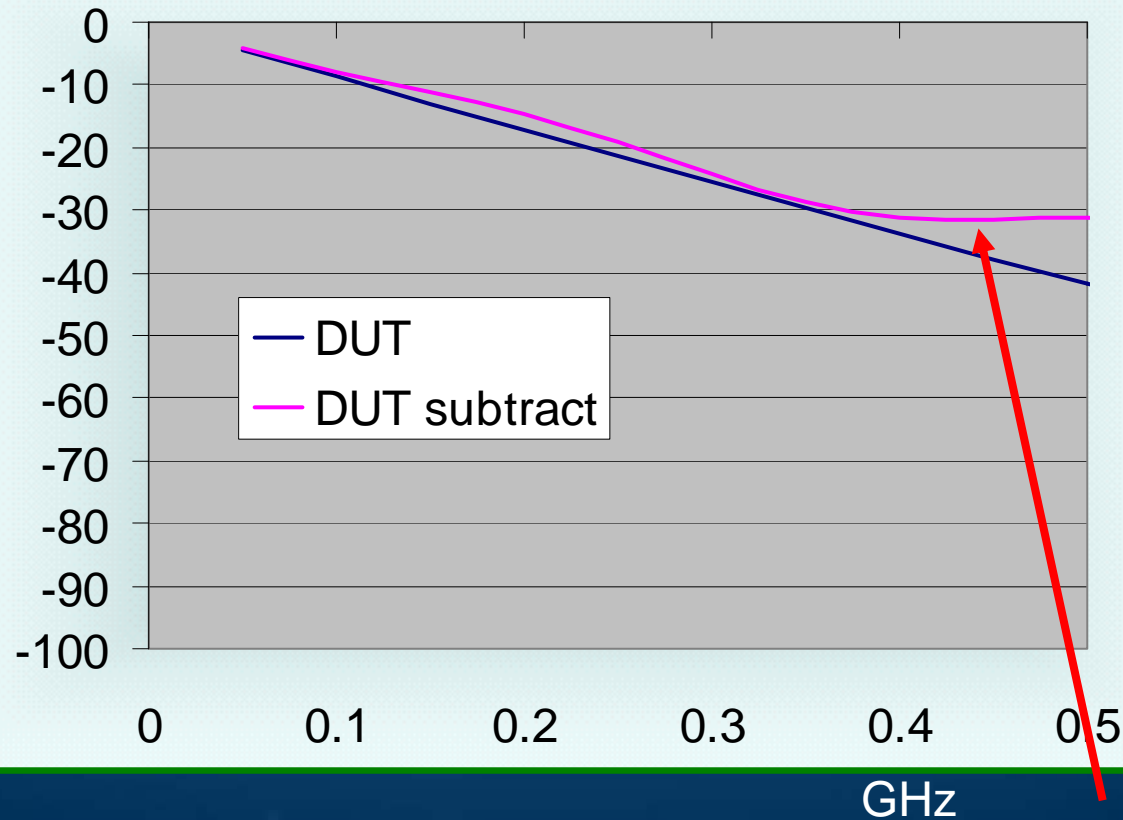
Frequency dependence example

- Beyond possible measurement error there is at least one other compelling reason to examine capacitance and inductance as a function of frequency:



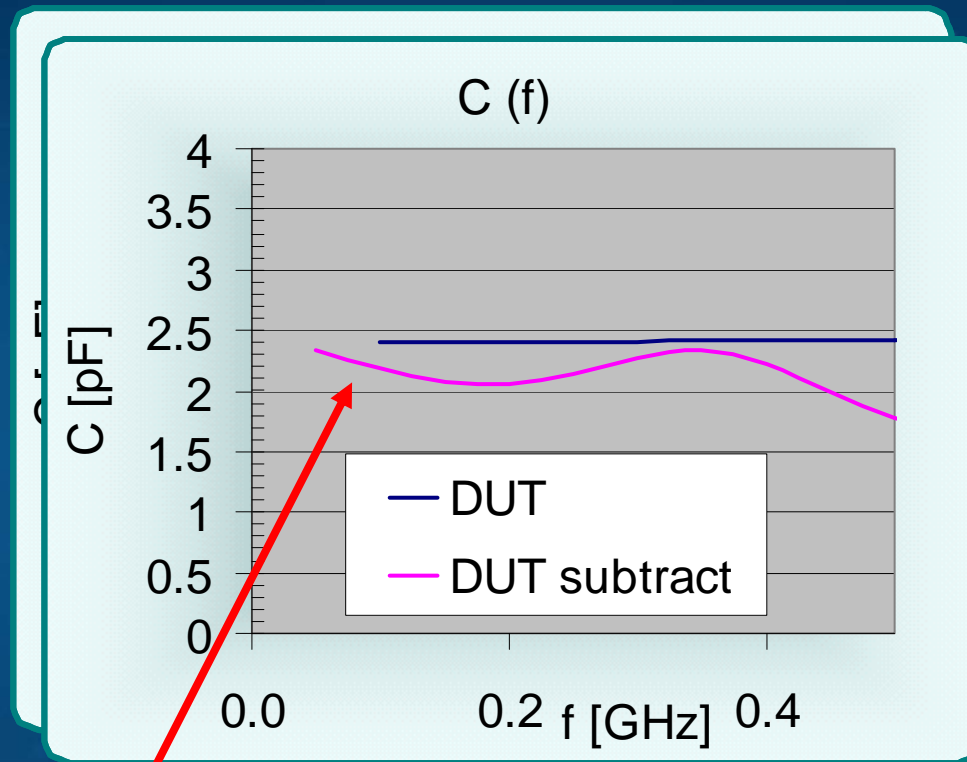
Phase de-embedding by subtraction (capacitance)

deg



The error term seems to become significant above 400 MHz

Capacitance as a function of frequency



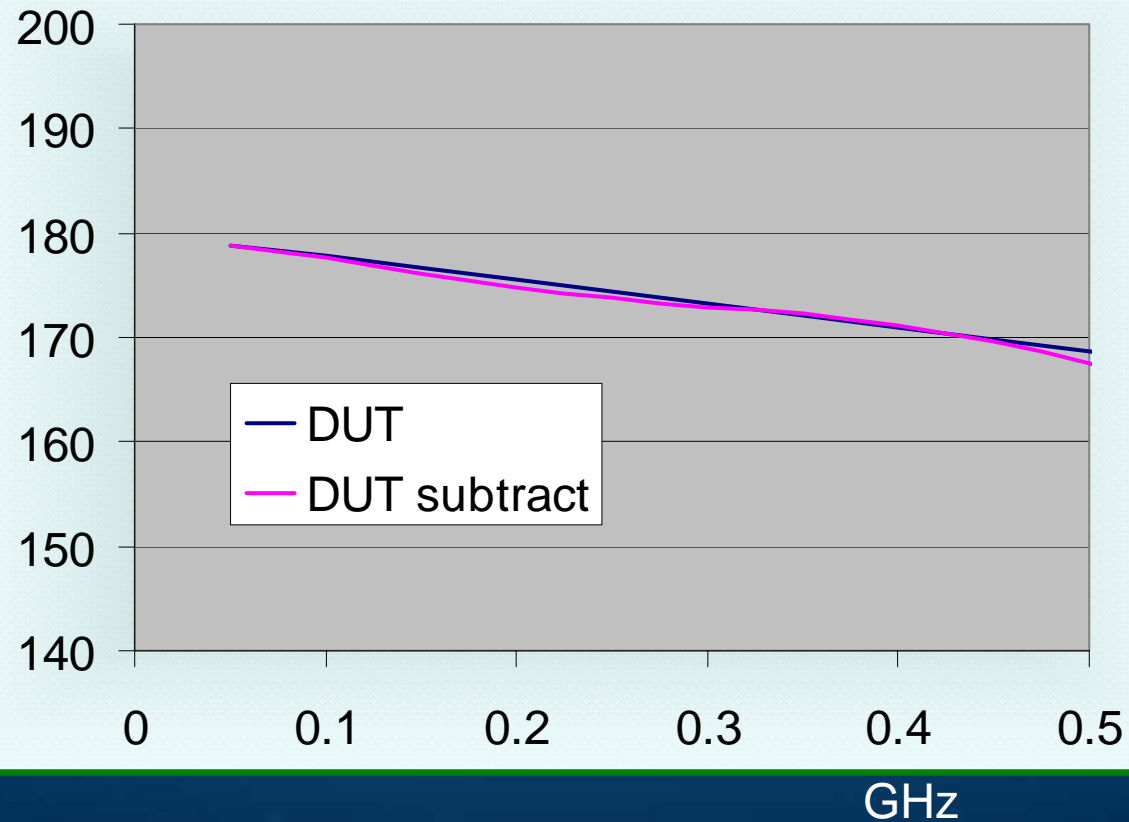
DUT:
direct
measurement
of sample

DUT subtract:
de-embedded

The error term becomes noticeable above 50 MHz, whether this is significant or not depends on the application and end user requirements

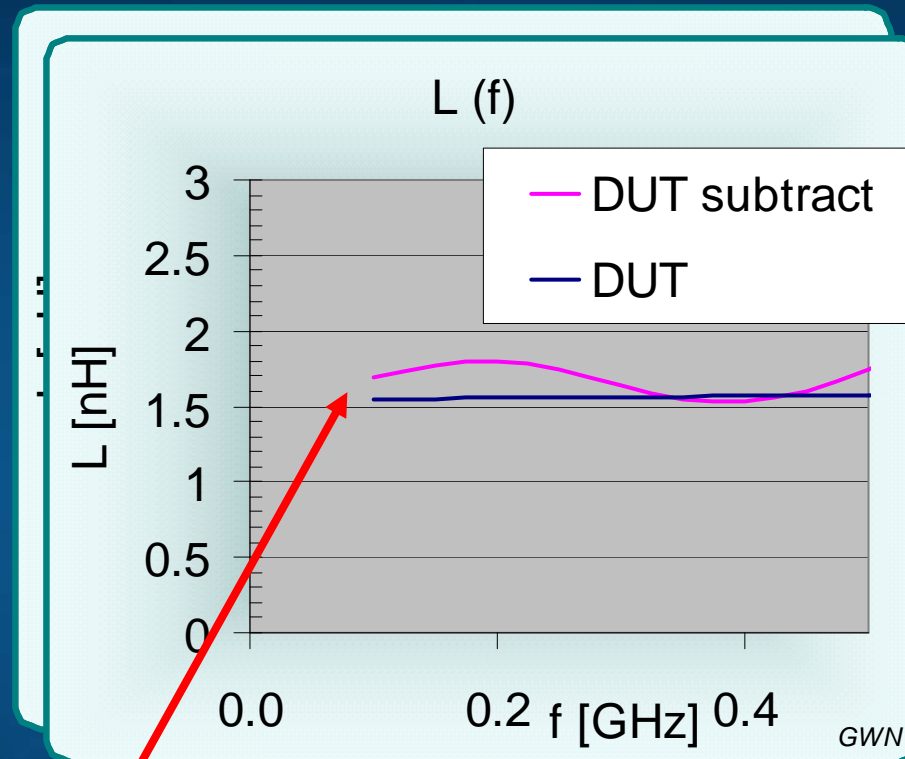
Phase de-embedding by subtraction (inductance)

deg



Only small error terms are present

Inductance as a function of frequency

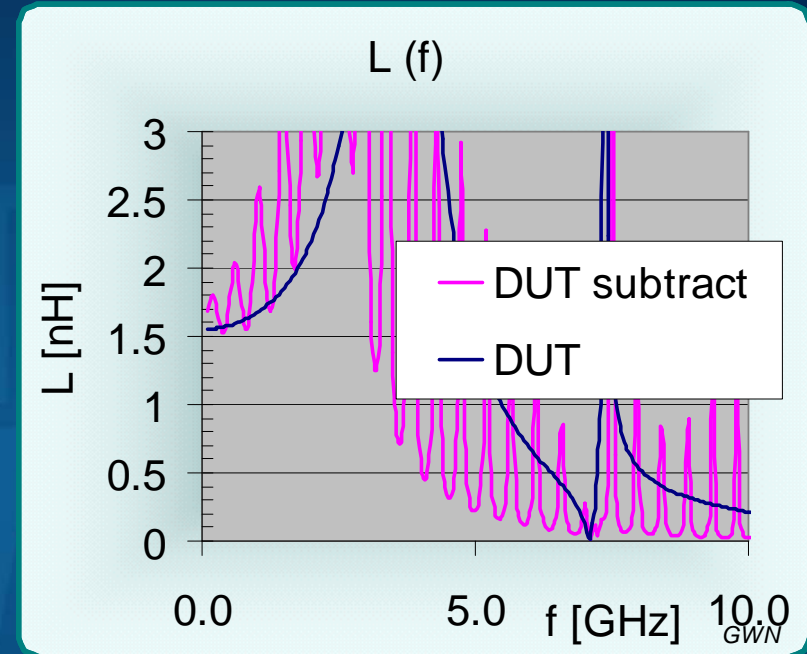
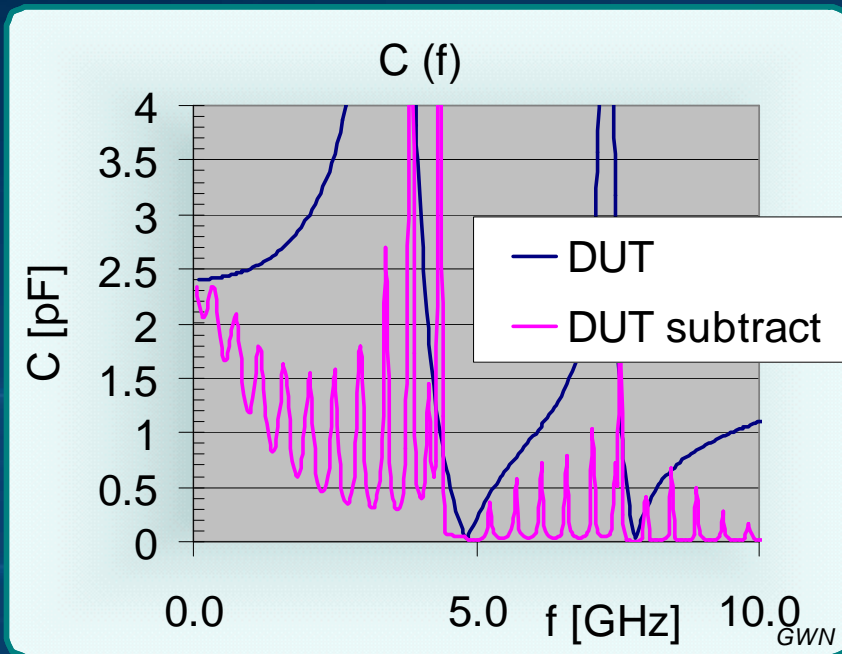


DUT:
direct
measurement
of sample

DUT subtract:
de-embedded

The error term becomes noticeable above 50 MHz, whether this is significant or not depends on the application and end user requirements

Extended frequency range results



Subtraction is not a valid technique at elevated frequencies.

Reason: Transmission lines cause impedance transformation.

DUT:

direct measurement of sample

DUT subtract:

de-embedded

De-embedding with a VNA (vector network analyzer)

- **Acquire data at the wafer level with a calibration wafer**
 - SOL and other standard calibration techniques
- **Use VNA's built-in calibration to remove path contributions**
 - Requires 'capable' VNA
- **Use VNA data externally with 'capable' software to remove path contributions**
- **Extract desired information from S-parameters**

De-embedding with a VNA

- A modern VNA is capable of removing contributions from imperfect interconnects
- **Problem: Calibration to the desired reference plane**
 - It is generally necessary to provide at least a short and open and a load. While the open is relatively easy to provide, both short and load present problems.

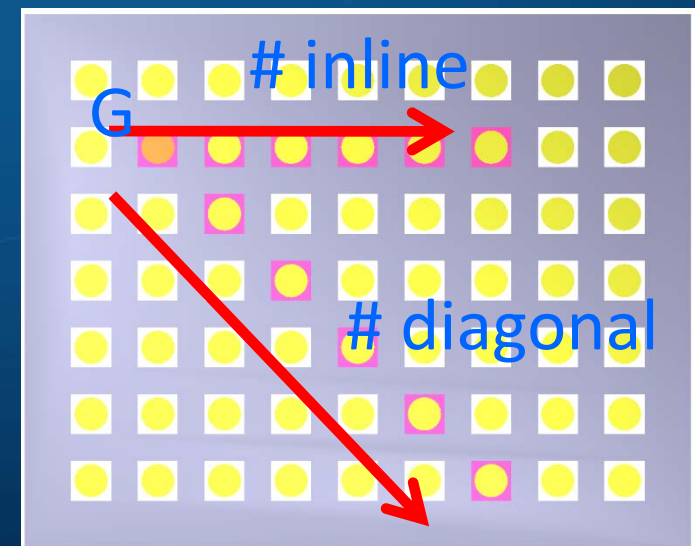
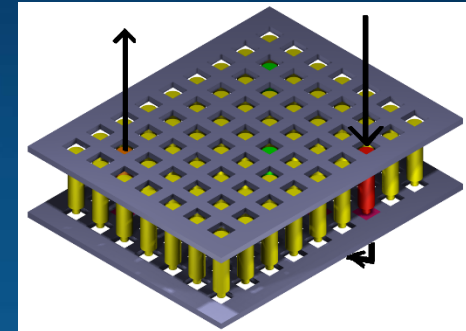
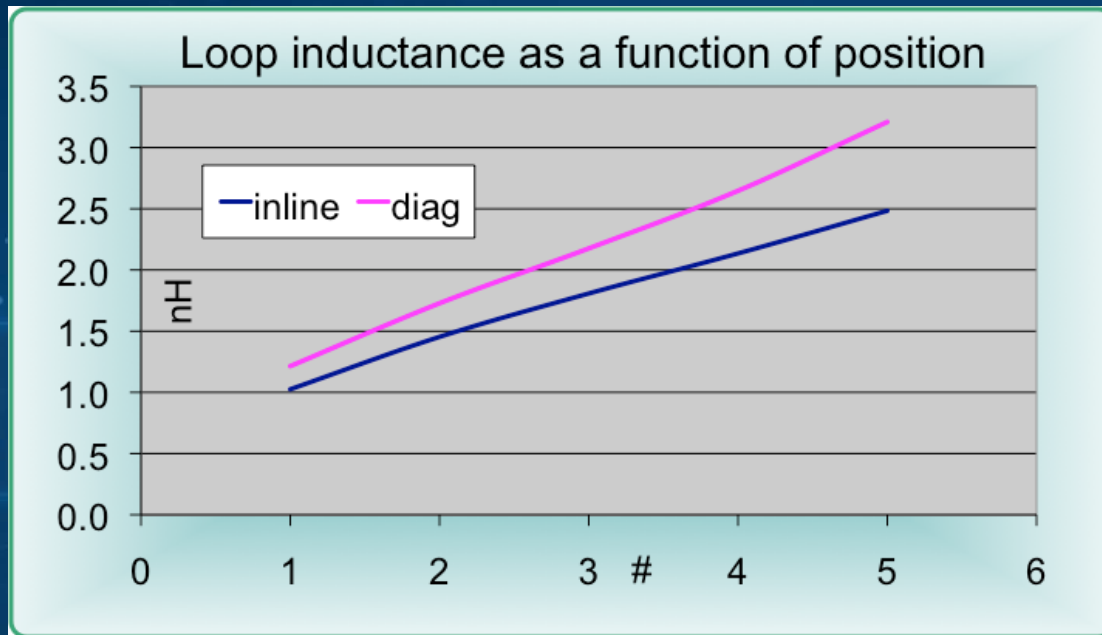
Calibration method examples

- SOLT, SOL
- TRL
- 1-port AFR

Calibration issues

- When attempting to measure inductance it is necessary to provide a good short circuit at the reference point.
- Distance from signal to ground becomes a problem since there will be “spreading inductance” in the ground return. This is particularly significant if the reference plane is to be atop the probes

Ground position dependence of inductance



Inductance as a function of location with respect to ground 'G'

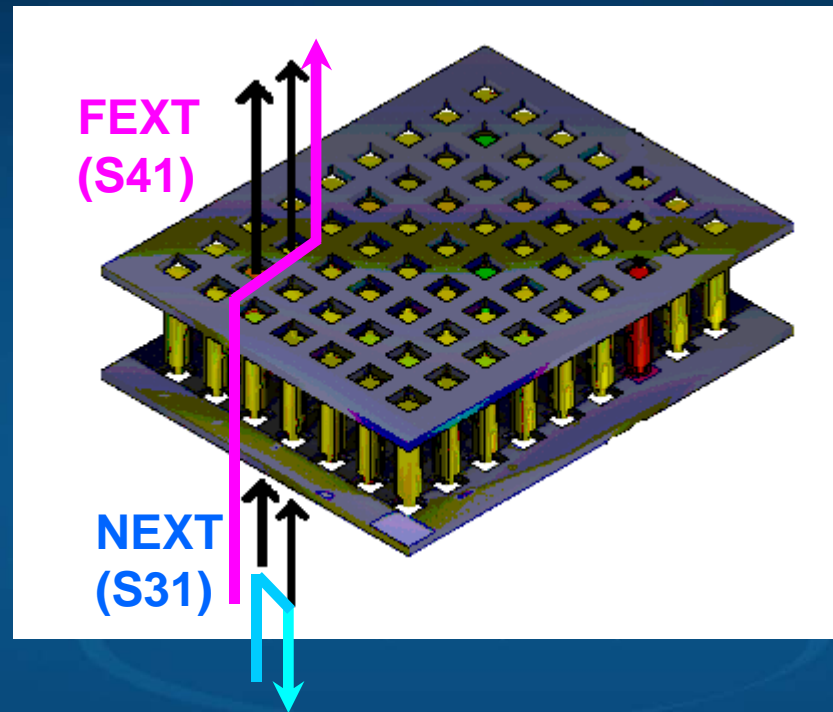
Load calibration

- **‘Spreading’ inductance can falsify results**
 - Design PCB or interpose such that sufficient grounding is available near the connection if interest
 - Use alternate techniques, e.g. calibrate to base of probes and characterize probes separately, then cascade models with the unknown DUT.

What about 'lesser' VNAs ?

- Unless advanced algorithms are applied in the VNA the calibration will not be able to properly remove effects of impedance discontinuities.
- In this case, de-embedding must be performed externally:
 - Advanced circuit analysis model software
 - with advanced matrix algorithms (for example based on T-parameters)

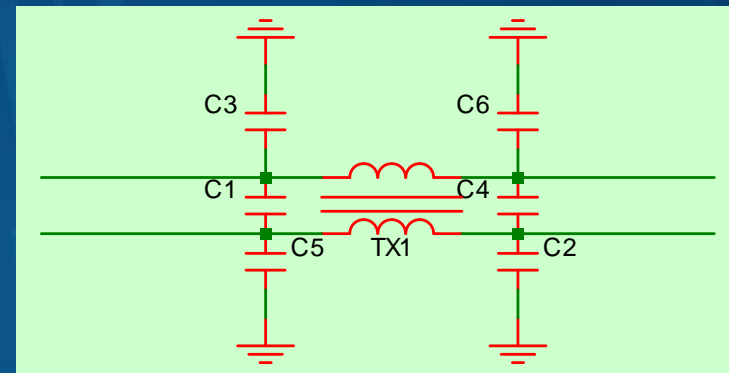
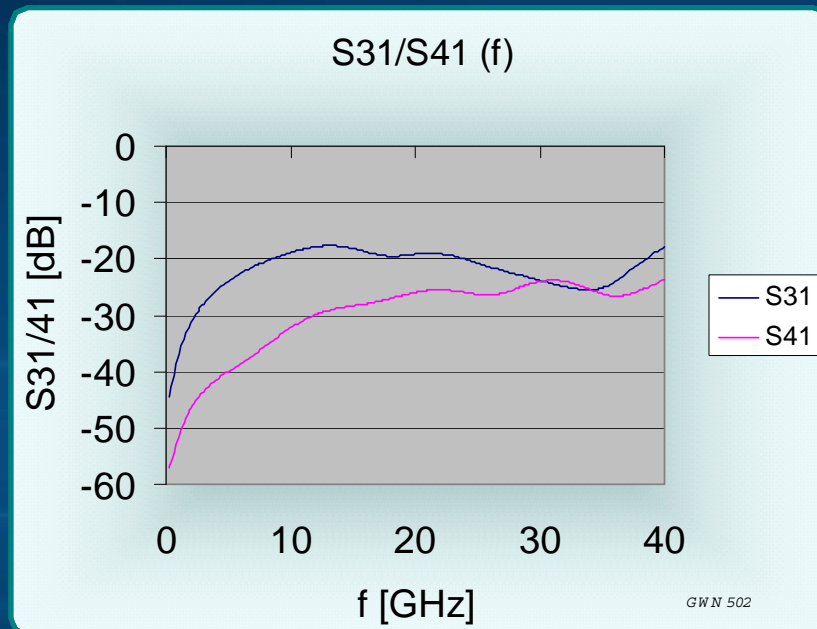
Mutual inductance and capacitance



It is possible to extract mutual inductance and capacitance from a set of measurements on two adjacent contacts.

Calibration for two adjacent channels will be different but conditions are favorable and only a small error results.

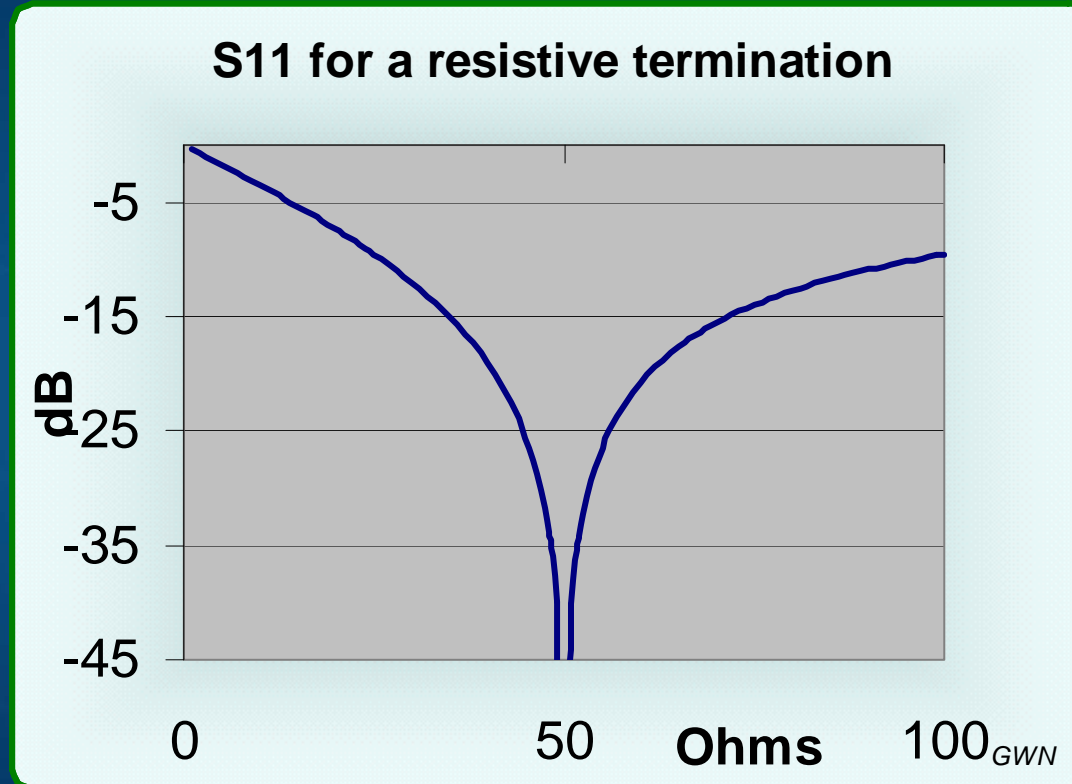
Example



In its simplest form a set of probes can be represented as a PI network composed of coupled inductors together with capacitors to ground and mutual capacitance. This model can then be matched to measurement results to determine mutual elements.

Resistance measurement with a VNA

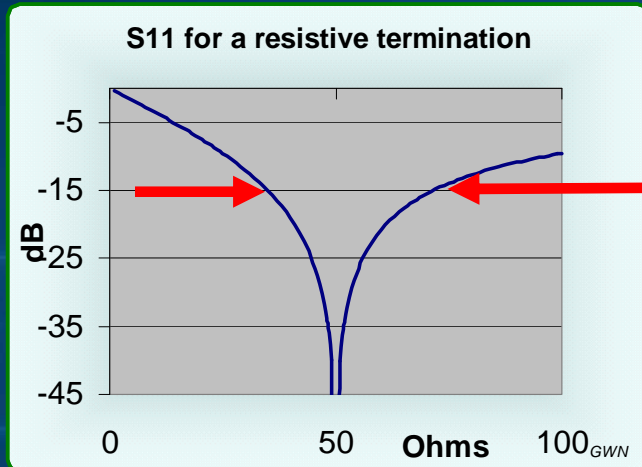
$$RL(S11) = -20 \cdot \log \left(\frac{R - Z_0}{R + Z_0} \right)$$



Z0 :
50 Ohms

Return loss as a function of load resistance

Ambiguity in results



Two resistance values with identical S11 value exist

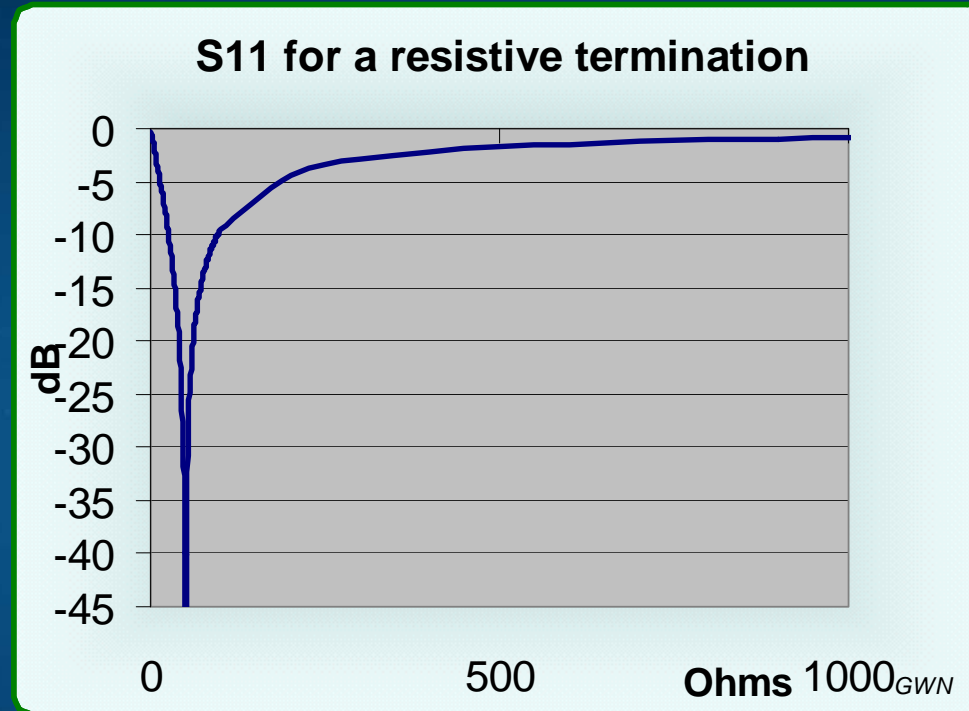
Phase for $R > Z_0 = < 0$ deg at low frequencies

Phase for $R < Z_0 = < 180$ deg at low frequencies

$Z_0 :$

50 Ohms

Resistance measurement limitations



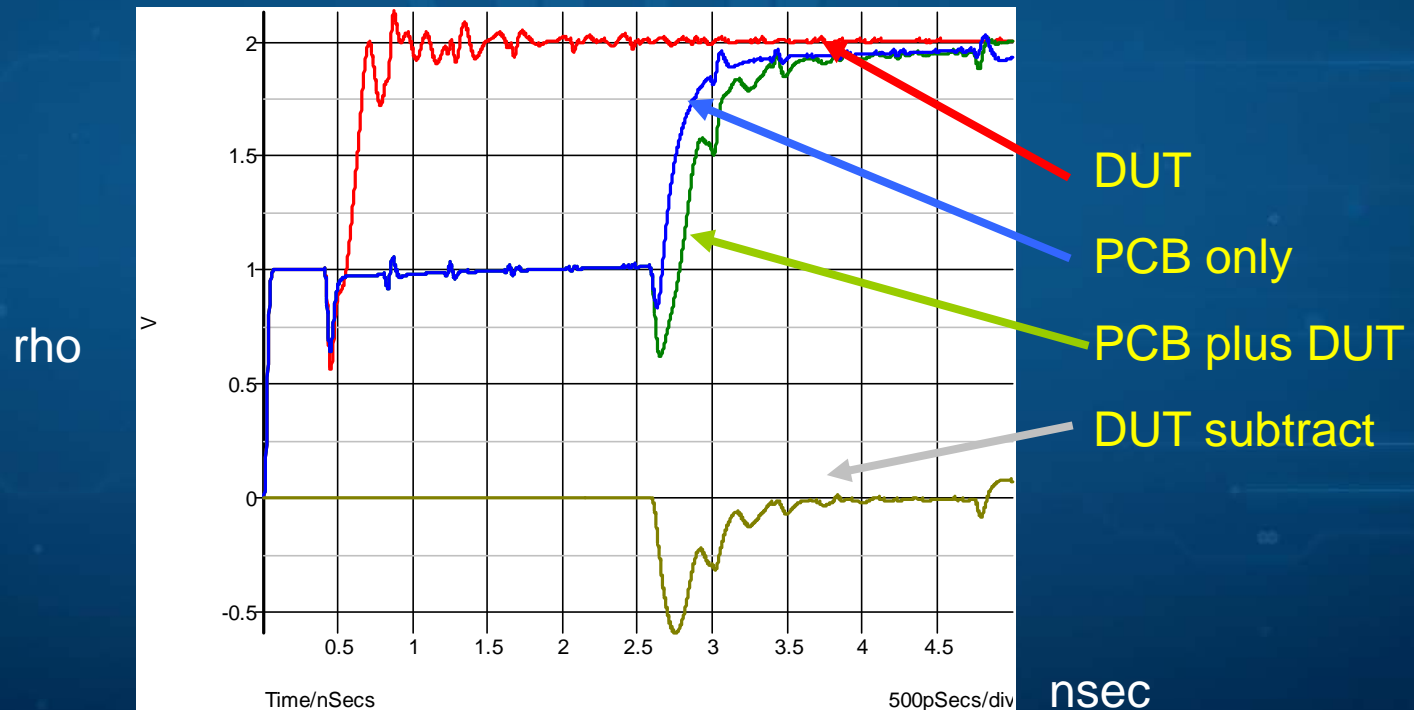
Z0 :
50 Ohms

Accurate measurement of high resistance values is difficult with a 50 Ohm VNA

Alternate measurement methods

- Time domain response

- Can give a general idea of device properties
- Rise time can deteriorate seriously through probe card



Alternate calibration methods

- Known DUT substitution

