



SW Test Workshop

Semiconductor Wafer Test Workshop

June 7 - 10, 2015 | San Diego, California

Determining Probe's Maximum Allowable Current



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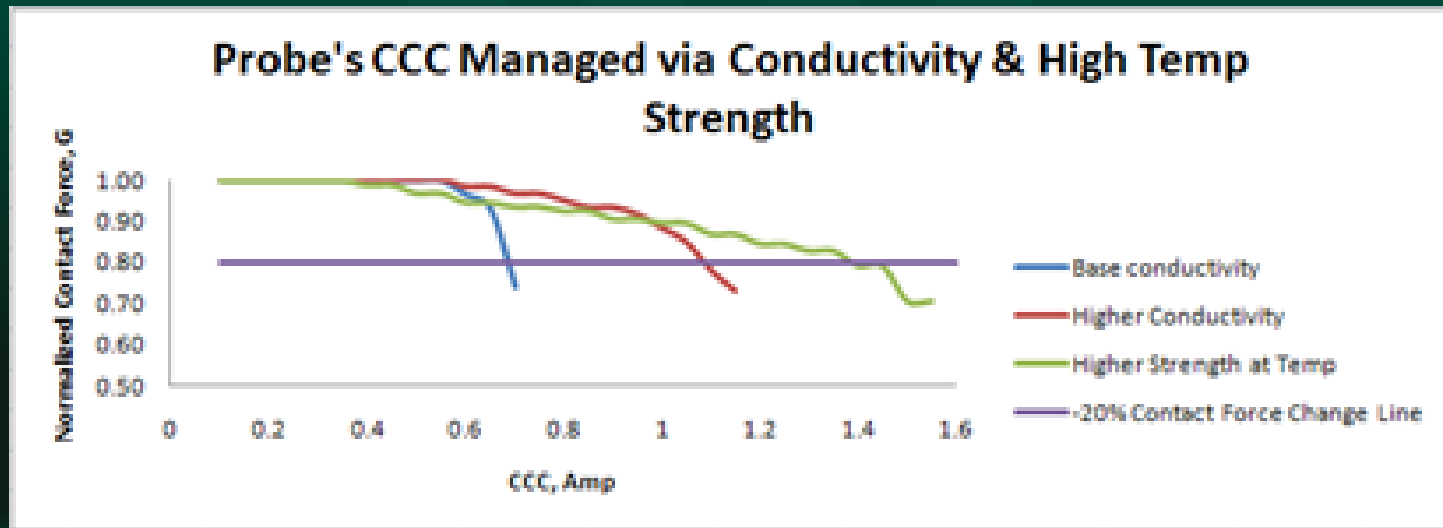
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Overview

- ISMI CCC Spec vs. what wafer test engineer needs to know
- Introducing Maximum Allowable Current (MAC) concept
- Method for finding singular MAC value
- Confirmation of MAC performance in repeatable loading
- Relationship between MAC and CCC
- MAC vs. current pulse width
- Ways to minimize transient currents in wafer test
- Conclusions

Definition of CCC

- CCC = Current which results in a 20% contact force reduction
 - Below plot typical of SEMI-defined methodology
- CCC modulated by several variables
 - Here, improvement achieved through probe material conductivity (electrical and thermal) and high temperature strength increase

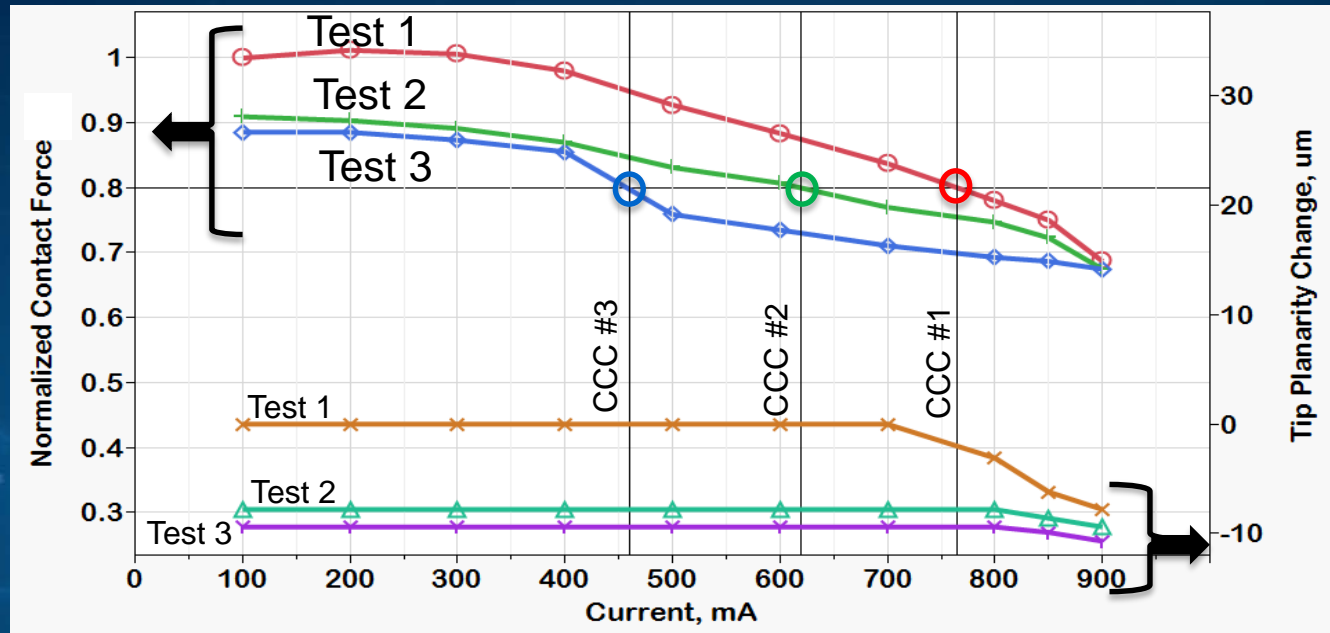


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CCC-level Current Damages Probes

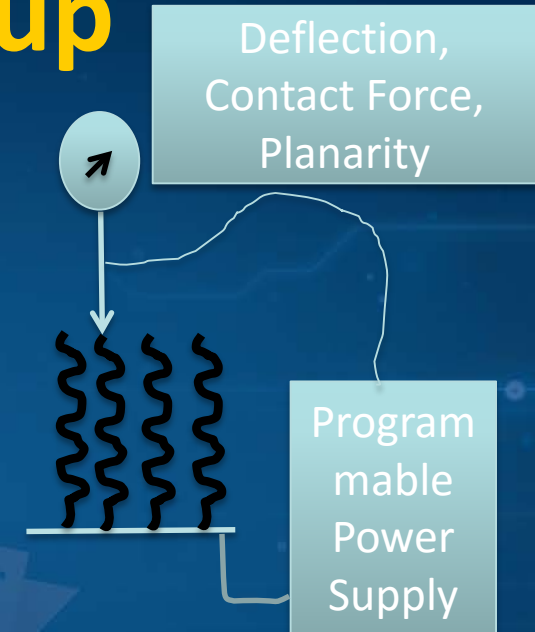
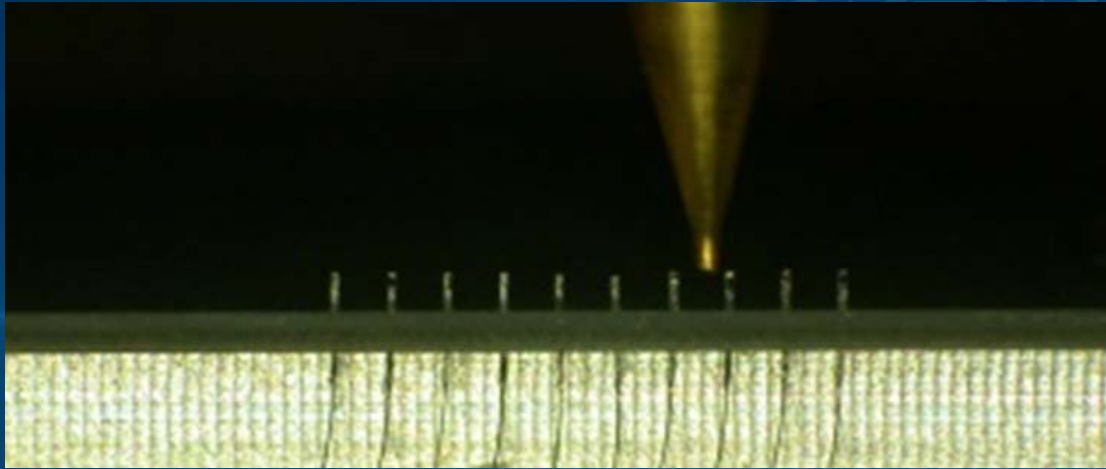


- The same probe tested for CCC three times shows diminishing actual CCC and Tip planarity, ~150mA reduction per test
- Probes cannot sustain CCC-level current due to loss of planarity and contact force
- CCC spec causes many misunderstandings between users and probe card suppliers
 - Why can't I use CCC spec for current clamp setting?
 - Why does probe card contact performance degrade over time after exposure to CCC?

Probe ISMI-CCC Spec Does not Define Current that Probe Could Carry After Multiple Exposure in Production

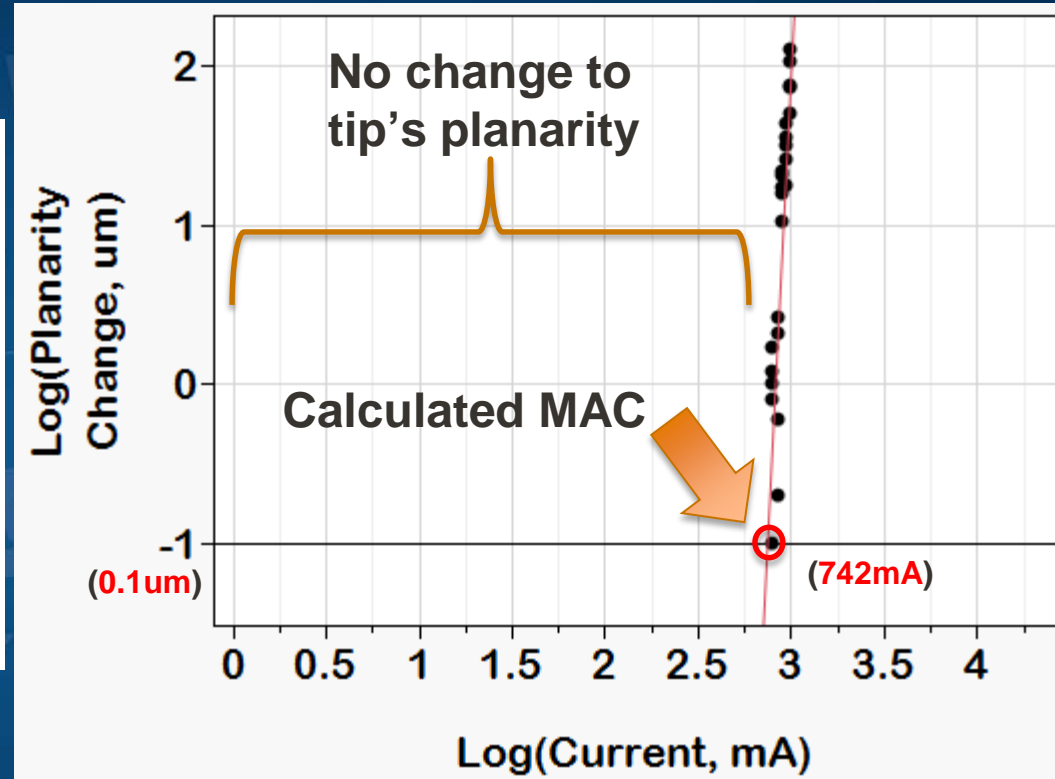
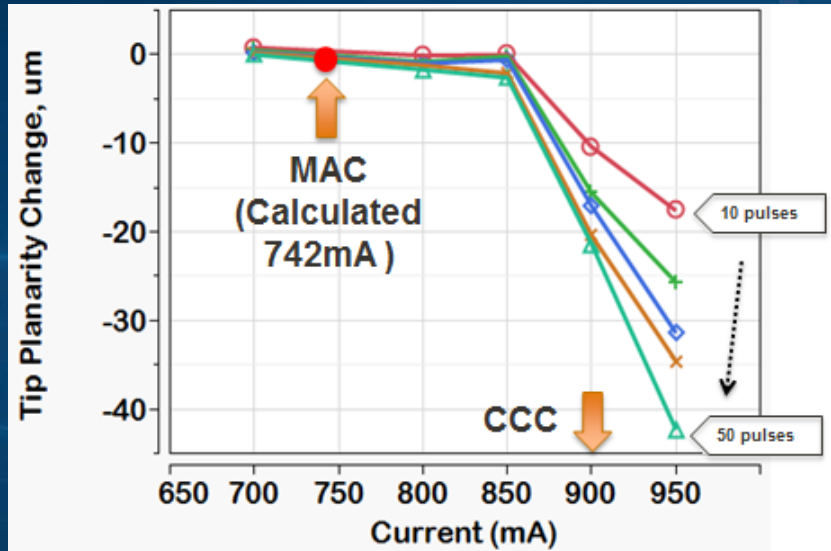
- **Disparity between what test engineer needs to know about the probe and what ISMI-CCC spec defines:**
 - Test engineer asks for maximum current that can be carried by the probe thousands of times without changing probe's performance (planarity, alignment, contact force, CRES)
 - ISMI-CCC test itself causes a permanent damage to the probe - probe is deformed and contact force lowered by 20% after one current event
- **Methodology is needed to measure Maximum Allowable Current that can be applied over and over throughout product life time**
 - To help with setting power supply current clamp in tester program

Maximum Allowable Current Measurement Setup



- Use probe tip's planarity change in response to current pulses as a proxy for defining probe's Maximum Allowable Current (MAC)
- Each probe is tested at a unique current level in increasing number of pulses, (1 min On /1sec off) representing real life test scenario

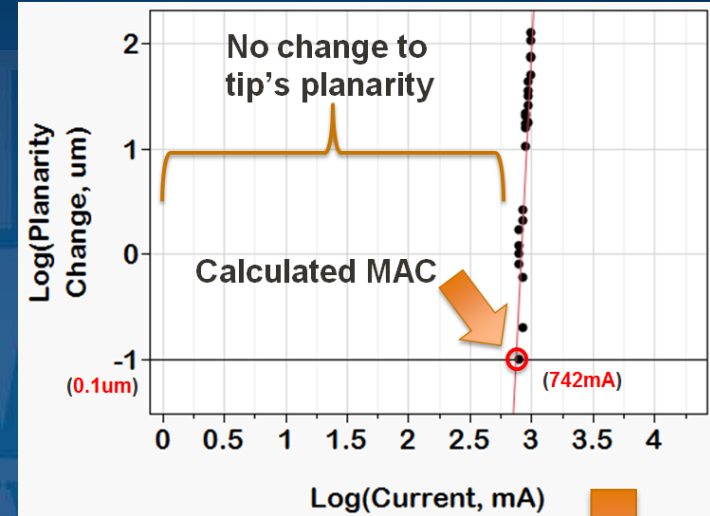
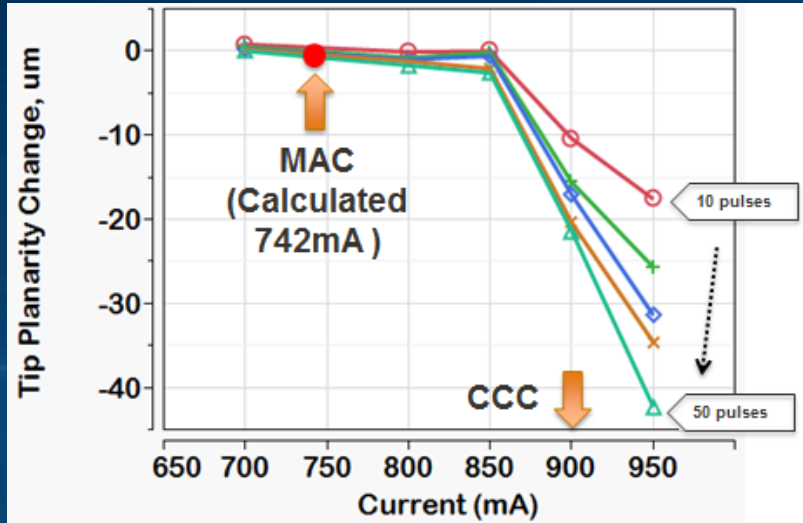
Maximum Allowable Current Calculation of MAC value



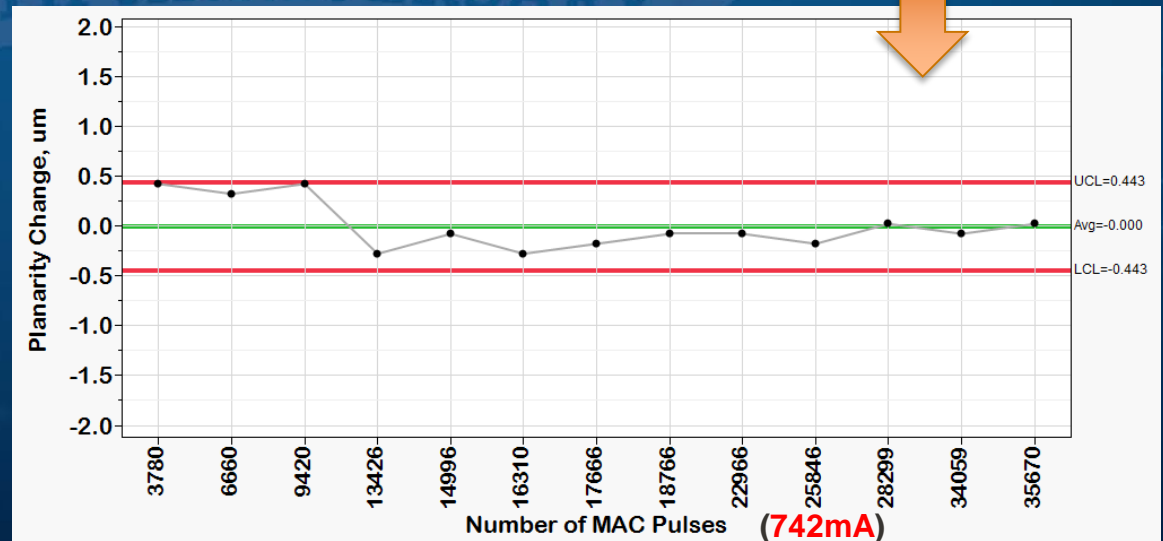
- Plotting Log of planarity change vs. Log of current (use linear scale) allows for linearization of otherwise asymptotic curve
- Finding best-fit line equation to the data is easy and used to calculate MAC, in this case $MAC = 10^{(2.8705)} = 742$ mA for planarity change = 0.1um

Confirmation of MAC concept, Stable Probe

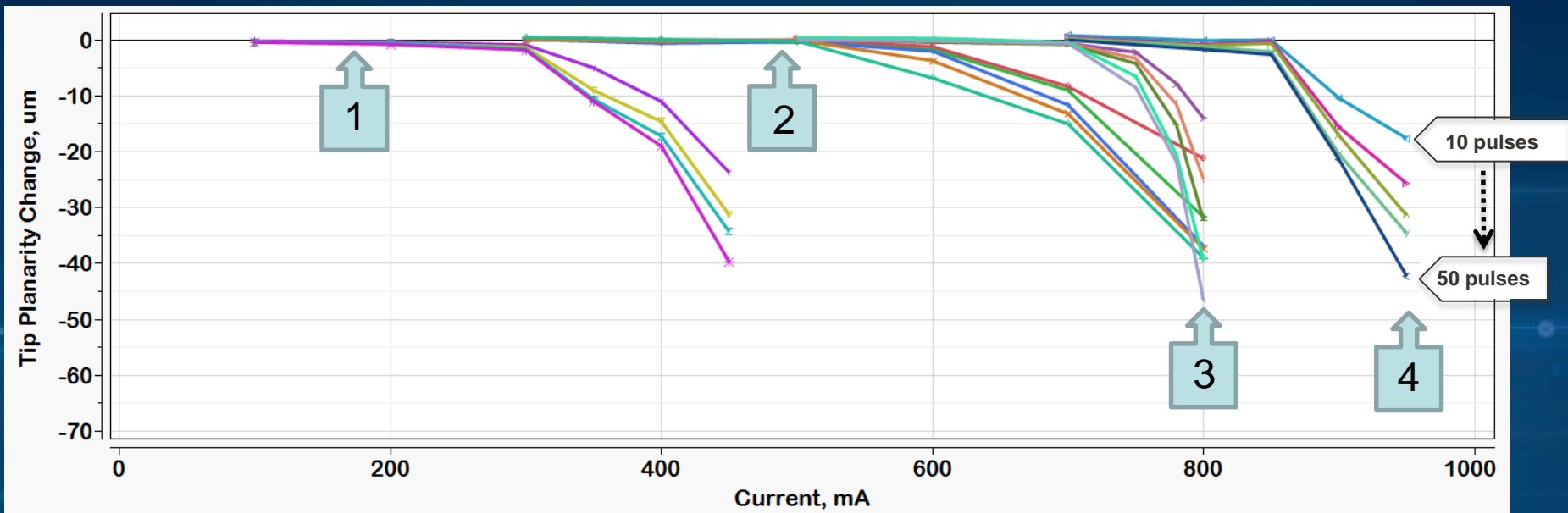
Tip Planarity after 35k MAC pulses



- No change to probe tip's planarity during the performed 35k MAC (742mA) pulses
- Each pulse 1min-on/1sec-off
- 75um probe deflection



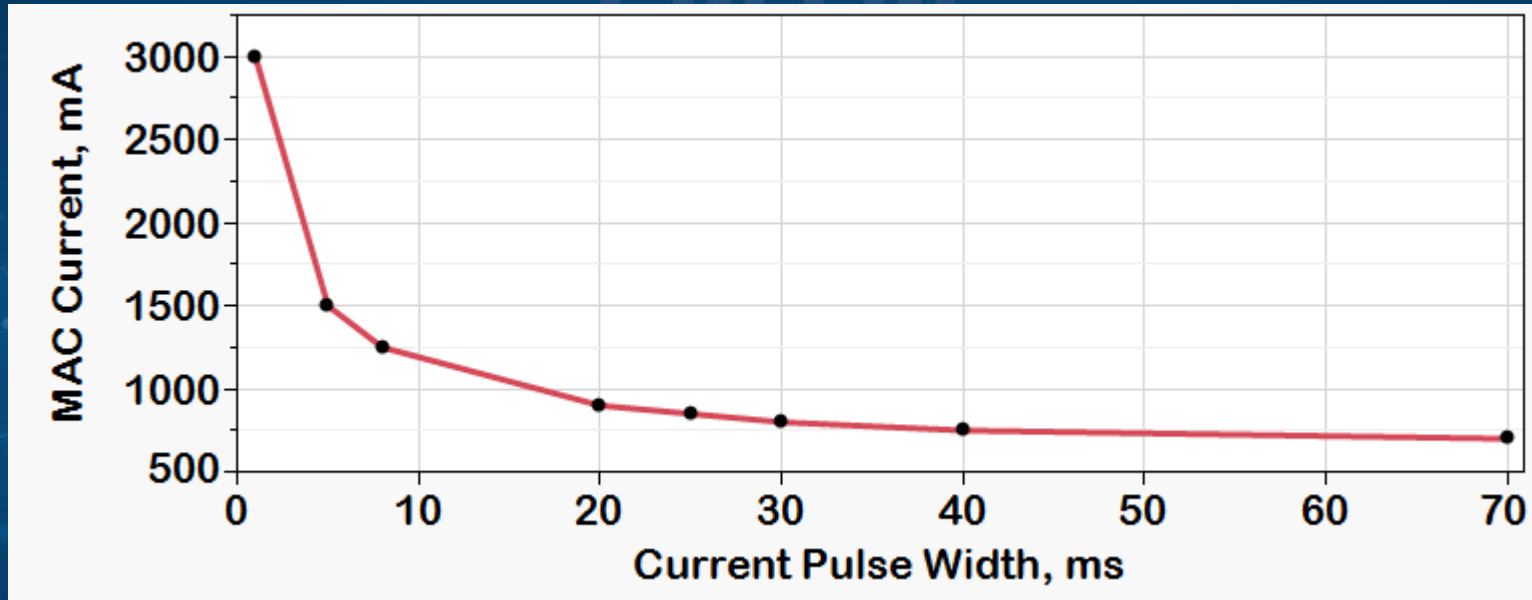
MAC vs. CCC for a Range of Probes



- **MAC/CCC Ratio is not a constant, is probe architecture dependent**

Probe	ISMI CCC, mA	MAC, mA	MAC/CCC
1	450	278	~0.6
2	800	478	~0.6
3	800	637	~0.8
4	900	742	~0.8

MAC vs. Current Pulse Width for a 900mA CCC/742mA MAC probe



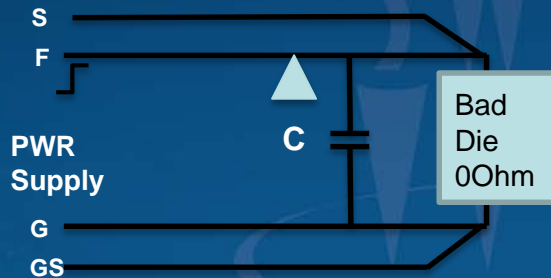
- For current pulse $\geq 70\text{ms}$ the MAC value does not change
- Practical current pulses used in wafer tests exceed 70ms, therefore, shorter pulses cannot be used to “increase” MAC
- Ultra short pulses ($<1\text{ msec}$) can help “transient current” management

Impact of Test and Power Supply on Probes

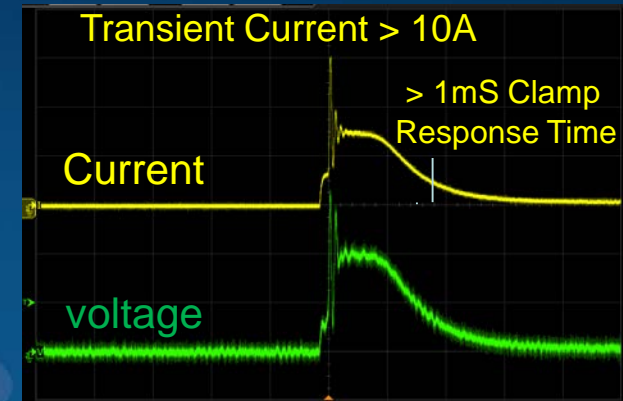
- Significant static and transient currents can happen during wafer test due to electric shorts in faulty chips
 - >2A current have been experienced
- Faulty devices must be screened out at lower voltage setting with current clamp limits set \leq MAC at the beginning of the wafer test
 - Full voltage and higher clamp limits are applied only to confirmed good die
- Management of power supply is needed in the test program to protect probes:
 - Current range, clamp limits and the response time -> example 1
 - Power supply slew rate (dv/dt) and transient current magnitude -> example 2

Example 1: Current Profile and Clamp Response Time

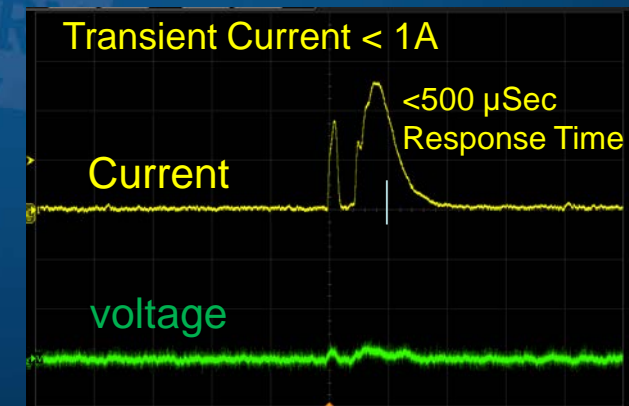
- **Test Case: Clamp response time for the same power supply under 100mV step into a shorted device (Vdd shorted to Vss) at different current range**



Higher Current Range



Lower Current Range

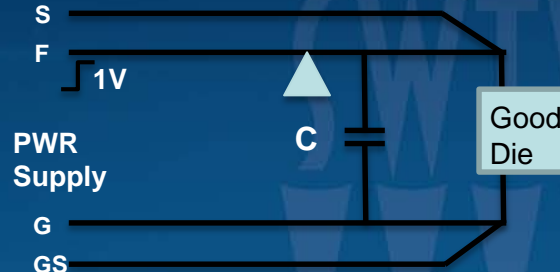


- **Current clamp is effective in limiting static current; however, its response time is not fast enough to completely limit the transient current**
- **To protect probes from damage, transient current magnitude and duration must be limited**
 - Select lower current range of the power supply to reduce transient current spikes
 - Reduce clamp response time by switching off large capacitance

Example 2: Slew Rate Effect on Transient Currents

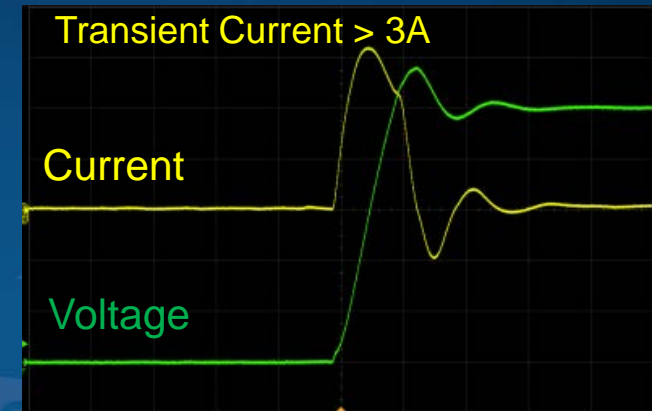
- **Test Case: Transient current response versus Voltage slew rate. Same power supply.**

No current clamp



- **Case 1 :**
 - Fast Slew Rate 50 x
 - > 3A peak current within 1 milli-second
- **Case 2 :**
 - Slow slew rate 1x (digitally controlled in steps)
 - < 200mA peak current
- **Slower slew rate minimizes magnitude of current surge to protect probes; however, it can have a small impact on test time**
- **Actual current going through the probes depends on device and capacitor impedance**

Case 1: 50x slew rate



Case 2: 1x slew rate



Conclusions

- **The Maximum Allowable Current (MAC) represents actual current that probe can safely deliver, a more reliable specification than CCC**
- **MAC is defined as current level at which probe will not change its planarity or cause permanent damage in repeated use**
 - Duty cycle representative of test time and prober indexing time
- **MAC is lower than CCC, however the MAC/CCC ratio is not a constant number – varies based on probe architecture**
- **For current pulse shorter than 1 millisecond, a probe can sustain significantly higher current than MAC without damage**
- **Current clamp is effective in limiting static current; however, its response time is not fast enough to completely limit the transient current**
- **Slower power supply slew rate minimizes magnitude of transient current to protect probes**