Panel Discussion

Chair: Michael Huebner
FormFactor Inc.
Panel Discussion

- Panel members
  - Mark Ojeda (Spansion/Cypress) Panel: I/II
  - Rey Rincon (Freescale) Panel: II
  - Al Wegleitner (TI) Panel: I/II
  - Clark Liu (PTI) Panel: I
  - Kurt Guthzeit (Micron) Panel: II
  - Marc Loranger (FFI) Panel: I/II
  - Darren Aaberge (MJC) Panel: II
  - Raffaele Vallauri (Technoprobe) Panel: II
  - Phill Mai (JEM) Panel: I
  - Rob Carter (MPI) Panel: I/II
  - Debbora Ahlgren (Feldman Engineering) Panel: I/II
Session 4 – Panel Discussion I

• How will probe cards look like 2-5 years from now?
  – What will be the next big innovation?
    • Which one is our biggest challenge?
  – Will we have more wafer test or less?
  – Will Cantilever go further?

• Panel members
  – Mark Ojeda (Spansion/Cypress)
  – Al Wegleitner (TI)
  – Clark Liu (PTI)
  – Marc Loranger (FFI)
  – Phill Mai (JEM)
  – Rob Carter (MPI)
  – Debbora Ahlgren (Feldman Engineering)
How will probe cards look like 2-5 years from now?
- The challenge is a larger array size coupled with reduced pad pitch
- Relentless charge to lower test cost = more parallelism at wafer test
  - Memory has driven parallelism to full wafer test for many companies
  - Logic test is about to take the learnings of memory to make strides at higher
- More functions on smaller chips driving pad pitch to 50um on peripheral
  - This complicates the drive to higher parallelism
  - Need to develop a full wafer contact with a 50um pad pitch
  - Need up to 60,000 probes on a probecard
How will Probe Cards look in 2-5 years from now

• Memory Innovations
  – pad size and pitch due to reduced die sizes
  – Next generation after DDR4 and LPDDR4
  – More stacked memories
  • HBM

• Key drive will be to reduce the cost of test
  – Increase in parallelism
  – New ATE systems aid by with increased parallelism and test time reductions
Session 4 – Panel Discussion I

• How will probe cards look like 2-5 years from now?
  – What will be the next big innovation?
    • Biggest challenge from WLP Probing!

  – Will we have more wafer test or less?
    • Yes, More and More Complex!

  – Will Cantilever go further?
    • Yes, Form Cycle Time / Cost / Engineering still keep going.

  – [See more at S06_03_Clark_WLP Probing Opportunity and Challenge]
Will we have more wafer test or less?

A debate-able response!!

• In general, yes!! More wafer test
  – Ensuring the quality/reliability of devices that are packaged in a variety of ways
  – Enabling the distributed manufacturing base of fabless & IDMs alike

• But, for WL-CSP???
  – Numerous interesting alternatives are emerging!
Session 4 – Panel Discussion I

- How will probe card look like 2-5 years from now?
  - What will be the next big innovation?
    - Biggest challenge from Tester Resource Instrumentation!
    - Probe card sensors to self check card – BIST for probe card
    - MUX Tester on the probe card

- Will we have more wafer test or less?
  - Yes, Significantly > Complexity
  - Package test Move into Probe, Burn-In – Stress into Probe
  - High Voltage, Current, Speed, BAW, Radar

- Will Cantilever go further?
  - Yes, but limited
  - Cycle Time / Cost / Engineering – prototype first
  - Move to vertical after engineering – exchange heads – same pcb
Session 4 – Panel Discussion I

How will probe cards look like 2-5 years from now?
Q: Will Cantilever go further?

Current LCD Driver Probe Card Technology
Pitch: 4-rows staggered 9/18/27/36 um
Digital Data Rate: 4 Gbps
Future:
• Technology advances are improving capabilities
  • Higher Pin Counts
  • Faster Data Rates
  • Finer Pitches
• Cantilever technology continues to provide a competitive edge to many new and existing users via unsurpassed C.O.O.
• Continued growth is expected from LCD Driver expansion along with acceptance in markets such as CMOS Image Sensors, tight 3DIC applications and others

Fact: The CPC, although not gaining market share when compared to other technologies, remains a growing and healthy industry solution!!!
Will Cantilever Go Further?

Advantages:
- Short lead time
- Inexpensive
- Fine pitch (<50 um)
- Coax structure for RF or parametric

Disadvantages:
- Pad geometry/multiparallelism limited
- Limited material selection (W, ReW, P-7, BeCu)
- Probe-to-probe variation

Development:
- Materials/Composites
- Automated probe manufacturing
Session 4 – Panel Discussion II

• **Increase in parallel test and the consequences**
  - Test strategies Memory and SOC and implication on probe cards
    - What are the strategies, plans for SOC/Memory?
    - Tester vs. DFT vs. more capable probe cards
    - Strategies to increase component density, routing density

  - **Infrastructure of high parallel probe cards:**
    - Analyzers (is there still a need – can you repair these cards on analyzers)
    - Repair strategies for super high pin count
    - Which infrastructure changes are needed
    - Docking of huge probe cards

  - High parallel Micro Bump probing is there a need, what would be the challenges?
Panel Discussion

- Panel members – Panel II
  - Mark Ojeda (Spansion/Cypress)
  - Rey Rincon (Freescale)
  - Al Wegleitner (TI)
  - Kurt Guthzeit (Micron)
  - Marc Loranger (FFI)
  - Darren Aaberge (MJC)
  - Raffaele Vallauri (Technoprobe)
  - Rob Carter (MPI)
  - Debbora Ahlgren (Feldman Engineering)
Tester vs. DFT vs. more capable probe cards

- **New reduced pin DFT is allowing higher parallelism**
  - Current testers require more DC fan out to take advantage
  - Probe card components have increased 4x from older DFT
  - Switch control has moved from tester resources to a dedicated comm bus for needed control

- **Different designs for each supplier is not desired but happening due to component space**
  - Each supplier has slightly different keep outs
  - Some have proprietary circuits

- **We should move sharing off of the probe cards**
  - It is limiting max parallelism
  - With unique designs we can lose supplier competition
Increase in parallel test and the consequences

- **SoC Test**
  - Need to learn from memory
    - Better DFT for increasing parallelism

- **Memory Test**
  - Must reduce pins per DUT
    - Fewer input only, less I/O and fewer DC pins
  - Increase parallelism to track next generation ATE capability
  - Spring counts up to 150K
Session 4 – Panel Discussion II

• **Increase in parallel test and the consequences**
  
  – Higher parallelism necessitates better DFT
    - Silicon cost of DFT continues to reduce making it more palatable in design
    - Reduce component density on probecard PCB
    - Reduce routing complexity of probecard PCB
    - Anything else raises the cost of the probecard, now the highest expense for many companies.

  – Infrastructure of high parallel probe cards:
    - Analyzers tend to cause more problems then they solve
    - In house repair is becoming prohibitively expensive
    - Need local repair facilities to minimize turn around time
    - Docking of huge probe cards is tricky due to the forces of large pin counts.
Infrastructure of high parallel probe cards:

Large Multisite Direct Dock (DD) probe cards

- Analyzers
  - Decided to not purchase NPI analyzer tools for our latest 2 technology nodes.
  - FPV probe cards – Field repairable by onsite FSL repair technicians
  - Test program Contact tests and PMI checks along with FPV technology reliability enabled this strategy
  - Analyzer tools are being purchased for production

- Repair strategies
  - Used tester and prober to help identify suspect probes
  - Major repairs sent back to PC vendor
  - 95% of probe card issues were handled by local support team

- This experience proved to be successful
Session 4 – Panel Discussion II
Infrastructure of high parallel probe cards

![Graph showing the increase in probe count over years]

- 30K @ 80 μm pitch
- SWTW

Feldman & Ahlgren
Session 4 – Panel Discussion II

• **Increase in parallel test and the consequences**
  – Infrastructure of high parallel probe cards:
    • Analyzers will still be a must for testing alignment, planarity (with and w/o applied load) and leakage.
    • Simplest repairs and debug should be performed on analyzers. Probe card flipping would be needed for that.
    • Larger check plates, axes and cleaning/leakage chucks will be needed ensuring high mechanical rigidity (200 Kg or even 300 Kg force to be considered)
    • Docking of huge probe cards must replicate as close as possible test cell docking system

  – High parallel Micro Bump probing is there a need, what would be the challenges?
    • Main challenges will be related to overall system mechanical rigidity to control overall deflections and to the availability of advanced, high density interconnections
Increase in parallel test and the consequences

Infrastructure of high parallel probe cards

- Analyzers (is there still a need – can you repair these cards on analyzers)
  - Analyzers are needed to Isolate problems.
  - Analyzers will have to improve to handle high parallel probe cards
    - Test Speed
    - Structure to Handle the high forces
    - Planarity of Card

- Repair strategies for super high pin count
  - Card structure needs to be capable of on-site pin replacement
  - Tight tolerances are required to enable on-site repair
  - Quality of card needs to be improved – one bad pin brings the whole card down

- Which infrastructure changes are needed
  - Test metrology has to be upgraded to handle the high forces and pin counts
  - Automation in Assembly process

- Docking of huge probe cards
  - Planarity between Card and Chuck is critical
Session 4 – Panel Discussion II

• Increase in parallel test and the consequences?
  – Test strategies Memory and SOC and implication on probe cards?
    • Channel resources = BAPS
    • 14 - 20 Amps / DC / AC
  – Infrastructure of high parallel probe cards:?
    • Biggest challenge from MM Probing!
    • Full Wafer SOIC Probe
    • Self Monitoring / Leveling probe card – BMW monitoring model
    • Docking / Prober / High Forces
    • Ease of repair – reduce re-screen
  – High parallel Micro Bump probing is there a need, what would be the challenges??
    • Yes, x 128 x 256 > bump / micro-bump
    • 80K - 100K pins – low force – accuracy
    • Metallurgy - Pd, Au
Session 4 – Panel Discussion II

- High parallel Micro Bump probing - is there a need? If so, what will be the challenges?
- There is a definite need for Micro Bump Probing especially for mobile and other chip-to-chip 3DIC bonding device applications
  - The single most challenging aspect will be overall cost of test. Price trends for leading edge PC’s is forcing some chipmakers to seek alternate methods for cost control
  - Enter; MPI’s alternatives with improved performance:

Conclusion: Helping chipmakers in their call to be more competitive is also driving MPI’s engineering solutions

**Package SB Technology for Ultra-Thin Substrate**
- Pegboard (PB)
- Substrate
- Carrier

**Package SB Technology for Trace or Pad Redistribution**
- Package SB w/o Pads
- Redistribution will enable probing capability with new pads on substrate.

**Package SB Technology for Multi-DUTs Substrate**
- Multi-DUTs Substrate enhanced testing efficiency.

Improved Cost of Ownership and Faster Lead Times