



SW Test Workshop

Semiconductor Wafer Test Workshop

June 7 - 10, 2015 | San Diego, California

WLP Probing Technology Opportunity and Challenge



Clark Liu

PTI Group Overview

- **Founded** : May/15/97'
- **Capital** : USD 246 Millions
- **Total Assets** : USD 2.2B
- **Employees** : 11,100 (Greatek included)
- **Major Services** : Chip Probing, Bumping,
Packaging, Final Test & Module Assembly
- **IPO** : 4/3/03' in Taiwan



Group Overview- Business Model



- Vertical Integration Model to transform wafer to module system
- Well- proven design-in capability & flexible production capacity

Group Overview- Global Network

China
Suzhou Plant



Xi'an Plant



Payton in China



Southeast Asia
Singapore Plant



Hsinpu Plant



HSIP Plant



Chung-Li Plant



Greatek Electronic



**HuKou Industrial Park
Headquarter**



Customer Success !!

Put more resource for next technology!

Tip Alignment

- Probe Tip Alignment – 0.3 mil Radial

June 10 - 13, 2012 IEEE Workshop

Test Method

Daisy Chain Bump Structure

June 07 - 11, 2012 IEEE Workshop

Planarity

- Probe Planarity < 0.5 mil (12µm)

Probe Mark

*Over-Drive: 40µm
probing: 2 TDs
Probe Mark Area Under 30%

IEEE SW Test Workshop

June 12 & 15, 2011 San Diego, CA

Evaluation of New Probe Technology on SnAg and Copper Bumps

Alexander Wang (GLOBALFOUNDRIES), Amy Leung (MicroProbes), Darko Matic (Nixia)

2011: 150µm Pitch Cu Pillar Probing

28nm Mobile SoC Copper Pillar Probing Study

Intel, Micropress, Jase Hwang (Intel Mobile Communications), Amy Leung (MicroProbes), Darko Matic (Nixia)

IEEE SW Test Workshop

2012: 120µm Pitch Cu Pillar Probing

IEEE SW Test Workshop

June 9 - 11, 2013 San Diego, California

Probing Study of Fine-pitch Copper Pillars

Alexander Wang (GLOBALFOUNDRIES), Amy Leung, Yeh Hsiang-Li, Andrew Hsieh, Mike Shivers (Star Trek), Darko Matic (Nixia)

2013: 100µm Pitch Cu Pillar Probing

- In 2014, Cu Pillar is becoming the mainstream flip-chip packaging technology (Source: Yole)
- Key issue is "How to best prepare for fine-pitch Cu Pillar probing in high volume production?"



Wittig, Leung, Nguyen, Masi, Kister, Slessor

June 8-11, 2014

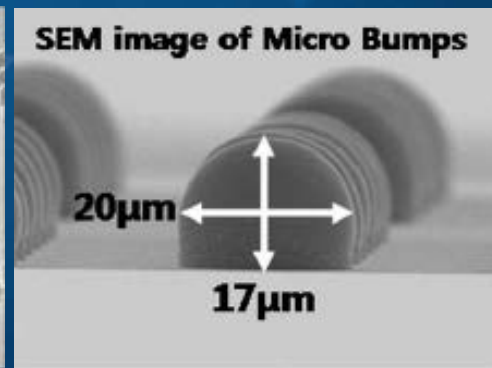
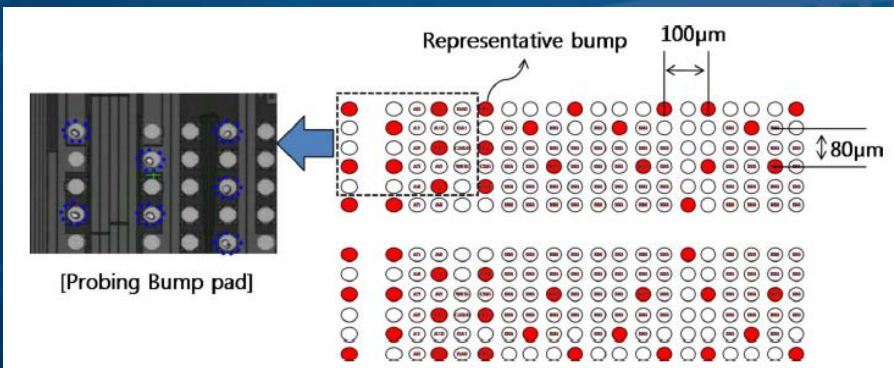
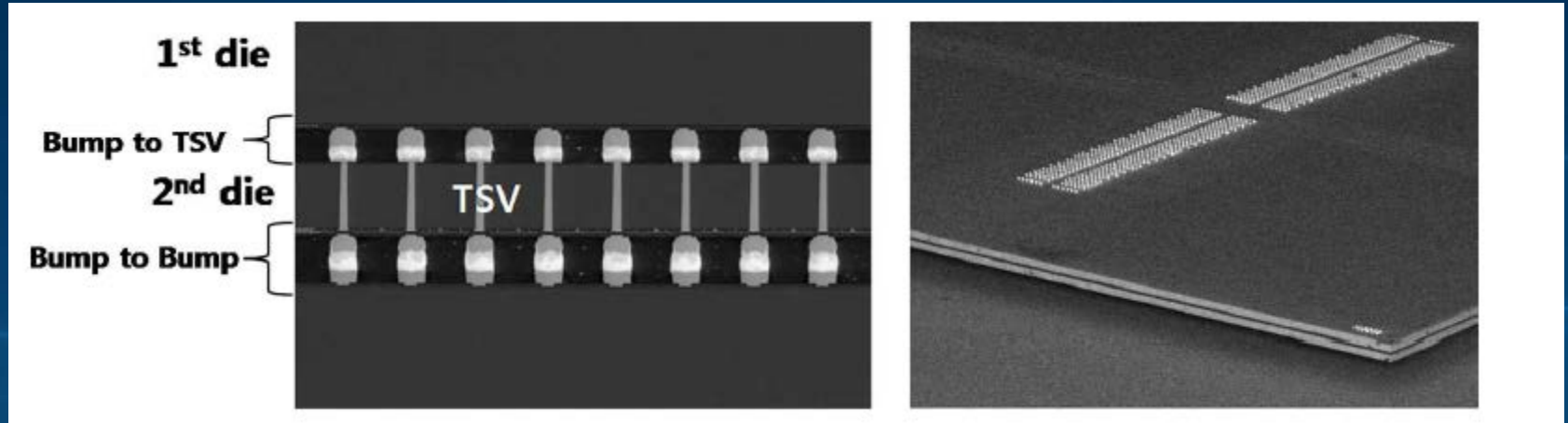


IEEE Workshop

2012 SWTW ASE_SV 50µm Pitch Array

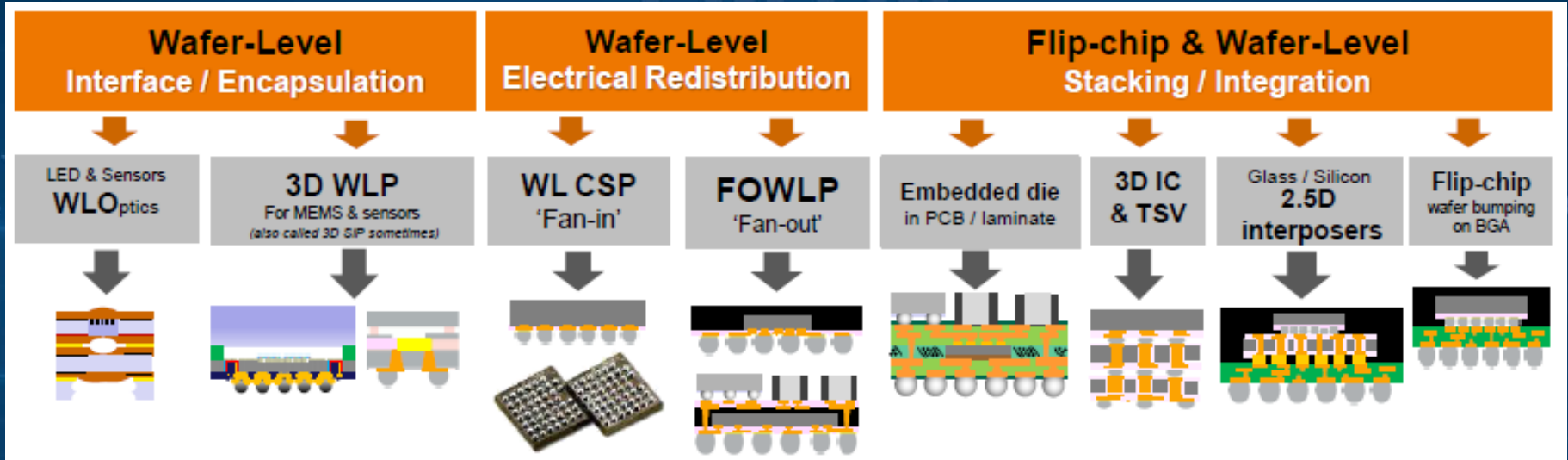
2014 SWTW FFI 80µm Pitch CPB

Probing at 2G Wide I/O Bump Pad



Source : 2011 IEEE _ Samsung

WLP(Wafer Level Packages)



Wafer-level-packages have emerged in many different varieties that can be categorized into different advanced packaging technology platforms

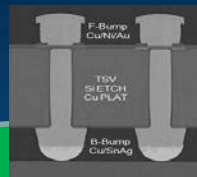
Source : 2013 SEMI _ Yole

Map of WLP manufacturing companies



Source : 2015 Yole

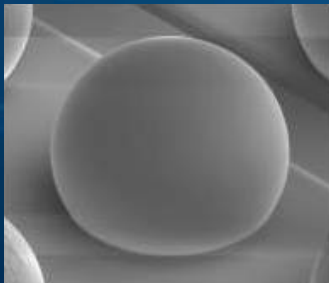
WLP Key Connection Technology



Wafer Level Package



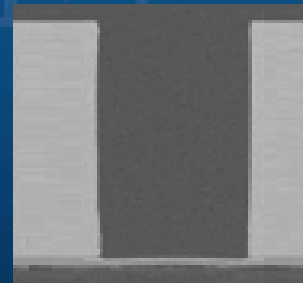
Bump



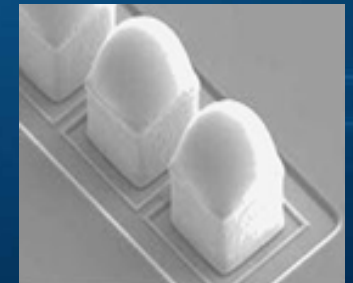
RDL



TSV



CPB



From Kid View!

Wafer Level Package

Bump
like



RDL
like



TSV
like

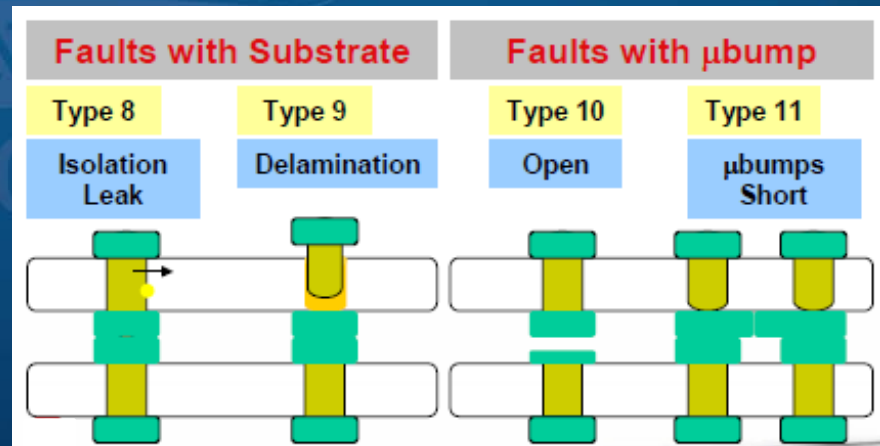
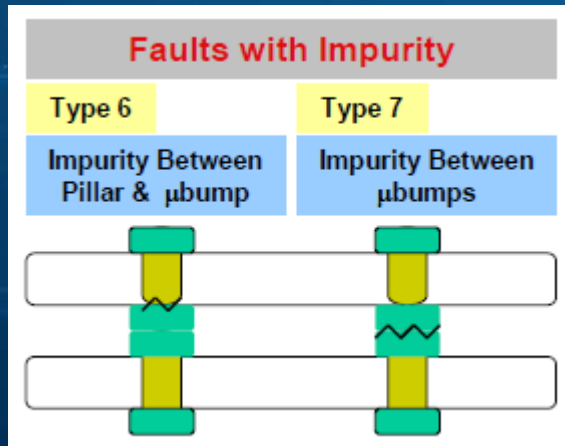
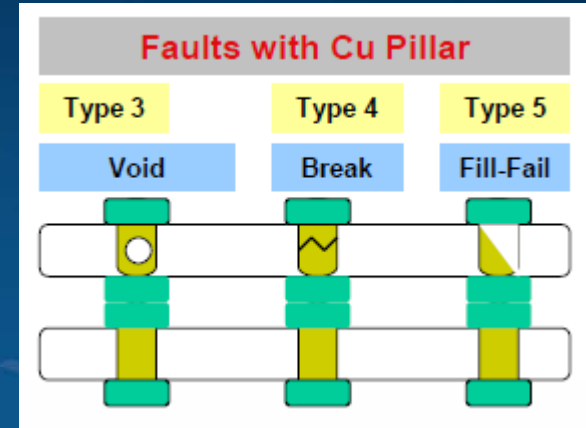
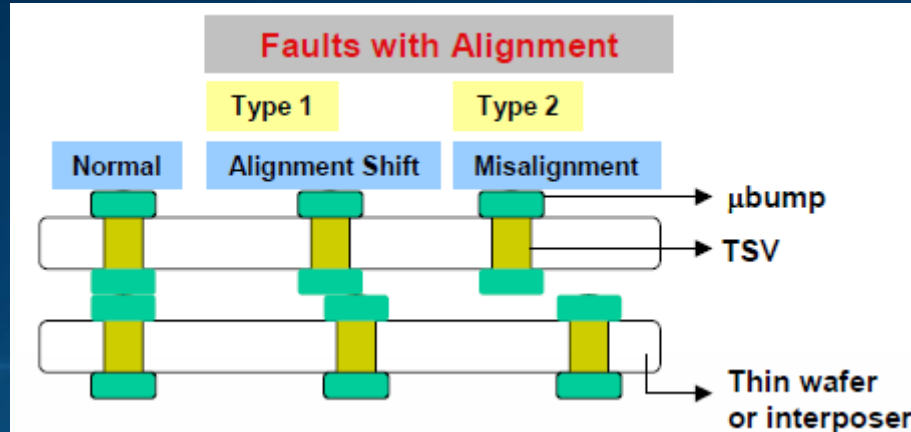


CPB
like



Electrical Tests for WLP Connectivity

Fault Model

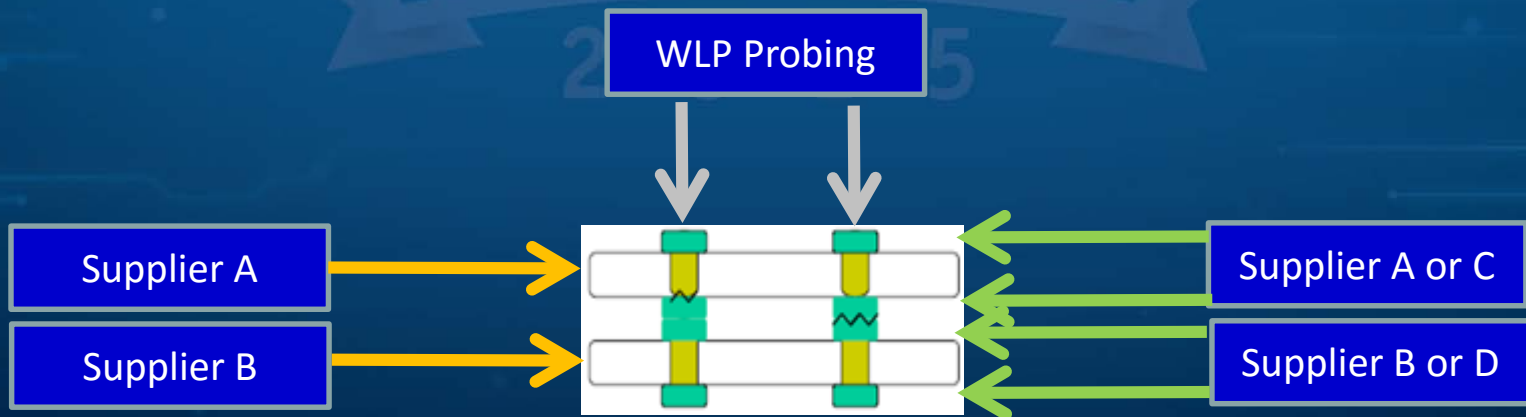


Source : 2010 IEEE 3D IC Workshop _TSMC

Fault Model for different test items

Fault Detection of Test Items											
Test Item	Fault Detection										
	Misalignment		Abnormal Cu pillar			Impurity		Substrate		micro-bump	
	Type 1	Type 2	Type 3	Type 4	Type 5	Type 6	Type 7	Type 8	Type 9	Type 10	Type 11
Continuity test		V		V					V	V	
Resistance test	*V	V	*V	V	*V	*V	*V	V	V	V	*V
Capacitance test	*V	V	*V	V	*V	*V	*V	V	V	V	*V
Leakage test	*V	V	*V	V	*V	*V	*V	V	V	V	*V
AC test	V	V	V	V	V	V	V	V	V	V	V

* means need high resolution measurement tool/method



Source : 2010 IEEE 3D IC Workshop _TSMC

WoW !



Source : Taipei 101

Challenge?

Opportunity?

Cost?

New Model?

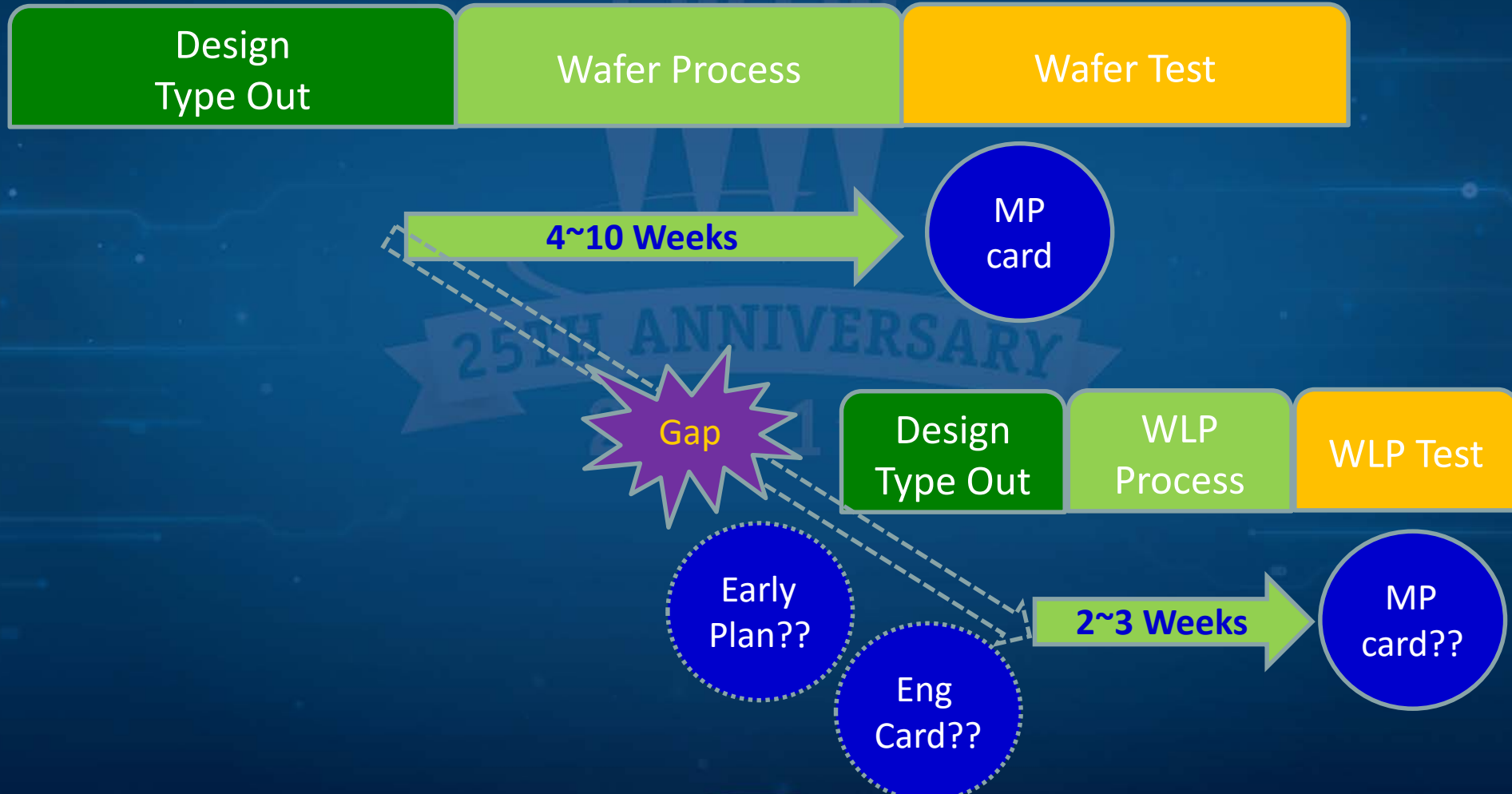
Technology?

Cooperation?

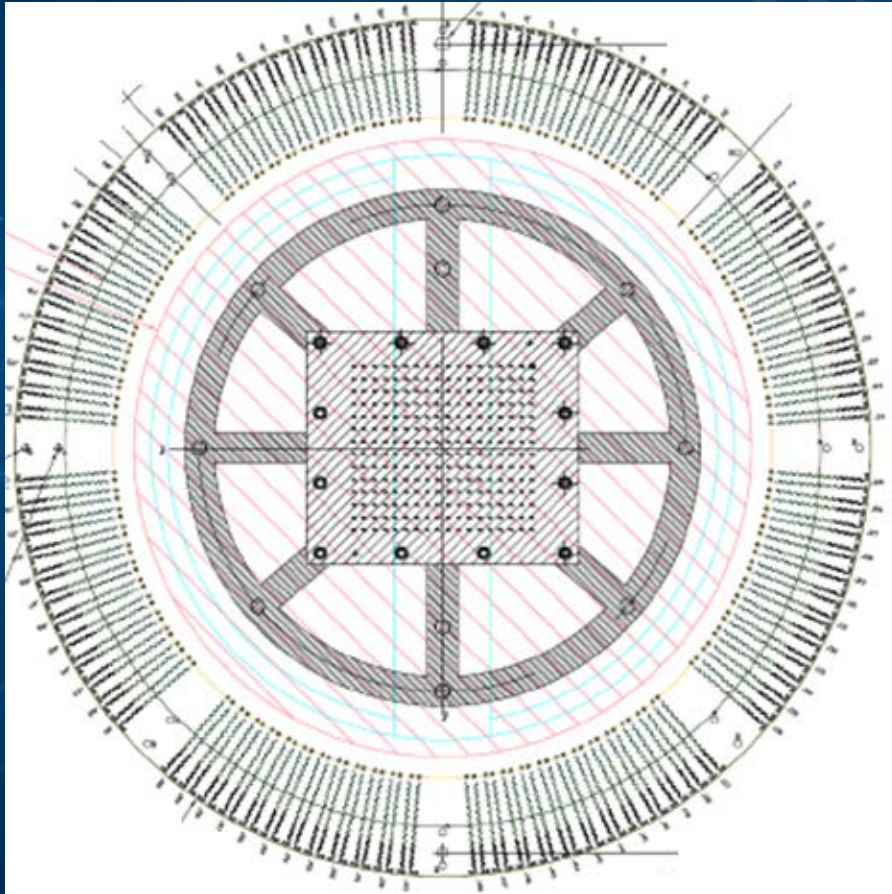


Source : NTHU

Case1: Tools Short Delivery Cycle Time?



[Ex] WLCSP 256DUT Probe card

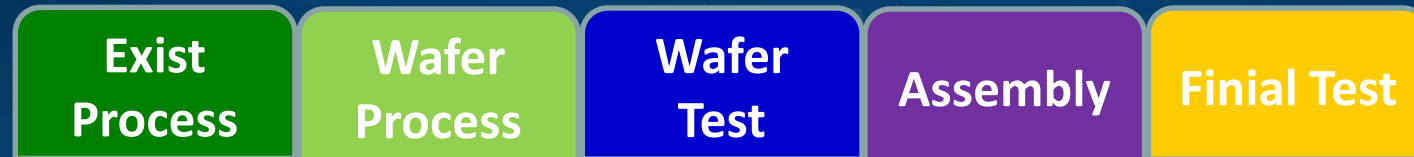


- **Bump Type: WLCSP**

- a. Diameter: 300um
- b. Height: 170um \pm 10%.
- c. Pitch: 500um
- d. TD : 10
- f. Total Pin Count 2560 Pins

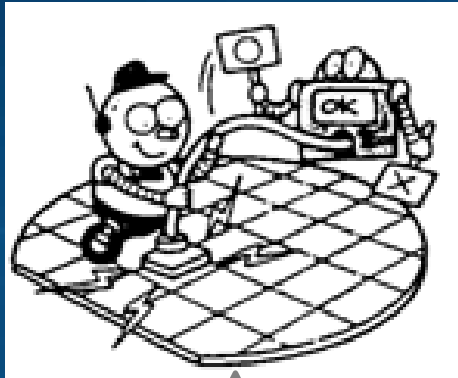
Delivery Time 8 Weeks

Case2: Process Change for more Chip Probing?

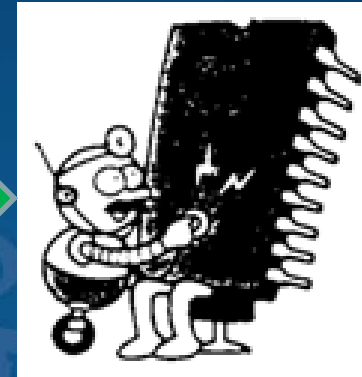


More WLP Test or More Finial Test?

- WLP Test



- Finial Test



Fine Pitch

Contact Force

Silicon Base

um

Pitch Limit

Clean/10K
Cleanness

Package Base

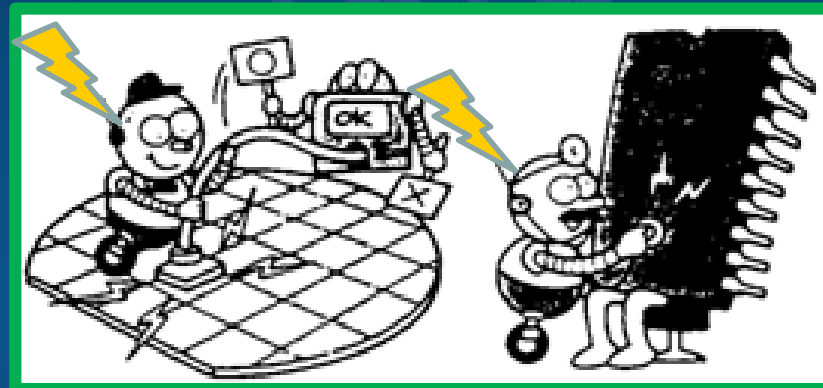
mm

Pictures Source : Mitsubishi

Wafer Test or Final Test Vendor @ WLP Testing?

- Wafer Test Vendor

- Final Test Vendor

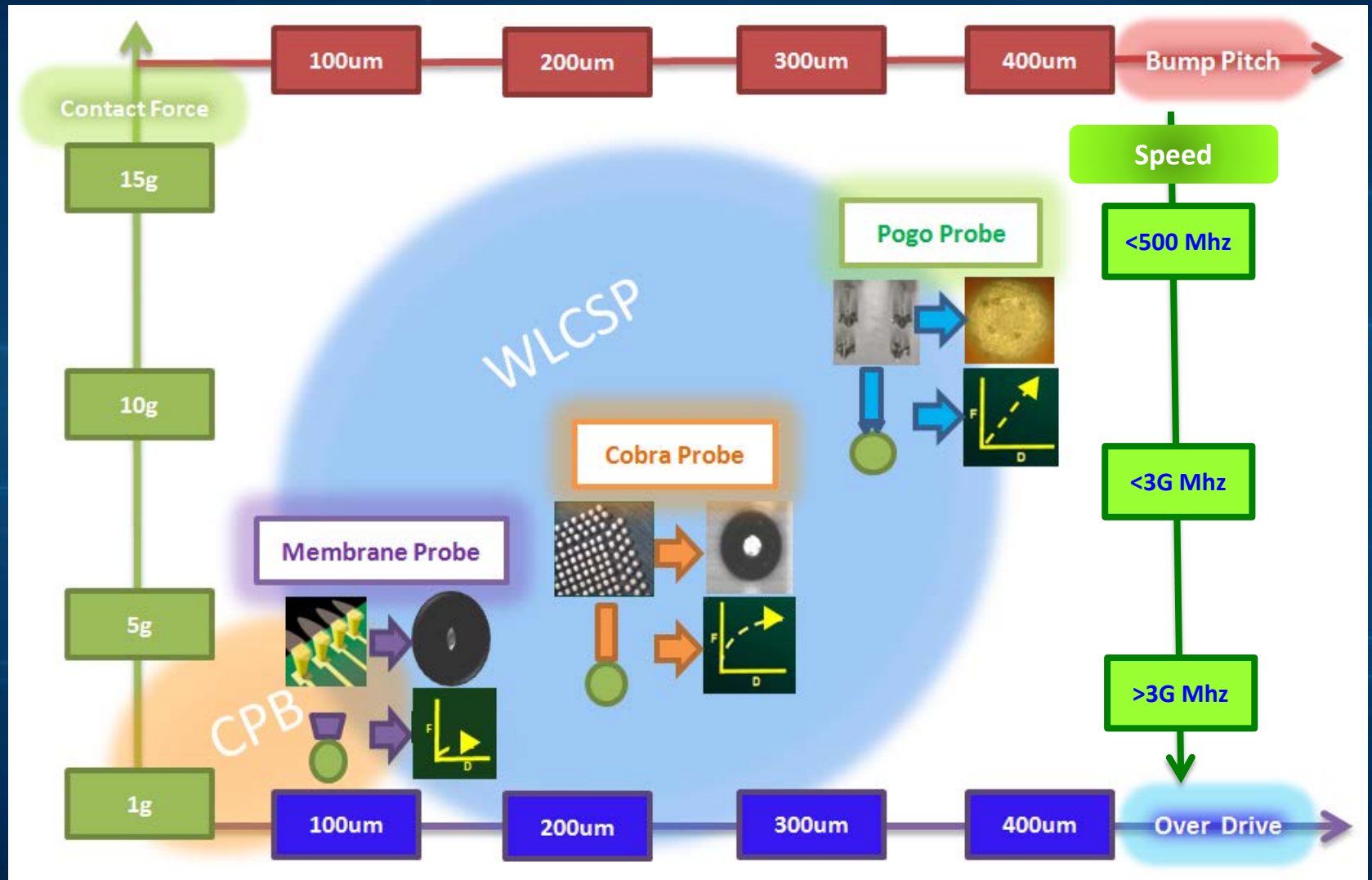


- Cycle Time Challenge
- Cost Challenge
- New Process Challenge

- Cooperation Model Challenge
- Wafer Level Requirement and Quality

Gap

WLCSP / WLCPB Probe Card



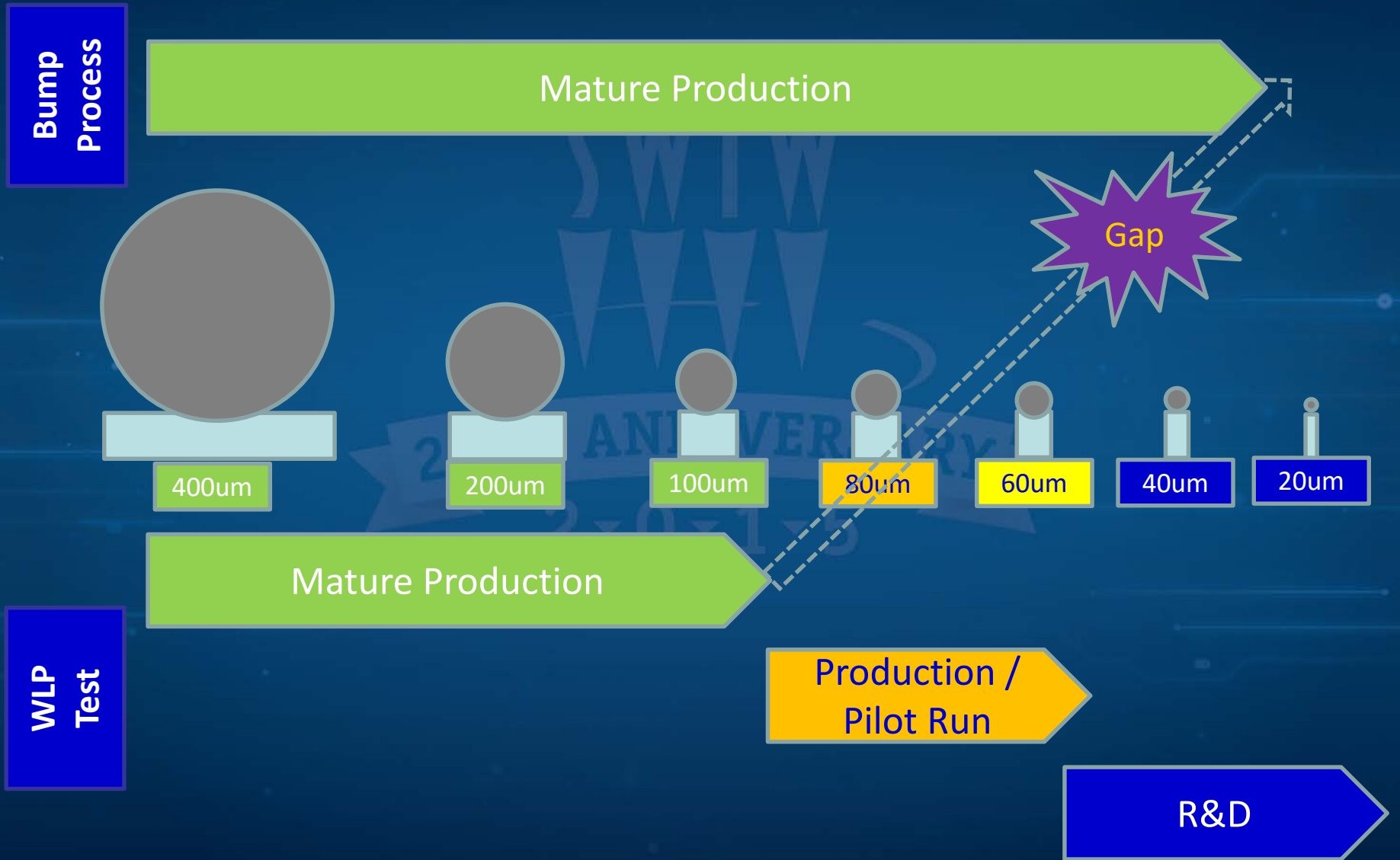
Source : SWTW

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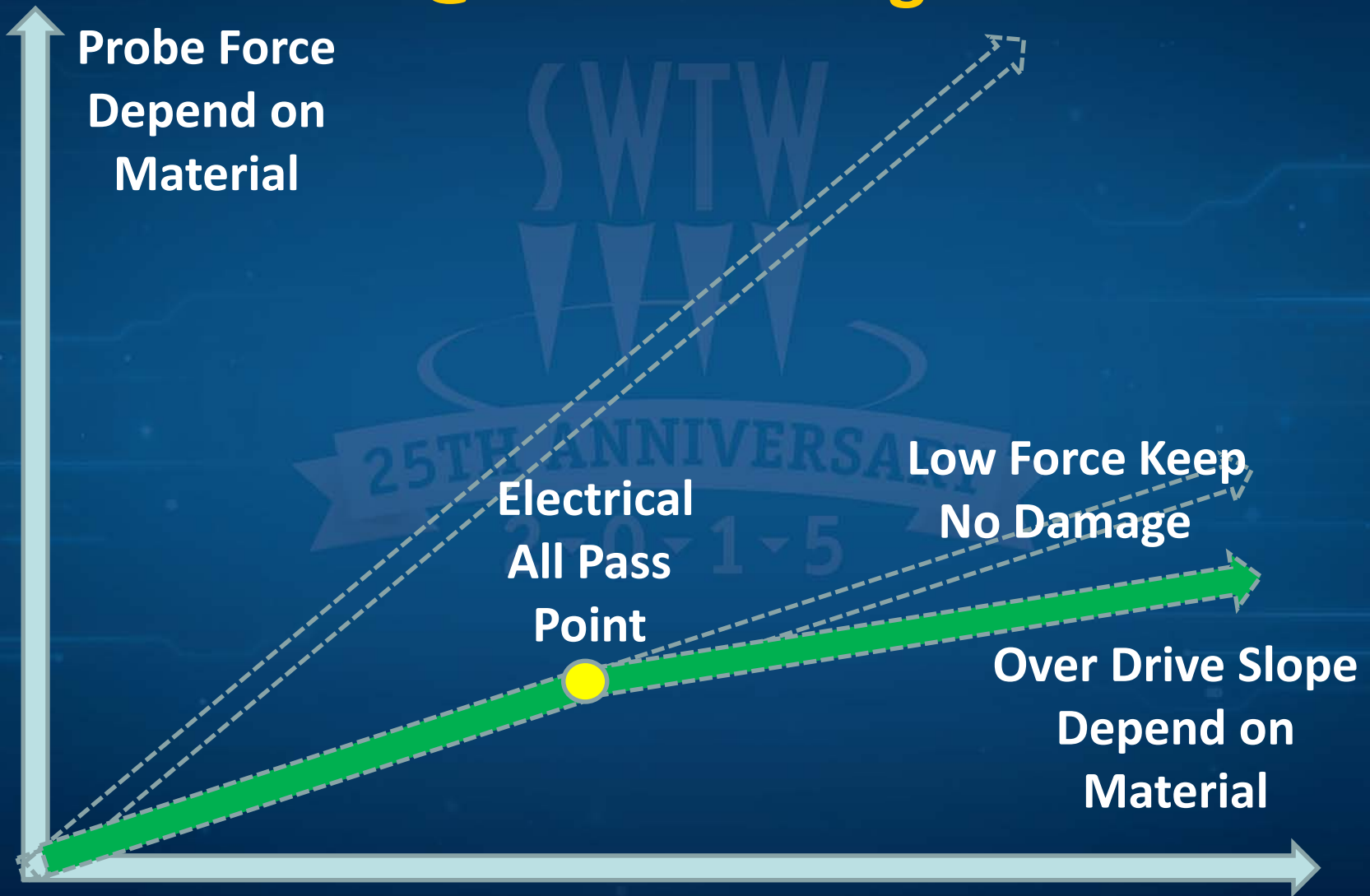
25TH ANNIVERSARY
2015

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Bump Process & WLP Probing Roadmap



Ideal Probe Force v.s Over Drive @ WLP Probing

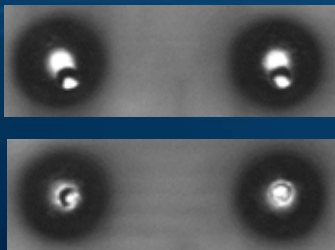


Case 3: Probe mark analysis Technology

AOI Probe Mark
Analysis Challenge

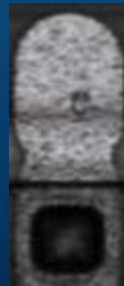
Probing
Position / Depth
/ Sharp

Bump



Different
Layer

RDL



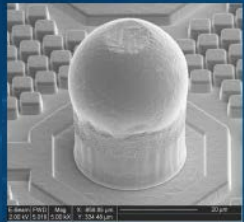
OD / Force
/ Probe area
/ Bump Height

CPB

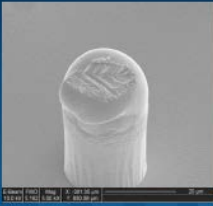


What Expect data from those Probe mark?

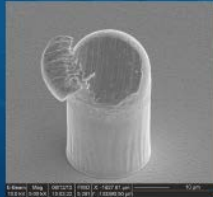
Cu Pillar Probe Mark Photo Gallery



Pass
Good Probe Mark on
30um Cu Pillar



No Pass
Misaligned Probe Tip



No Pass
Cu Pillars with Sheared
Solder Cap



No Pass
Probe force too high

Wittig, Leong, Nguyen,
Masi, Kister, Slessor

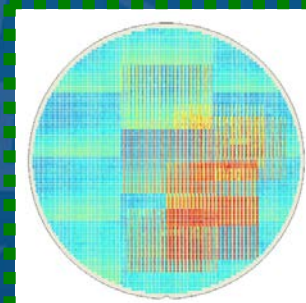
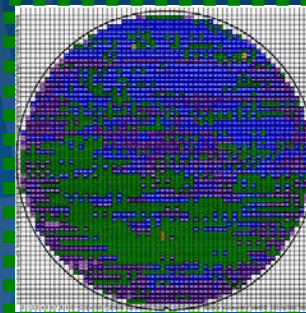
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AOI
Probe
mark
Analysis

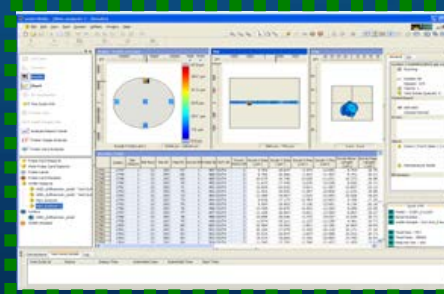


User
Expect
Data

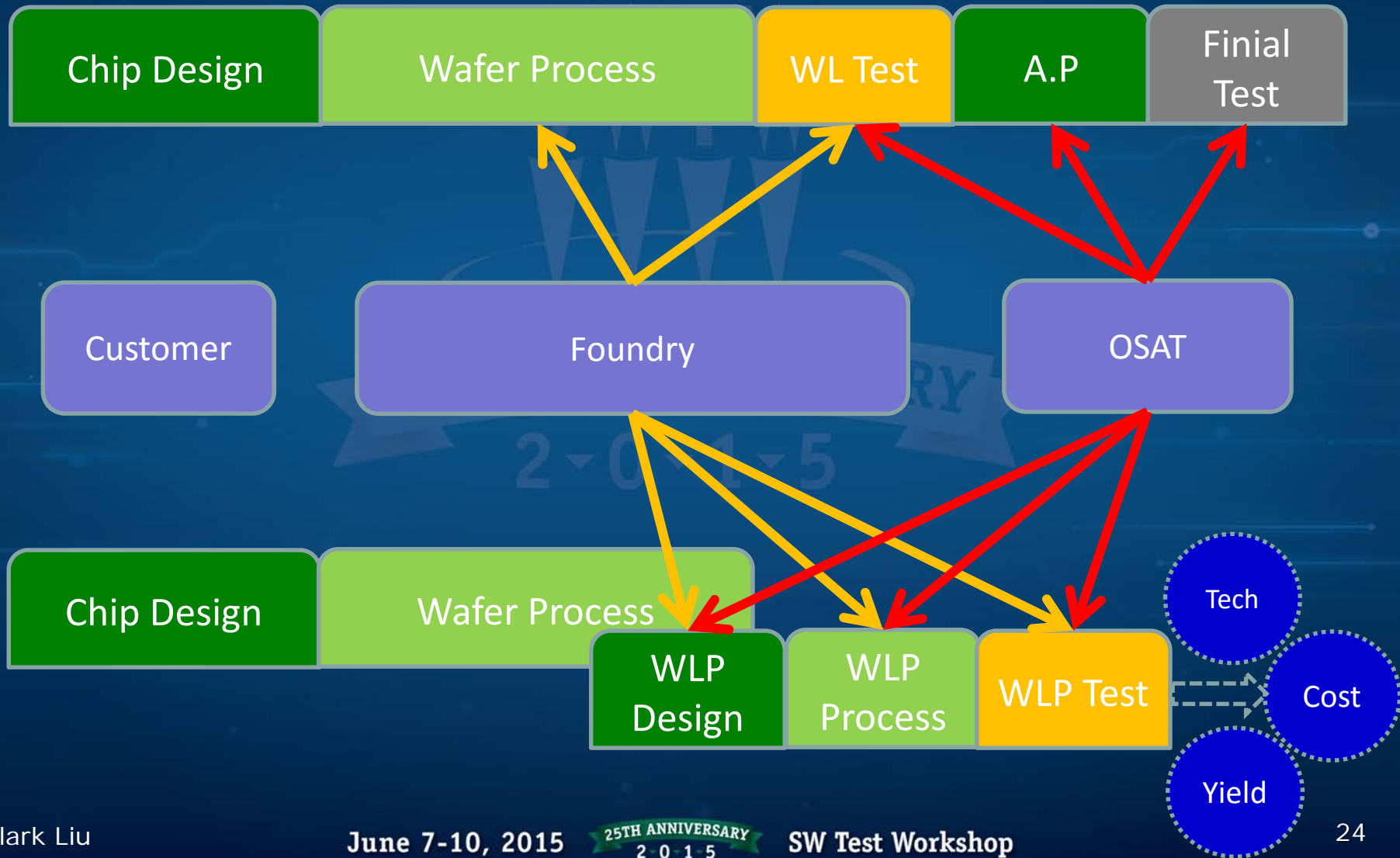
Data Mining:

- (1) Prober Performance
- (2) Probe card Performance

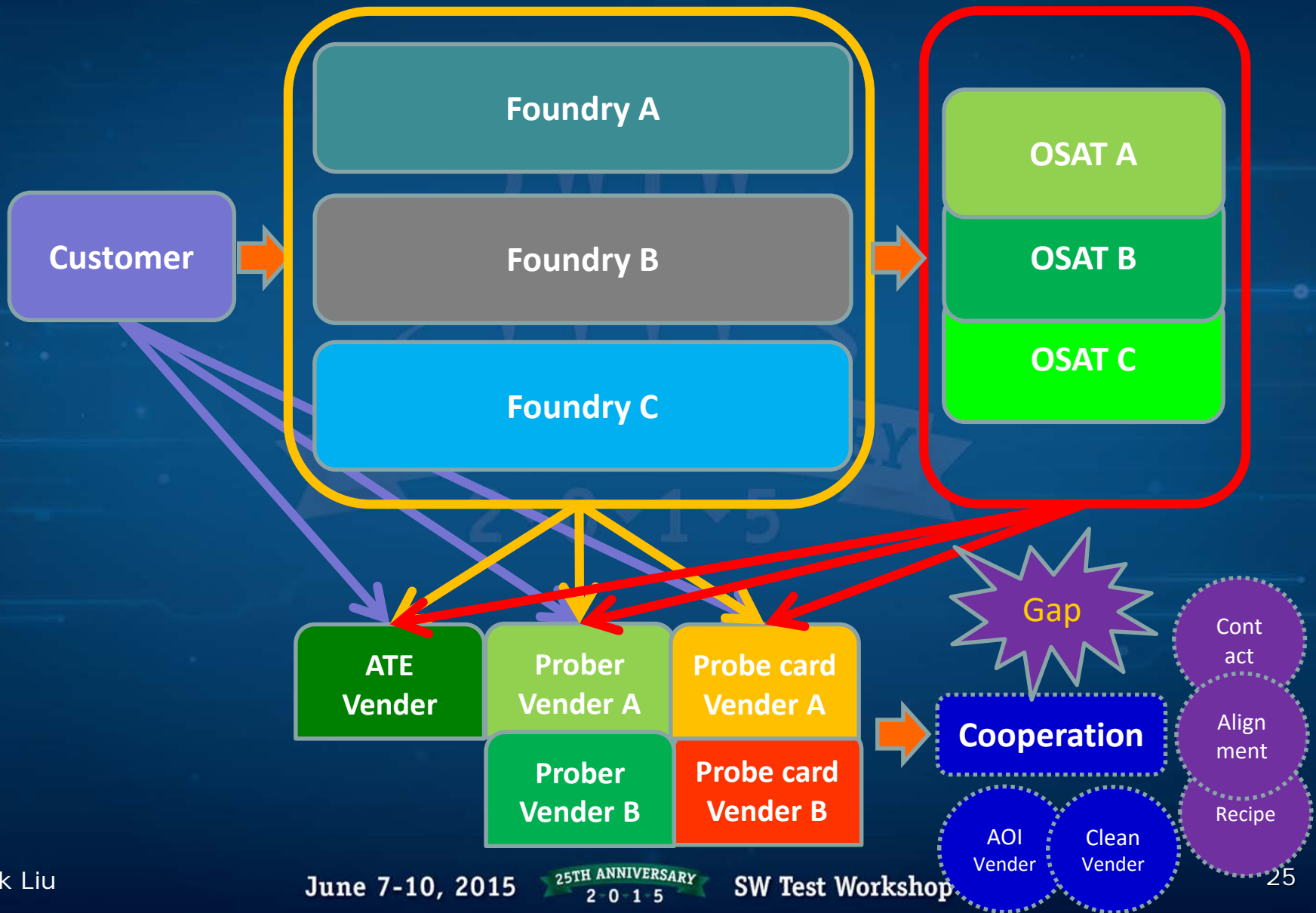
[Keep Under Development]



Case 4: Business or Process Change?



Same Issue but different site?



Conclusion



- Cooperation from Customer to Supplier (Design House /Foundry/OSAT/Vender).
- New opportunity for Wafer/Finial Test I/F vender.
- The Evolution Business Model will start change something.