SW Test Workshop
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Leveraging Multiprobe Probe Card learnings to help Standardize and improve Parametric and WLR Testing

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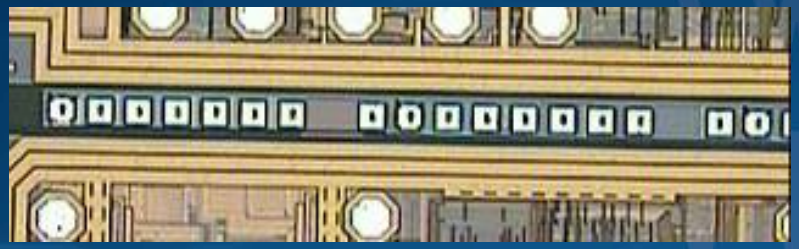
Agenda

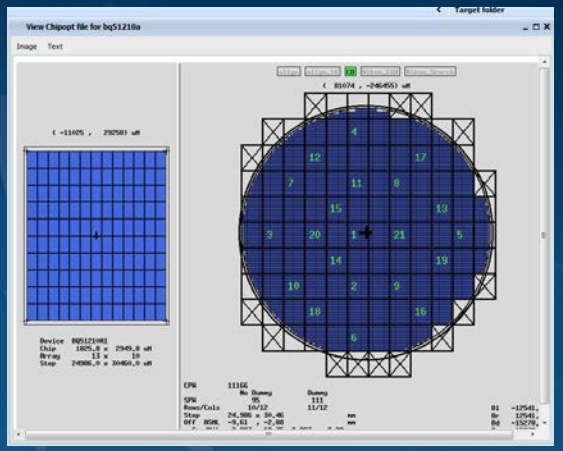
- Introduction
- Overview
- Similarities
- Differences
- Current Problems
- Summary
- Questions

Introduction

- Within TI, we have vast experience using probe cards for Multiprobe testing. We use various probe technologies to probe a wide array of features and metallurgies.
- TI has implemented a process called Design for Probe, that is used within TI to help ensure that our devices use the correct probe card technology and vendor. Processes like DFP have given us the ability to standardize many of our settings and requirements across all probe vendors allowing TI to transfer probe cards and technologies across the world.
- Parametric and WLR testing also requires the use of probe cards to help with probing, but we do not have the same standards in place as in multiprobe. There are some key differences for parametric and WLR probing, but also many similarities with probe.
- In this presentation, I will discuss some of the similarities and differences from multiprobe and provide some ideas on how we can leverage the long history of learnings at multiprobe to help benefit and improve our processes for parametric and WLR testing.

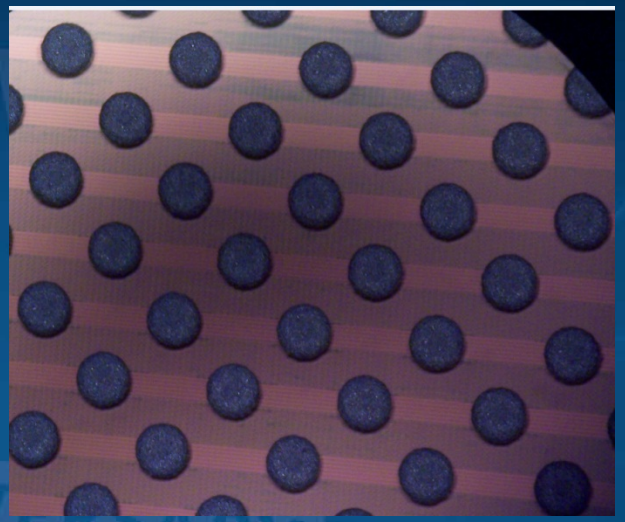
Parametric Testing Overview





- Parametric testing is a process used to monitor production processes in attempt to improve yields.
- It is many times referred to as scribe test because the DUTs reside in the non-revenue-generating wafer area between the product die, called the scribe (or street).
- Structures typically have 5-26 “sub-sites” within a reticule field, each typically with around 5-20 pads .
- Wafer level reliability testing is a statistical process control tool that is used to monitor production processes by inducing high stresses (time and temperature) on parts / structure.
- Because of the high stresses, WLR helps to shorted test cycles and time generally would be required.

Multiprobe Overview



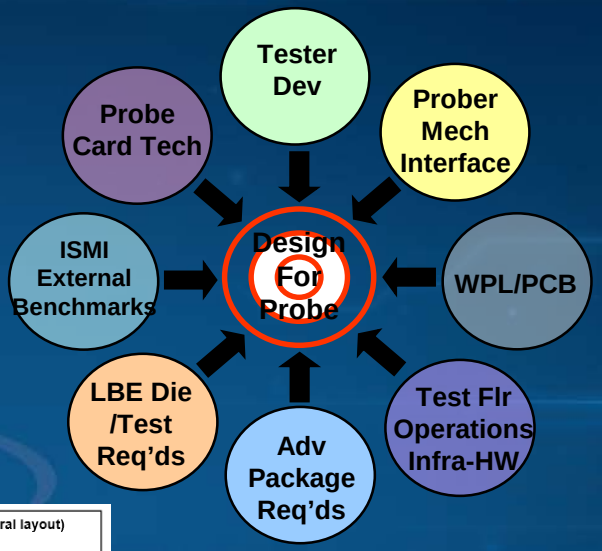
- Wafer Probe (sort), or functional testing, is a step in semiconductor fabrication process where electrical excitation is applied to individual die in wafer form to test the functionality of the embedded circuits without inducing excessive bond pad damage or any underlying metal damage.
- In multiprobe there is often push for testing multiple die in parallel helping to increase the throughput.

Similarities

- **There are many similarities between the two types of testing.**
- **Because of the large knowledge base and long history of standardizing practices at multiprobe, many of those same practices can be leveraged for parametric and WLR.**
  - Probe Card Technology Decision
  - Cleaning / Probing Procedures
  - High Temperature testing

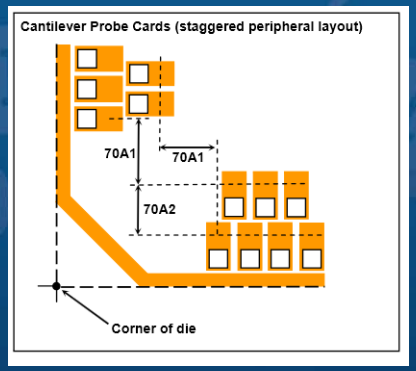
Design For Probe

DFP-Design For Probe is a risk-review process involving a cross functional team of experienced probe test members whose objective is to target probe solutions that are aligned to TI's Roadmap and Best Practices.



Benefits

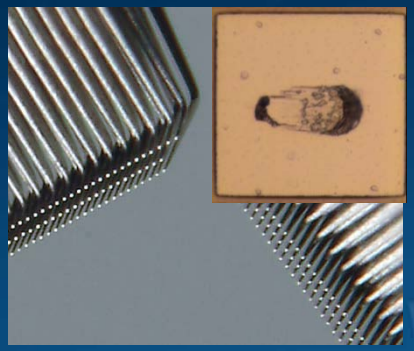
- **Optimize the Probe Card technology selection!**
  - Build the right Probe Card for your device.
  - Take advantage of the latest qualifications
  - Understand each test floor's strengths for smooth offload.
- **Maintain Probe Card Build Spec**
  - Monitor vendor compliance to avoid probe card mis-builds and lost cycle time
- **WPL assists with RFQ to ensure best pricing!**
- **Design Rules for various silicon technologies.**
- **Help to provide robust solutions that can easily be transferred across various TI sites worldwide.**

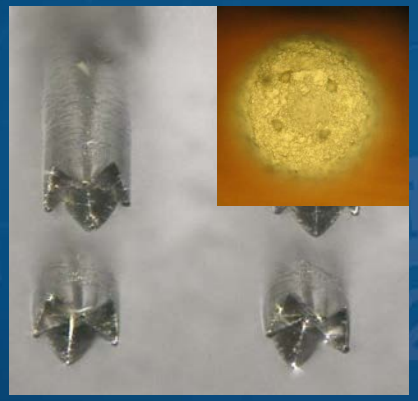


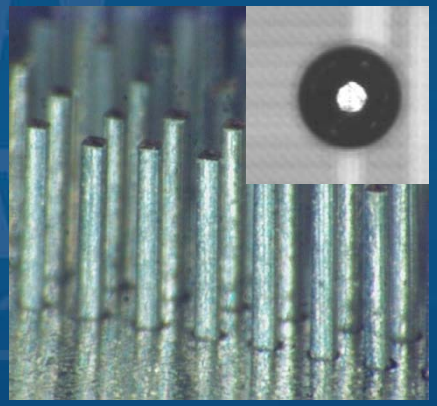
Ex: Cantilever design rules below for pad layout.

Rule Code	Description		Size on Silicon (µm)
70A1.	Minimum distance perpendicular to the die edge between the probe points furthest from the die edge or that side to the closest probe point to the die edge on the adjacent sides.	Single Site	NA
		Multi Site	125
70A2	Maximum distance from center of probe pad to center of staggered probe pad.	Dual Inline or 2x2 Quad Site	125
		Single Site or Dual Diagonal	300
70A3	Minimum distance between probe points		50
70B1.	Probeable core pad minimum pitch		100
70B2	Minimum core pad dimension must be this amount or larger than the minimum peripheral pad dimension.		10
70J1.	Maximum multisite die matrix	Single Site	24000
		Dual Inline (Shelf)	30500
		Dual Diagonal	22800
		Quad Site (Shelf)	24000
70K1.	Distribution of probed pads (layout of probed pads must be placed so as to avoid high concentrations of probes that can restrict escape routes in the PCB of multisite probe cards)		Max

Probe Card Technologies







- In multiprobe, many different probe card technologies are available depending on the application.
- Many of these same vendors / technologies can be utilized in parametric testing as well.
- Leverage probe card pricing if we can use same vendors / technologies in both.

Qualification Process

Multiprobe

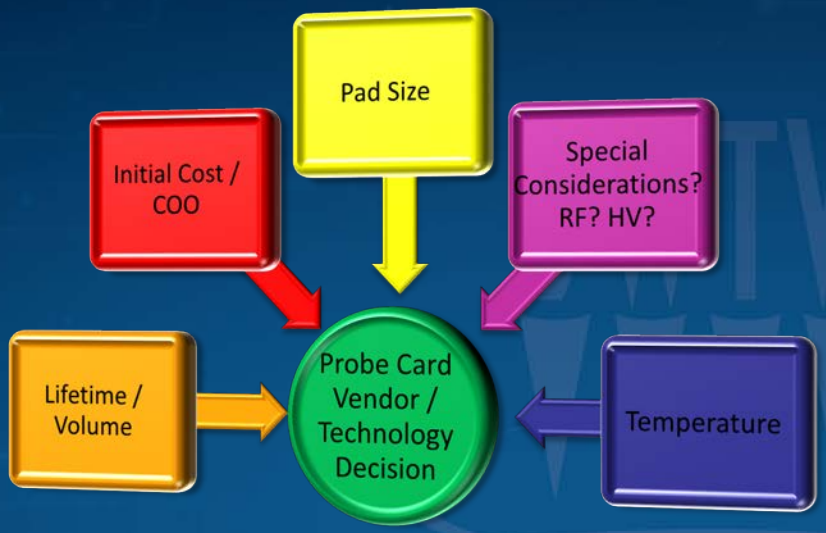
	Parameter		Requirement	Total Qual	Cleaning Qual
Standard	Incoming Inspection of Probe Card On Analyzer *(If not available, then must rely on Outgoing Vendor Data)	Planarity Check	Planarity of +/- 50um *Confirm with specific site as to requirements per technology.	X	
		Alignment Check (x/y)	Alignment of: Cantilever: +/- 9um Vertical +/- 12um *Confirm with specific site as to requirements per technology.	X	
	Visual Inspection		Corrrect wiring/solder points/residues on probe card. Place photos in "Photos" tab.	X	
	Outgoing Analyzer Results from Vendor		Pass / Fail	X	
	Device Characterization	Prober Device File Setup	Needle Alignment Settings defined.	X	
		Bin to Bin Correlation	98% bin to bin from baseline card to new probe technology or LBE/PDE acceptance.	X	
		Cres Over Time	Limit of 3 Ohms Standard deviation on 100k TD and a minimum 100 wafers probed. Confirm cleaning optimized to keep Cres consistant.	X	x
		Life time study	100k TD and a minimum 100 wafers Probed in production or accelerated probing and cleaning wear study to show the TD vs. Tip length as it relates to probe card end of life. (life expected must be (>750K TD)	X	x
		Thermal Agility	X, Y, Z correction across a wafer must be lest the 30um min to max without dramatic swings not including stops to the prober with in a wafer once the card gets to temps	X	
		Cleaning Optimization	Optimize on cleaning OD / Recipe. (Record recipe in Probe & Cleaning Recipe Tab) Define cleaning Block rotations	x	x
	Quality	MSDS Sheet	New materials require MSDS sheet. No polyethylene allowed, high temp transfer study is needed.	X	x
		AVI Fail Rate	Fail rate must be less the 0.25% across 20 EWR lots at all temperatures.	X	
		Bump Damage (FC or WCSP)	Damage must meet all packaging requirments.	X	
	Dielectric Cracking Study (if needed)	Max TD Test	Dielectric cracking study Automotive requirement 9x TD in the same location and max production probing OT)	X	
		Punch Through	No under layer metal exposure on automotive products QSS states for Al technologies "shall not expose underlying passivation or underlying metal equal to or greater than 25% of the pad width adjacent to the edge of the pad or exceeds 1.0mil2 near the center of the bond pad.	X	

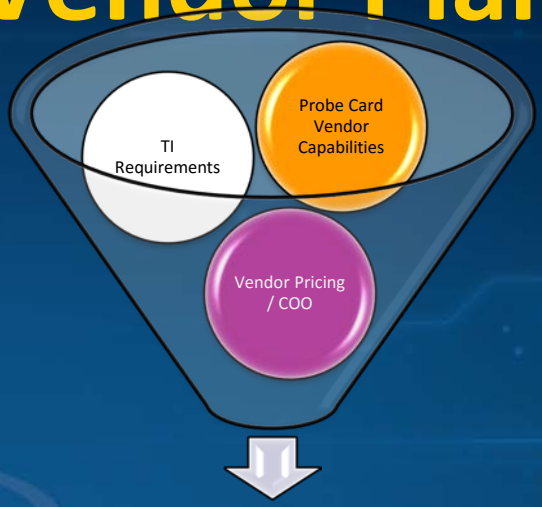
Parametric / WLR

	Parameter		Requirement	Total Qual	Cleaning Qual
Standard	Incoming Inspection of Probe Card On Analyzer *(If not available, then must rely on Outgoing Vendor Data)	Planarity Check	Planarity of +/- 50um	x	
		Alignment Check (x/y)	Alignment of +/- 12um	x	
		Leakage Spec Pin / Pin	Leakage of <100nA	x	
	Visual Inspection		Corrrect wiring/solder points/residues on probe card	x	
	Outgoing Analyzer Results from Vendor		Pass / Fail	x	
	Characterization of Test System	Leakage Test (Pin to Pin)	Leakage < 1pA @ 100V for low leakage. Leakage < 10pA @ 100V for standard cantilever. (Adjust value per tester)	x	
		Cres Data @ OD	Stable and controlled Cres at optimal OD. (Discretion of Parametric Team) CRES data on Conti-short structure (sanity modul) @ OD. *(If no santiy module available for CREs, then can use blank unstructrued Al wafer and create basic Cres test to verify CREs.)	x	
		Probe Mark Check @ OD	Check marks at different OD and measure scrub length/width to find optimal OD. Probe Mark should be well centered on pad at optimal OD where constant CRes. Take pictures for documentation.	x	
		Pad Damage (If needed)	If active circuitry then must chracterize probe mark damage / depth using dielectric cracking study. Test at nominal OD and max OD at x1 TD to 6x Tds. *(Instructions on how to perform cracking study can be found in Dielectirc Cracking Study tab)	x	
		Wafer Correlation Data	Sameness and accuracy test for all PCD scrap parameter. Minimum should be 3 wafer. If basline probe card available can correlate to that.	x	
		Lifetime Monitoring Test	Run on prod test with 500 wafers or at least 500KTds. (may vary depend on loading) Cres should not creep over time. monitor CRES over time. Measurements should be recorded at various intervals (50-100kTds) to help predict wearout of card. (length, diameter, debris, abrasion)	x	
		Cleaning Optimization	Optimize on cleaning OD / Recipe. (Record recipe in Probe & Cleaning Recipe Tab)		x
WLR	Preheat Soak Time		Evaluate and characterize Soak time for high temperature (125°C / 150°C / 200°C). Must have stable x/y/z alignment of tips at temperature. Once card at equilibrium, marks should be centered and not touching PO.	x	
	Probe to Pad Alignment over Time		Verify no shift in needle x/y/z after 30min test time. Probe marks should not be increasing after time. Cres should be stable and controlled at optimal OD after 30min test time.	x	
	Max Current at Probing Temperature over Time		Verify maximum current over time at testing temperature. No burnt needles / overstressed or melted pads.	x	

- **In wafer probe, we have always used a standard qualification document that allows us to look at both mechanical and electrical properties of the probe technology and compare against TI requirements.**
- **We utilize the same document for parametric and WLR testing.**

Qualified Probe Card Vendor Plan

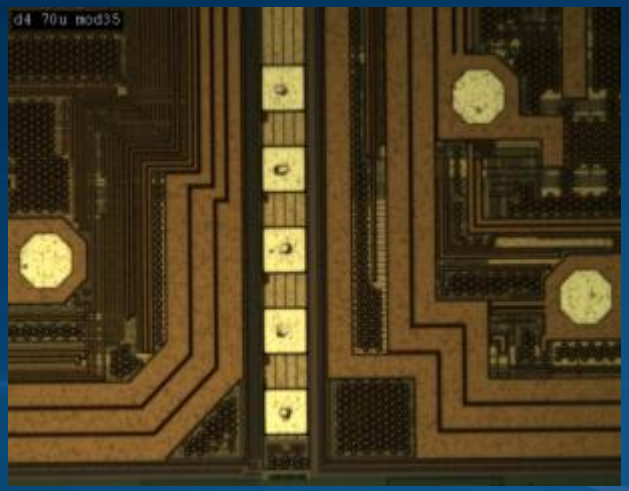


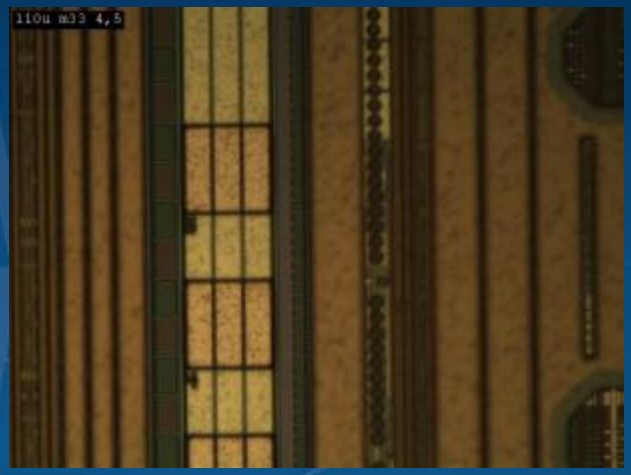


Qualified Vendor List

1. **Set list of requirements expected of probe card vendors**
2. **Establish the actual capabilities of each of the probe vendors**
   - Need help from sites to help gather data to "qualify" vendors and present in Qual Worksheet
3. **Build database of all vendor's data and qual reports**
4. **Narrow down list to solid number of Qualified vendors for each application (3?)**
   - Compare vendor capabilities with TI requirements and against each other
   - Add specs to provide guidelines for probe card build based upon qualifications
   - Helps to leverage PC pricing by limiting supplier base (WPL help)
5. **From this, we could then build database to help automate Probe Card Vendor / Technology Decision. (Ties into PBD)**

Pad Cracking DOEs

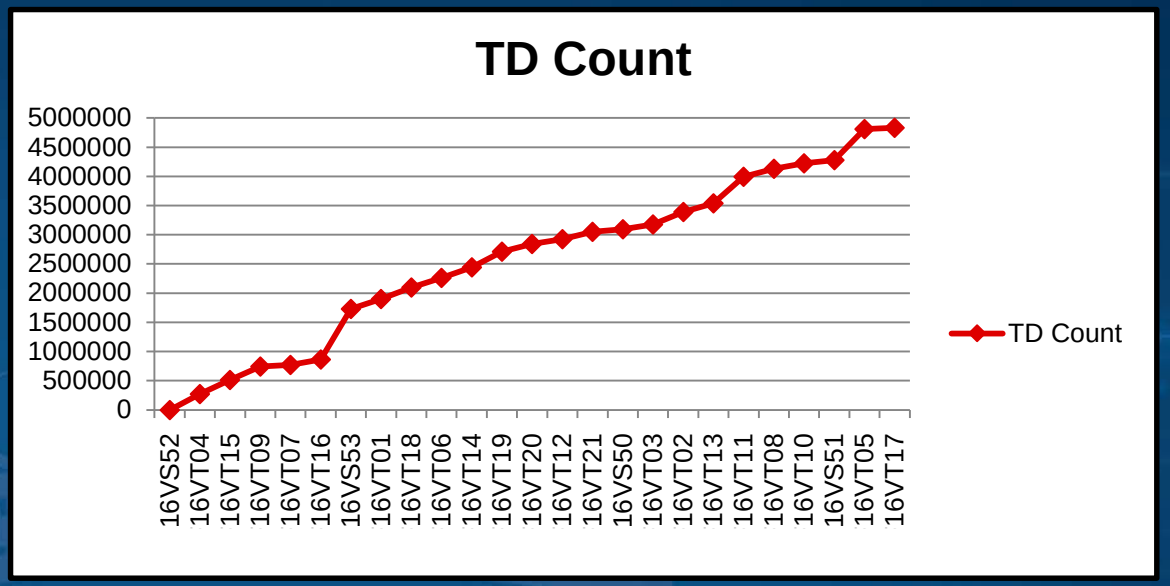




- **We use dielectric cracking studies in both multiprobe and parametric testing to help us understand the forces of a given technology and whether or not it will cause excessive damage to pad or underlying metals.**

Probing / Cleaning Settings

Probing / Cleaning Recipe	Probe Tech	Category
		Vendor
		Specific
	Probe OT Method	FT/LT
	Probe OT	(µm)
	Cleaning Media	(Material)
	Clean Freq	(PTd)
	Clean OT	(µm)
	Clean Tds	(CTd)
	Clean Pattern	(shape)
	Tester	
	Cleaning block Rotations	#
	Planarity Spec	um
	Lifetime	Tds
	Temperature	oC
	Analyzer Available	



- There are many lessons learned in cleaning optimization in the multiprobe area.
- The key learnings can be used for parametric as many of the same technologies and vendors are used.
- Optimized cleaning recipes can help to determine and predict lifetime and wear of the probe cards.
- Lifetime and cost numbers can be used to create COO-Cost of Ownership models which can predict over a certain amount of volume which vendor / technology is optimal.

High Temperature Testing

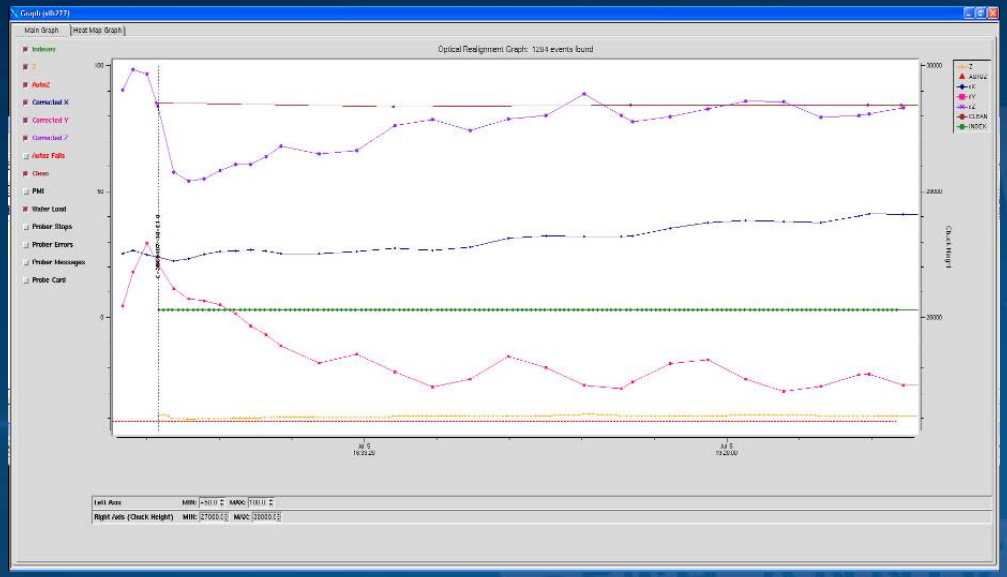


Table #9 – High Voltage Specs*	
Item	Parameter
Voltage	>50V considered HV
Pad size	>70x70um
Needle Spacing	0.333 mm per 1kV (Follow HV spacing guidelines on probe needle solder points and wire wraps)
CDA Purge	Required to keep humidity low
Probe Type	Needles of same type should be grouped together. (For Ex: All HV needles should be grouped together)
PWR & GND	Group like pins together (PWR with PWR and GND with GND). PWR GND PWR configuration could induce arcing.

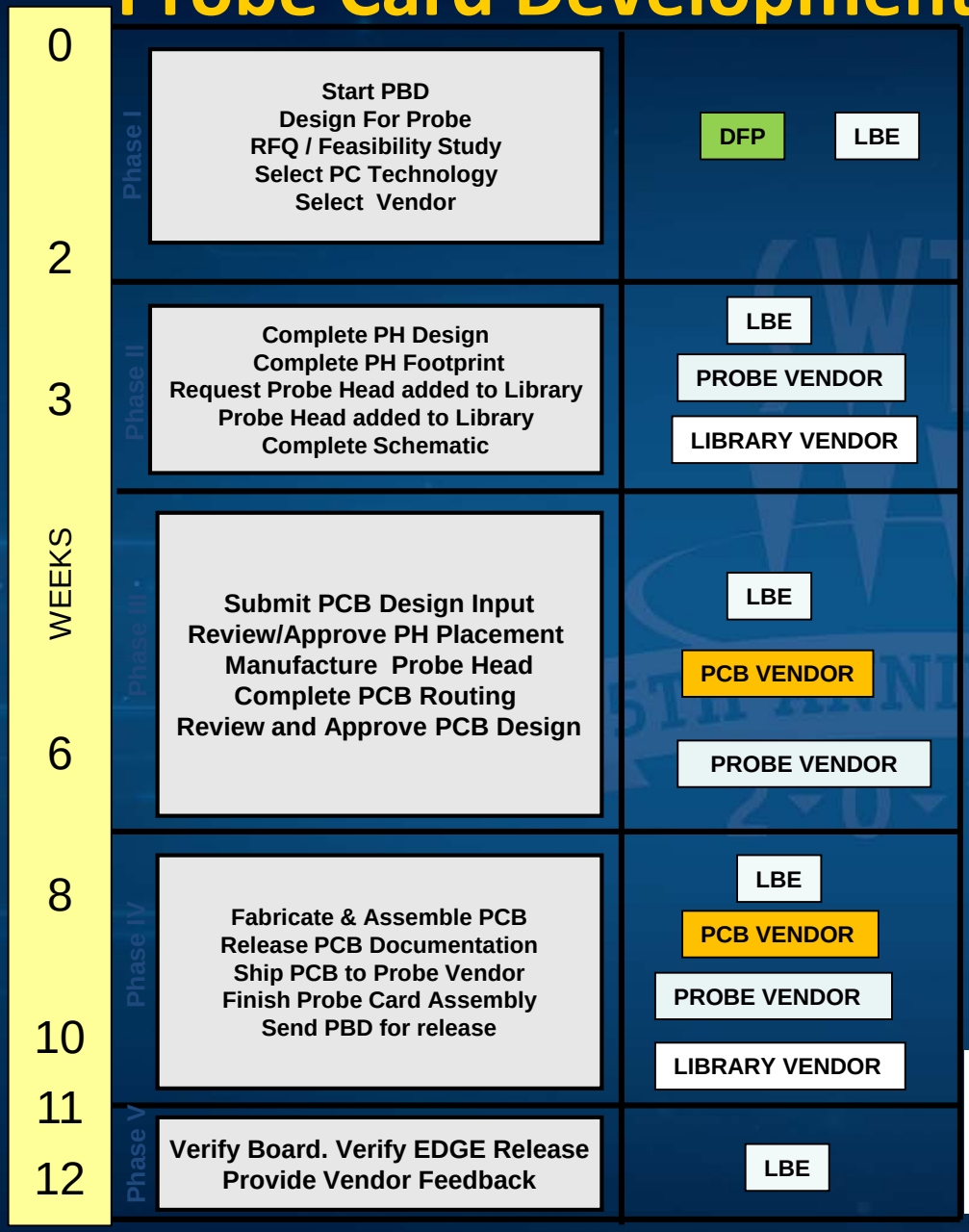
Example of high voltage specs.

- Both multiprobe and parametric WLR have high temperature testing.
- Maintaining steady and robust solutions at these higher temperatures becomes difficult as pad sizes shrink giving way to less margin for alignment.
- Leveraging tools like auto-realignment can help to maintain current z position of needle as it expands due to the temperature rise.
- Both multiprobe and parametric testing are also pushing for applications that need 1kV test capability and we are using learnings from both applications to develop rules / specs surrounding high voltage testing.

Differences

- **There are also many differences between the two types of tests.**
- **Some of these differences actually make parametric testing a simpler process from a probing aspect.**
- **Also easier to transfer knowledge from multiprobe back to parametric.**
  - Probe Card Flow / Order Process
  - Probed Test features
  - Number of sites / pins
  - One probe card for a technology vs one specific device
    - In multiprobe, each probe card design is custom to that specific device.
    - In parametric we have ability to test multiple devices within a certain technology using one probe card.
    - This allows the cards to run on setup longer without having to change for individual devices like at multiprobe.

Probe Card Development Flow / Ownership



Phase I

- LBE requests Probe Build Document (PBD) and PCB EDGE #s
- LBE initiates the Probe Build Document (PBD)
- PBD sent to DFP Team for recommendations *(optional)*
- PBD is sent to Probe Vendor for quote/feasibility
- Vendor copy DFP on RFQ communications
- LBE selects the Probe Vendor

Phase II

- Probe vendor will design the probe head
- Probe Vendor then request the footprint's upload to the CAD library for PCB design

Phase III

- LBE submits the Probe Card schematic and PBD to PCB Vendor
- LBE works with the PCB Vendor to complete the PCB design.
- LBE and Probe Vendor review PCB design
- LBE approves the PCB design

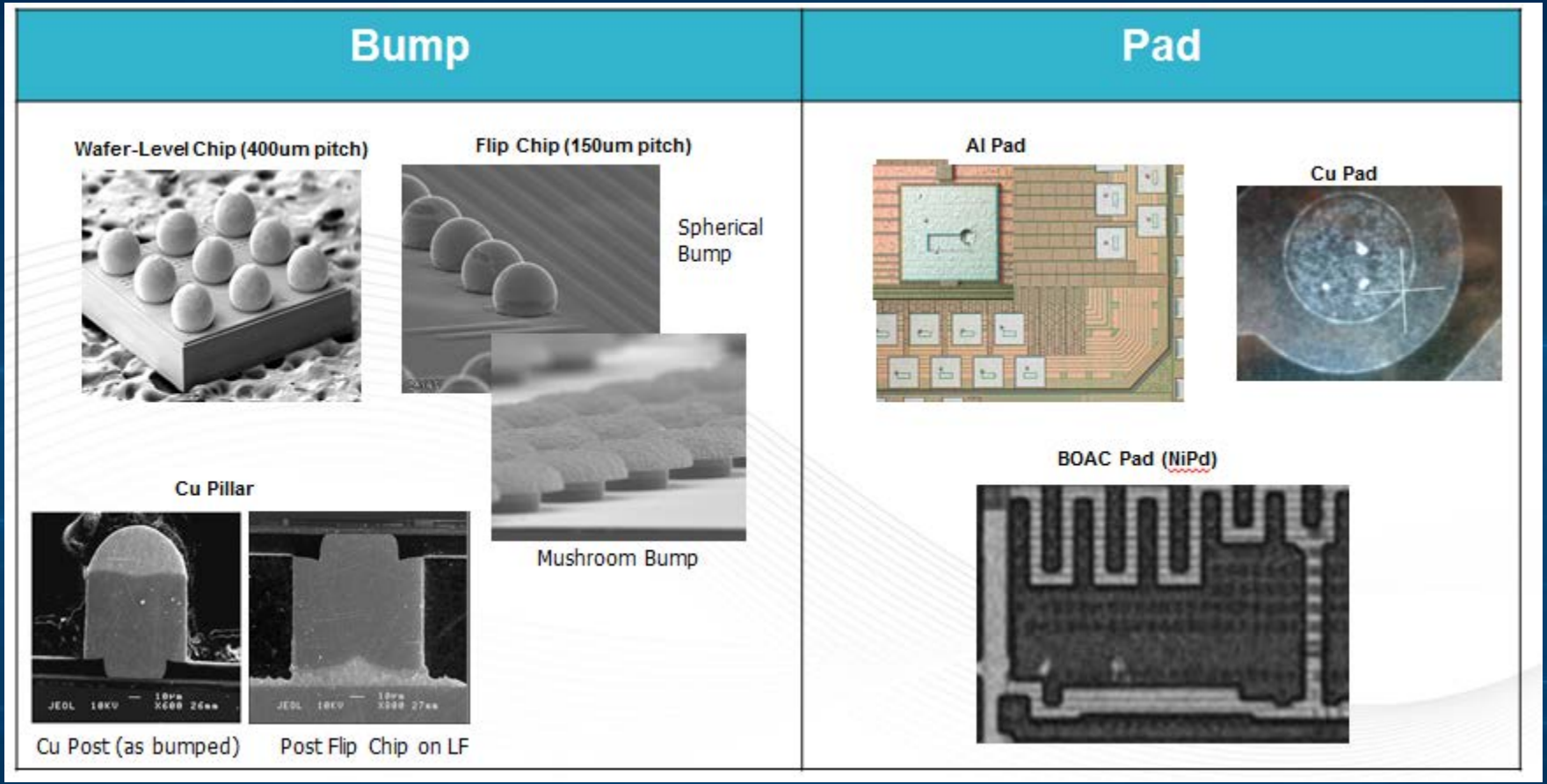
Phase IV

- PCB vendor manufacturing and test of the PCB
- PCB Vendor ships PCB and doc packet to Probe Vendor & provides PCB documentation to TI.
- Probe Vendor assembles and tests Probe Head on PCB
- Probe Vendor delivers finished Probe Card & PBD to TI

Phase V

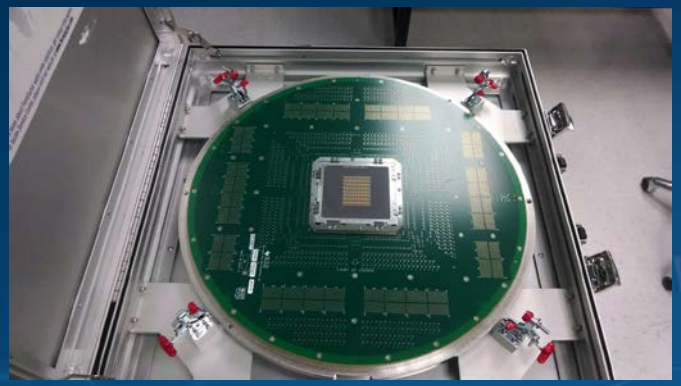
- LBE checks out the probe card functionality
- LBE confirms PCB and PBD are released to EDGE

Probed Test Features



- For parametric we are typically probing Al or NiPd pads where as in Multiprobe there are many more types of features

Site / Pin Count



Some multiprobe probe cards test >100sites and upwards of 20k probes.

Parametric cards are typically single site with less than 20 pins.

- **Multiprobe has the ability to test multiple devices at once in parallel.**
  - We have some devices testing 128 sites.
- **Some of these devices can have upwards of 20k probes per probe card.**
  - Should be easier to maintain a 20pin card versus 20k in terms of alignment / planarity.
- **Generally, parametric testing is single site with less than 2 dozen probes.**

Design Rule Standardization

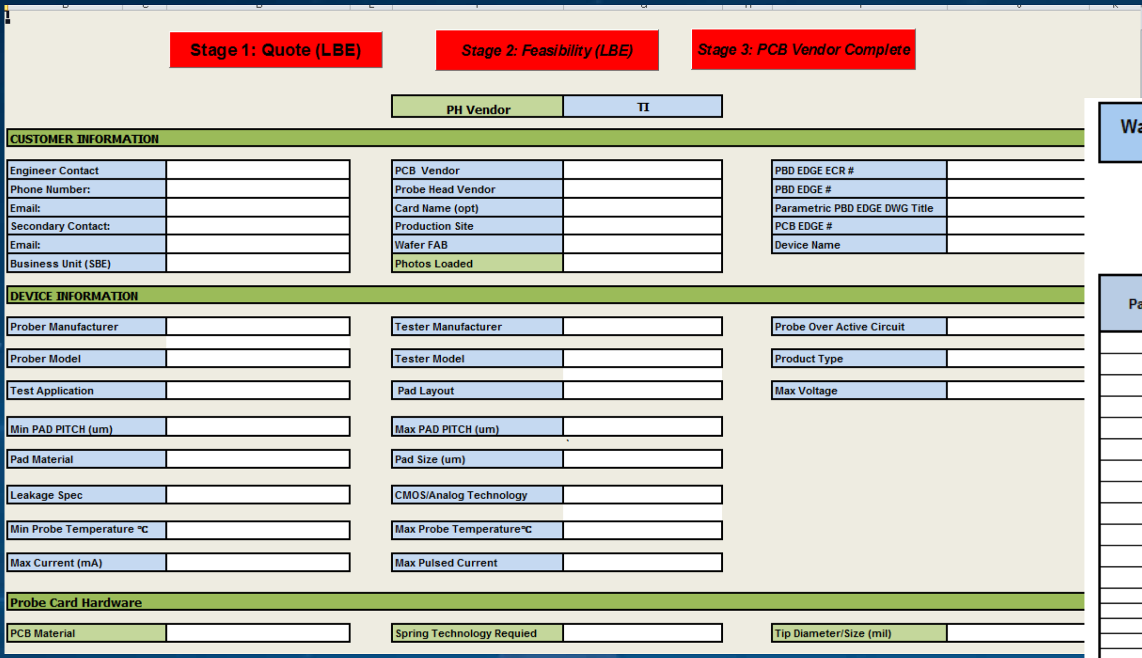
Goal is to move to standard pad frame on all products to reduce probe card costs

Card will be built in a 5-6-5 configuration
All measurements are from center of pad to center of pad

52um Scribe	80um Scribe
Small Pitch (S) = 126.0um Large Pitch (L) = 216.0um	Small Pitch (S) = 114.1um Large Pitch (L) = 249.9um

- **In multiprobe, each different technology has design rules associated with the pad size / pitch etc.**
- **We are leveraging this same idea to try and standardize on certain pad frames across multiple technologies for parametric.**
- **Looking at possibility to also standardize pad dimensions.**

Hardware Documentation



Stage 1: Quote (LBE) | Stage 2: Feasibility (LBE) | Stage 3: PCB Vendor Complete

PH Vendor	TI

CUSTOMER INFORMATION

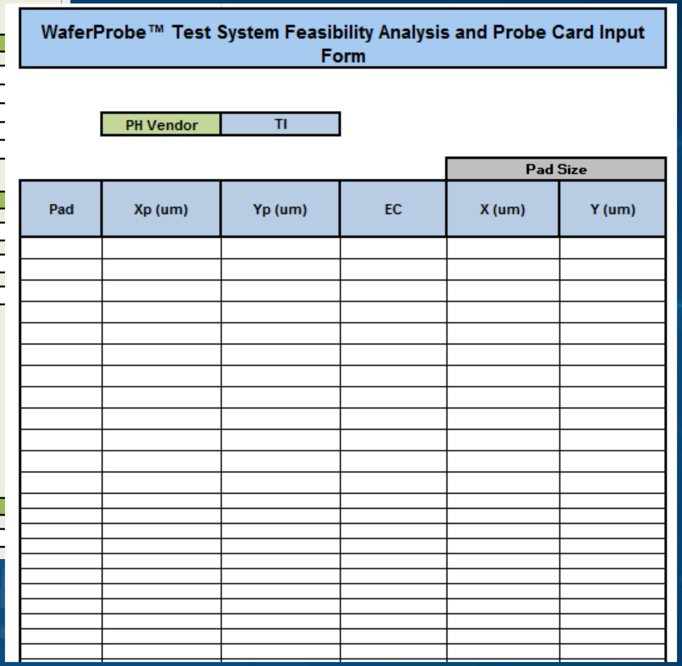
Engineer Contact		PCB Vendor		PBD EDGE ECR #	
Phone Number:		Probe Head Vendor		PBD EDGE #	
Email:		Card Name (opt)		Parametric PBD EDGE DWG Title	
Secondary Contact:		Production Site		PCB EDGE #	
Email:		Wafer FAB		Device Name	
Business Unit (SBE)		Photos Loaded			

DEVICE INFORMATION

Prober Manufacturer		Tester Manufacturer		Probe Over Active Circuit	
Prober Model		Tester Model		Product Type	
Test Application		Pad Layout		Max Voltage	
Min PAD PITCH (um)		Max PAD PITCH (um)			
Pad Material		Pad Size (um)			
Leakage Spec		CMOS/Analog Technology			
Min Probe Temperature °C		Max Probe Temperature°C			
Max Current (mA)		Max Pulsed Current			

Probe Card Hardware

PCB Material		Spring Technology Requied		Tip Diameter/Size (mil)	



WaferProbe™ Test System Feasibility Analysis and Probe Card Input Form

PH Vendor	TI

				Pad Size	
Pad	Xp (um)	Yp (um)	EC	X (um)	Y (um)

- The Probe Build Document (PBD) is an Excel form that contains the specific requirements for the probe card design, manufacturing, and maintenance.
- Provides all TI Vendors with the information required for quote and feasibility analysis.
- Provides manufacturing information needed to develop onsite repair / maintenance activities

Build Specifications

Table #12 – Cantilever Acceptance Guidelines (Where Cantilever is Accepted)	
Bond Pad Size	≥ 70x70um for a single probe [1]
# of Tiers	< 4 tiers
Core pads	No core pads
Probe Count	< 500
Probe Temperature	30ºC to 85ºC
Engineering	For production probing, both cantilever and vertical technology can be selected depending on various parameters, but for the engineering development (MQ) cantilever can used.
Offloads	Test floors must accept incoming cantilever devices as long as no production issues with card. [2]
Volume	1 million TDs over life of device

Pad Probing – Cantilever & Blade Probe Card – Parametric

#	Parameter	Parametric/WLR – HP 4062, Keithley S-400, Keithley S-600
1 2 3 4 5 6 7	PC Board Thickness, PCB Keep Out Area, PC Board Material, Probe Depth, PCB Leakage, Probing Methods Test Temperature	Refer to Table #1:
8	Probe Material (wire)	WRe or BeCu
9	Probe Tip Diameter	Refer to Table #5a
10	Contact Force	2.75 grams/mil (-10%, +20%) Note #4
11	Substrate	N/A
12	Maximum Pin Count	N/A
13	Guide Plate Material	N/A
14	Build Method	Straight Build (± 12°)
15	Maximum Tiers	2 Tiers (Maximum) Note #2
16	Wire Diameter	Wire Diameter must support 2 tiers maximum
17	Tip Shape	Flat
18	Tip Length	≥ 7 mils
19	Tip Angle	Tip Angle is 5° off vertical ± 2°
20	Ring Material	Ceramic
21	Epoxy Temperature Rating	≥ 150°C Note 4
22	Probe Ring or Blade Clearance	≥ 381 µm
23	Probe Ring Stiffener	See Cantilever Card Notes*
24	Maximum Overtravel	Refer to Table #2
25	Planarity	< 12.5 µm
26	Alignment	± 6.35 µm Note #3
27	Analyzer Verification	Analyzer verification performed at best OT to match pad/bump conditions Note # 4
28	Contact Resistance (CRes)	< 2.0 Ohms Note #7
29	Components	N/A

- **Probe Card Build Spec is the document which we use to outline the specifications we hold our probe card vendors to.**
- **We have rules governing the selection of certain technologies depending on the characteristics of the device (See above example)**
- **For parametric, we can also incorporate these kind of specifications depending on the application, high voltage / WLR temp testing/ small pad size / etc…**

Current Probe Issues / Limitations

- **Some of the major challenges we face today in probe are also similar to problems we may see in parametric testing.**
  - Decreasing Pad dimensions
    - Always a push for smaller pads with smaller pitches
    - Harder and hard for probe card to maintain alignment
    - Risk breaking PO on edge of pad
  - Temperature
    - Continued push for high / ultra high temperature testing >150oC
    - Some applications calling for 175 /200oC
    - Must ensure that the setup is at equilibrium
    - Prober can accurately maintain the z position of the probe as it expands due to the temperature

Summary

- In the past, many of the TI multiprobe test sites around the world have had their own standards / operating procedures that differed from site to site.
- In the recent years, TI has tried to unite all the test sides as one body under group called the OMPT Team (One MAKE Probe Team).
- Parametric and WLR at TI has also created a worldwide team comprised of members from each fab with a goal to help unite and standardize across the fabs in terms of hardware / infrastructure/ and processes just like in multiprobe.
- This open communication between the fabs is key in sharing best practices and key learnings or new qualifications between ALL of TI's facilities.

Questions

Thanks to the PTS Team and WW Parametric Team at TI and all the probe card vendors we use.