Verification of HBM through Direct Probing on MicroBumps

Marc Loranger
FormFactor

Sung Wook Moon
SK hynix

June 5-8, 2016
Outline

• HBM market
• HBM test flow
• Device structure overview
• Key test challenges addressed
  – Signal delivery and simulation results
  – Direct on MicroBump probing results
• Summary
High Bandwidth Memory (HBM)

• **Market requirement**
  – Increase data bandwidth well above current GDDR5 technology
  – Decrease power per GB/s of bandwidth
  – Smaller size
    • Improve power distribution
    • Signal transmission

• **Long term roadmaps**
  – Expand into server applications and high performance computing when reliability is proven
High Bandwidth Memory (HBM)

- **Stacked Memory on Logic Architecture**
  - 2, 4 to 8 die stacked on a Logic Die
  - TSVs are typically employed to stack the memories
  - HBM stack is then mounted on a 2.5D interposer with a processing element
- 1st key application is high performance graphics
Typical HBM Test and Assembly Flow

- Presentation focuses on this Test insertion

Marc Loranger
SW Moon

SW Test Workshop - June 5-8, 2016
HBM 2 Direct Probe on Micro Bumps Requirement

- **Array size**
  - 6022µm x 2832µm

- **Test requirement**
  - 2.133 Gb/s Functional test of the stack
  - All 8 device channels

- **HBM Array Structure**
  - Total TSV Micro Bumps: 3990
    - 55µm Micro Bump Pitch
  - Total IO Micro Bumps: 1728
  - Direct access micro bumps: 176
  - Total Power Supplies: 3 – 1056
  - Total ground Micro Bumps: 1030

Marc Loranger
SW Moon

SW Test Workshop - June 5-8, 2016
HBM MicroBump Test Challenges

• **Electrical**
  – Number of signals
    • 8 Channel device with ~220 1GHz signals per channel
    • Objective is to test all channels at full application test rate of 2Gbps
  – Key issues to address
    • Signal fidelity from ATE to DUT
    • Signal fidelity of DUT generated signal at the ATE input
    • Cross talk due to small pitch of MicroBumps and contactor space transformer design

• **Mechanical**
  – Probe impact on the MicroBumps due to at temperature testing with long test times
Simulation Test Cell Overview

• **Contactor is FormFactor Apollo MF-40**
  – ~4000 springs
  – 55µm spring pitch
    – HBM bump pitch

• **ATE configuration**
  – UltraFLEX KGS High Speed Memory Stack tester

• **Device handler**
  – Testing can be done pre singulation of the Stack on a prober or post singulation using a die level handler
Signal Fidelity Simulations

- **Conditions**
  - 90pS ATE driver rise time (1V swing 20% to 80%)
  - 1.2V swing used
  - Driver pre-emphasis enabled to optimize signal performance at the DUT

- **Model description**
  - 3 adjacent signals in the space transformer were extracted using Cadence Sigrity SI tool from the space transformer design files
  - Selected longest space transformer signals from the MicroBumps to the PCB
    - Worst case signal path and cross talk environment
  - PCB model used known correlated models for high speed design

- **Simulations**
  - Clock – with cross talk to signals on both sides of the clock
  - Eye diagram
Simulation Model Diagram

- **Signals of Channel F selected for model**
  - Longest signals in Space transformer (ST)
  - Includes region that is *not impedance controlled* as signals escape through the power region
ATE to DUT

Clock waveform

- Low attenuation of the signal due to the probe card
- Cross talk coupling ~90mV (m5-m3)
ATE driver to DUT
PRBS 9 – Eye diagram

Single Signals on Center trace

Eye Diagram with induced cross talk
Signals on Center trace displayed
PRBS – 9 signal on 2 adjacent traces
90 degrees out of phase

Marc Loranger
SW Moon

SW Test Workshop - June 5-8, 2016
DUT generated signal at the ATE input

• **Key issue**
  – Original concern was that the HBM drivers would not be able to drive the transmission line to the tester

• **Models**
  – SK hynix IBIS models of the HBM2 drivers were used in the simulation model
  – DUT Voh = 1.2V
  – 4 of the device selectable drive strengths were simulated to determine which would be most viable from a signal fidelity perspective
  • 6mA, 9mA, 12mA and 15mA
IBIS Drive Strength Overview

• Eye diagrams observed at probe card ATE connection

• Optimum drive strength is either 9mA or 12mA
  – 12mA used for the subsequent simulations
DUT 12mA IBIS driver to ATE
PRBS 9 – Eye diagram

No ATE load

DUT (IBIS 12mA) to ATE
2.0Gb/s PRBS9

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage (V)</td>
<td>1.62</td>
</tr>
<tr>
<td>Current (mA)</td>
<td>12</td>
</tr>
<tr>
<td>Frequency (MHz)</td>
<td>2000</td>
</tr>
<tr>
<td>Symbol Rate (Gbps)</td>
<td>2</td>
</tr>
<tr>
<td>Eye Height (mV)</td>
<td>676.0</td>
</tr>
<tr>
<td>Eye Width (ps)</td>
<td>450.0</td>
</tr>
<tr>
<td>Rise Time (ps)</td>
<td>157.3</td>
</tr>
<tr>
<td>Fall Time (ps)</td>
<td>174.3</td>
</tr>
</tbody>
</table>

Marc Loranger
SW Moon
DUT 12mA IBIS driver to ATE
Clock and Cross talk

Single Signals on Center trace

Induced cross talk signal on Center trace with clock on 2 adjacent traces

- Cross talk on victims ~150mV (m2-m1 and M14-m13)
MicroBump Probing

• Challenges – Assembly Yield Impact
  – MicroBump damage due to probing on the MicroBumps
  – MicroBump damage due to at temperature testing
  – MicroBump damage from long duration test at temp

• Evaluations
  – MicroBump “coining” vs. Over travel vs. temperature vs. Test time
    - Coining round bump damage due to flat tip probe contact
MF40 Flat tip scrub mark vs. Over Travel on MicroBumps

- 25°C short duration
- MicroBump Measured diameter 33.5µm

Marc Loranger
SW Moon

SW Test Workshop - June 5-8, 2016
### MicroBump Damage Experiment matrix and results

<table>
<thead>
<tr>
<th>Over Travel</th>
<th>Room Temp</th>
<th>90°C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.1 Min</td>
<td>0.1 Min</td>
</tr>
<tr>
<td></td>
<td>10 Min</td>
<td>10 Min</td>
</tr>
<tr>
<td></td>
<td>60 Min</td>
<td>60 Min</td>
</tr>
<tr>
<td>60µm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>6.4µm</td>
<td>14.6µm</td>
</tr>
<tr>
<td></td>
<td>12.4µm</td>
<td>23.5µm</td>
</tr>
<tr>
<td></td>
<td>15.1µm</td>
<td>24.1µm</td>
</tr>
<tr>
<td>80µm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>8.4µm</td>
<td>13.5µm</td>
</tr>
<tr>
<td></td>
<td>13.1µm</td>
<td>23.2µm</td>
</tr>
<tr>
<td></td>
<td>15.8µm</td>
<td>25.2µm</td>
</tr>
</tbody>
</table>

- Increasing temperature will increase amount of “coining”
- 50mA of DC current flow does not affect the size of the “coining” on the top of the MicroBump
Post Touch Down MicroBump Photos

- **TD Duration**
  - 6 Sec
  - 600 sec
  - 1 Hour

- **Room temp**
  - 90°C

- **90°C**
  - 60µm OT
    - 6.4µm
    - 12.4µm
    - 15.1µm
  - 80µm OT
    - 8.4µm
    - 13.1µm
    - 15.8µm

Marc Loranger
SW Moon

SW Test Workshop - June 5-8, 2016
Direct on MicroBump Probing

Summary

• **Electrical Test – Signals paths**
  
  – Simulation models of the DUT and of the Space Transformer show testing can be done at the device specified operating rate of 2Gb/s on the full 8 channels of the HBM Stack

• **MicroBump Probing**
  
  – Using fine pitch FormFactor MF-40 probes at the 55µm HBM bump pitch shows increasing MicroBump coining when probing at 90°C for > 10 min

• **Future work**
  
  – Evaluation of MicroBump probing on singulated stacks
We thank the following for providing support to the development of this material

Kelvin Ching
Clarence Gapay
Uyen Nguyen
Doug Ondricek
Todd Swart