Automated Testing of Bare Die-to-Die Stacks

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Presentation Outline

1. Introduction
2. Experimental Set-Up
   - Test Equipment
   - Misalignment Correction Algorithm
   - Test Algorithm
   - Stacked Test Chips
   - Types of Carriers
   - Automatic Re-Align in Action
3. Experimental Results
   - Results on Dicing Tape on Tape Frames for Ø100mm Wafers
   - Results on Sheets of Single-Sided Thermal-Release Tape
   - Results on Double-Sided Thermal-Release Tape of Ø300mm Carrier Wafers
4. Conclusion
Die-to-Die (D2D) Stacking

- D2D stacking is an efficient way to generate stacks
  - Allows to
    - Stack dies of different sizes
    - Stack pass-tested dies on pass-tested dies
  - Often utilized for research test chips at IMEC
    - Small and medium quantities
- Transport of D2D stacks in waffle packs
Options for Post-Bond D2D Stack Testing

1. Per-Stack Placement on Prober
   - Risk of falling out of waffle pack
   - Risk of loosing stack tracking
   - Manual lifting, placement on chuck
   - Per-stack probe-to-pad alignment
   - Requires engineering presence
   - Bottle-neck in test throughput

2. Stacks in Bare-Die Tray
   - Need to hold dies in tray during probing, e.g. through vacuum
     - Custom-made trays with vacuum distribution
     - Expensive, need one per die size
     - Cheaper alternative: drill holes in waffle pack
   - Requires transfer from original waffle pack into tray and vice versa – so far, manual
   - Requires per-stack probe-to-pad alignment
Concept: Pick-n-Place Array on Carrier Substrate

- Pick-n-place D2D stacks in matrix structure on wafer(-like) carrier substrate
  - Allows for
    - Loading a single substrate implies loading many D2D stacks in parallel in probe station
    - Automatic index stepping over D2D array by probe station
    - Possible reuse of substrate form factor by OSAT
  - Requires
    - Temporary bonding of D2D stacks to carrier substrate
    - Rather accurate pick-n-place (PnP) operation
    - Ability to still correct small PnP mis-alignments on probe station
    - Marking of bad dies: physical (inking) or electronic (wafer map)

- Substrate Options
  1. Tape on tape frame
  2. Tape sheets
  3. Carrier wafer
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Test Equipment – CM300 Probe Station

**Specification**
- Cluster configuration
  - Two probers: left/right
  - Shared MHU auto-loader
- Thermo chucks

**Substrate Loading**
- Via auto-loader
  - Ø300mm wafers
- Via front-side load port
  - Wafers up to Ø300mm
  - Tape frames for wafers up to Ø300mm

**Location**
- IMEC’s 300mm fab (in-line)
Misalignment Correction Algorithm

Software Functions in Velox

- ReAlign 2 H: wafer; x, y, z, and θ; after loading new wafer or temperature changes
- ReAlign 2 C: nth die; x, y, z; accuracy improvement on small pads
- AlignChip: single die; x, y, z, and θ; for singulated dies and positioners

Correction with AlignChip

- Use with Platen Camera: field-of-view 1.50 mm × 1.10 mm
- Correction possible as long as alignment pattern is in FoV
- Constrained capability to resolve rotational misalignments
  - θ_stack: rotation around center of die stack (ideally to be applied)
  - θ_chuck: rotation around center of chuck (installed mechanism)
- Search area can be enlarged by stepping around
- Can use alternative (back-up) alignment pattern
Test Algorithm

Algorithm:
Step 1: SetUpProject
for all tape frames do {
    Step 2: ManualOperation
    Step 3: AutomatedOperation
}

Step 1: SetUpProject
1: Measure x,y StepNextDie index
2: Training of AlignChip plug-in: pattern recognition and Home setting
3: Training of DetectWaferHeight plug-in
4: Create “wafer” map:
   5: Maximum number of die stacks in x and y (e.g., 7×7)
6: Input x,y StepNextDie index as measured in Step 1.1
7: Define coordinate system (e.g. origin (0,0) is SW die stack)
8: Define probe route (e.g., snake bottom-up)
9: Load probe-card training model (or re-train probe card)

Step 2: ManualOperation
1: Place tape frame on chuck with center die on center of chuck
2: Indicate in wafer map dies stacks to-be-probed/skipped
3: Move chuck to Platen Camera
4: Move manually to (nearby) dicing street of center bottom die
5: Align2Point for first coarse alignment of tape frame
6: Move manually to Home position on center die stack

Step 3: AutomatedOperation
1: Perform AlignChip on center die stack
2: Perform DetectWaferHeight
   % SynchronPosition is defined (by means of pattern recognition of cross % on chuck) and wafer height detection is performed on center die
3: for all dies stacks do {
4:     StepNextDie % first sub-die (0,0) is base to start AlignChip
5:     Move under Platen Camera
6:     AlignChip
7:     FindFocus: invokes LabVIEW algorithm for calculation ContactHeight
8:     AlignChip % Second time, just to be sure
9:     Move to ProbePosition % Now perfectly aligned
10:    Set Home
11:   for all sub-dies do {
12:       Contact; measure; Separate; write data to file
13:     }
14: }
Rectangular “Wafer” Maps with Skip Option

In Step 1 (for all substrates)
- Maximum number of dies stacks in x and y
- Input x,y StepNextDie index measured in Step 1.1
- Define coordinate system (e.g., SW stack is origin)
- Define probe route (e.g., snake bottom-up)

In Step 2 (individually for each substrate)
- Indicate in wafer map dies stacks to-be-probed/skipped
Stacked Test Chips

- Two-die test-chip stacks
  - PTCO: 5.2×5.2mm²
  - PTCP: 10.2×10.2mm²

- Post-bond testing on bare PTCO/P stacks
  - Probing on multiple probe-pad modules
  - All probe-pad modules are located on the front-side (= top-side) of the bottom die
  - Each probe-pad module is IMEC’s standard 2×12 module
Types of Carriers

1. Dicing Tape on Tape Frames for ø100mm Wafers
   - Blue dicing tape manually laminated on frame
   - PTCO/P D2D stacks in arrays of max. 7×7=49 stacks/frame
   - In total: 372 PTCO/P stacks on 15 frames

2. Sheets of Single-Sided Thermal-Release Tape
   - White tape with thick polyester backing layer
   - Can serve as stand-alone carrier
   - PTCO/P D2D stacks in arrays of max. 9×9=81 stacks/sheet

3. Double-Sided Thermal-Release Tape on Carrier Wafers
   - Transparent tape affixed to a blank ø300mm carrier wafer
   - Allows to use the probe station’s auto-loader
   - PTCO/P D2D stacks in arrays of 7×7=49 stacks/wafer
Automatic Re-Align in Action

Extra-long cantilever needles to compensate for stacked-die height

Validation of correct operation by checking probe mark locations

Training of alignment pattern (here: alignment cross on bottom die)

Contact view: side-view camera

Top die in stack

Probe needles left-hand

Probe needles right-hand

Top-view camera

Bottom die
Results on Double-Sided TR Tape – 2/2

Test sequence and video by Bart De Wachter
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Results on Dicing Tape on Tape Frame – 1/2

- **Tape Frames for Ø100mm Wafers**
  - 100mm used due to pick and place compatibility
  - Manual loading via front port chuck pull-out
  - Reused tape frames sometimes bent: difficult for chuck’s vacuum
  - Tape wrinkles due to manual lamination; most of them disappeared over time
Results on Dicing Tape on Tape Frame – 2/2

- Re-Align Operation Largely Successful
  - Performance: ~30 seconds/stack
    - Two AlignChip invocations (Step 3.6 + 3.8)
    - Two alignment patterns per AlignChip

- Re-Align Issues
  - Two instances 90° rotated: manual mistake in PnP preparation
  - Two instances with obscured alignment patterns due to underfill fillet/out-bleeding

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<tr>
<th>Die Location</th>
<th>Wafer Map Location</th>
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<th>y_c (µm)</th>
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Minimum: 133 267 0.371
Maximum: -203 0 -0.388
Average(abs): 67.6 95.8 0.163
Std.dev(abs): 62.5 82.4 0.112
Results on Single-Sided TR Tape – 1/2

- Sheets of Thermal-Release Tape
  - Stand-alone tape sheets, no frame necessary
  - No bent frames, no tape wrinkling
  - Better PnP accuracy, narrower ‘streets’
  - Manual loading via front port

- Re-Align Operation Largely Successful
  - Performance: avg. 13.1 seconds/stack
    - One AlignChip invocation (Step 3.6; skipped Step 3.8)
    - Two alignment patterns

- Re-Align Learnings
  - Stacks 6+7: too large $\theta_{\text{stack}}$, skipped in wafer map
  - Stack 45: large $\theta_{\text{stack}}$, missed alignment for Stacks 46+47
### Results on Single-Sided TR Tape – 2/2

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</table>

### Minimum
- $x_c$: -66.0 µm
- $y_c$: -57.0 µm
- $\theta_c$: -0.131°
- $t_{AC}$: 12.6 s
- $t_{SND}$: 0.8 s

### Maximum
- $x_c$: 70.1 µm
- $y_c$: 77.7 µm
- $\theta_c$: 14.3°
- $t_{AC}$: 14.3 s
- $t_{SND}$: 1.5 s

### Average (abs)
- $x_c$: 25.7 µm
- $y_c$: 24.3 µm
- $\theta_c$: 13.1°
- $t_{AC}$: 13.1 s
- $t_{SND}$: 0.9 s

### Standard Deviation (abs)
- $x_c$: 18.9 µm
- $y_c$: 17.6 µm
- $\theta_c$: 0.5°
- $t_{AC}$: 0.5 s
- $t_{SND}$: 0.1 s
Results on Double-Sided TR Tape – 1/2

- Thermal-Release Tape on Ø300mm Carrier Wafer
  - Enable loading with auto-loader

- Re-Align Operation Successful
  - Performance: avg. 5.9 seconds/stack
    - One AlignChip invocation
    - One alignment pattern
  - Long compared to StepNextDie (= 0.9 s), but a lot faster than manual alignment!

<table>
<thead>
<tr>
<th>Die Stack Location</th>
<th>$x_c$ (µm)</th>
<th>$y_c$ (µm)</th>
<th>$\theta_c$ (°)</th>
<th>$t_{AC}$ (s)</th>
<th>$t_{END}$ (s)</th>
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Minimum -19.3 -0.2 -0.072 5.4 0.8
Maximum 28.3 397.4 0.113 12.1 2.1
Average(abs) 9.5 240.7 0.036 5.9 0.9
Std.dev(abs) 7.3 116.9 0.024 1.2 0.2
Presentation Outline

1. Introduction
2. Experimental Set-Up
   - Test Equipment
   - Misalignment Correction Algorithm
   - Test Algorithm
   - Stacked Test Chips
   - Types of Carriers
   - Automatic Re-Align in Action
3. Experimental Results
   - Results on Dicing Tape on Tape Frames for Ø100mm Wafers
   - Results on Sheets of Single-Sided Thermal-Release Tape
   - Results on Double-Sided Thermal-Release Tape of Ø300mm Carrier Wafers
4. Conclusion
### Comparison Experimental Results

- **Dicing Tape on Tape Frame**
  - Re-align works, but...
    - Bent frames, wrinkled tape
    - Less accurate PnP

- **Single-Sided TR Tape**
  - Re-align works

- **Double-Sided TR Tape**
  - Re-align works
    - Carrier wafer enables auto-loader

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<tr>
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<th>$x_c$</th>
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<th>$\theta_c$</th>
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<td><strong>Minimum</strong></td>
<td>-203µm</td>
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<td>+133µm</td>
<td>+267µm</td>
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* Two times AlignChip, two patterns each

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<td>-57.0µm</td>
<td>-0.131°</td>
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<td><strong>Maximum</strong></td>
<td>+70.1µm</td>
<td>+77.7µm</td>
<td>+0.137°</td>
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<td>±24.3µm</td>
<td>±0.047°</td>
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<td><strong>Std.dev(abs)</strong></td>
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<td>±17.6µm</td>
<td>±0.035°</td>
<td>0.5s</td>
<td>0.1s</td>
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* One time AlignChip, two patterns each

<table>
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<tr>
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<th>$\theta_c$</th>
<th>$t_{AC}^*$</th>
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<tr>
<td><strong>Minimum</strong></td>
<td>-19.3µm</td>
<td>-0.2µm</td>
<td>-0.072°</td>
<td>5.4s</td>
<td>0.8s</td>
</tr>
<tr>
<td><strong>Maximum</strong></td>
<td>+28.3µm</td>
<td>+397.4µm</td>
<td>+0.113°</td>
<td>12.1s</td>
<td>2.1s</td>
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<tr>
<td><strong>Average(abs)</strong></td>
<td>±9.5µm</td>
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<td>1.2s</td>
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* One time AlignChip, one pattern
Summary

- Demonstrated feasibility of automated index stepping and re-align on arrays of pick-n-placed bare D2D stacks on substrate carriers
  1. Blue dicing tape on tape frames (for Ø100mm wafers)
  2. Sheets of white single-sided thermal-release tape
  3. Sheets of transparent double-sided thermal-release tape on Ø300mm wafers

- AlignChip of CM300’s Velox
  - Features: back-up alignment patterns; stepping to increase search area
  - One invocation for one alignment pattern is mostly sufficient
  - Execution time: AlignChip = 5.9s; StepNextDie = 0.9s; test time = XX s

- Upside potential with exceeded $\theta_{\text{stack}}$
  - $\theta_{\text{stack}} \geq 1.7^\circ$: AlignChip might lose its way, especially out of chuck center
  - Further improvement: AlignChip; Probe; \textit{Undo AlignChip}; StepNextDie

- Significant test throughput improvement for IMEC
  - An option for industrial small/medium-volume production testing
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- **Nitto Denko** *(Genk / Osaka)*
  - Bart Peeters

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Thank you for your attention