SW Test Workshop
Semiconductor Wafer Test Workshop

PROBING CU PILLAR APPLICATIONS W/ VERTICAL TECHNOLOGIES

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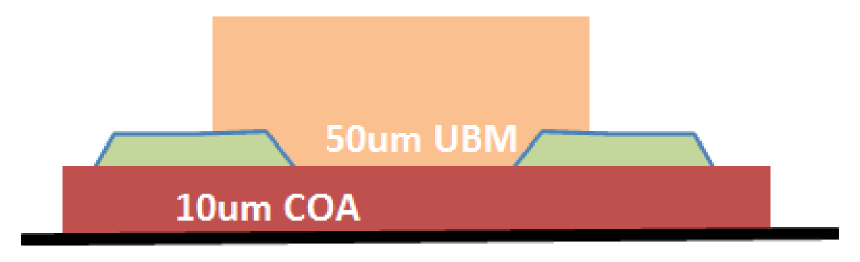
Agenda

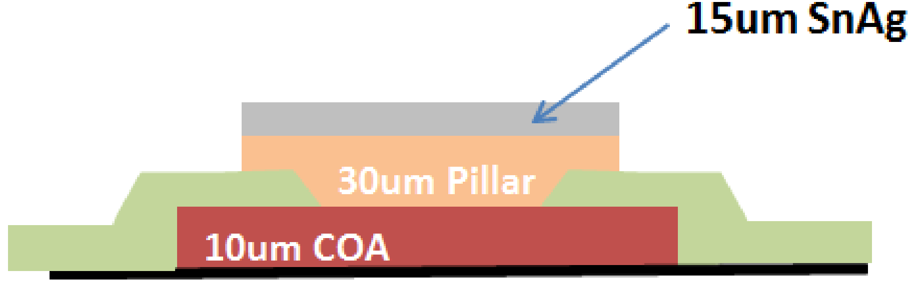
- Overview
- Approach
- Devices
- Lessons Learned
- Next Steps
- Summary

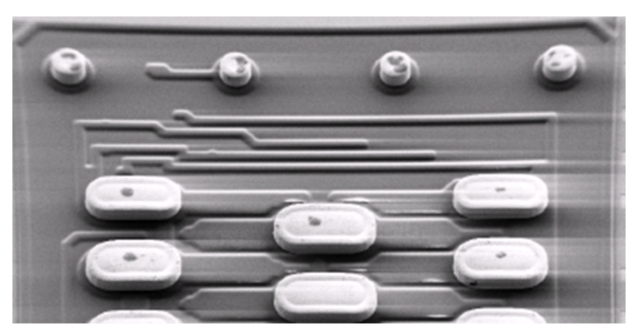
Overview

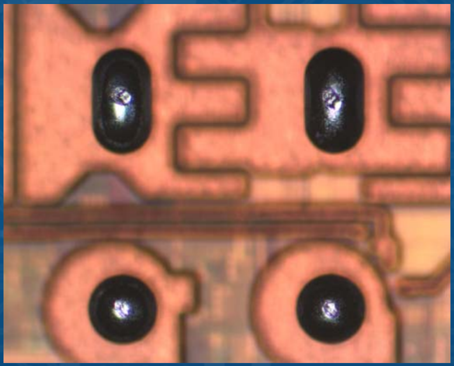
- TI has seen an influx of devices requiring the probing of Cu pillar devices. There are different flavors of these types of device with a bare Cu top and Cu capped with solder.
- Historically, cantilever has been the baseline technology for probing these devices. As the geometries get smaller and requirements become more stringent the need to move toward a more robust vertical probe card technology is
- This paper will review the qualification process of a new vertical technology for Cu pillar probing and lessons learned in the process.

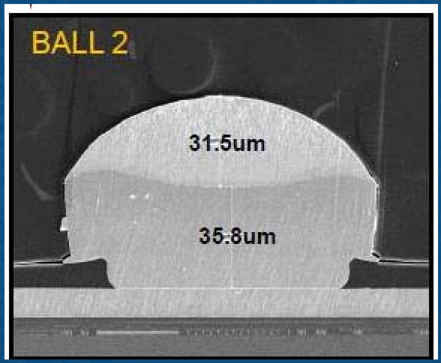
Cu Pillar Feature Overview







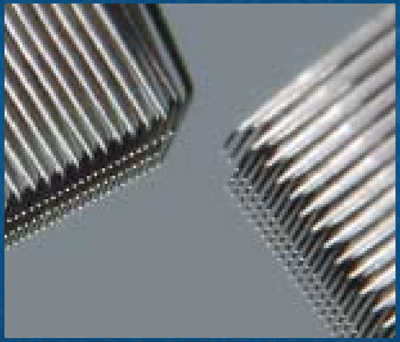




- At TI we have multiple feature types for Cu Pillars.
- Some are pure Cu while some are Cu topped with a solder cap.
- The dimensions of these pillars can vary as well depending on device.
- We probe both variants of pillars.

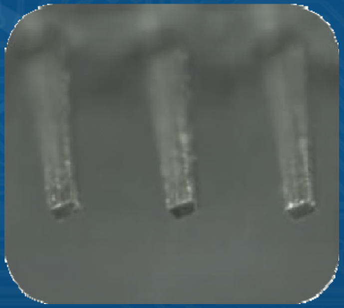
Cu Pillar Probing Overview

Technology	Status
Cantilever	Qualified
Pogo Pin	In Process
Vertical	In Process



Cantilever Probe Tip

Popo Pin Probe Tip



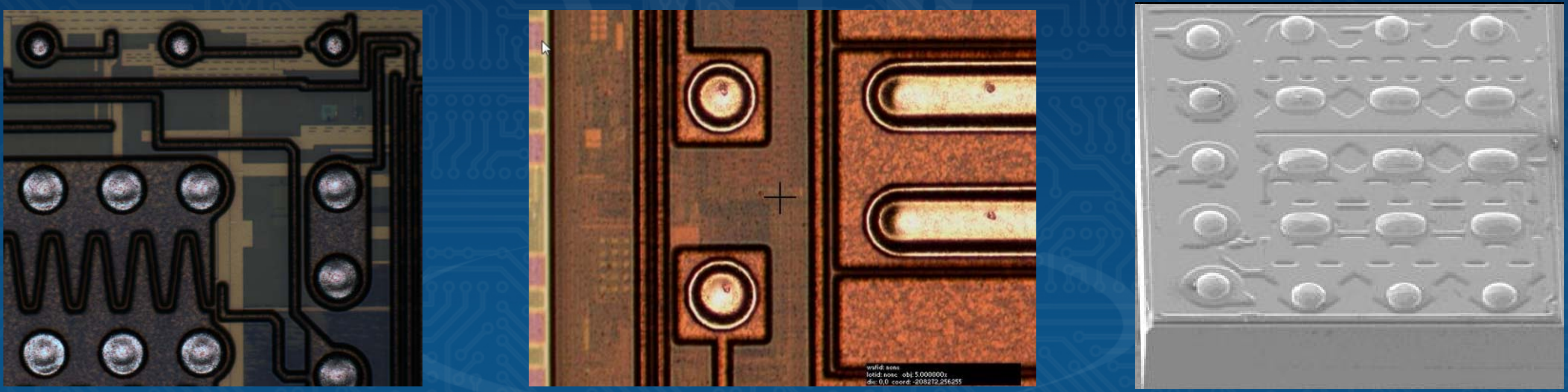
Technoprobe MEMs Probe Needle

- **In the Cu pillar space we have various technologies**
- **For this presentation I will focus on Technoprobe's MEMs vertical technology.**

Approach

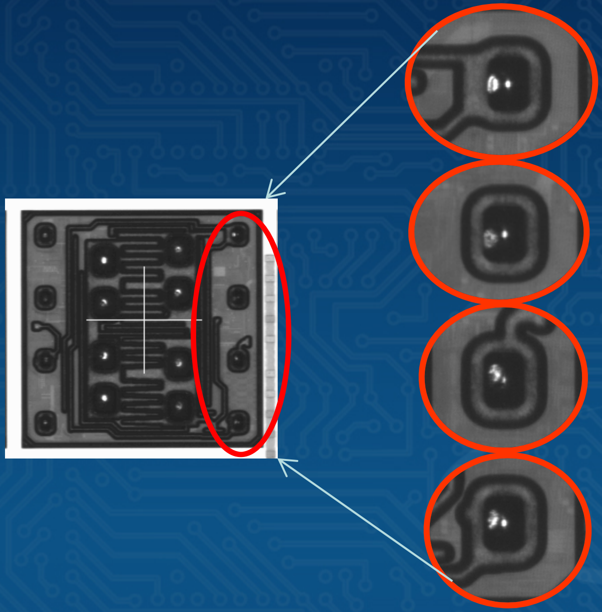
- **TP6xxx and LP8xxx were identified as test vehicles for probing on Cu pillar with vertical probe technology. Technoprobe has been selected as the vertical vendor to take the existing TP6xxx and LP8xxx platforms (PCB, and HW) and only replace the Cantilever head with a vertical probe head.**
  - The TP6xxx device has one insertion at room temperature.
  - The LP8xxx device has two insertions at room temperature and a 24hr bake at 125oC for data retention.
- **This presentation will show comparisons between the Technoprobe MEMs vertical probe and cantilever, a technology previously qualified on Cu pillar at TI.**

Example Pillar Structures

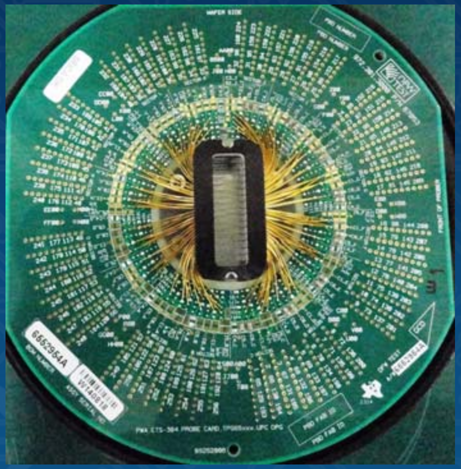


- These are examples of different Cu pillar devices within TI.
- Cu and Cu topped with AlCu.

Cantilever Probe Technology



Examples of misalignment of pillars using cantilever technology causing failures hitting on edge of pillars.



- Cantilever technology has traditionally been the baseline for probing on Cu pillars within TI.
- Smaller feature sizes and adds more stringent requirements such as high temp, challenges cantilever on probing Cu pillars.

Technoprobe Vertical Technology

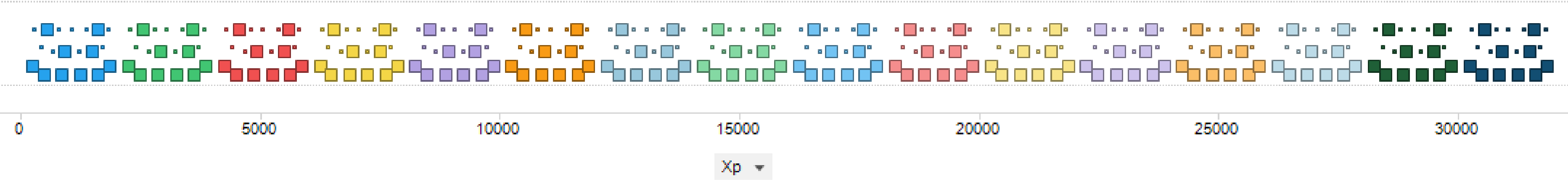
ITEM	TP – M2XLT*	TP – M3*
x, y accuracy	< ± 8 µm	< ± 10 µm
Planarity	≤ 20 µm	≤ 20 µm
Min pitch	80 µm	90 um
Max Tip Diameter	12 um	50 um equivalent
Usable Tip - um	285 -0/+15	350
Recommended OD (Max 100 um after 1st)	90 µm	90 µm
Max frequency (Mhz)	Wired~ 70 Interposer~ 500	Wired~ 70 Interposer~ 500
Working temperature	-40 / 200 °C	-40 / 150 °C
Contact Force at OD	2.5 g	4.5 g
Cleaning Type	Mipox	Mipox
Current (mA)	410 – LCR2	600 – LCR2
Needle Material	Palladium Alloy	Palladium Alloy

*Naming conventions used specific for TI.

- **TI uses Technoprobe's standard M2XLT pin for pad probing so this was used as a starting point for Cu pillar application.**
- **Technoprobe's M3 was another option they typically recommend for bump or pillar.**

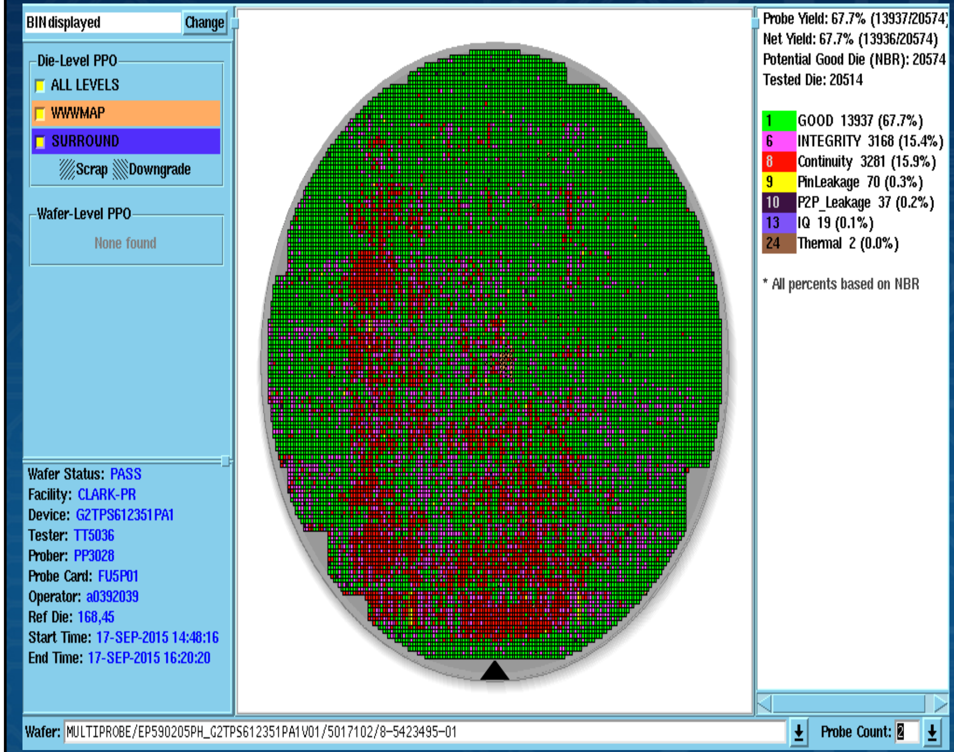
TPS6xxx: Device Parameters and Test Cell Configuration

Device Parameters	
Silicon Node	LBC7
Testing Temp	30-85oC
Pillar Metallurgy	Cu
Pillar Dimensions	90x90um / 75x225um
Min Pitch	380um
Current	100mA
Bandwidth	10mHz
# Probes / Site	10
# of Sites	16
Total # Probes	160
Tester	ETS-364 Razorback
Prober	TSK



Example of device array layout pattern.

TPS6xxx: Correlation Run – M2XLT vs M3XLT



Probe Yield: 67.7% (13937/20574)
Net Yield: 67.7% (13936/20574)
Potential Good Die (NBR): 20574
Tested Die: 20514

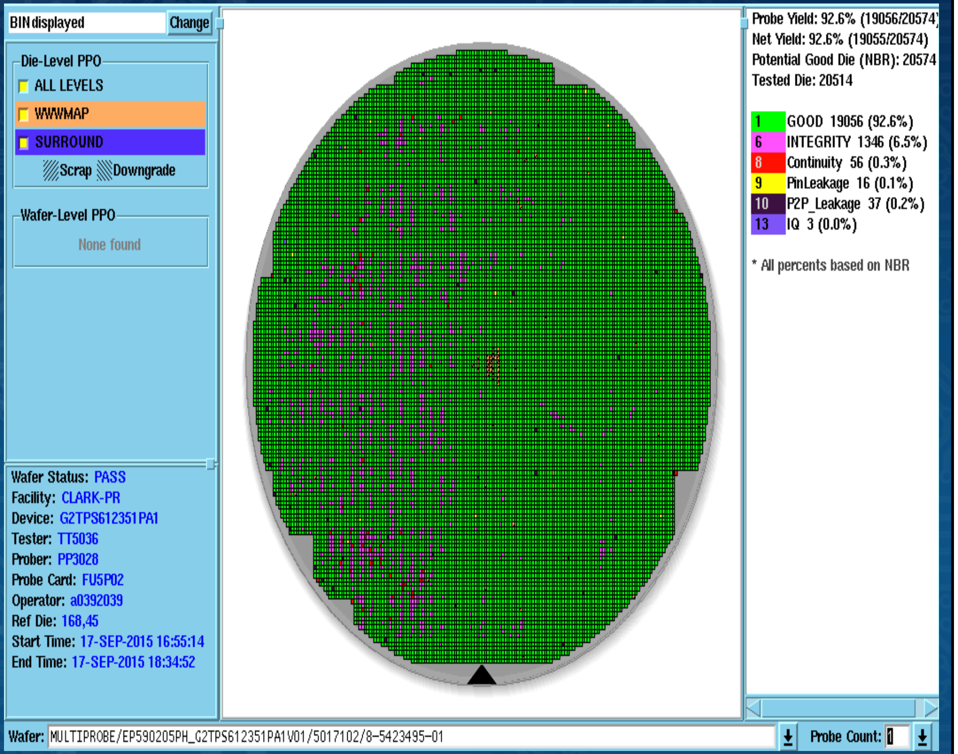
1 GOOD 13937 (67.7%)
6 INTEGRITY 3168 (15.4%)
8 Continuity 3281 (15.9%)
9 PinLeakage 70 (0.3%)
10 P2P_Leakage 37 (0.2%)
13 IQ 19 (0.1%)
24 Thermal 2 (0.0%)

* All percents based on NBR

Wafer Status: PASS
Facility: CLARK-PR
Device: G2TPS612351PA1
Tester: TT5036
Prober: PP3028
Probe Card: FU5P01
Operator: a0392039
Ref Die: 168,45
Start Time: 17-SEP-2015 14:48:16
End Time: 17-SEP-2015 16:20:20

Wafer: MULTIPROBE/EP590205PH_G2TPS612351PA1V01/5017102/8-5423495-01
Probe Count: 2

TP M2XLT
AutoZ Planarity = 5um
Cleaning = 200x5
Yield = 67.7%
Fail Contributor – CONT and INTEGRITY tests



Probe Yield: 92.6% (19056/20574)
Net Yield: 92.6% (19055/20574)
Potential Good Die (NBR): 20574
Tested Die: 20514

1 GOOD 19056 (92.6%)
6 INTEGRITY 1346 (6.5%)
8 Continuity 56 (0.3%)
9 PinLeakage 16 (0.1%)
10 P2P_Leakage 37 (0.2%)
13 IQ 3 (0.0%)

* All percents based on NBR

Wafer Status: PASS
Facility: CLARK-PR
Device: G2TPS612351PA1
Tester: TT5036
Prober: PP3028
Probe Card: FU5P02
Operator: a0392039
Ref Die: 168,45
Start Time: 17-SEP-2015 16:55:14
End Time: 17-SEP-2015 18:34:52

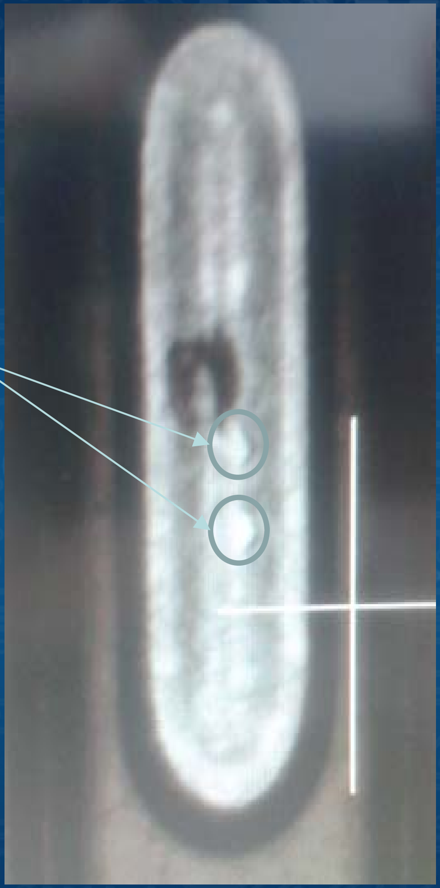
Wafer: MULTIPROBE/EP590205PH_G2TPS612351PA1V01/5017102/8-5423495-01
Probe Count: 1

TP M3XLT
AutoZ Planarity = 17um
Cleaning = 200x5
Yield = 92.6%

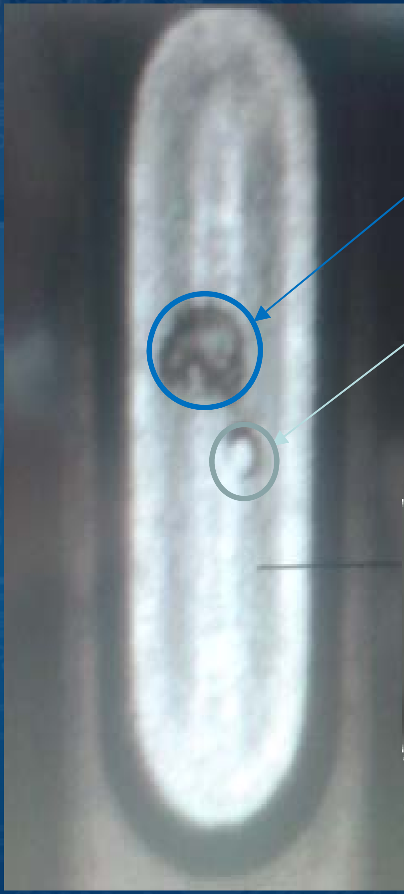
- Initially in Clark, TI tried to utilize the M2XLT as it was already qualified on pad.
- The data showed much better results on initial correlation for M3XLT when compared with M2XLT.

Example Technoprobe Probe Marks

M2 had light marks, multiple insertion is needed to make them visible.

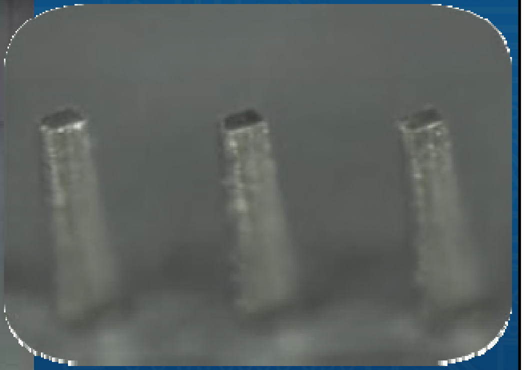


TP M2-XLT



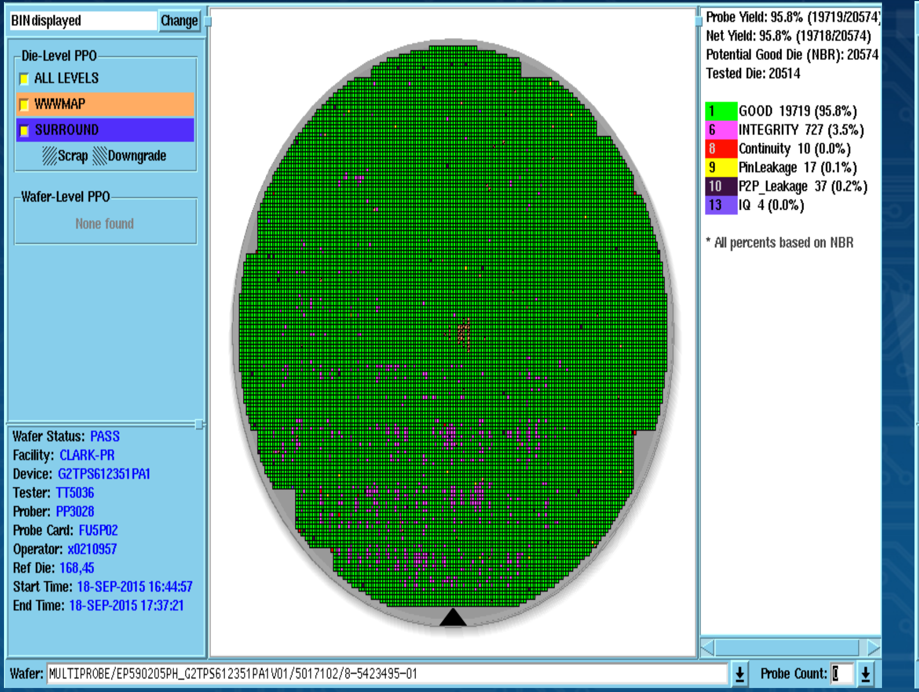
Cantilever probe mark

M3's marks are highly visible even on its first insertion



TP M3-XLT

TPS6xxx: Correlation Run – M3XLT vs Cantilever



Probe Yield: 95.8% (19719/20574)
Net Yield: 95.8% (19718/20574)
Potential Good Die (NBR): 20574
Tested Die: 20514

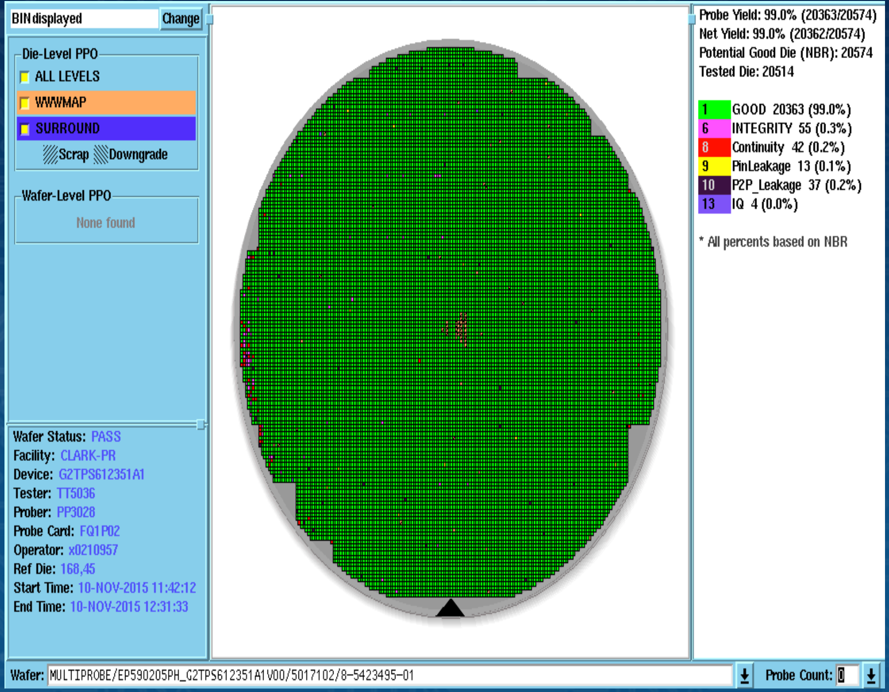
- 1 GOOD 19719 (95.8%)
- 6 INTEGRITY 727 (3.5%)
- 8 Continuity 10 (0.0%)
- 9 PinLeakage 17 (0.1%)
- 10 P2P_Leakage 37 (0.2%)
- 13 IQ 4 (0.0%)

* All percents based on NBR

Wafer Status: PASS
Facility: CLARK-PR
Device: G2TPS612351PA1
Tester: TT5036
Prober: PP3028
Probe Card: FU5P02
Operator: x0210957
Ref Die: 168,45
Start Time: 18-SEP-2015 16:44:57
End Time: 18-SEP-2015 17:37:21

Wafer: MULTIPROBE/EP590205PH_G2TPS612351PA1V01/5017102/8-5423495-01
Probe Count: 0

TP M2XLT
Cleaning = 50x5
Yield = 95.8%



Probe Yield: 99.0% (20363/20574)
Net Yield: 99.0% (20362/20574)
Potential Good Die (NBR): 20574
Tested Die: 20514

- 1 GOOD 20363 (99.0%)
- 6 INTEGRITY 55 (0.3%)
- 8 Continuity 42 (0.2%)
- 9 PinLeakage 13 (0.1%)
- 10 P2P_Leakage 37 (0.2%)
- 13 IQ 4 (0.0%)

* All percents based on NBR

Wafer Status: PASS
Facility: CLARK-PR
Device: G2TPS612351A1
Tester: TT5036
Prober: PP3028
Probe Card: FQ1P02
Operator: x0210957
Ref Die: 168,45
Start Time: 10-NOV-2015 11:42:12
End Time: 10-NOV-2015 12:31:33

Wafer: MULTIPROBE/EP590205PH_G2TPS612351A1V00/5017102/8-5423495-01
Probe Count: 0

Cantilever
Cleaning = 75x4
Yield = 99.0%

- **Next, the M3XLT was compared with the baseline cantilever technology.**
- **The cleaning interval was reduced from 200Td to 50Td.**
  - INTEGRITY test failure was greatly reduced from 6.5% to 3.5%
  - CONT test failure was reduced from 0.3% to 0.05%
- **Yield increased from 92.6% to 95.8% but is still not satisfactory compared with Cantilever (99%)**

EE0_READ1 Distribution

LSL: 0dB
USL: 85dB

Cantilever 75x4 cleaning

M2 200x5 cleaning

M3 50x5 cleaning

M3 200x5 cleaning

	FQ1P02	FU5P01	FU5P02	
	0	2	0	1
Avg	85.0679	82.9361	84.7547	84.414
Min	0	0	0	0
Max	247	255	255	255
StdDev	4.91454	37.0706	16.8267	22.7903
Count	20420	17124	20448	20403

Alpha level = 0.05
Root MSE = 22.705
sqrt(2)q* = 3.633

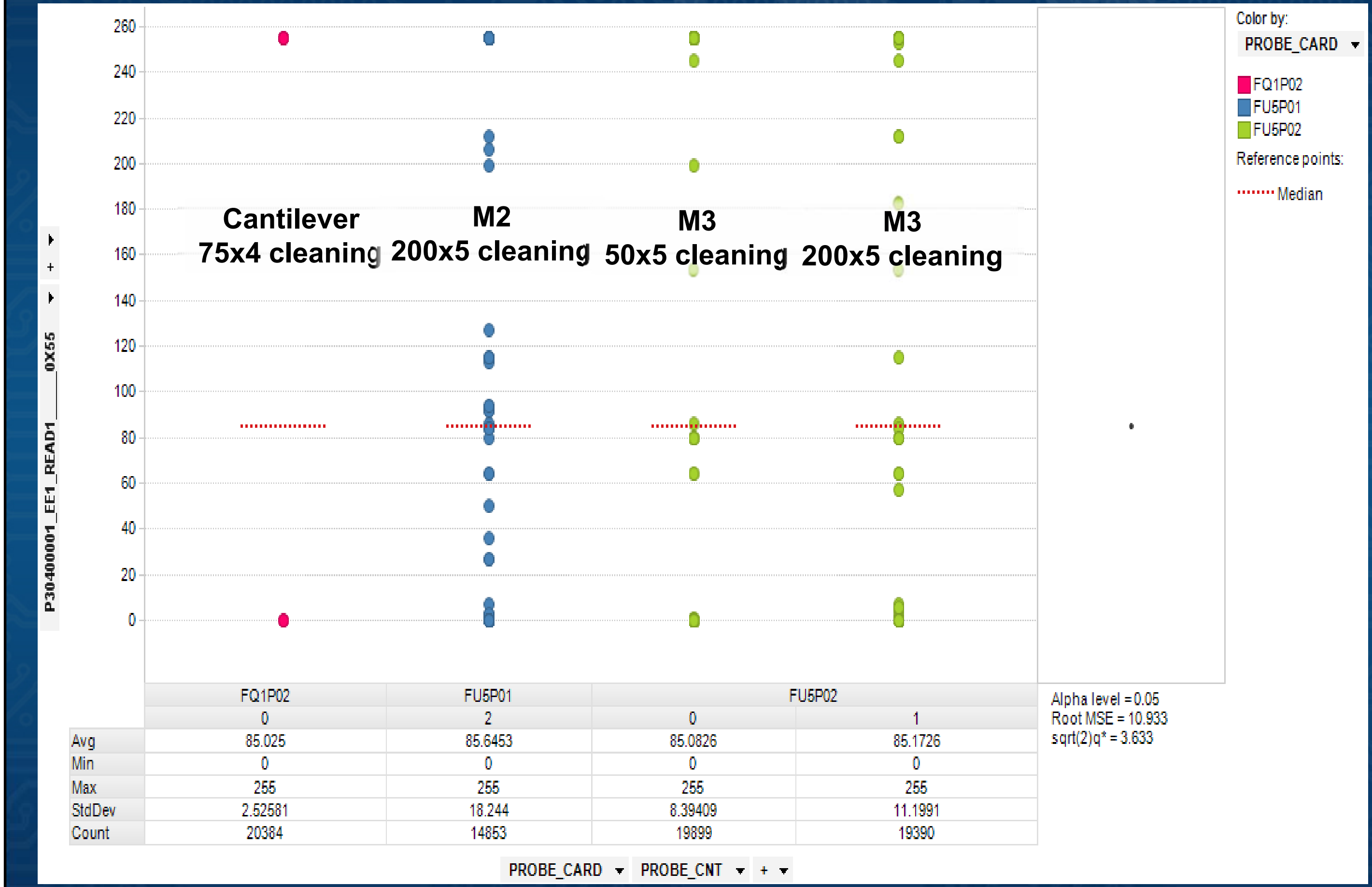
EEPROM Test distribution is much better on Cantilever.

M3 though had a better reading over M2 even when cleaning was still at 200 die interval.

Reduction of cleaning interval further improved M3's performance but it is still not comparable to baseline.

EE1_READ1 Distribution

LSL: 0dB
USL: 85dB



	FQ1P02	FU5P01	FU5P02	
	0	2	0	1
Avg	85.025	85.6453	85.0826	85.1726
Min	0	0	0	0
Max	255	255	255	255
StdDev	2.52581	18.244	8.39409	11.1991
Count	20384	14853	19899	19390

Alpha level = 0.05
Root MSE = 10.933
sqrt(2)q* = 3.633

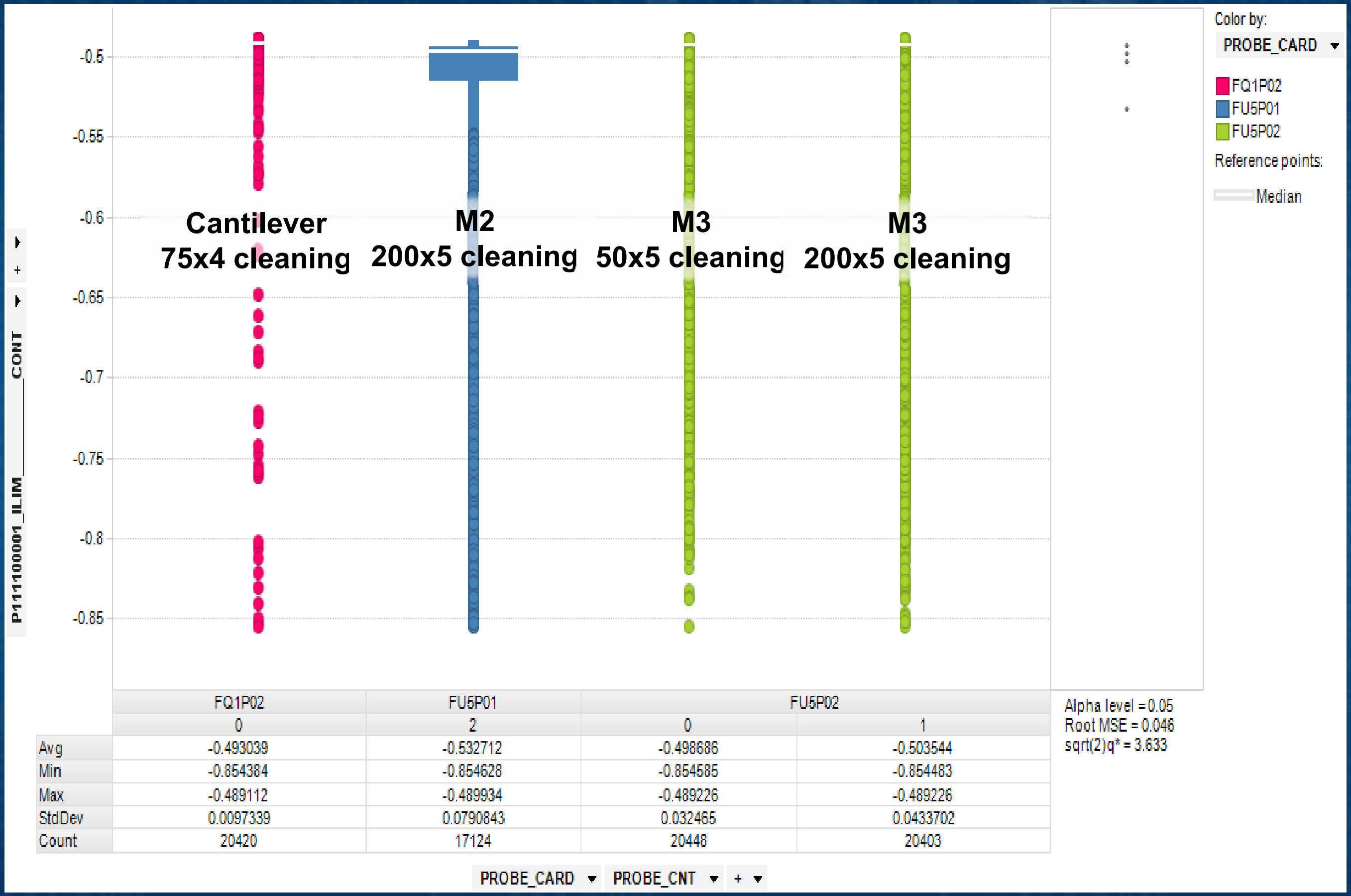
EEPROM Test distribution is much better on Cantilever.

M3 though had a better reading over M2 even when cleaning was still at 200 die interval.

Reduction of cleaning interval further improved M3's performance but it is still not comparable to baseline.

ILIM (CONT) Distribution

LSL: -0.9V
USL: -0.1V



	FQ1P02	FU5P01	FU5P02	
	0	2	0	1
Avg	-0.493039	-0.532712	-0.498686	-0.503544
Min	-0.854384	-0.854628	-0.854585	-0.854483
Max	-0.489112	-0.489934	-0.489226	-0.489226
StdDev	0.0097339	0.0790843	0.032465	0.0433702
Count	20420	17124	20448	20403

Alpha level = 0.05
Root MSE = 0.046
sqrt(2)q* = 3.633

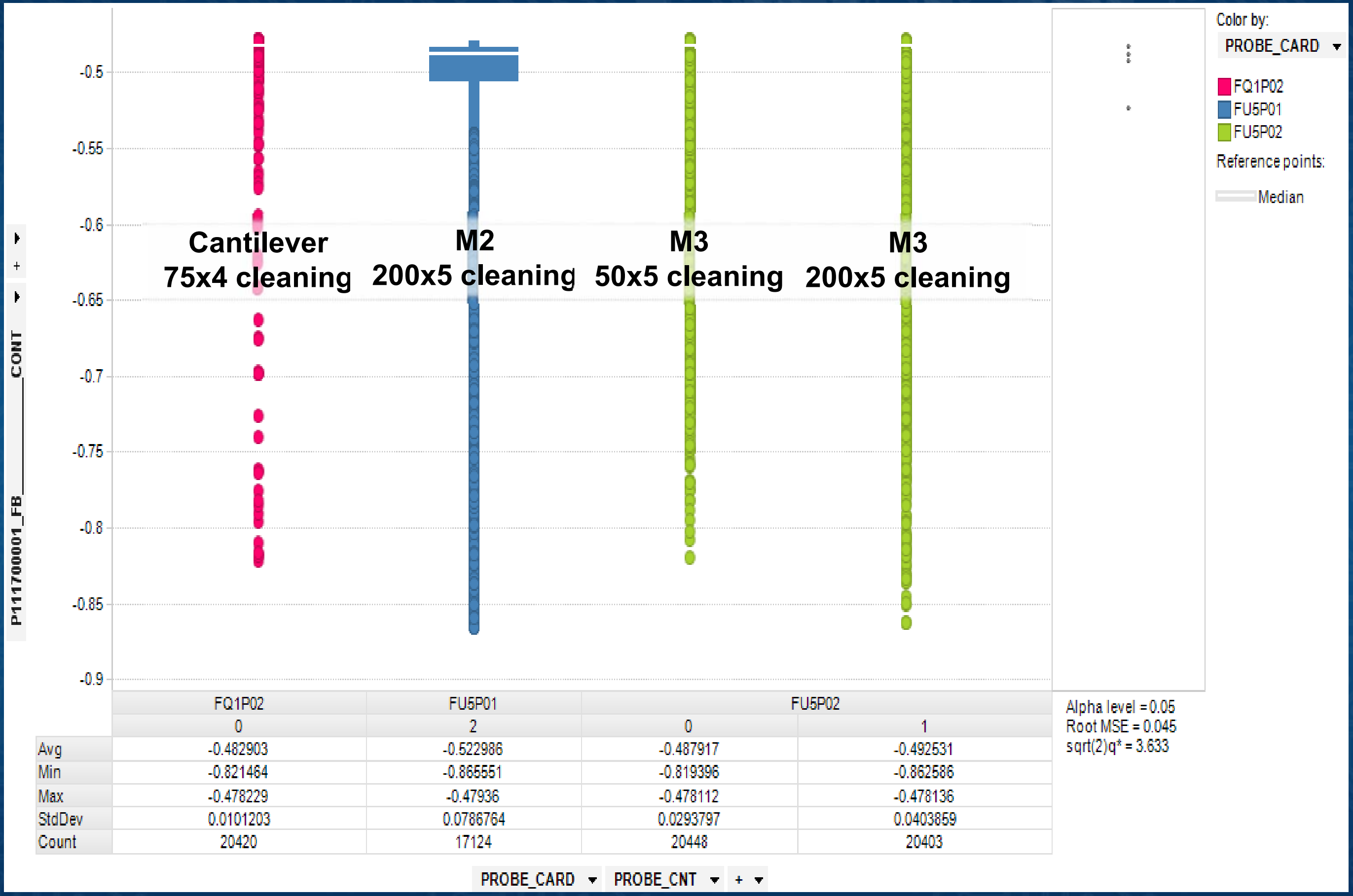
CONT Test distribution is much better on Cantilever.

M3 though had a better reading over M2 even when cleaning was still at 200 die interval.

Reduction of cleaning interval further improved M3's performance but it is still not comparable to baseline.

FB (CONT) Distribution

LSL: -0.9V
USL: -0.2V



Cantilever 75x4 cleaning

M2 200x5 cleaning

M3 50x5 cleaning

M3 200x5 cleaning

	FQ1P02	FU5P01	FU5P02	
	0	2	0	1
Avg	-0.482903	-0.522986	-0.487917	-0.492531
Min	-0.821464	-0.865551	-0.819396	-0.862586
Max	-0.478229	-0.47936	-0.478112	-0.478136
StdDev	0.0101203	0.0786764	0.0293797	0.0403859
Count	20420	17124	20448	20403

Alpha level = 0.05
Root MSE = 0.045
sqrt(2)q* = 3.633

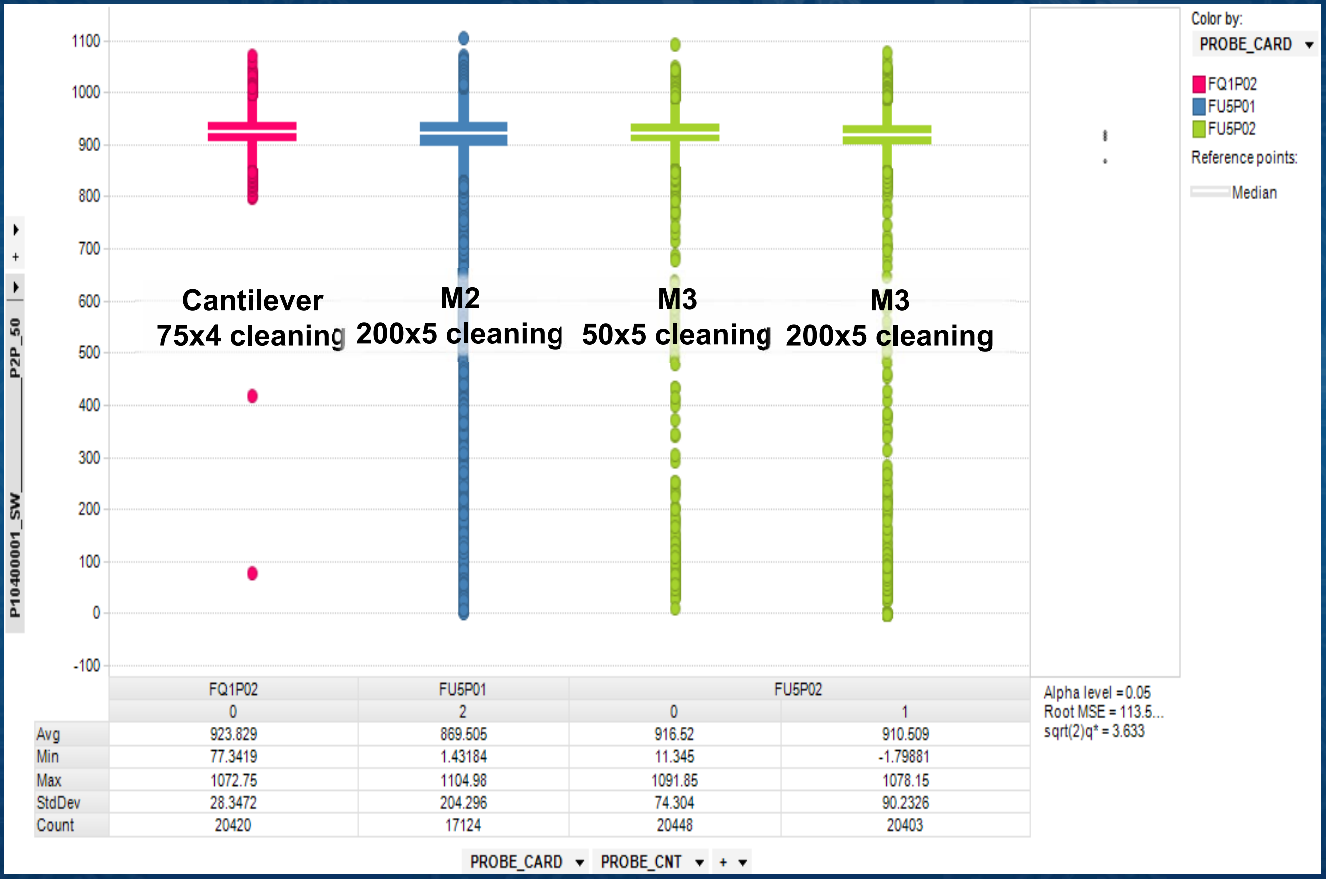
CONT Test distribution is much better on Cantilever.

M3 though had a better reading over M2 even when cleaning was still at 200 die interval.

Reduction of cleaning interval further improved M3's performance but it is still not comparable to baseline.

SW (P2P) Distribution

LSL: 300nA
USL: 2000nA



	FQ1P02	FU5P01	FU5P02	
	0	2	0	1
Avg	923.829	869.505	916.52	910.509
Min	77.3419	1.43184	11.345	-1.79881
Max	1072.75	1104.98	1091.85	1078.15
StdDev	28.3472	204.296	74.304	90.2326
Count	20420	17124	20448	20403

Alpha level = 0.05
Root MSE = 113.5...
sqrt(2)q* = 3.633

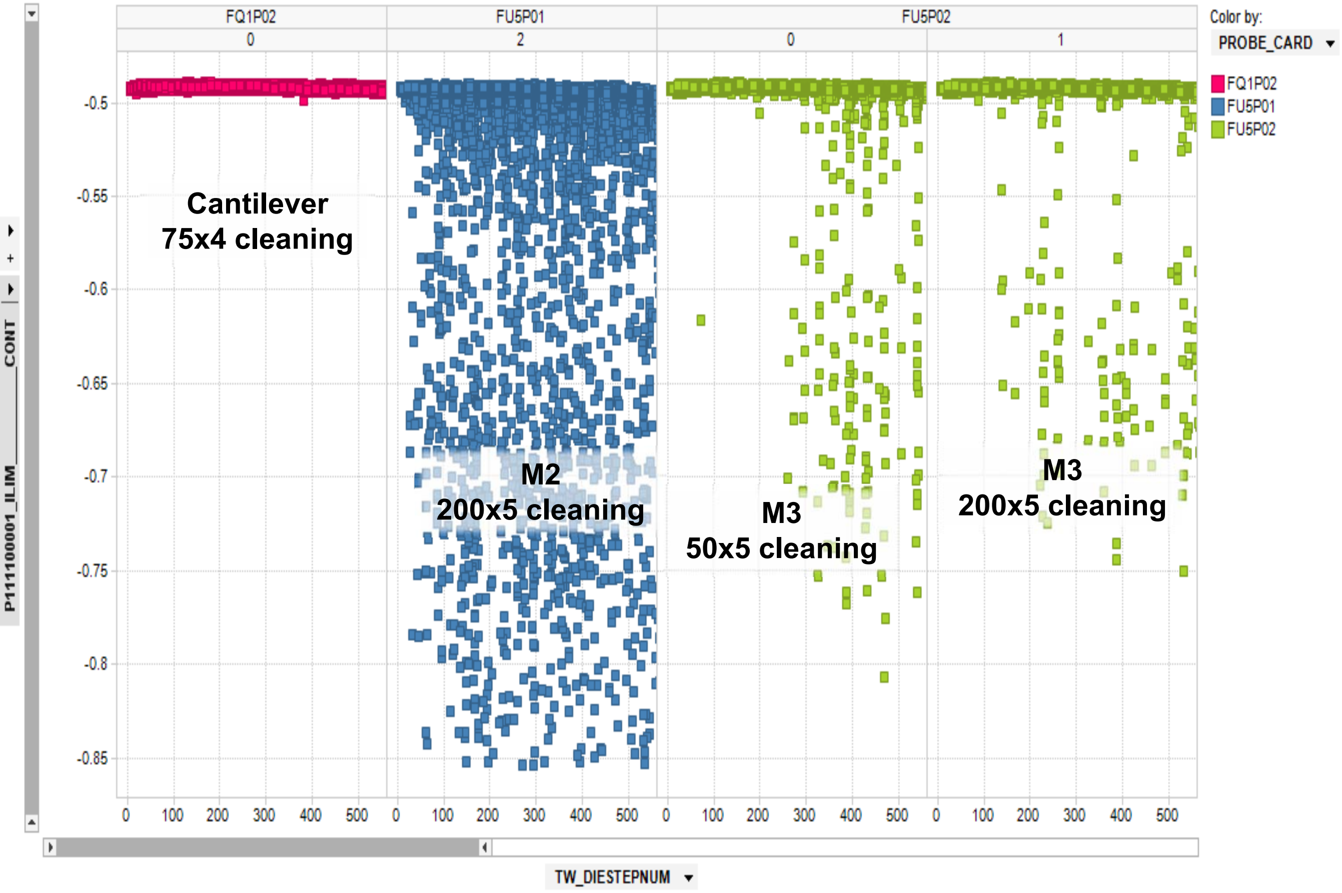
P2P Test distribution is much better on Cantilever.

M3 though had a better reading over M2 even when cleaning was still at 200 die interval.

Reduction of cleaning interval further improved M3's performance but it is still not comparable to baseline.

Readings vs TD (ILIM_CONT)

LSL: -0.9V
USL: -0.1V



Cantilever 75x4 cleaning

M2 200x5 cleaning

M3 50x5 cleaning

M3 200x5 cleaning

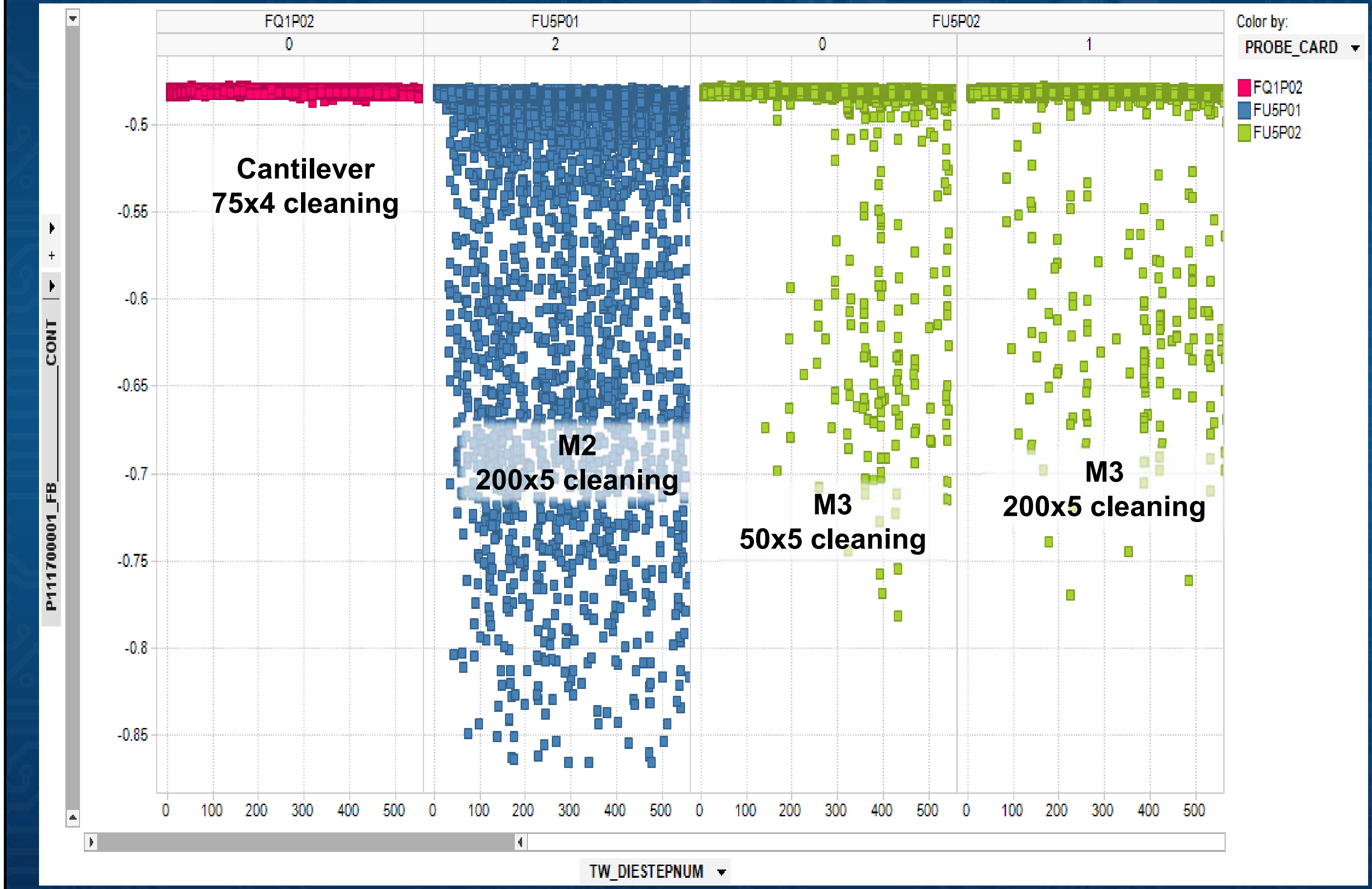
Cantilever is consistent all through out its TD.

M2 had not reached the 200 die mark before it started to get worst.

M3 had some outliers before the 1st cleaning mark and it is getting worst as TD accumulates.

Readings vs TD (FB_CONT)

LSL: -0.9V
USL: -0.2V



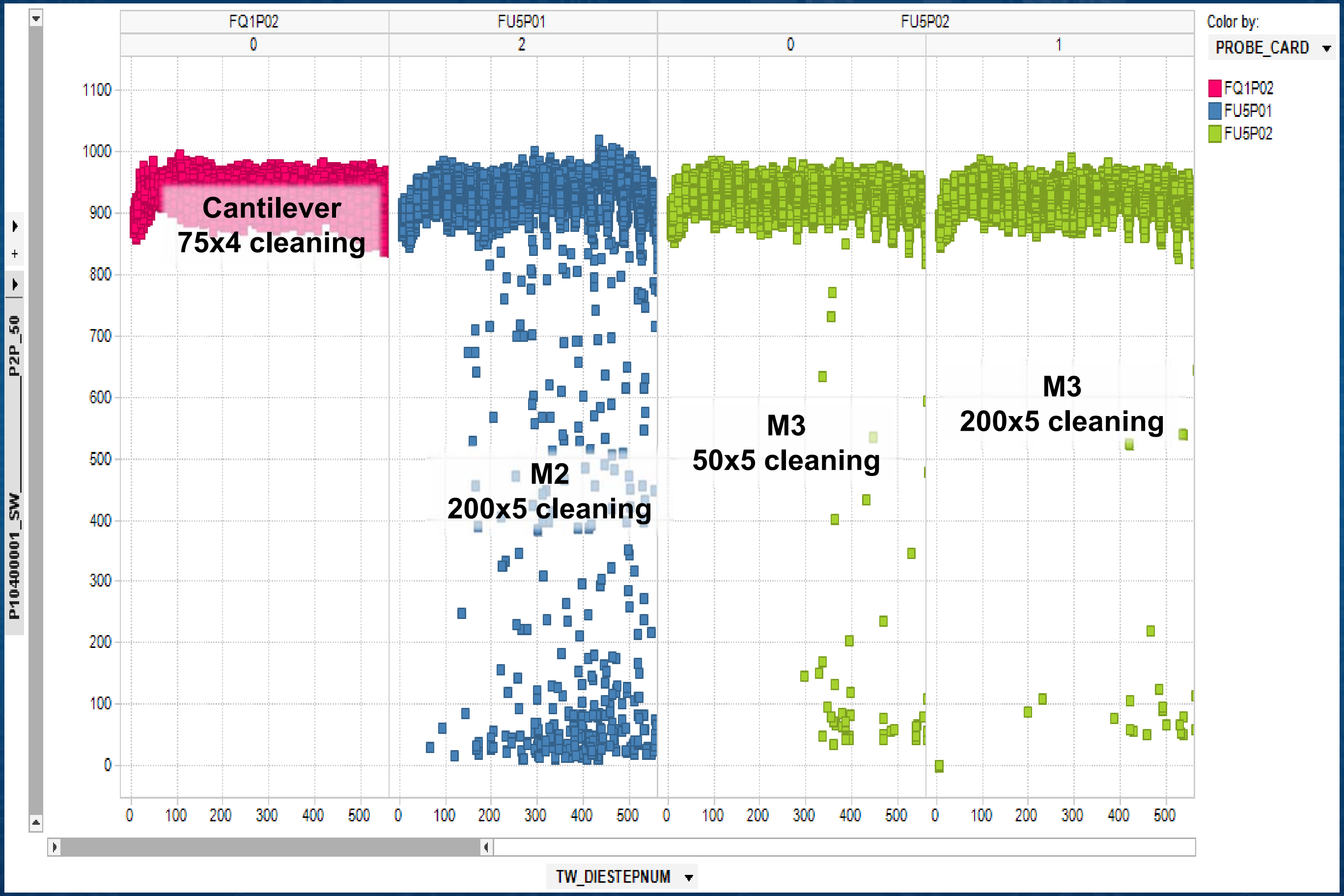
Cantilever is consistent all through out its TD.

M2 had not reached the 200 die mark before readings started to get worst.

M3 had some outliers and it is getting worst as TD accumulates but not as bad as M2. Cleaning interval reduction also minimized the number of outliers.

Readings vs TD (SW_P2P)

LSL: 300nA
USL: 2000nA



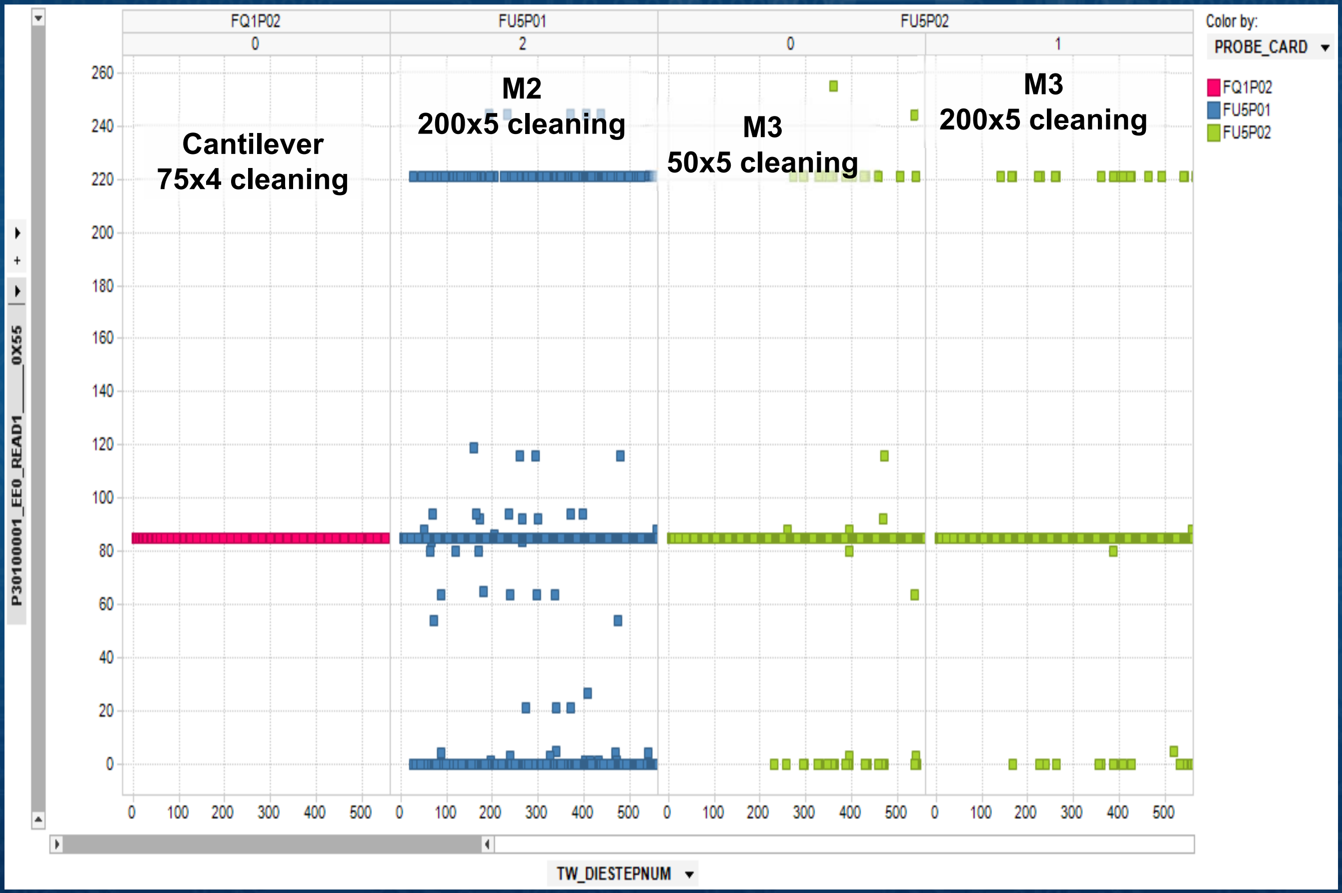
Cantilever is consistent all through out its TD.

M2 had not reached the 200 die mark for cleaning before it started to get worst.

M3 had some outliers and it is getting worst as TD accumulates. Cleaning interval reduction also minimized the number of outliers.

Readings vs TD (EE0_READ1)

LSL: 0dB
USL: 85dB



Cantilever 75x4 cleaning

M2 200x5 cleaning

M3 50x5 cleaning

M3 200x5 cleaning

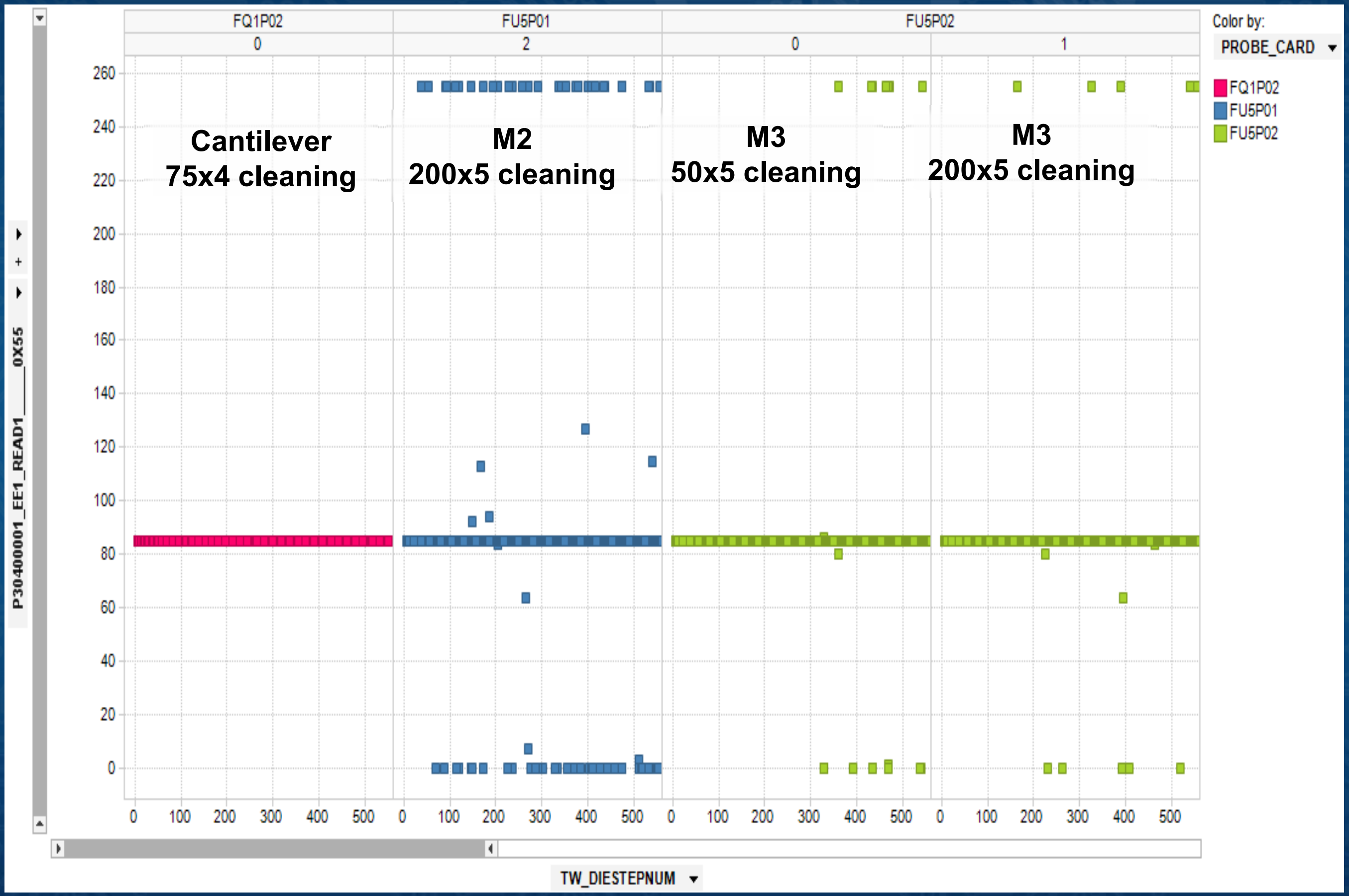
Cantilever is consistent all through out its TD.

M2 had not reached the 200 die mark for cleaning before it started to get worst.

M3 had some outliers and it is getting worst as TD accumulates. Cleaning interval reduction also minimized the number of outliers.

Readings vs TD (EE1_READ1)

LSL: 0dB
USL: 85dB



Cantilever is consistent all through out its TD.

M2 had not reached the 200 die mark for cleaning before it started to get worst.

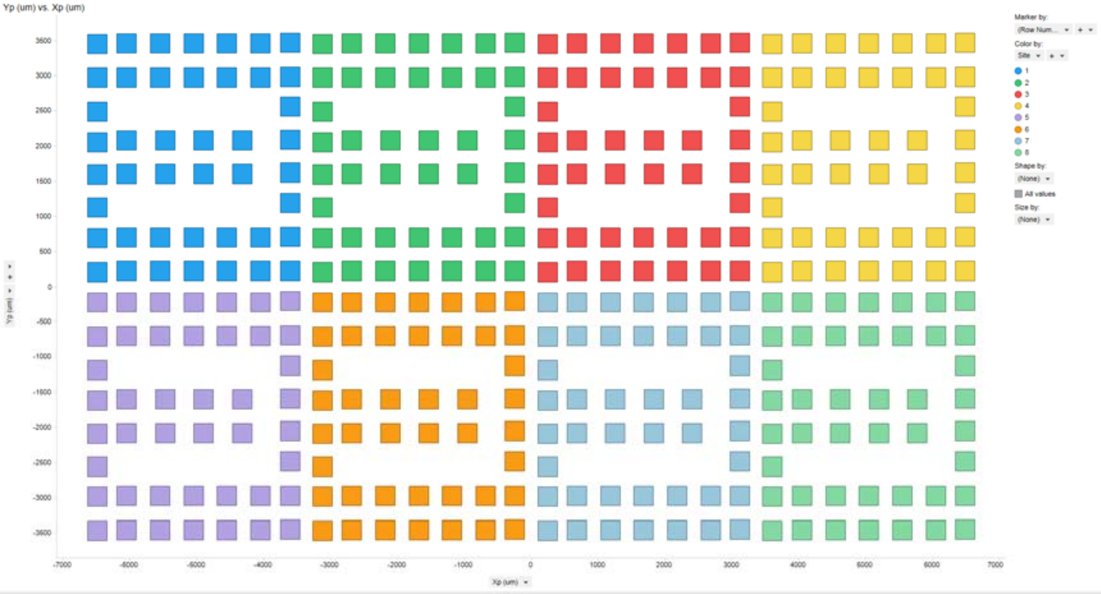
M3 had some outliers and it is getting worst as TD accumulates. Cleaning interval reduction also minimized the number of outliers.

TPS6xxx Summary

- Higher BCF vertical solution (M3XLT) had better contact on Cu Pillar pads which can be observed on its probe marks and smaller failure rate for BIN6/8.
- M3XLT's electrical performance is better than M2XLT.
- Cantilever (baseline) is still better compared to the Vertical solutions in terms of yield and test distribution
- Changing cleaning parameters had positive impact to minimize electrical fails but the overall performance is still not comparable to baseline (Cantilever)
- Optimizing probing / cleaning settings to improve yield and electrical performance.

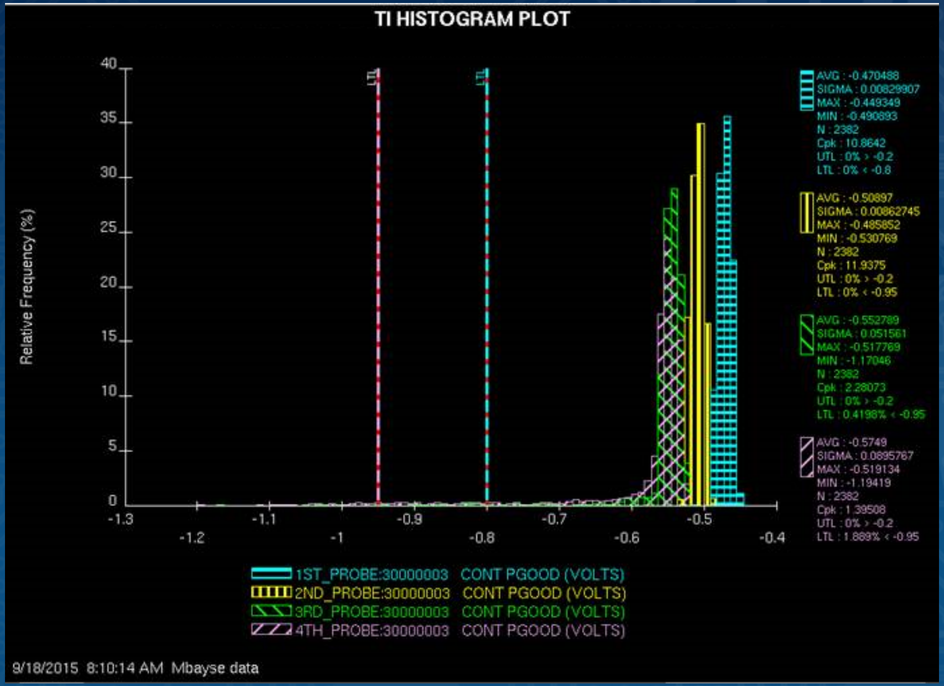
LP8xxx: Device Parameters and Test Cell Configuration

Device Parameters	
Silicon Node	LBC8-HV
Testing Temp	30oC
Pillar Metallurgy	Cu
Pillar Dimensions	90x90um diam.
Min Pitch	500um
Current	100mA
Bandwidth	10mHz
# Probes / Site	44
# of Sites	8
Total # Probes	352
Tester	ETS-364 Razorback
Prober	EG4090



Example of device array layout pattern.

LP8xxx: Initial Cantilever Data



	Insertion	Continuity (Opens)	Continuity (Shorts)	Comments
1	MP1	1.57%	2.03%	
2	MP1	1.49%	2.03%	Effectively no change from first probe insertion
3	MP2 (Bake)	7.95%	2.07%	Continuity open yield loss increases – not sure if related to bake or continued probe insertions.
4	MP2 (Bake)	56.09%	1.74%	Continuity open yield loss significantly increases – not sure if related to bake or continued probe insertions. Probed 2 days after probe insertion #3 (approximately 7 days after bake).

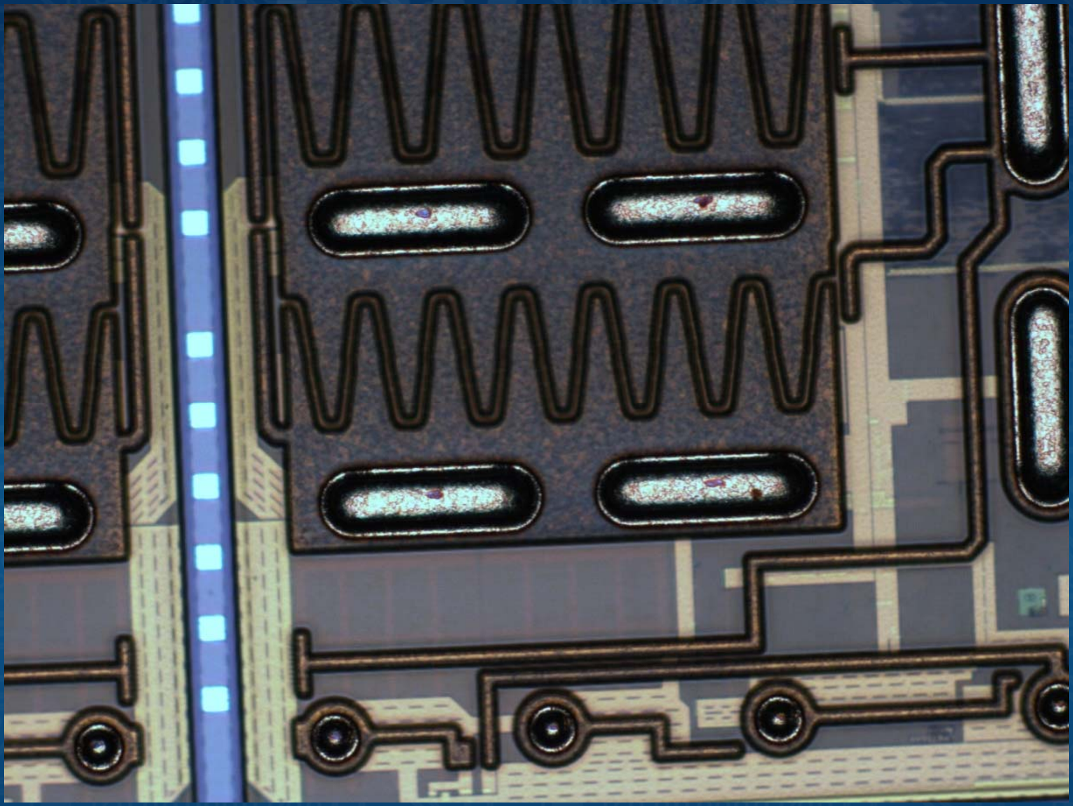
- **Cantilever was the baseline probe card technology for this device.**
- **Table above shows the difference in continuity failures between prebake and post bake.**
    - Large increase in open failures after bake. The current should go down from prebake. Result show~~n~~ current went up 1uA post bake.
    - Wafer was probed 4 more times post bake and opens were seen ~6-8% on each run.
- **TI decided to evaluate Technoprobe’s M3XLT technology here to see if could help improve on these contact related failures.**

LP8xxx: Cantilever results with Bake

Probe #	Continuity (Opens)	Comments
1	6.96%	
2	5.95%	
3	8.2%	(Increased failures due to tips getting dirty. After clean similar results)
4	6.59%	

- Initial cantilever results showed the increase after bake, a wafer was probed 4 times without bake to compare results.
- Data shows clearly that there are contact issues when adding bake with cantilever.

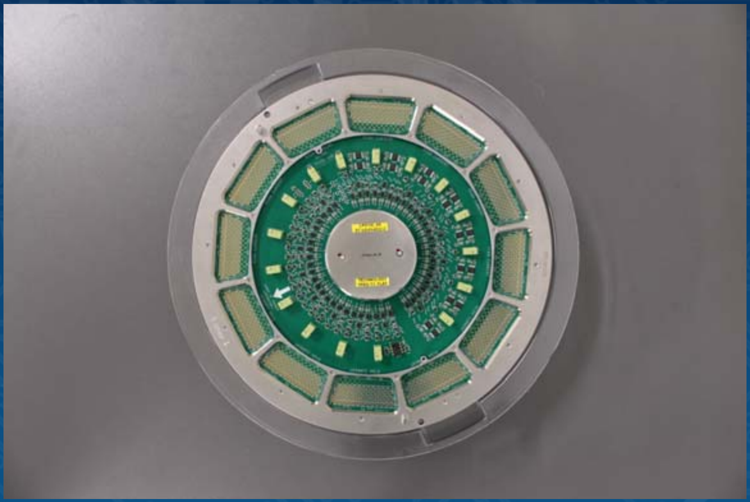
LP8xxx Cantilever Probe Marks



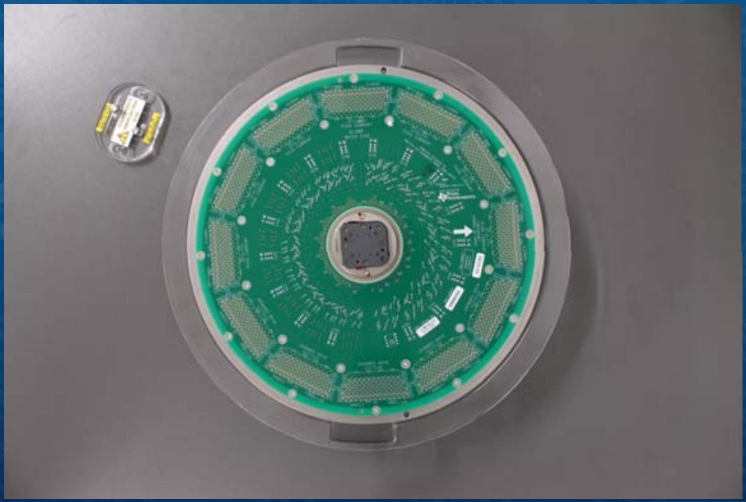
- **Cantilever marks after multiple passes on the device.**

LP8xxx: Technoprobe M3 Head

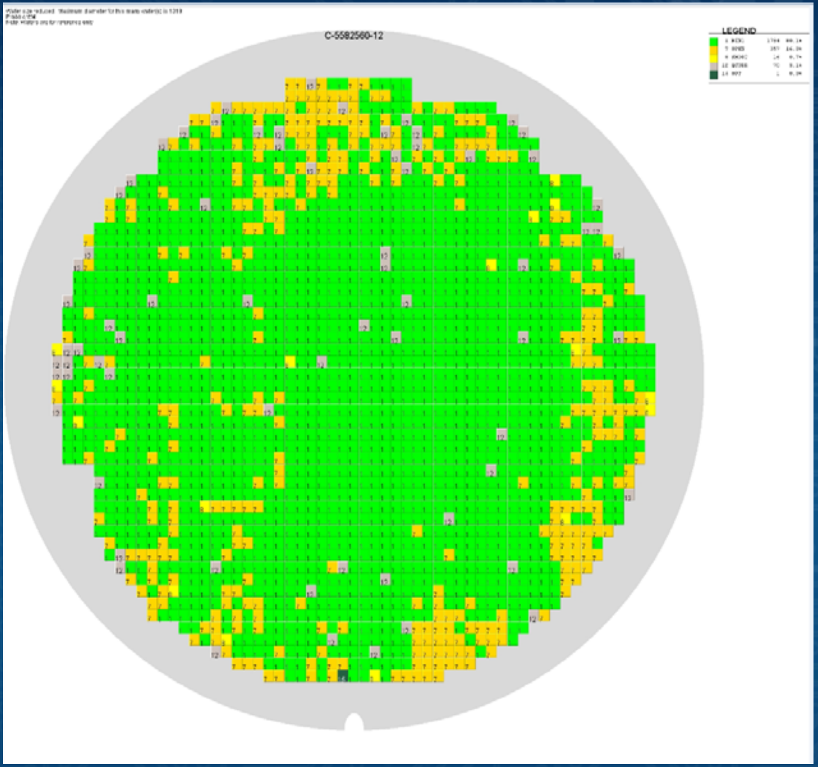
Tester Side

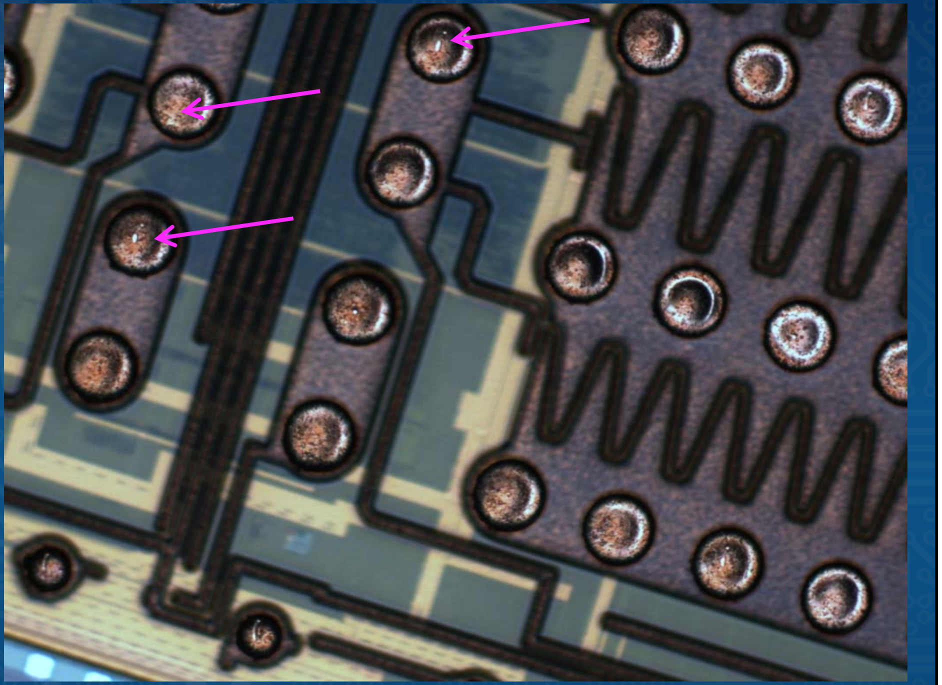


DUT Side



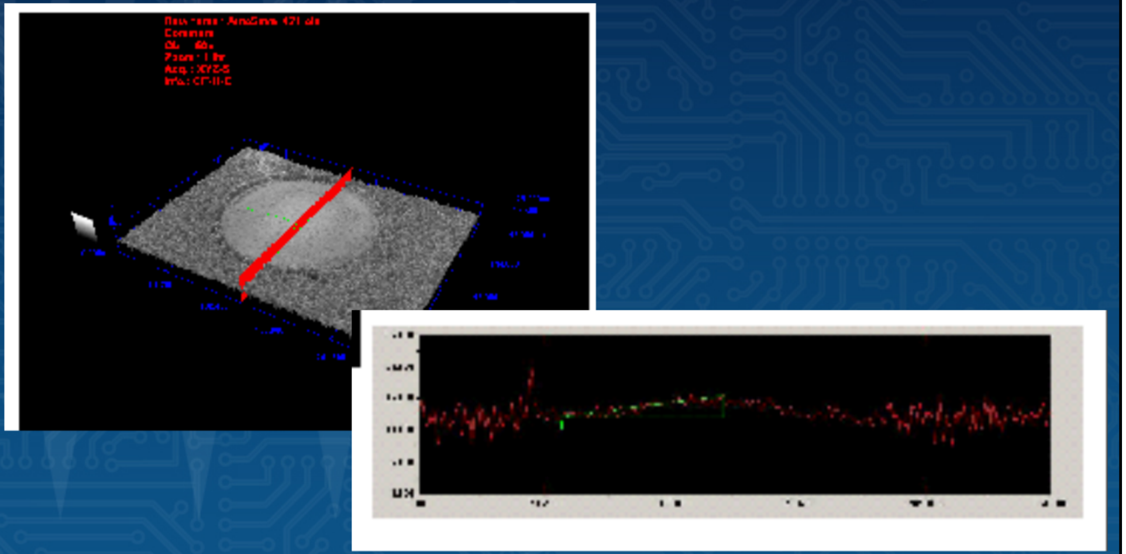
LP8xxx: Initial M3XLT Results on wafer Prebake





- **Initial results using the M3XLT showed a large number of open failures (16.1%) on prebake wafer using radiused 9um tip.**
- **The photo of the probe indicate pin is sliding on pillar.**

LP8xxx: Analysis of Cu Pillar Feature



- Cu pillars are raised ~3um in center.
- Pins sliding on curvature of the pillars.
- Technoprobe’s pin uses a radiused tip causing pin to slide on curvature of the pillar.
- Moving to a flat tip to prevent this.

Technoprobe M3 Open Issues

- **The increased opens found when probing with the 9um radiused tip caused sliding on the Cu pillar.**
  - Based upon the initial results, Cantilever was seeing ~1-2% opens pre bake and ~7% post bake.
  - The TP M3XLT card was seeing ~16% opens prebake.
  - The Cu pillars being probed had a slight curvature towards the center of the pillar. The pin was sliding as it hit this curvature.
- **The tip was increased to 18um and flattened to reduce the opens down to ~9.4% prebake.**
  - Probed wafers indicated correlation between over travel and open failures.
  - The higher the OT the more the pin slide creating failures.

LP8xxx: Overview of TP Tip Changes

Technology	Tip Shape	Tip Diam	Cleaning Pattern
M3XLT	Radiused	9um	Z up
M3XLT	Flat	18um	Octagon
M3XLT	Flat	40x55um	Octagon
M3 w/ Hard Tip	Flat	40x55um	X Only

- **The data from the 18um flat tip showed correlation between the OT and Tip diameter**
  - The 18um tip was still sliding if OT applied
  - Confirmed the results showed better results with lower OT.
- **Technoprobe chose to move to a bigger diameter 40x55 flat tip to reduce sliding and open failures.**
  - Cleaning settings were looked at as a possible source for improvement

LP8xxx: 40x55um Probe Matrix

	Tip	OT	Open Failures	Cleaning	Logpoint	Double Touch
1	40x55um		33%	Octagon	Prebake	
2	40x55um	4mil	1.34%	X only	Postbake	Yes
	40x55um	4.5mil	1.43%	X only	Postbake	No
	40x55um	4mil	1.8%	X only	Postbake	Yes
3	40x55um	4mil	0.49%.	X only	Prebake	No
	40x55um	2.7mil	0.5%	X only	Prebake	No
4	40x55um	3.5mil	1.05%	X only	Postbake	No
5	40x55um	4mil	0.7%	X only	Postbake	No

- **Initial results increased open failures with the 40x55um flat tip, but as over travel and cleaning were optimized, results improved.**

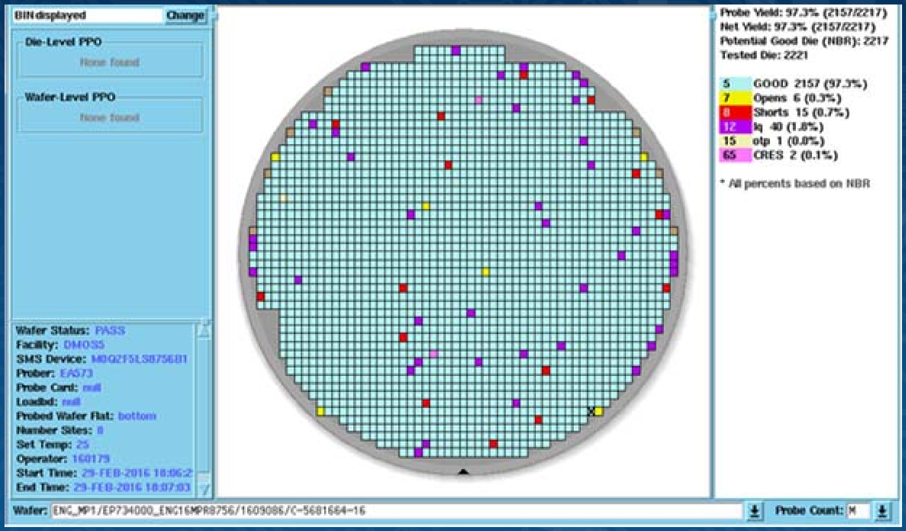
LP8xxx: Optimized Probe / Clean Settings

	Category	AVPC
Probe Tech	Vendor	TP
	Specific	M3 w/ hard tip
Probe OT Method	FT/LT	FT
Probe OT	(µm)	100
Cleaning Media	(Material)	3M
Clean Freq	(PTd)	60
Clean OT	(µm)	40
Clean Tds	(CTd)	1
Clean Step Input	(µm)	500
Clean Pattern	(shape)	X only
Cleaning Step Distance	(µm)	70
Cleaning block Rotations	#	20
Planarity Spec	um	25

- Prober
  - EG4090 plus
  - EGC9.5.x
  - Optical profiler Using FT (CPCS)
- Probe card:
  - Technoprobe (TP) TPEG M3 HC2 with hard tip
- Probing
  - OT set by operator
    - Pre-bake: 3 to 3.5 mils
    - Bake: 3.5 to 4 mils
- Cleaning - set by EG Product file
- Auto Probe
  - non-Testware
  - Testware
    - for AUTO Z

- **The optimized cleaning recipe for Technoprobe M3 w/ hard tip.**

LP8xxx: Yield after Optimized Settings



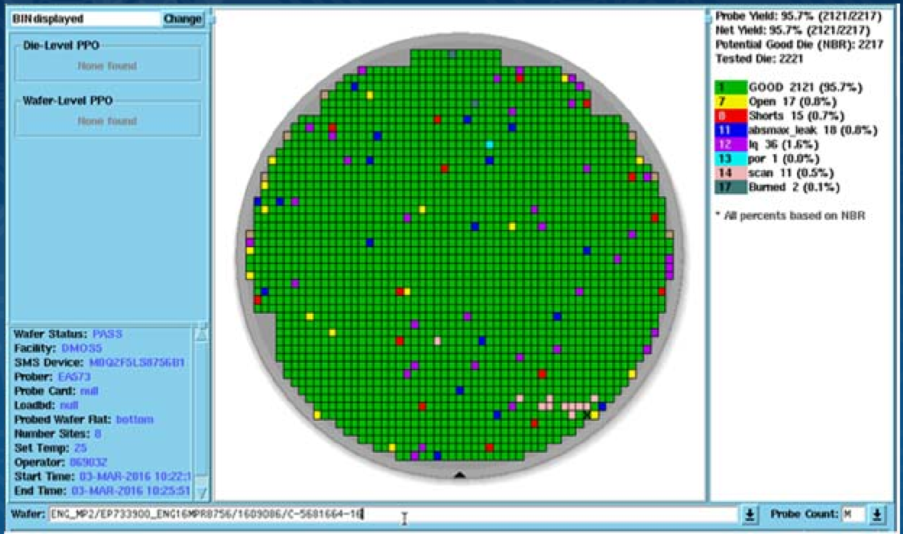
Probe Yield: 97.3% (2157/2217)
Net Yield: 97.3% (2157/2217)
Potential Good Die (NBR): 2217
Tested Die: 2221

5	GOOD 2157 (97.3%)
7	Opens 6 (0.3%)
8	Shorts 15 (0.7%)
12	Iq 40 (1.8%)
15	otp 1 (0.0%)
65	CRES 2 (0.1%)

* All percents based on NBR

Wafer Status: PASS
Facility: DMOS5
SMS Device: MDQ2F5LS8756B1
Prober: EA573
Probe Card: null
Loadbd: null
Probed Wafer Flat: bottom
Number Sites: 8
Set Temp: 25
Operator: 160179
Start Time: 29-FEB-2016 18:06:2
End Time: 29-FEB-2016 18:07:03

Wafer: ENG_MP1/EP734000_ENG16MPR8756/1609086/C-5681664-16



Probe Yield: 95.7% (2121/2217)
Net Yield: 95.7% (2121/2217)
Potential Good Die (NBR): 2217
Tested Die: 2221

1	GOOD 2121 (95.7%)
7	Open 17 (0.8%)
8	Shorts 15 (0.7%)
11	absmax_leak 18 (0.8%)
12	Iq 36 (1.6%)
13	por 1 (0.0%)
14	scan 11 (0.5%)
17	Burned 2 (0.1%)

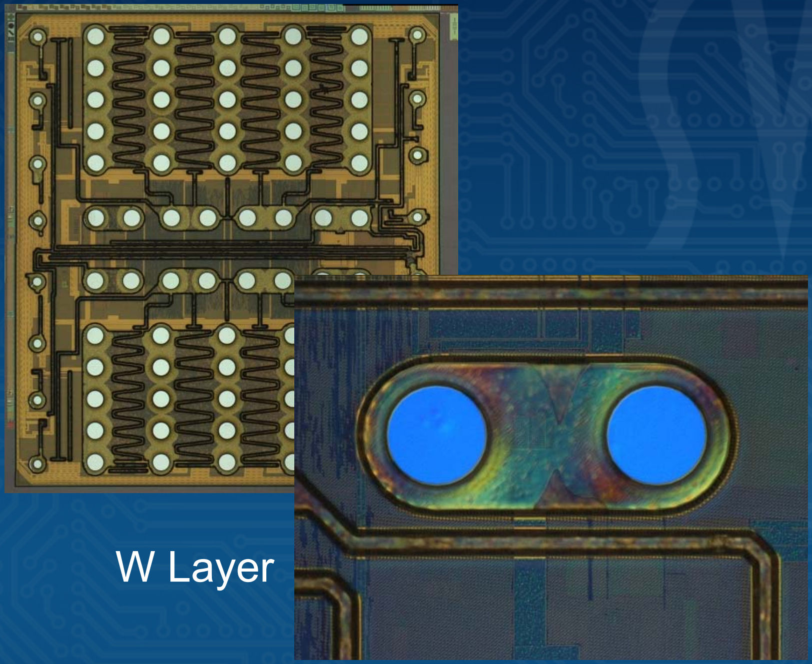
* All percents based on NBR

Wafer Status: PASS
Facility: DMOS5
SMS Device: MDQ2F5LS8756B1
Prober: EA573
Probe Card: null
Loadbd: null
Probed Wafer Flat: bottom
Number Sites: 8
Set Temp: 25
Operator: 069032
Start Time: 03-MAR-2016 10:22:1
End Time: 03-MAR-2016 10:25:51

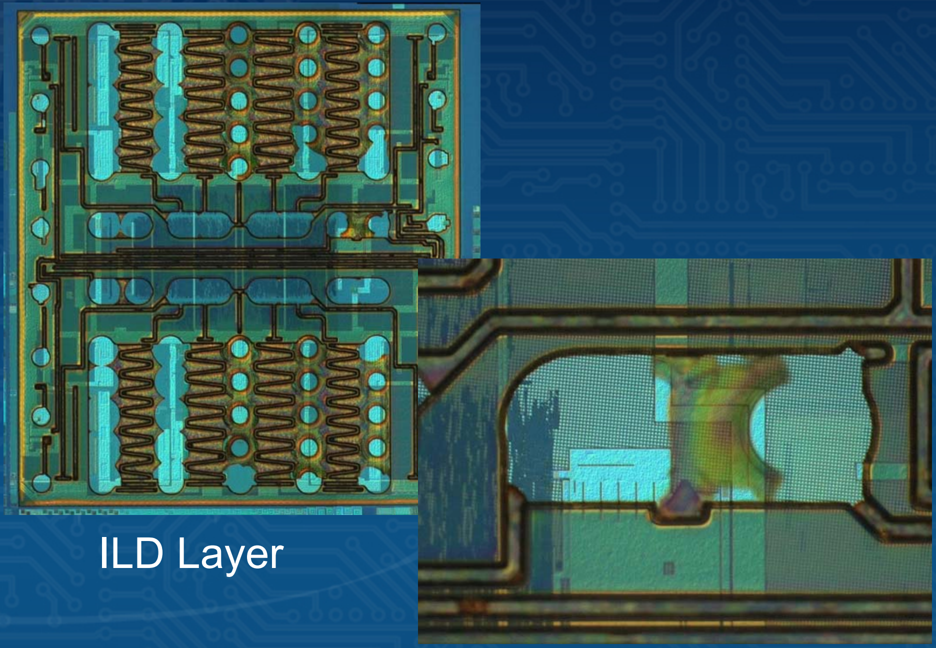
Wafer: ENG_MP2/EP733900_ENG16MPR8756/1609086/C-5681664-16

- Wafer probed both prebake and postbake with the optimized settings.
- Wafer yield >95% on both cases with less than 1% open failures.

LP8xxx: Diecracking Results



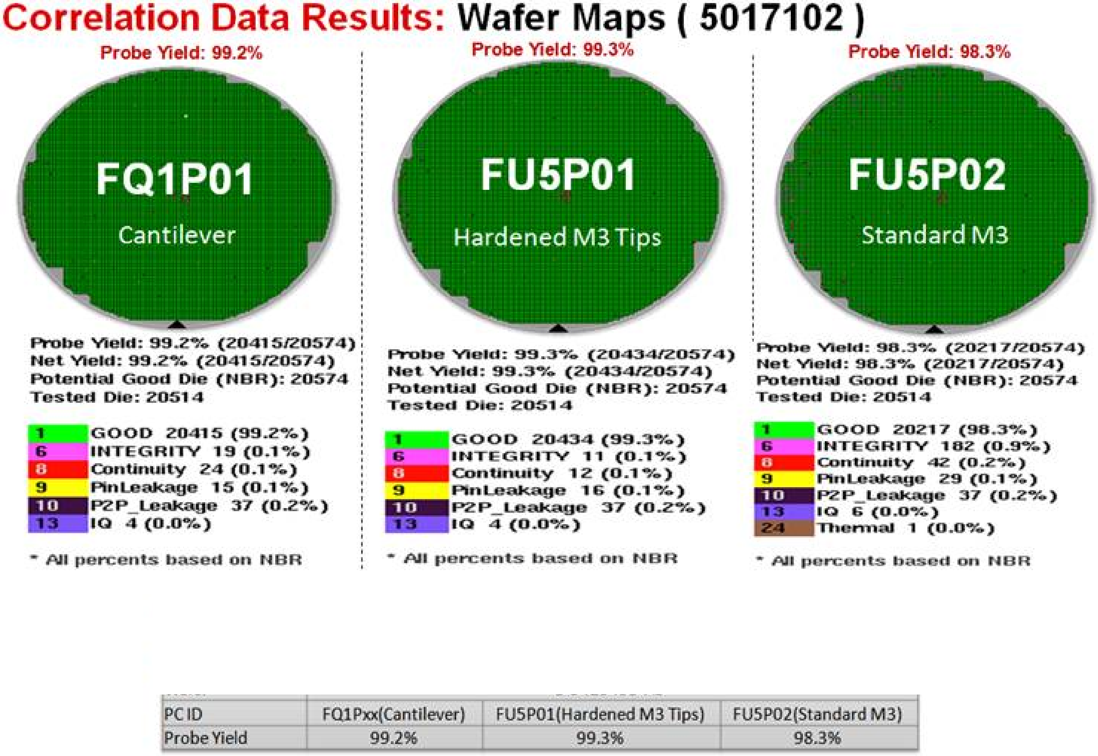
W Layer



ILD Layer

- To ensure that no reliability issues induced by probe, dielectric cracking studies were performed.
- Several LP8xxx devices were probed 10 times with maximum over-travel. 2 devices were selected from center and edge of wafere wafer to perform de-processing at the pads using Nomarski filter inspection to check for any ILD cracks.
- An optical microscope was inspected at the all pads on W and ILD layer and observed no cracks at both W and ILD layer on all 4 devices.

Other Device Yield Improvement



Correlation Data Results: Wafer Maps (5017102)

Probe Yield: 99.2%

FQ1P01

Cantilever

Probe Yield: 99.2% (20415/20574)
Net Yield: 99.2% (20415/20574)
Potential Good Die (NBR): 20574
Tested Die: 20514

Bin	Result
1	GOOD 20415 (99.2%)
6	INTEGRITY 19 (0.1%)
8	Continuity 24 (0.1%)
9	PinLeakage 15 (0.1%)
10	P2P_Leakage 37 (0.2%)
13	IQ 4 (0.0%)

* All percents based on NBR

Probe Yield: 99.3%

FU5P01

Hardened M3 Tips

Probe Yield: 99.3% (20434/20574)
Net Yield: 99.3% (20434/20574)
Potential Good Die (NBR): 20574
Tested Die: 20514

Bin	Result
1	GOOD 20434 (99.3%)
6	INTEGRITY 11 (0.1%)
8	Continuity 12 (0.1%)
9	PinLeakage 16 (0.1%)
10	P2P_Leakage 37 (0.2%)
13	IQ 4 (0.0%)

* All percents based on NBR

Probe Yield: 98.3%

FU5P02

Standard M3

Probe Yield: 98.3% (20217/20574)
Net Yield: 98.3% (20217/20574)
Potential Good Die (NBR): 20574
Tested Die: 20514

Bin	Result
1	GOOD 20217 (98.3%)
6	INTEGRITY 182 (0.9%)
8	Continuity 42 (0.2%)
9	PinLeakage 29 (0.1%)
10	P2P_Leakage 37 (0.2%)
13	IQ 6 (0.0%)
24	Thermal 1 (0.0%)

* All percents based on NBR

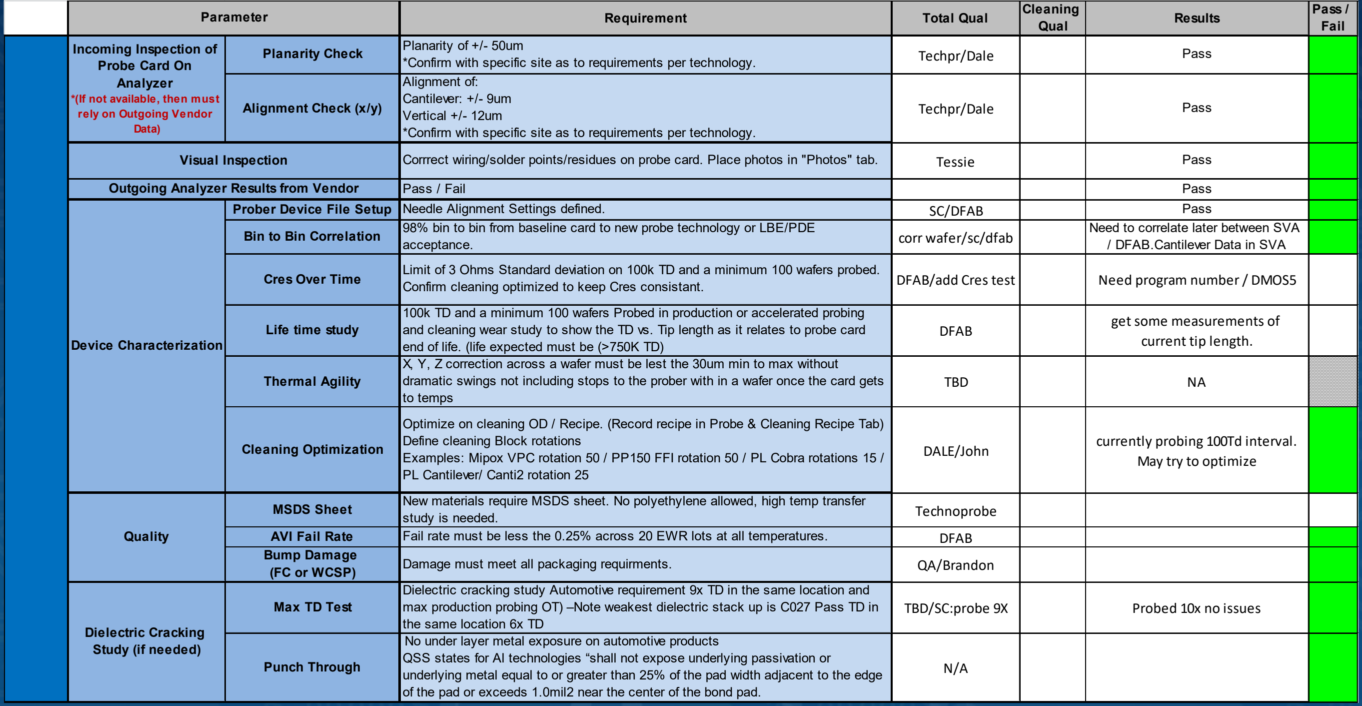
PC ID	FQ1Pxx(Cantilever)	FU5P01(Hardened M3 Tips)	FU5P02(Standard M3)
Probe Yield	99.2%	99.3%	98.3%

- **Device in TI Clark showed yield improvement when using Technoprobe M3 with hard tip.**

Lessons Learned

- **In developing the Technoprobe M3 vertical solution on Cu pillar, issues that had to be addressed:**
  - Continuity failures
    - Different tip shapes on the Cu pillar surface
    - Pins were sliding on the bare Cu Pillar
    - The Tip was changed to a flat 40x55um tip w/ hard material
  - Cleaning Setting Optimization
    - Optimize the probing and cleaning
- **Key factors for Cu Pillar**
  - Tip Shape
  - Cleaning Settings
    - Overtravel
    - # Clean

Next Steps



	Parameter		Requirement	Total Qual	Cleaning Qual	Results	Pass / Fail
	Incoming Inspection of Probe Card On Analyzer *(If not available, then must rely on Outgoing Vendor Data)	Planarity Check	Planarity of +/- 50um *Confirm with specific site as to requirements per technology.	Techpr/Dale		Pass	🟩
		Alignment Check (x/y)	Alignment of: Cantilever: +/- 9um Vertical +/- 12um *Confirm with specific site as to requirements per technology.	Techpr/Dale		Pass	🟩
	Visual Inspection		Corrrect wiring/solder points/residues on probe card. Place photos in "Photos" tab.	Tessie		Pass	🟩
	Outgoing Analyzer Results from Vendor		Pass / Fail			Pass	🟩
	Device Characterization	Prober Device File Setup	Needle Alignment Settings defined.	SC/DFAB		Pass	🟩
		Bin to Bin Correlation	98% bin to bin from baseline card to new probe technology or LBE/PDE acceptance.	corr wafer/sc/dfab		Need to correlate later between SVA / DFAB.Cantilever Data in SVA	🟩
		Cres Over Time	Limit of 3 Ohms Standard deviation on 100k TD and a minimum 100 wafers probed. Confirm cleaning optimized to keep Cres consistant.	DFAB/add Cres test		Need program number / DMOS5	
		Life time study	100k TD and a minimum 100 wafers Probed in production or accelerated probing and cleaning wear study to show the TD vs. Tip length as it relates to probe card end of life. (life expected must be (>750K TD)	DFAB		get some measurements of current tip length.	
		Thermal Agility	X, Y, Z correction across a wafer must be lest the 30um min to max without dramatic swings not including stops to the prober with in a wafer once the card gets to temps	TBD		NA	▨
		Cleaning Optimization	Optimize on cleaning OD / Recipe. (Record recipe in Probe & Cleaning Recipe Tab) Define cleaning Block rotations Examples: Mipox VPC rotation 50 / PP150 FFI rotation 50 / PL Cobra rotations 15 / PL Cantilever/ Canti2 rotation 25	DALE/John		currently probing 100Td interval. May try to optimize	🟩
	Quality	MSDS Sheet	New materials require MSDS sheet. No polyethylene allowed, high temp transfer study is needed.	Technoprobe			
		AVI Fail Rate	Fail rate must be less the 0.25% across 20 EWR lots at all temperatures.	DFAB			🟩
		Bump Damage (FC or WCSP)	Damage must meet all packaging requirments.	QA/Brandon			🟩
	Dielectric Cracking Study (if needed)	Max TD Test	Dielectric cracking study Automotive requirement 9x TD in the same location and max production probing OT) –Note weakest dielectric stack up is C027 Pass TD in the same location 6x TD	TBD/SC:probe 9X		Probed 10x no issues	🟩
		Punch Through	No under layer metal exposure on automotive products QSS states for Al technologies "shall not expose underlying passivation or underlying metal equal to or greater than 25% of the pad width adjacent to the edge of the pad or exceeds 1.0mil2 near the center of the bond pad.	N/A			🟩

- **Continue gathering volume data for Technoprobe M3 pin.**
  - Lifetime
  - Cres over time
- **Transfer knowledge / Learnings for other Devices**
  - TI increasing Cu pillar applications
  - Cu pillar w/ solder

Summary

- Cantilever has long been baseline for probe technologies on Cu pillar probing applications in TI.
- New rigorous requirements for TI’s devices required move to vertical on Cu pillar for many of its advantages.
- Technoprobe's M3 vertical probe technology was selected for evaluation.
- Initial-challenges that had to be overcome in terms of contact failures and cleaning settings.
- After resolving these issues, the M3 probes provided good results on probing the Cu pillars.

Questions

Thank you

- **Technoprobe**
  - Carmen Tomsu
  - Matt Simons
  - Steve Radford
- **DFAB / SVA Support**
  - Betty Hoang
  - Dale Anderson
  - John Hsia
  - Trey Lazear
- **TI Clark**
  - Ace Arricivita
  - Richard Incognito