



**SW Test Workshop**  
Semiconductor Wafer Test Workshop

# FeinProbe<sup>®</sup> Solution for WLCSP Applications



**Krzysztof Dabrowiecki**

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# Overview

- **Motivation**
- **WLCSP Market Drivers**
- **WLCSP Application Requirements**
- **Stages of FeinProbe® Internal Qualification and Testing**
- **Summary and Conclusion**

# Motivation

- **Diversification of semiconductor products:**
  - Smartphones/Tablets
  - Internet of Things/Wearables
  - Virtual Reality
  - Artificial Intelligence
  - 5G Connectivity
  - Automotive and much more others like Medical, Industrial, Military...
- **Increasing WLP (Fan-in and Fan-out) without substrates or interposer for IC chips**
- **Increasing final tests at wafer level**

# WLCSP Market Drivers

- Good electrical performance
- Good thermal performance
- Smaller and lower profile
- High power
- High system integration
- High I/O density
- Low cost

# General WLCSP Requirements

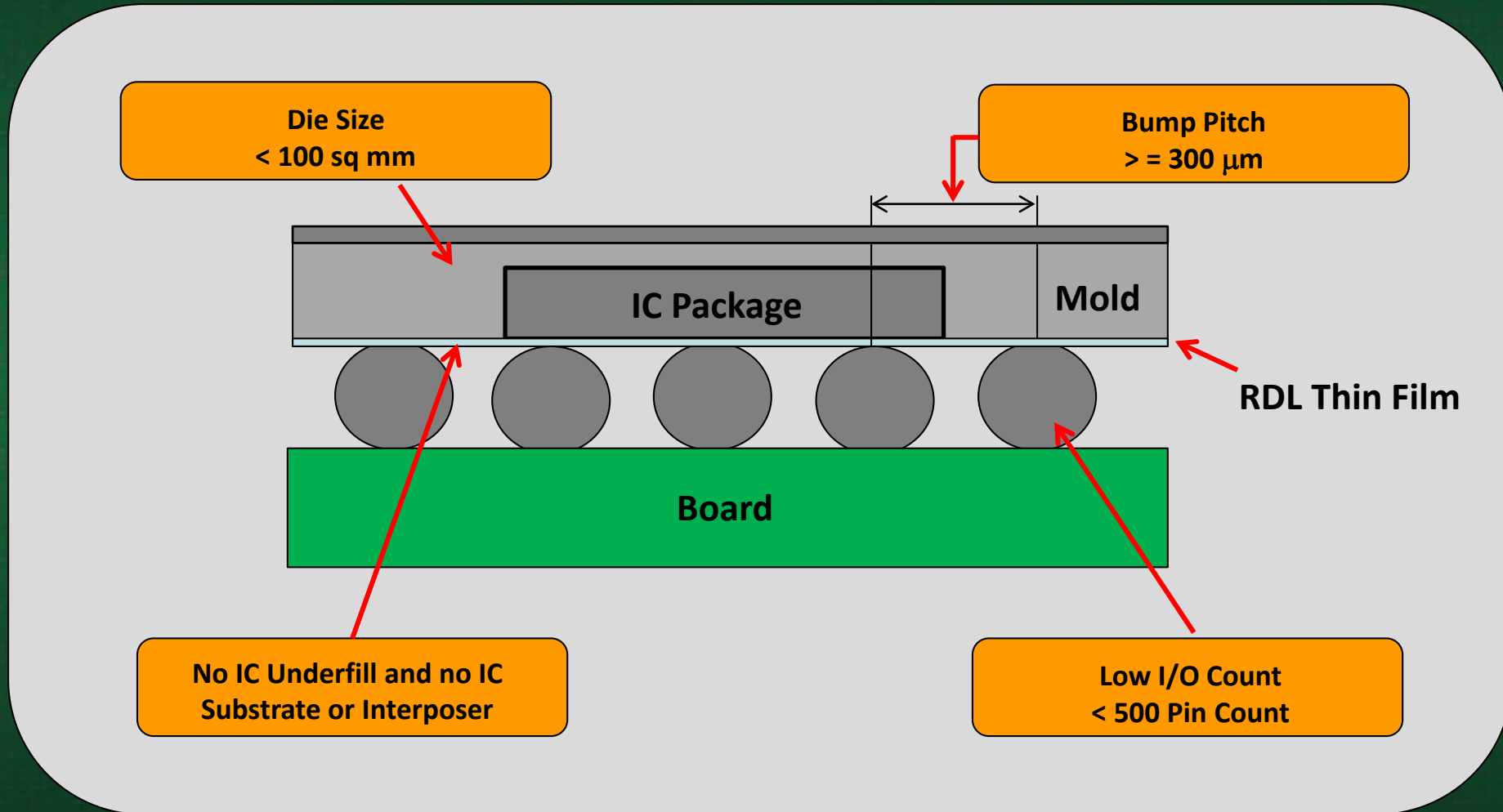
## Electrical

- ❑ Low resistance for DC measurements
- ❑ High bandwidth for functional tests or AC tests
- ❑ Low path inductance to reduce the noise on the DUT power and ground at its switching frequency
- ❑ High current capacity for power delivery and DC parametric tests
- ❑ Kelvin probes for analog and mixed signal

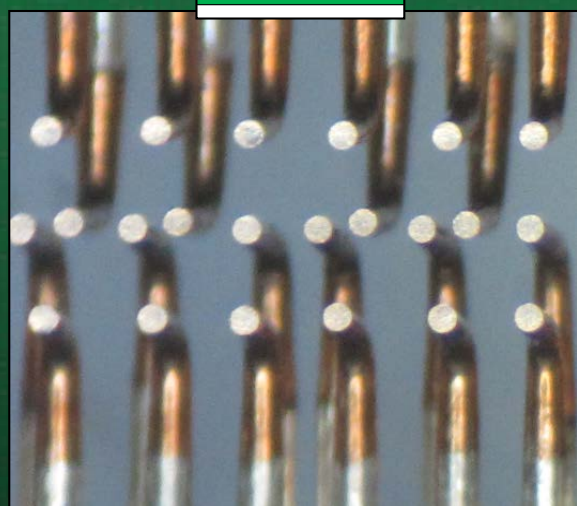
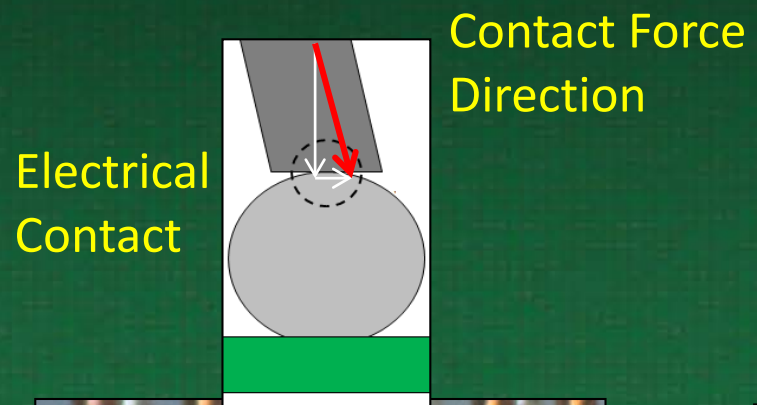
## Mechanical

- ❑ High contact force
- ❑ Short probe length for electrical parameters
- ❑ Large plunger compliance for reliable contacts
- ❑ Longer lifetime
- ❑ Effective cleaning method

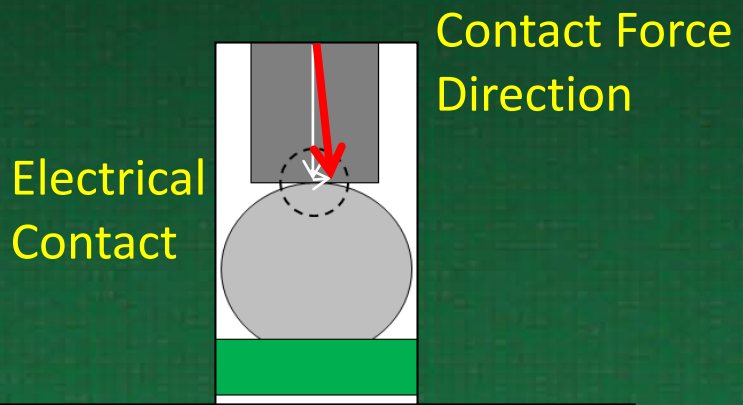
# Fan-out WLP Connection to PCB



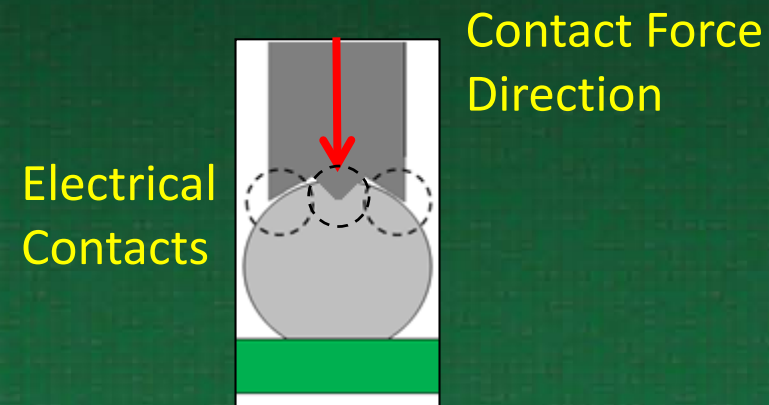
# Probe Card Technology for WLCSP Testing



Cantilever Technology



Buckling Beam/Hybrid BB Technology



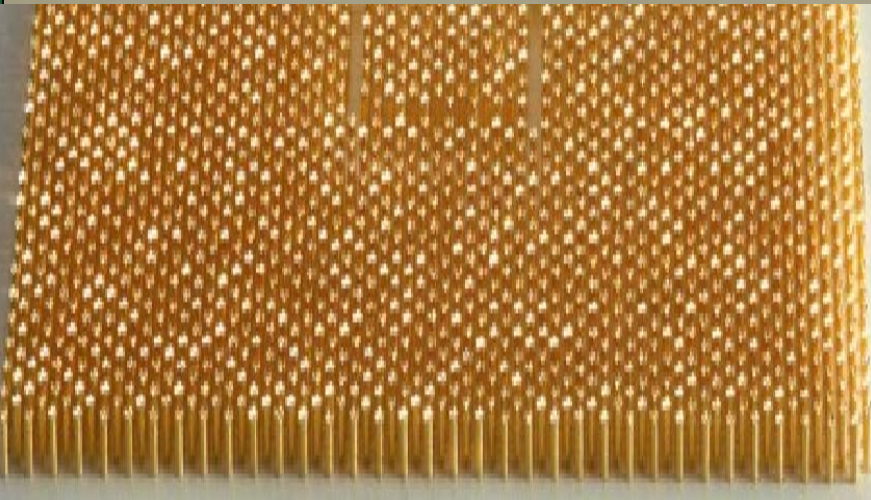
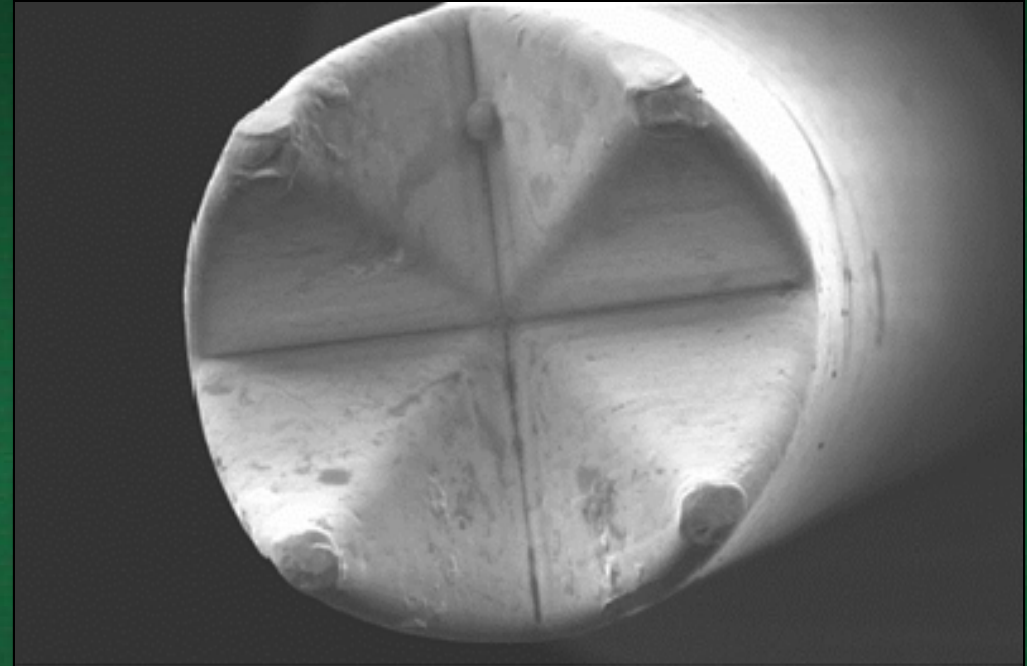
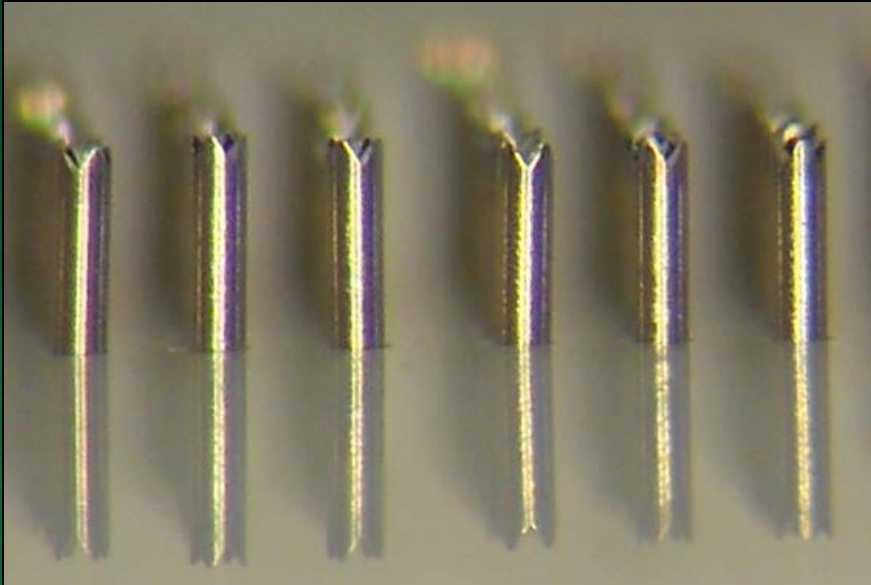
Spring Probe Technology

# FeinProbe® Spring Contact Advantage

- ❑ Stable and consistent contact resistance
- ❑ Self-aligning plunger tip
- ❑ High bandwidth
- ❑ High Current Carrying Capability (CCC)
- ❑ Large spring range force
- ❑ Large plunger tip compliant
- ❑ Low bump damage
- ❑ No probe coating required



# Crown Plungers of FeinProbe® Head

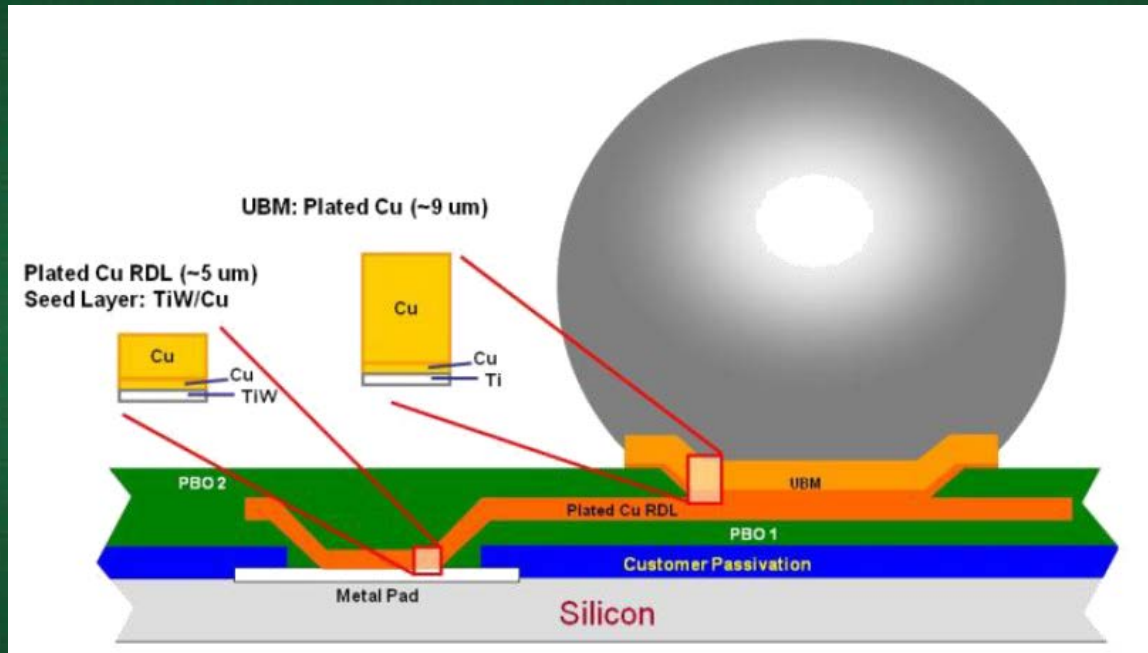


# Stages of FeinProbe® Qualification and Testing

- ❑ Finite Element of Solder Bump-Crown Tip Plunger Model
- ❑ Contact Force Test of Probe Head
- ❑ Path Resistance on Bumped Wafer
- ❑ Vector Network Analyzer Probe Test
- ❑ Probe Current Carrying Capability Method

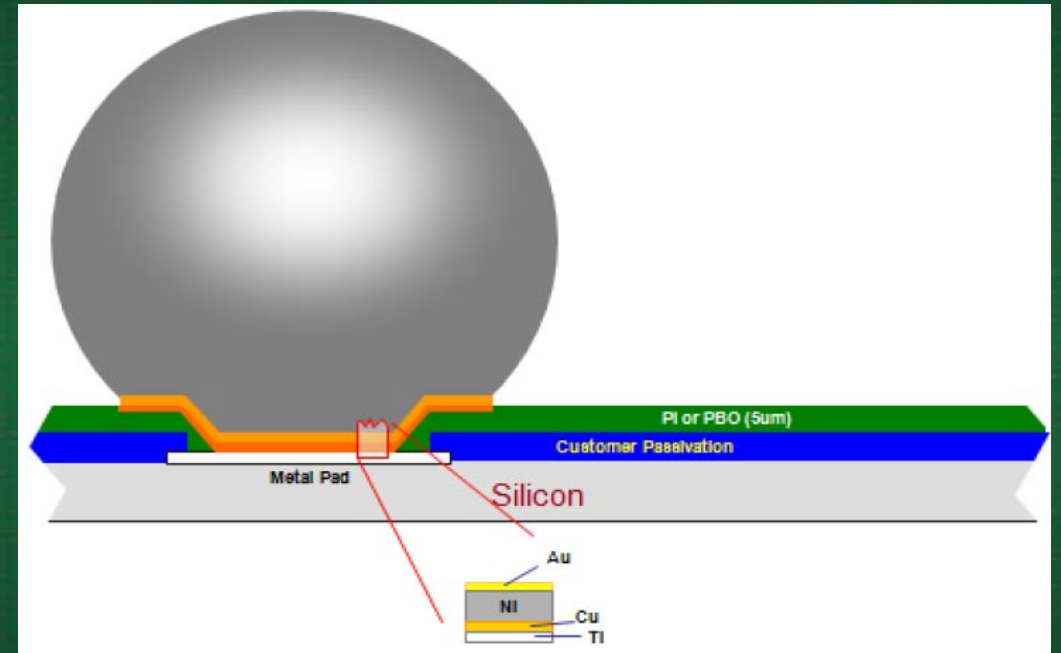
# Why Finite Element Bump-Probe Contact Study?

## Current WLCSP Technology Options



### CSP with RDL:

- 4 mask
- 9 um UBM Cu/Ti



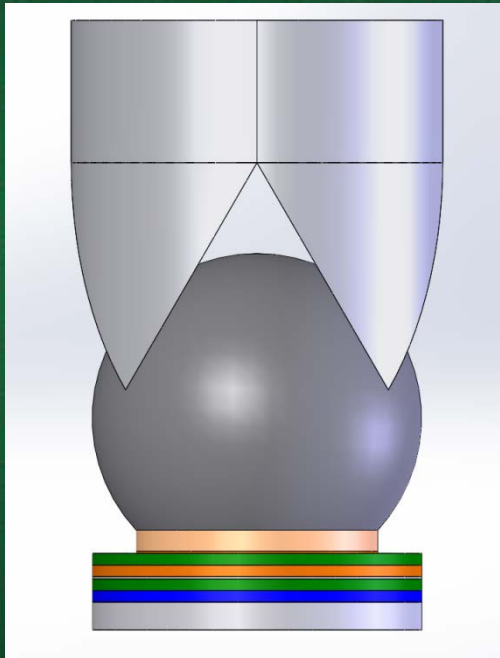
### Low cost solution:

- No RDL
- 2 mask
- 5 um UBM Au/Ni/Cu/Ti

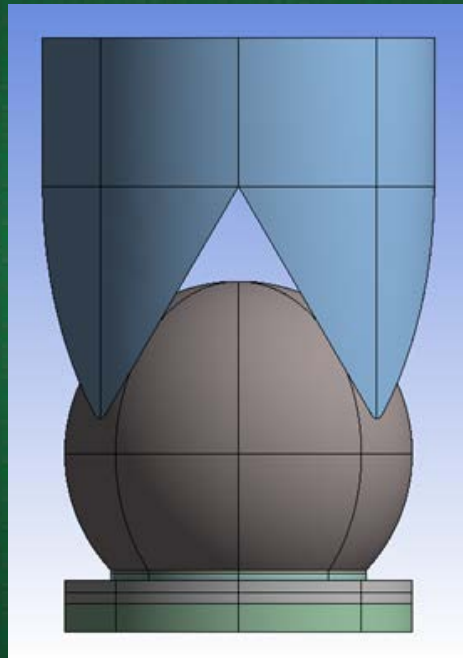
Source: C.Lee Amkor

# Finite Element Probe-Bump Models

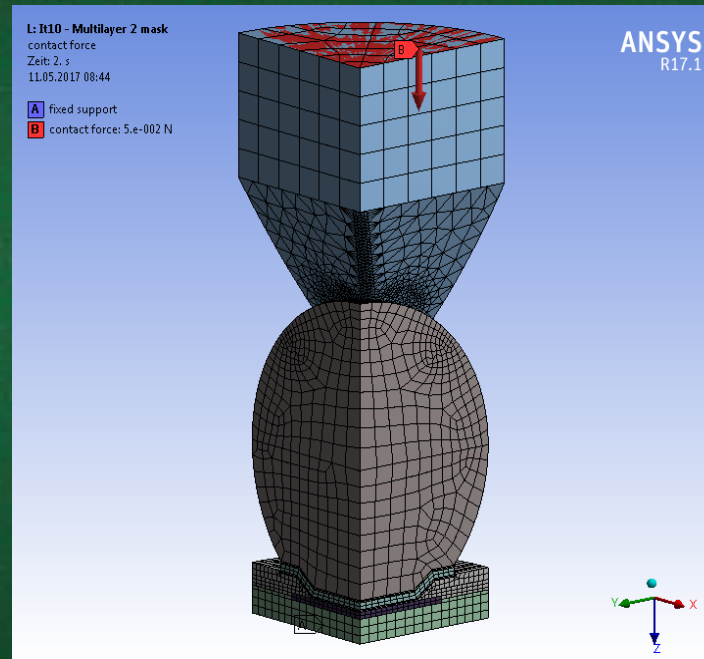
FE Model w/ 4 mask



FE Model w/ 2 mask



Boundary Conditions



FE model – Quarter

- Lead-free bump diameter 142um
- Crown plunger diameter 160um
- Plunger force  $F=20gf$

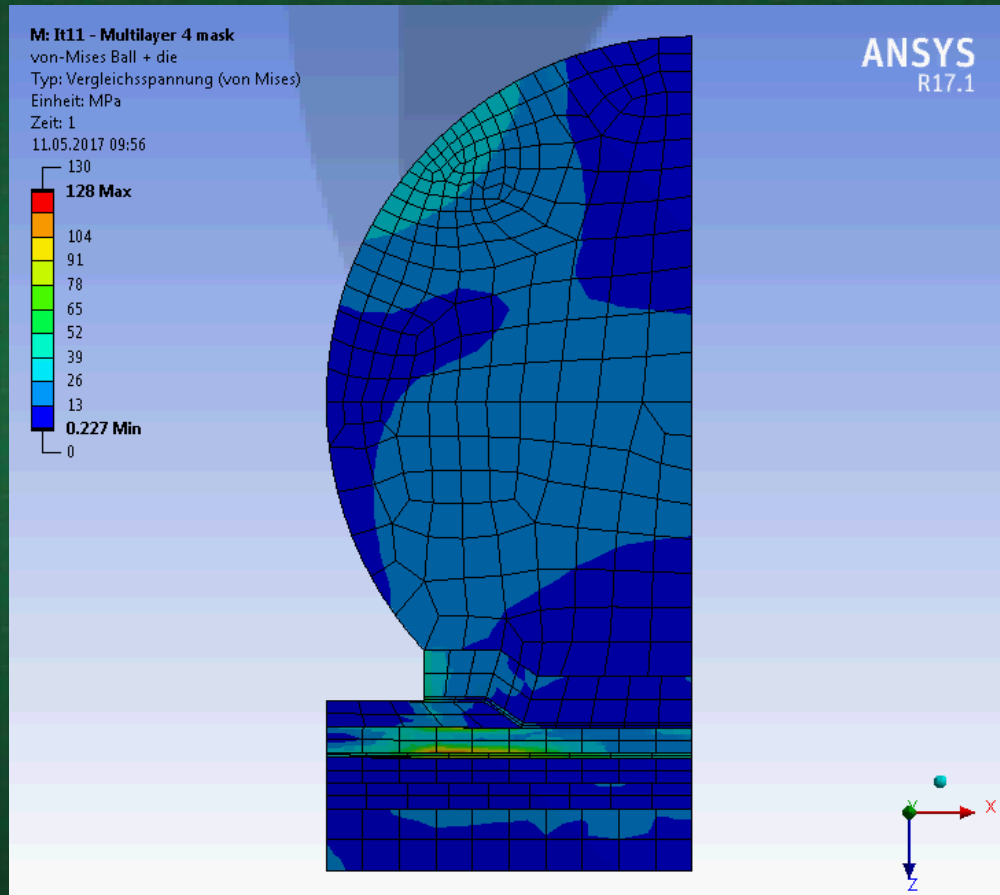
# Model Material Properties Table

Model part	Material	Young's Modulus E (GPa)	Poisson's Ratio (-)	Yield Point (MPa)	CTE (ppm/C)
Crown plunger	Pd alloy	110	0.35	930	11.7
Solder ball	Sn/Ag	50	0.36	34.2	25
Cu	Cu	117	0.34	62	16.8
PBO 1	PI	2.3	0.3	69	35
PBO 2	PI	2.3	0.3	69	35
Custom Passivation	PI	3.5	0.35	69	35
Silicon	Si	131	0.26	UTS 7000	2.54
Gold	Au	79	0.4	205	14.2
Nickel	Ni	207	0.31	138	13.3
Titanium	Ti	116	0.32	379	8.5

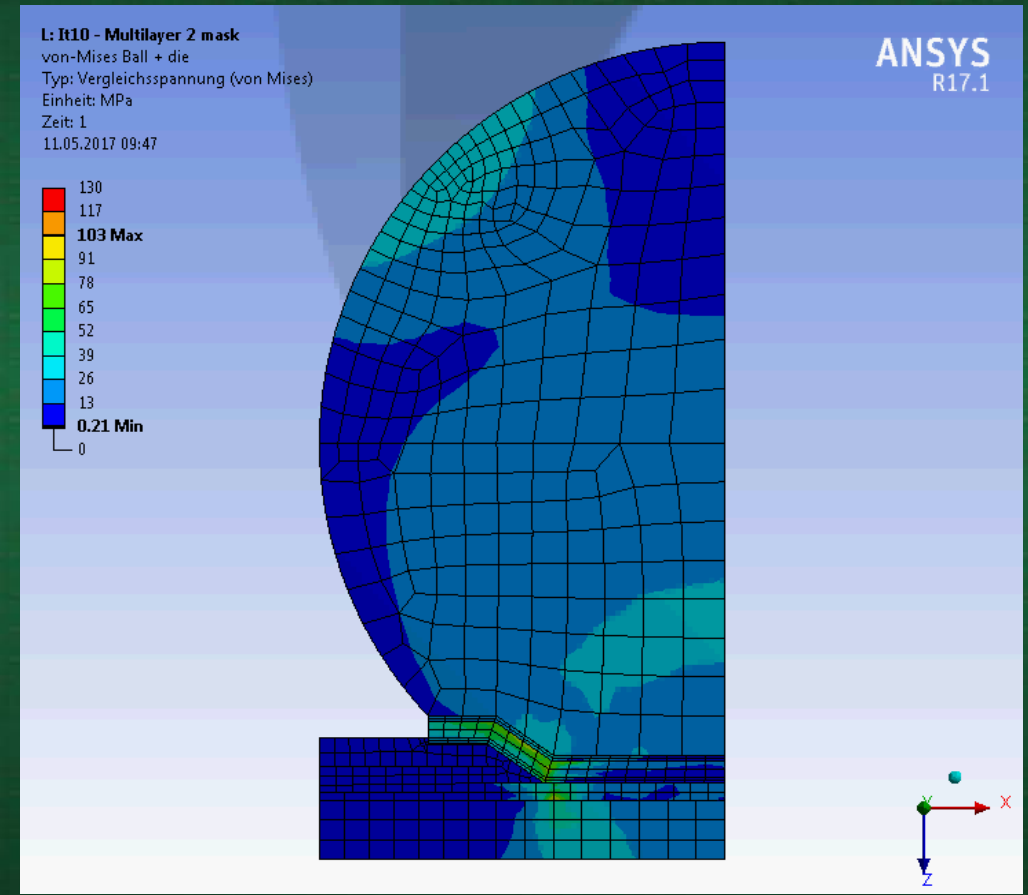
Source: Amkor, NIST, STATS ChipPAC, Japan Institute of Metals

# Model Stress Simulation

## FE Model w/ 4 mask

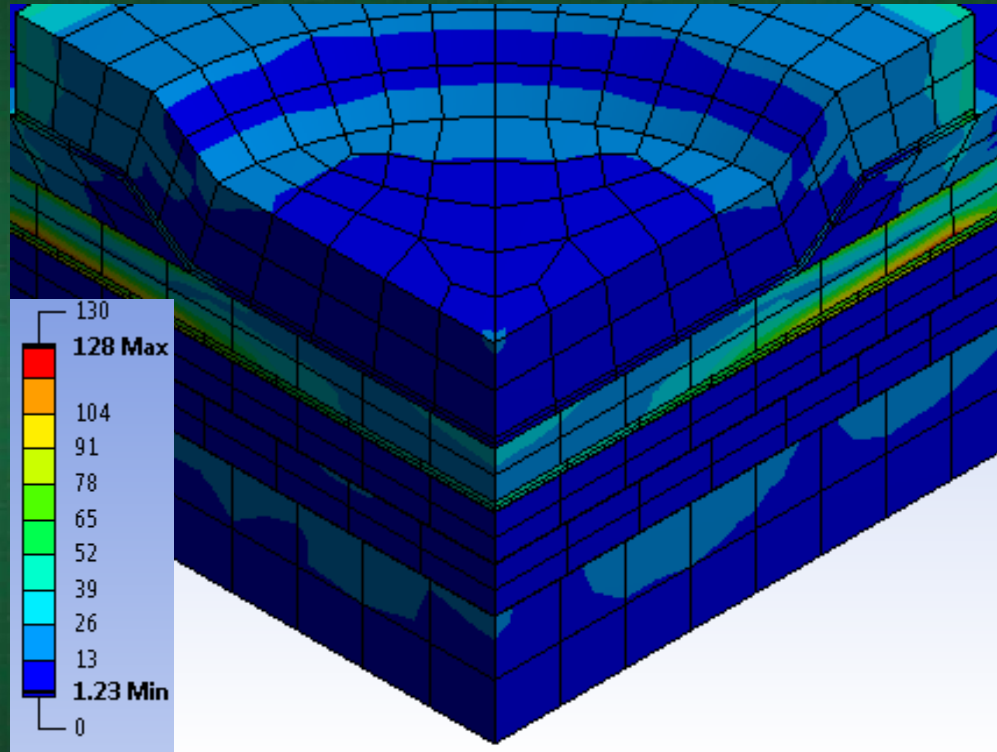


## FE Model w/ 2 mask



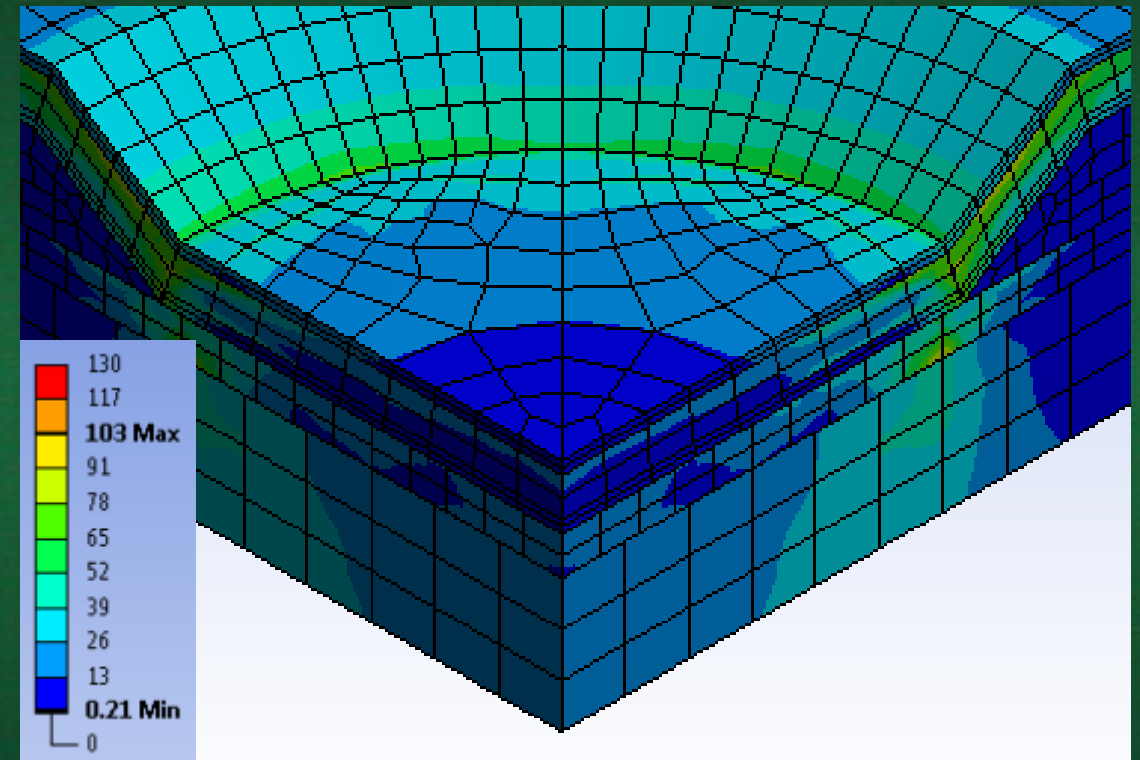
# Stress Calculation in the UBM

FE Model w/ 4 mask



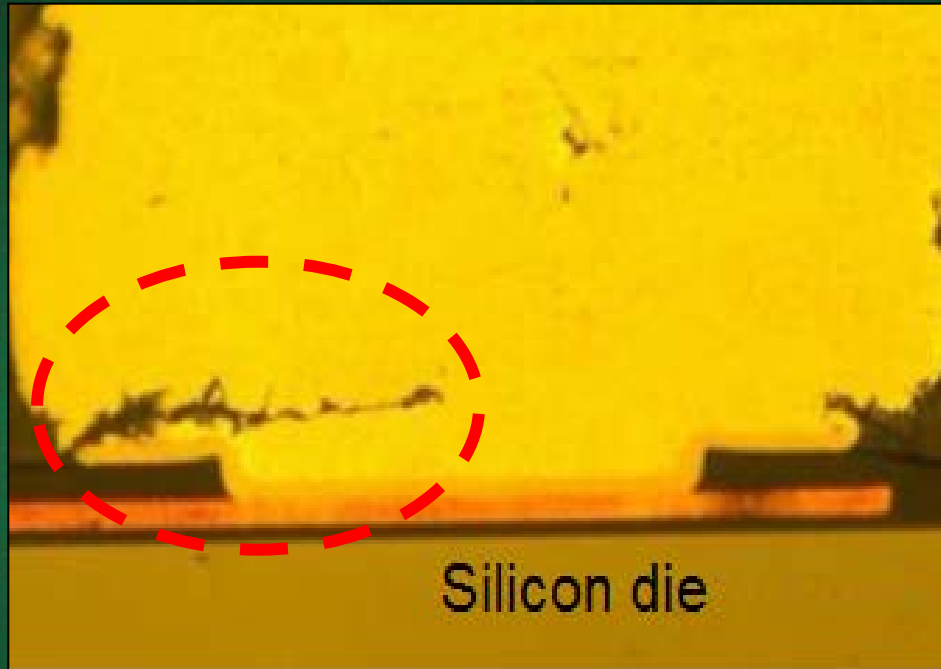
High stresses at the bottom of UBM  
and on the edge

FE Model w/ 2 mask

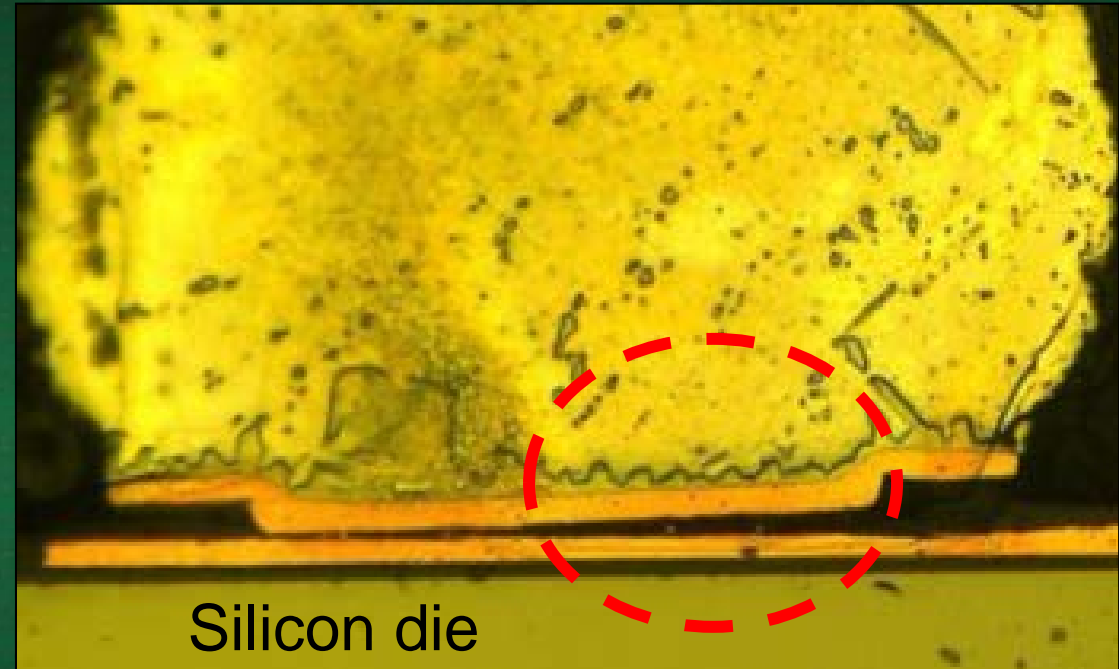


High stresses underneath of solder bump  
and on the edge

# Potential Bump Failures



Crack from UBM edge



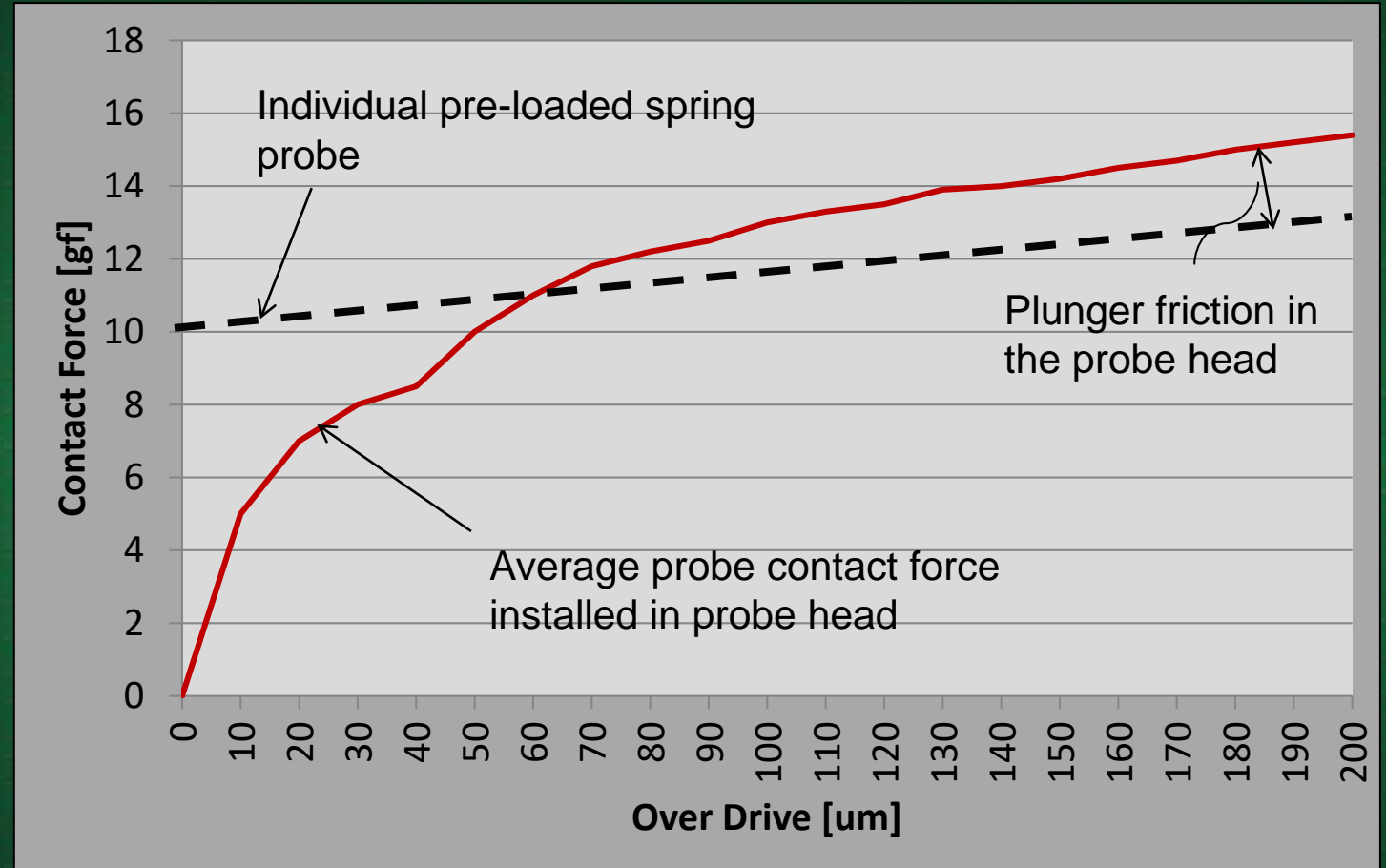
UBM and RDL detachment

The failure causes are related to high range of temperature and possible high stress concentrations in the UBM

Source: *Journal of Electronic Packaging*, 2015

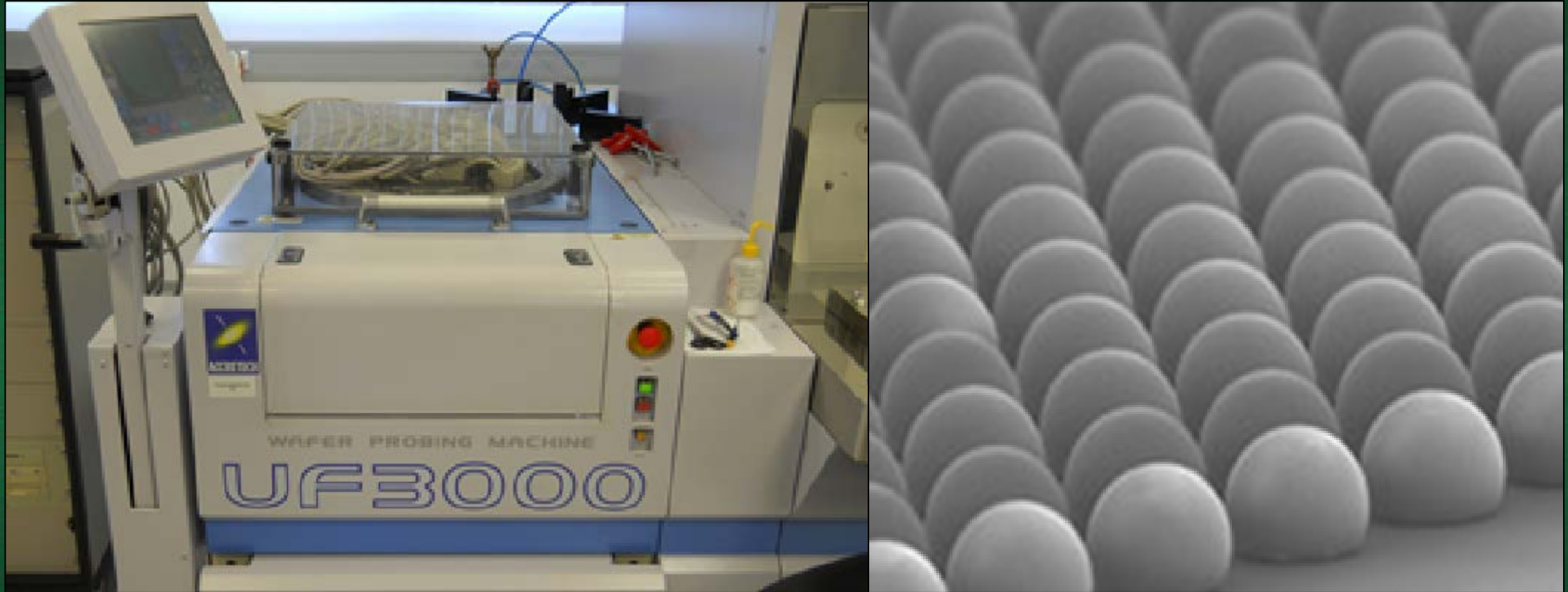


# Contact Force Test - Full Probe Head



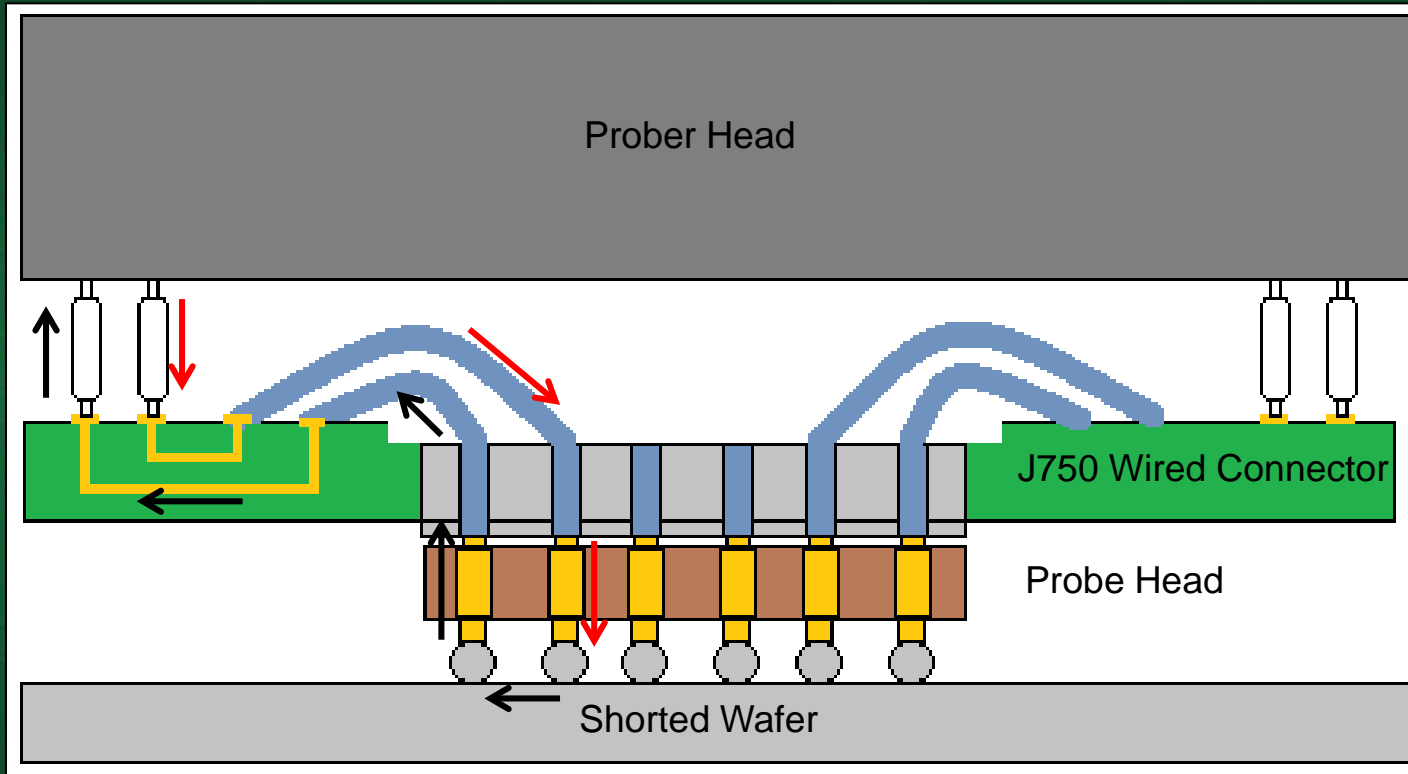
The contact force of test probe head measured by EAP500 system at RT

# Path Resistance Test



The bumped wafer SAC305: pitch 250um, bump size 142um  
The test over drive 175um

# Path Resistance Illustration

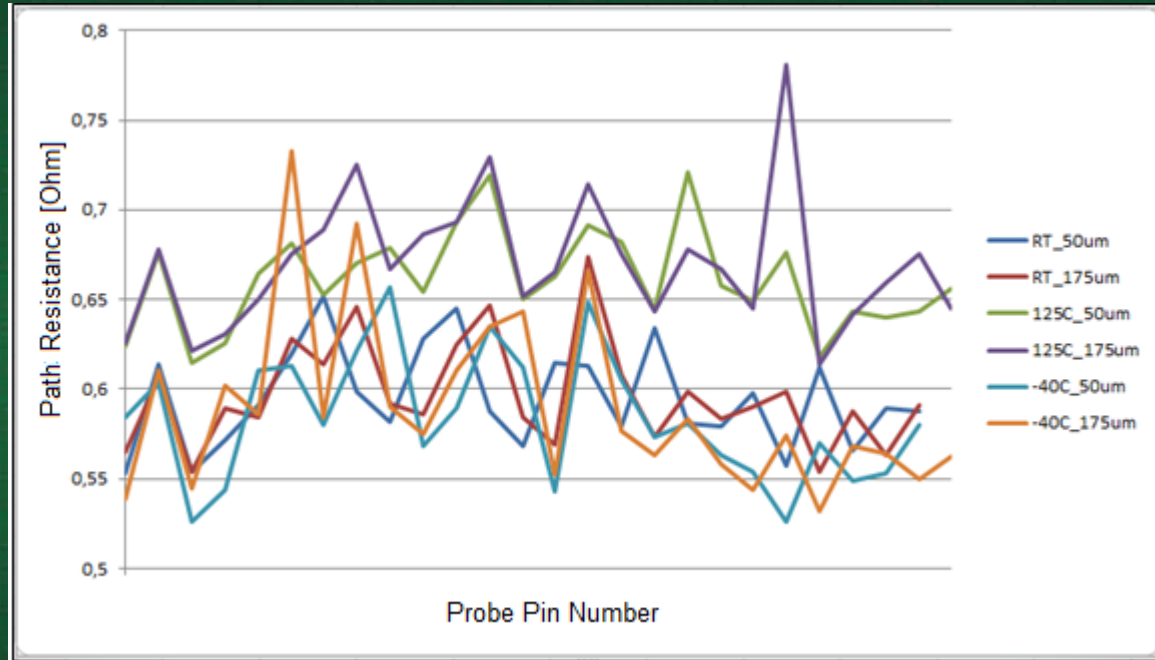


The path contact resistance contains material resistivity of wafer, solder bump, probe, connector wire, PCB solder, PCB trace and prober head pogo, and contact resistances of probe to bump, probe to wired connector, pogo to PCB and pogo to probe head

→ Signal Path  
→ Return Path

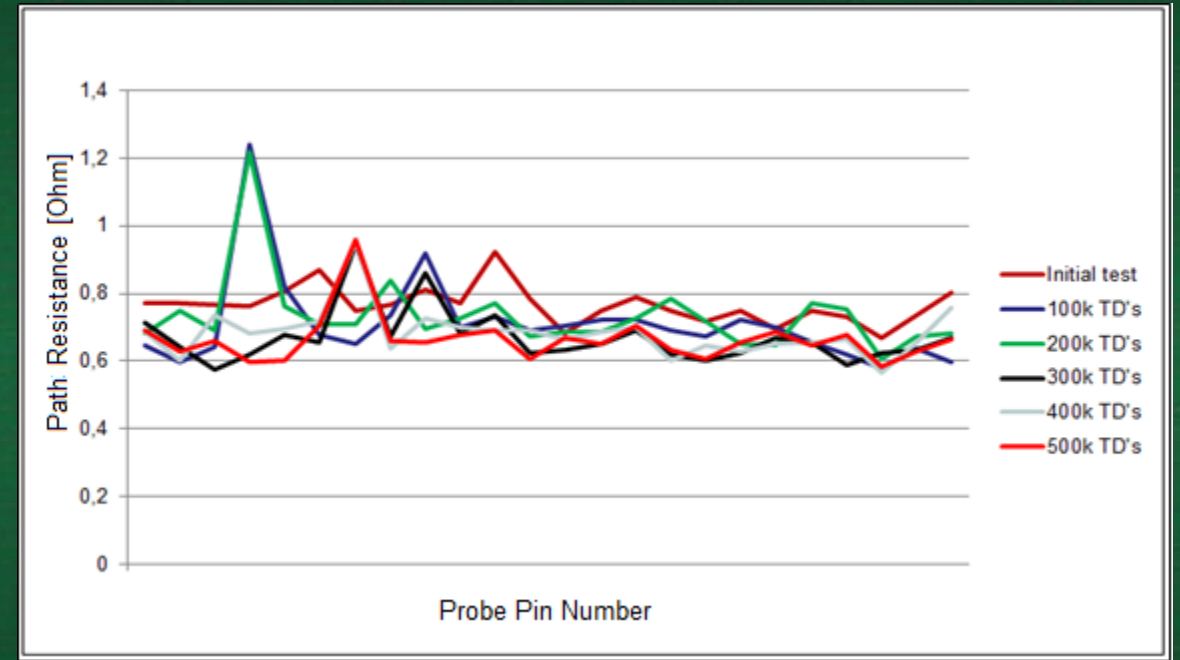
# Path Resistance and Life Test Charts

## At Varied Temperature and OD



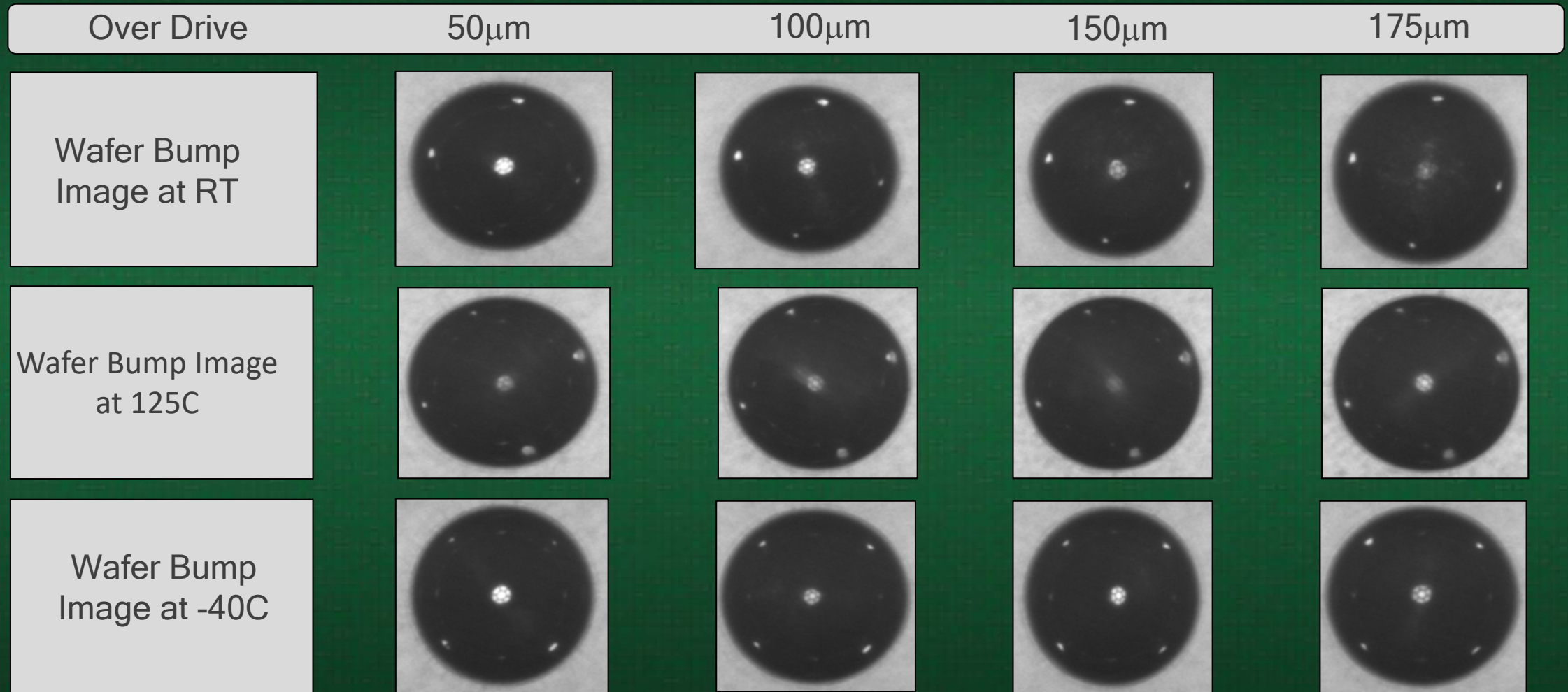
Path resistance at 125C is slightly higher (0.2 Ohm) than at RT and -40C

## Life Test at 175um OD

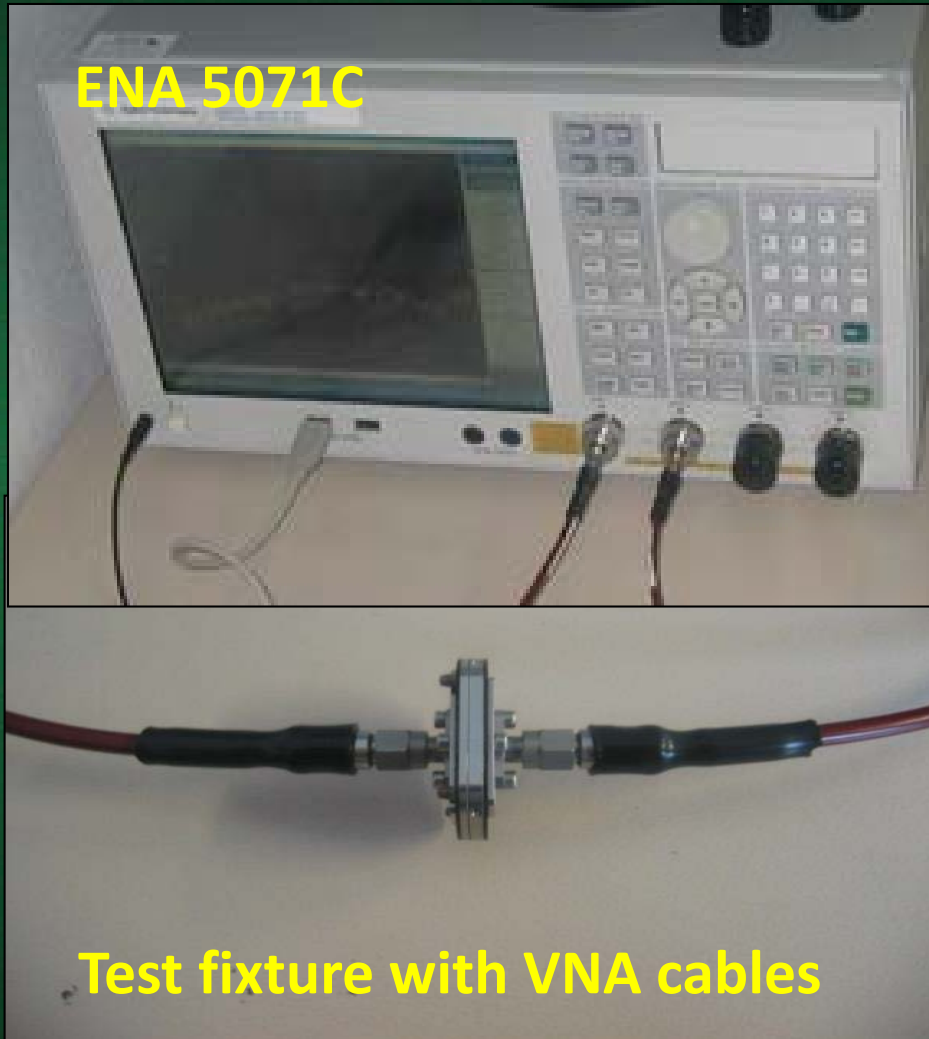


Path resistance at 175um OD shows a quite uniform and consistent profile up to 500k TD's

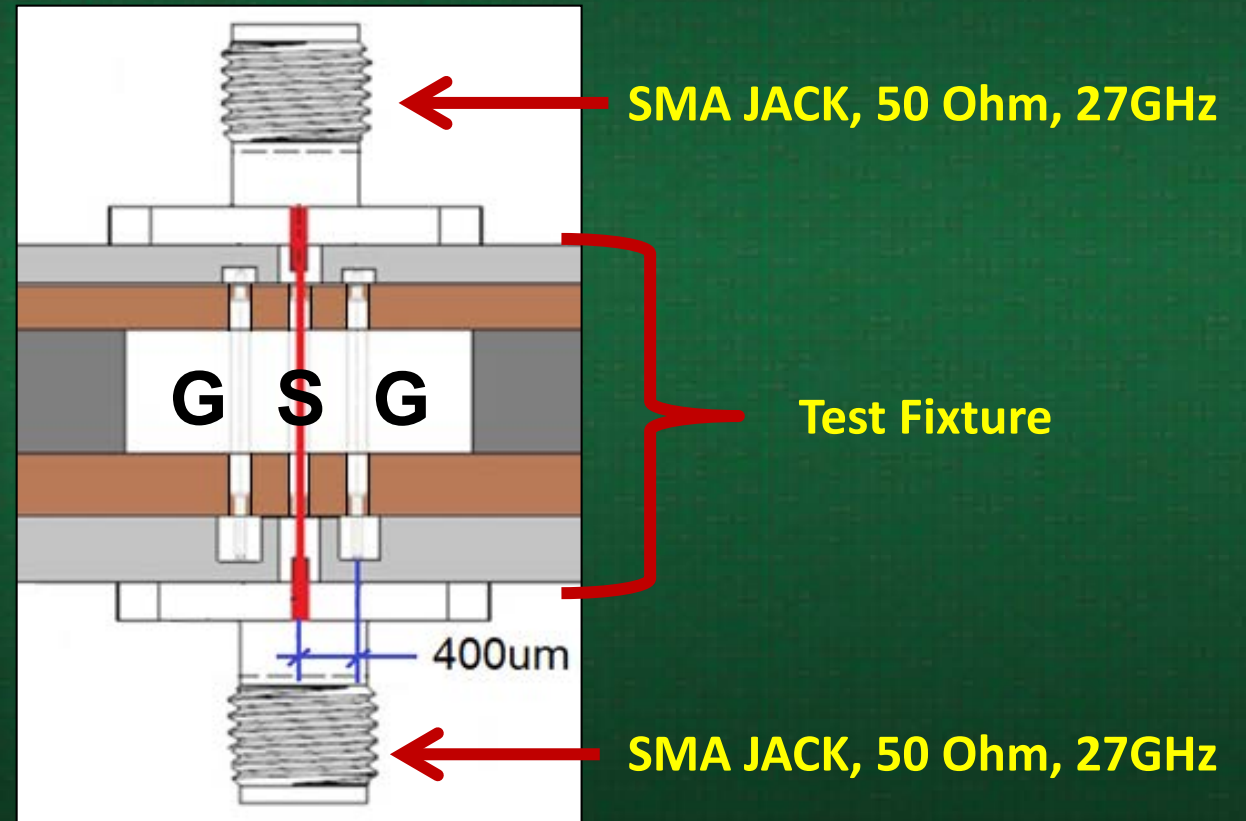
# Wafer Bump Scrub Marks



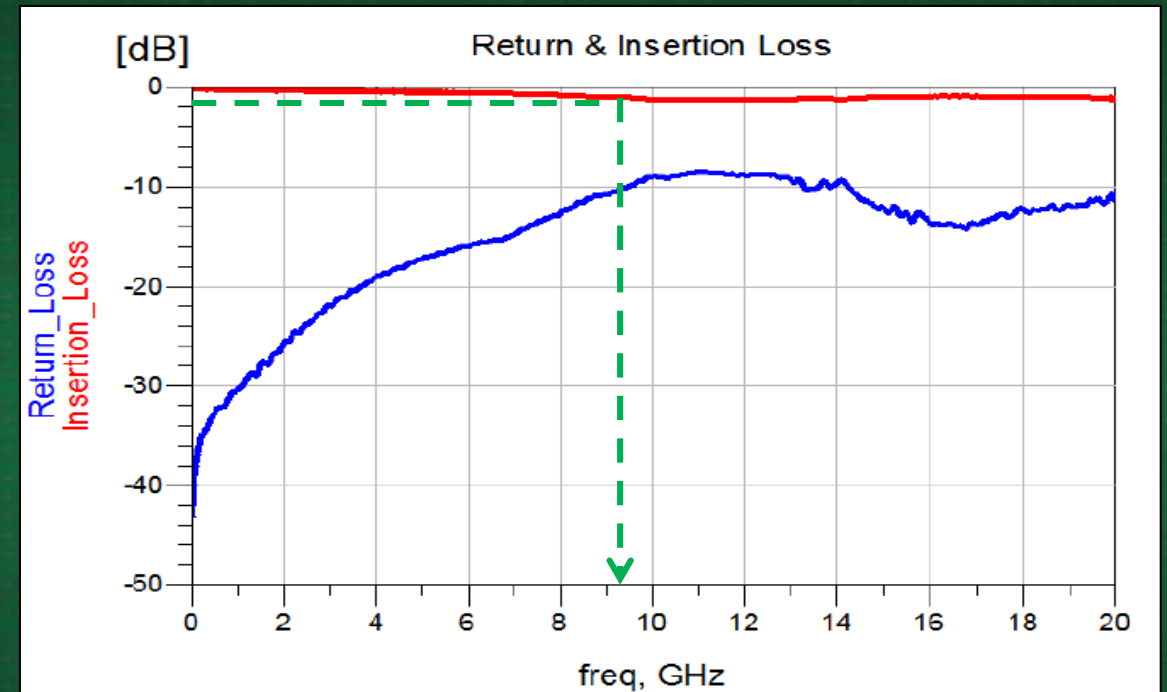
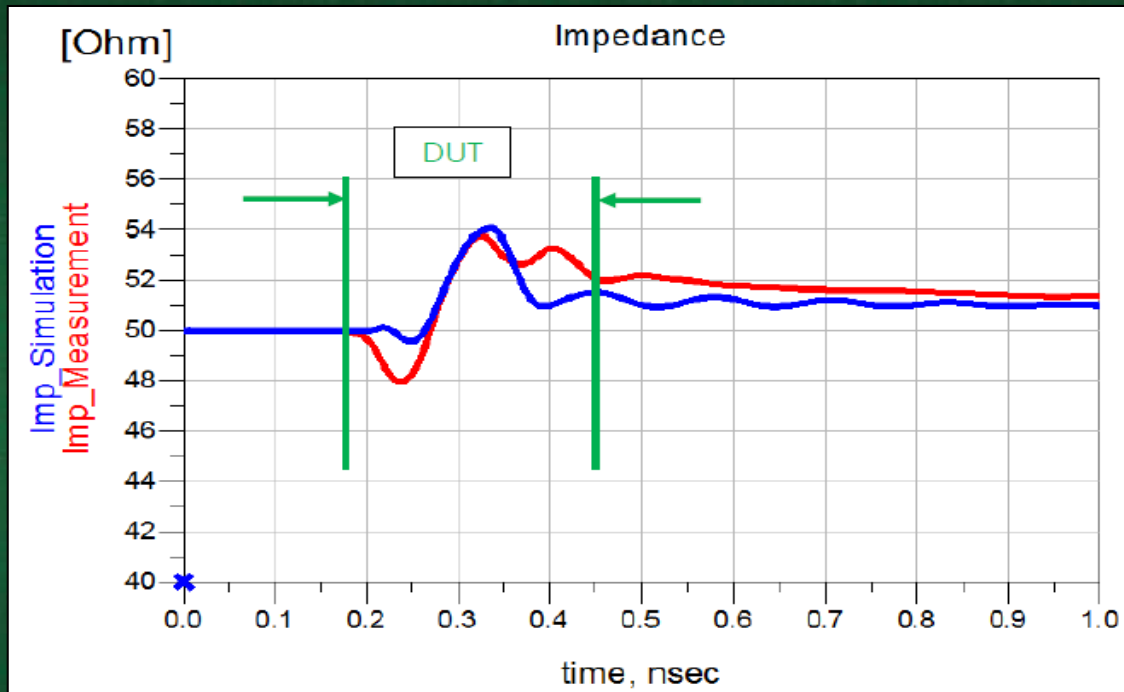
# Vector Network Analyzer Test



Configuration: G-S-G  
Probe pitch: 400um



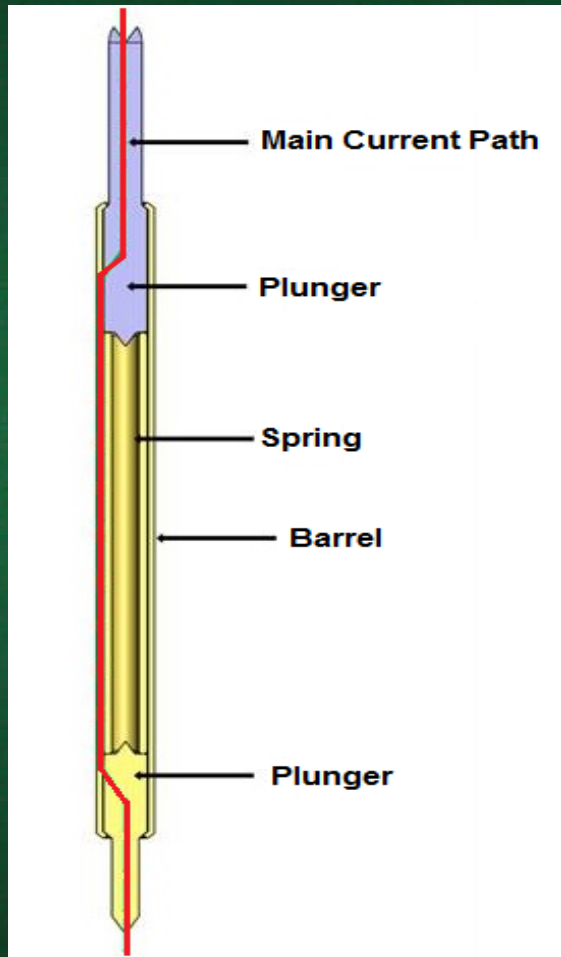
# Impedance and s-Parameters Measurements



The impedance characteristic was obtained by applying a signal with rise time 50ps (20-80%)

S21- Insertion Loss: 9.3GHz @ -1dB  
S11 – Return Loss: 9.5 GHz @-10dB

# Probe Current Carrying Capability - Method



The standard procedure of International Sematech Manufacturing Initiative (ISMI 2009) describing the probe current carrying capability test methods has not mentioned anything about a method how to define the CCC for spring probe.

Therefore based on our internal empirical researches and tests, the maximum continuous current has been defined as a maximum tolerable probe warming temperature during the current lab test.

In case of FeinProbe<sup>®</sup>, the temperature change of probes under the current has been defined for 20 degree (K) measured by thermocouples

$$T_p = K + T_e$$

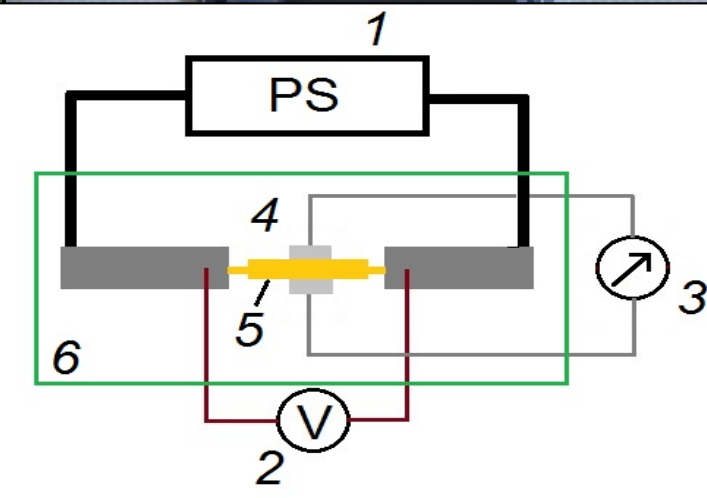
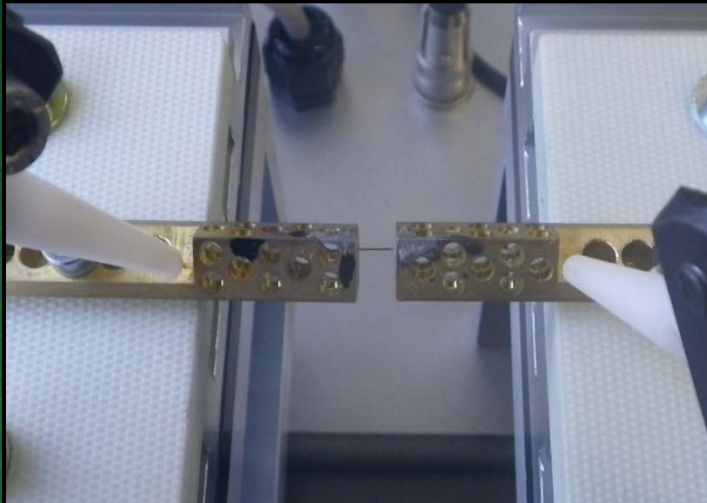
$T_p$  – probe surface temperature

$K$  – probe temperature change measured by thermocouples

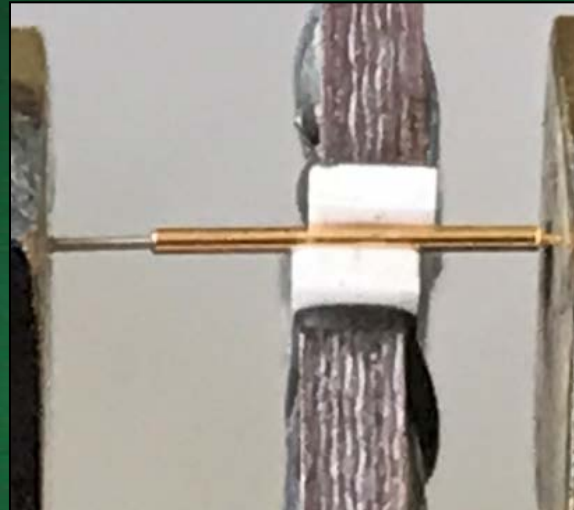
$T_e$  – environment temperature (RT)



# Probe Current Measurement Cases

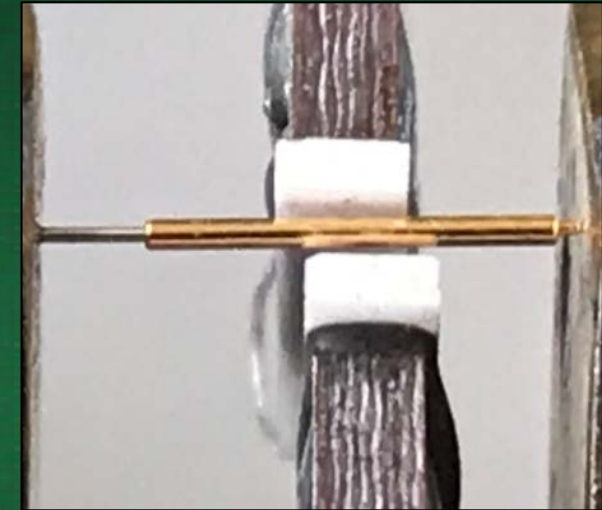


Case 1



Thermocouples touching the test probe

Case 2



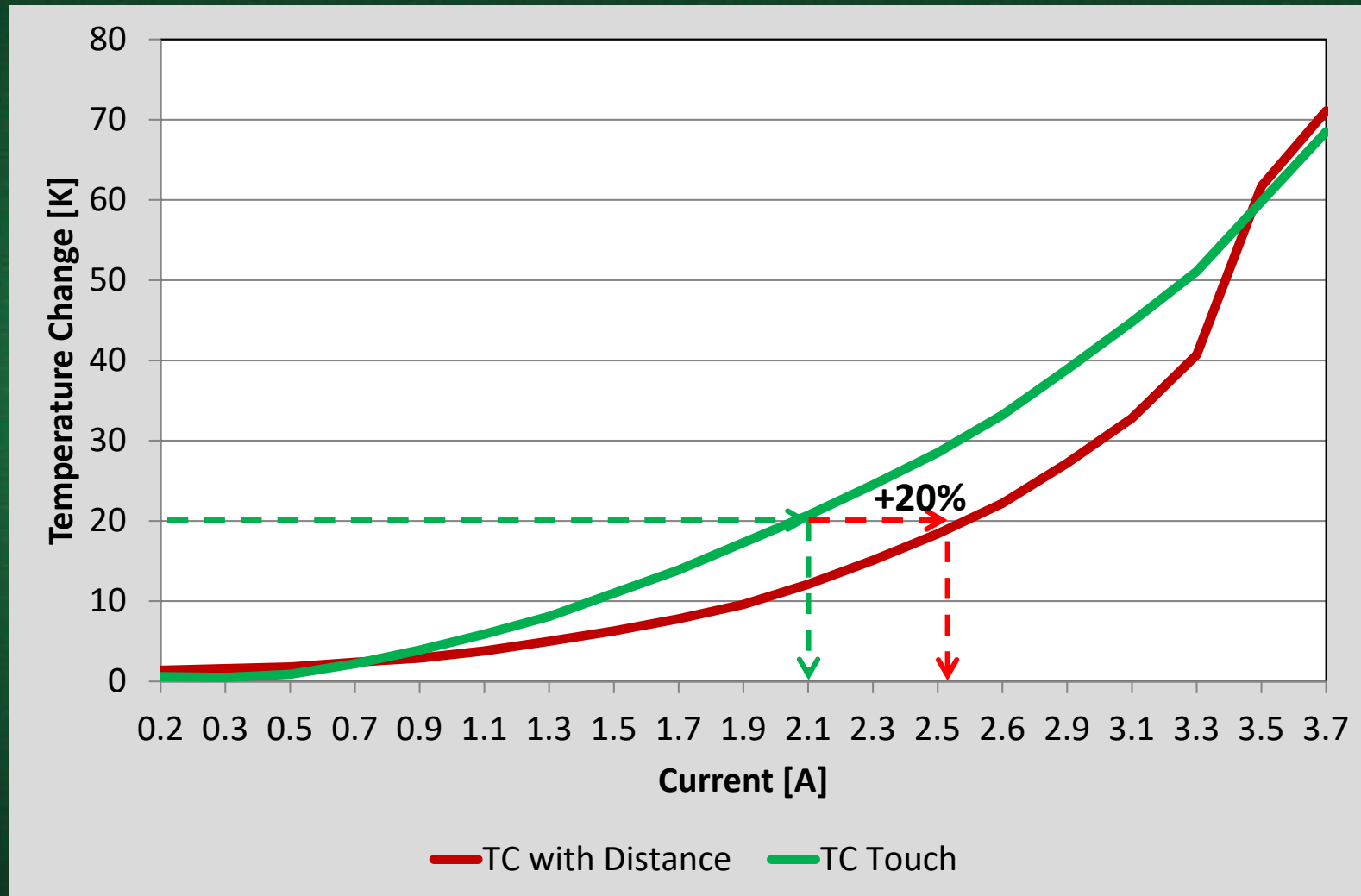
Thermocouples with distance to the test probe

## Schematic Diagram Description

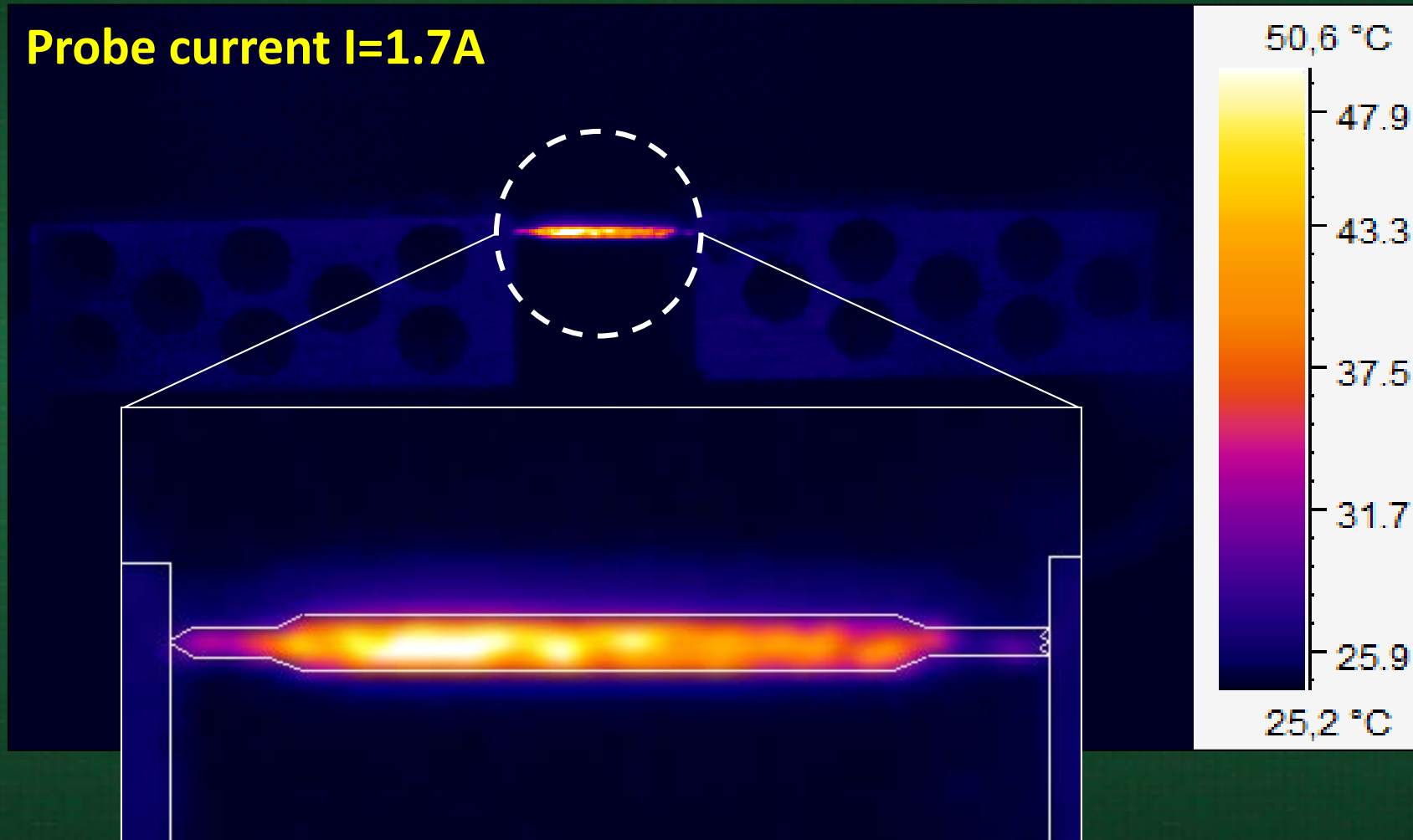
- 1 - power supply
- 2 - digital voltmeter
- 3 - thermocouple meter

- 4 - thermocouples
- 5 - spring probe
- 6 - probe station

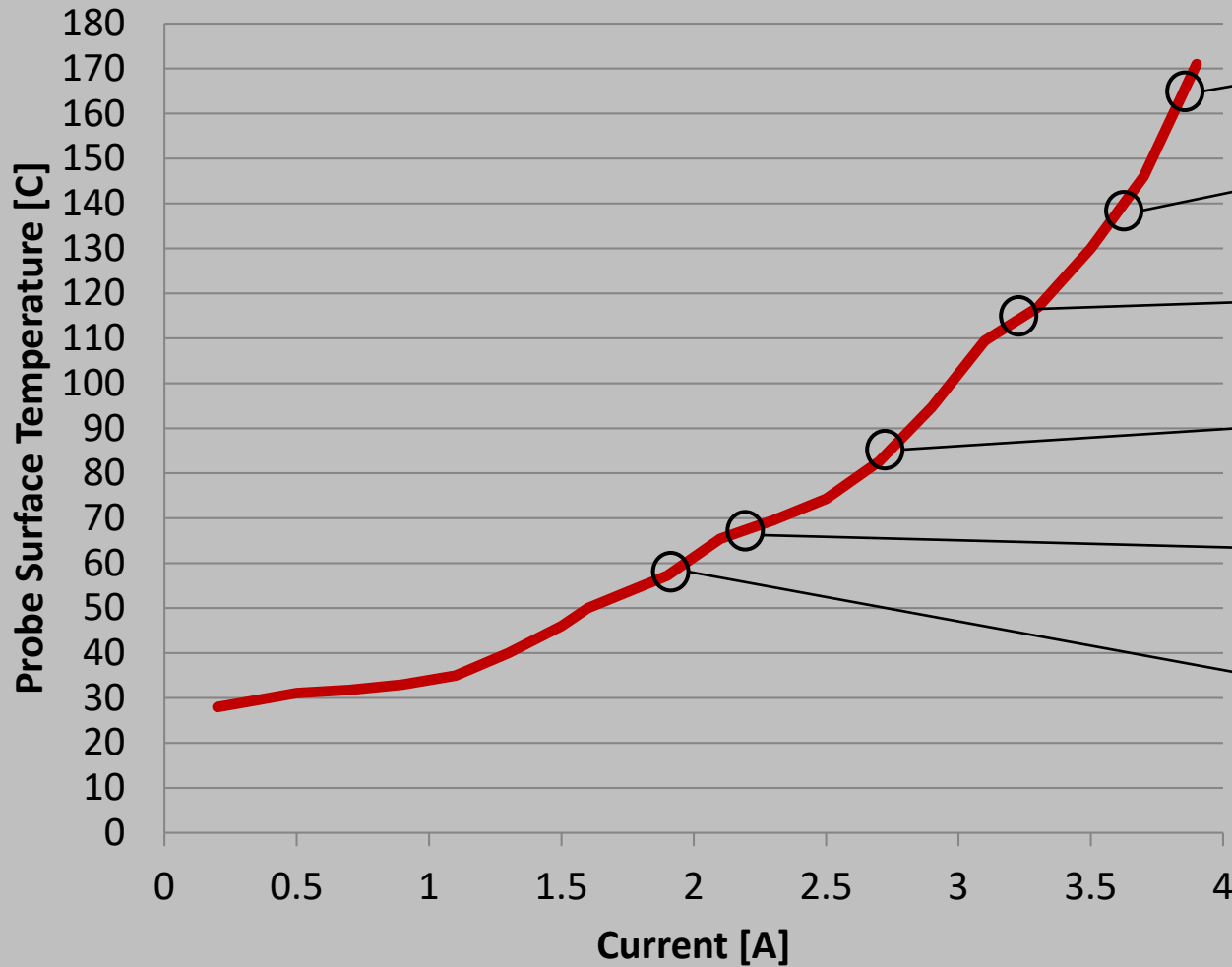
# Probe Temperature Change Chart



# Probe Image in the Eye of Infrared Camera

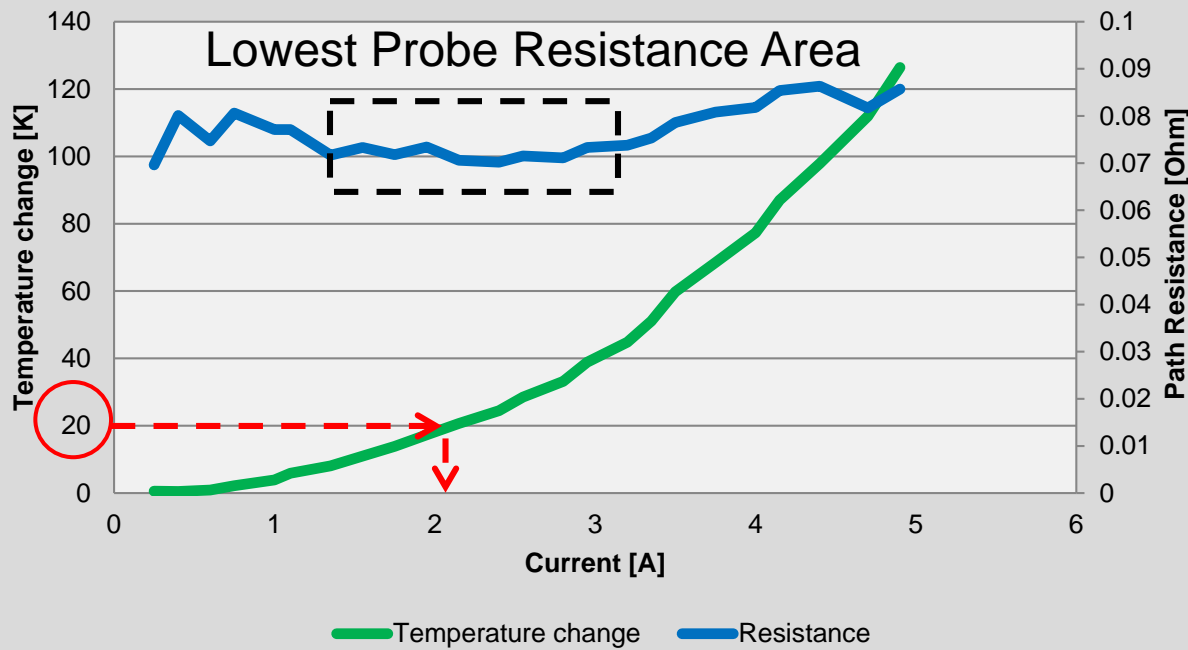


# Probe Surface Temp Measured by IC

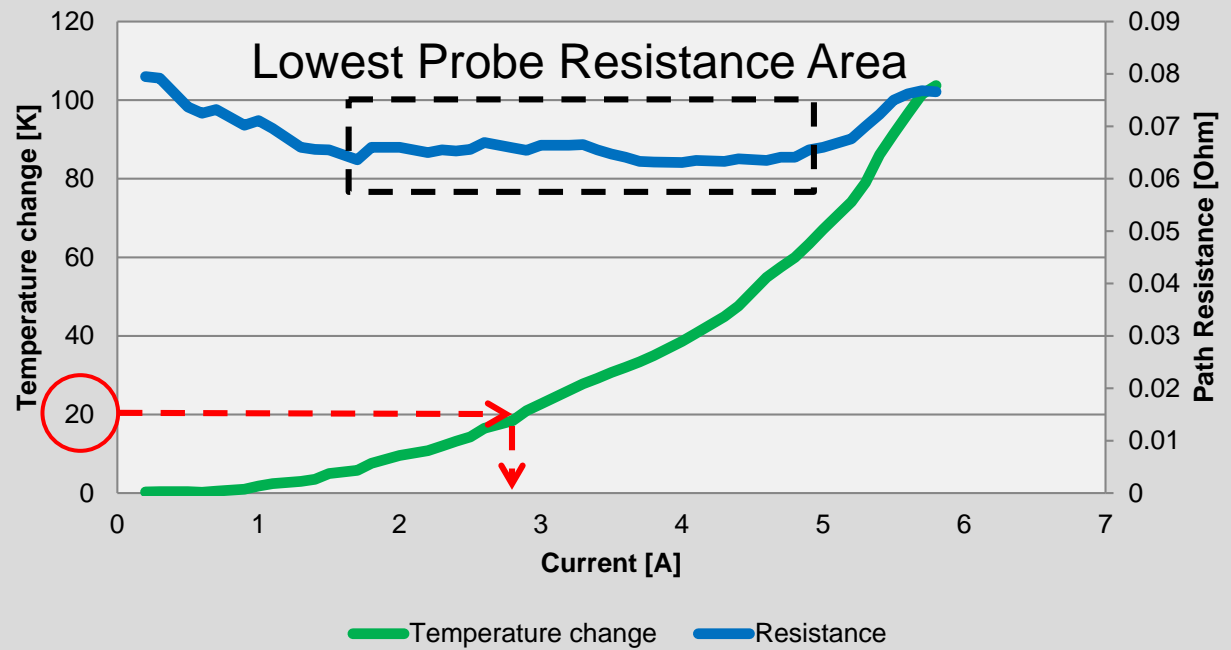


Note: Probe surface observation during the current test with TC. Test time for each current cycle  $t=2$  minutes

# FeinProbe® Current CC and Resistance Graphs



Probe length  $L=8.6\text{mm}$   
Continuous CCC= 2.1 A  
Path resistance = 70 mOhm



Probe length  $L=3.2\text{mm}$   
Continuous CCC= 2.8 A  
Path resistance = 65 mOhm

# Summary and Conclusions

- The advanced package technology exploring the 3D, complex and high pin count of FOCSP requires a reliable test solution and the presented five stages of qualification methodology can be a good approach to guarantee an appropriate contact solution
- The thinner and smaller UBM may cause a cracking or delamination issues of the under bump metallization during the wafer test

# Summary and Conclusions

- The update of ISMI procedure is needed to standardize the CCC measurement method for the spring probes. The presented approach is a suggestion for an alternative method

# Follow-on Work

- Study of the low spring force probe
- Study of the spring probe at high temperature



# Acknowledgments

I would like to thank colleagues at Feinmetall for their help in preparation of this presentation. Many thanks to Jörg Behr, Gunnar Volkmann and Jörg Burgold.

## Thank You