SW Test Workshop

Semiconductor Wafer Test Workshop

Power Integrity of Space Transformer on Probe Card

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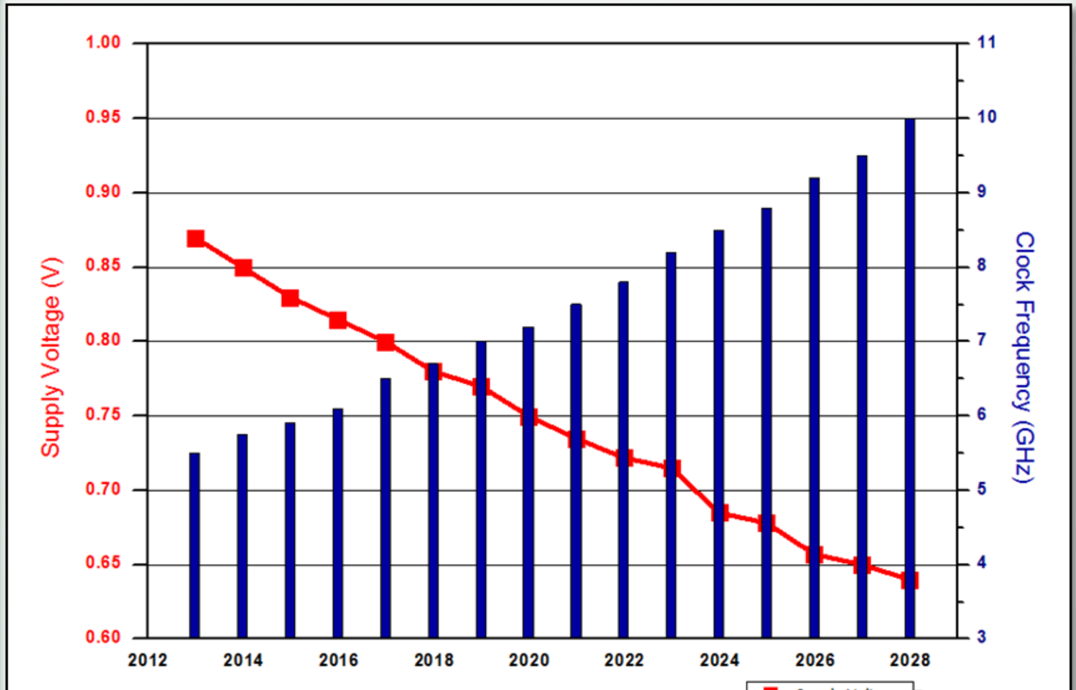
Overview

- *Introduction of Probe Card Test*
- *Basic Study for Power Integrity*
- *Power Integrity on Probe Card*
- *Summary*
- *Future Works*

Introduction of Probe Card Test

• *Increased Nosie Issue at Low Power and High Speed*



Ref. International Technology Roadmap for Semiconductor 2015 (ITRS)

Fig. Predicted Trends of the Supply Voltage and Clock Frequency

- ✓ *Supply Voltage decreases for Improving Device Reliability*
- ✓ *Low Power Consumption and Operation Requirement*
- ✓ *Noise Margin (Reducing of Supply Voltage)*
- ✓ *Timing Margin (Increasing of Clock Frequency)*

➢ ***Highly Design Consideration for Power Integrity on Probe Card***

Introduction of Probe Card Test

• *Memory Test Trends for Pad Pitch and Size*

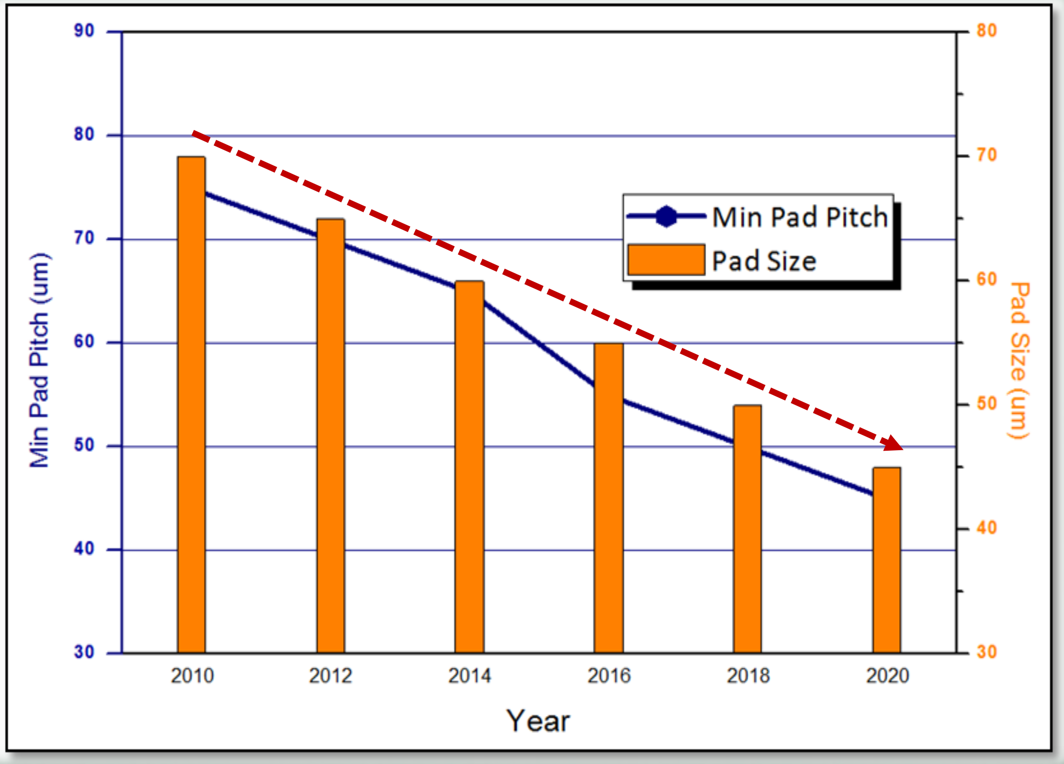


Fig. Predicted Trends of Pad Size and Pad Pitch

✓ *Shrink VIA Pad*

✓ *Increase Circuit Density*

✓ *To be Fine Pitch*

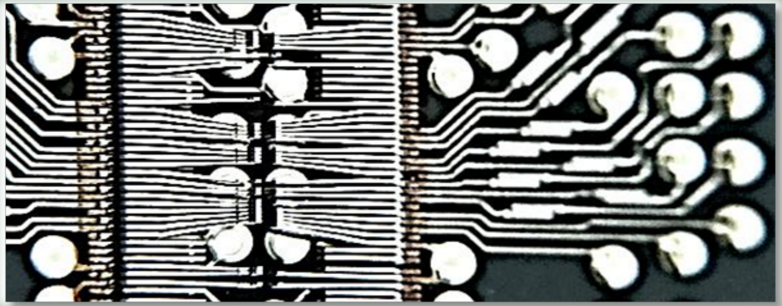


Fig. Probe of Multilayer Ceramic (STF)

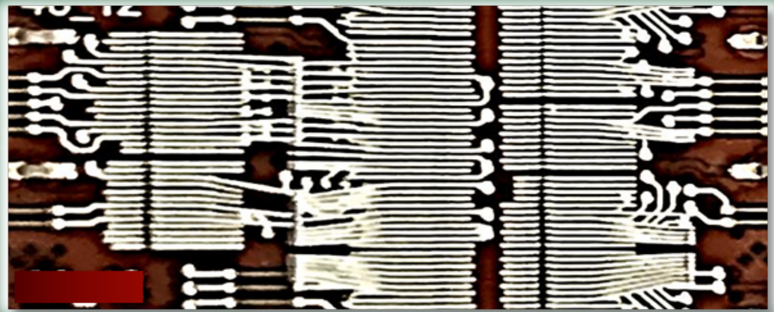
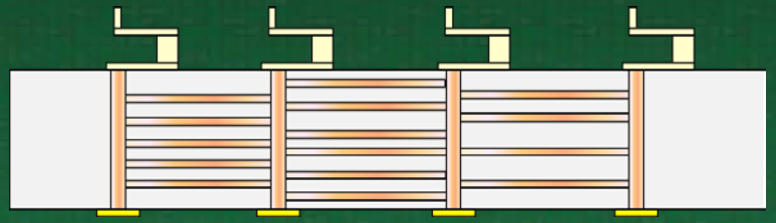
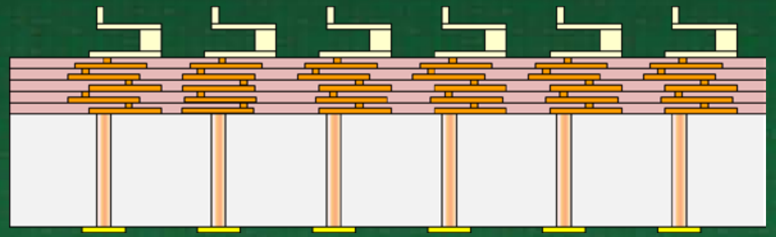


Fig. Probe of Polyimide Circuit (STF)

➢ ***Needs for High Density Circuit and Fine Pitch Design on Probe Card***

Introduction of Probe Card Test

- Different Types of Circuit Design on Space Transformer

Type A		Type B	
Type A Multi-Layer Ceramic (Space Transformer)		**Type B** Polyimide Thin Film With Ceramic (Space Transformer)	
	➢ Fine Pitch ★★★ ➢ Circuit Density ★★★ ➢ Technology ★★★		➢ Fine Pitch ★★★★★ ➢ Circuit Density ★★★★★ ➢ Technology ★★★★★
	▪ Multi-Layer Ceramic (Space Transformer) ▪ Power Plane, Ground Plane, Signal Trace ▪ Normal Type (Limit of High Parallel Device/DUT) ▪ Available for using Polyimide Thin Film on STF (Called it 'Hybrid' Type)		▪ Polyimide Circuit + Ceramic (Space Transformer) ▪ Power (Mesh/Trace), Ground (Mesh), Signal Trace ▪ Signal/Power Re-distribution on Polyimide Thin Film ▪ Highly Denser Circuit and Small VIA PAD on Polyimide Thin Film (For Fine Pitch)

Introduction of Probe Card Test

- *Power Delivery on Probe Card and Equivalent Circuit*

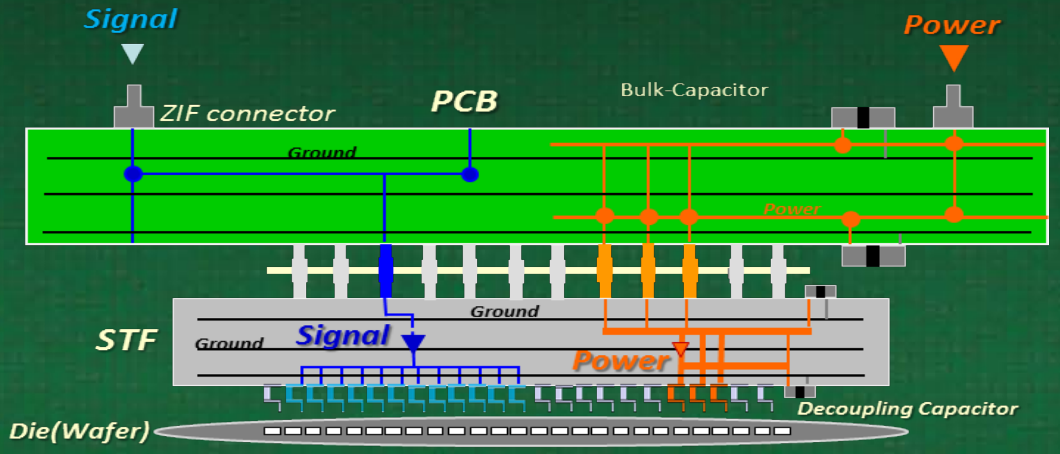


Fig. Power Delivery of Probe Card

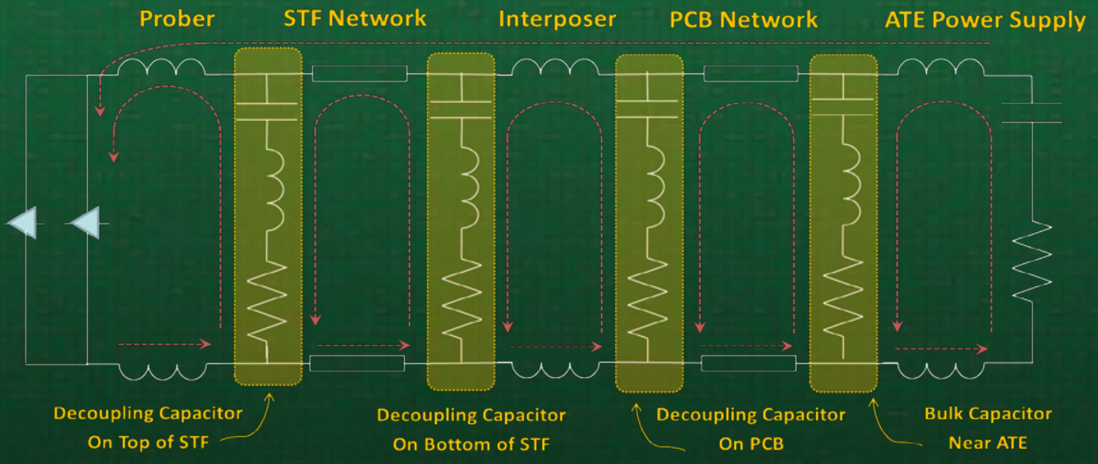


Fig. Equivalent Circuit of Probe Card

- ✓ *Low Impedance Path of Current flow at working Frequency*
- ✓ *Target Impedance using Decoupling Capacitor*
- ✓ *Low Inductance Capacitor on Space Transformer*
- ✓ *Design Consideration of Power and Ground*

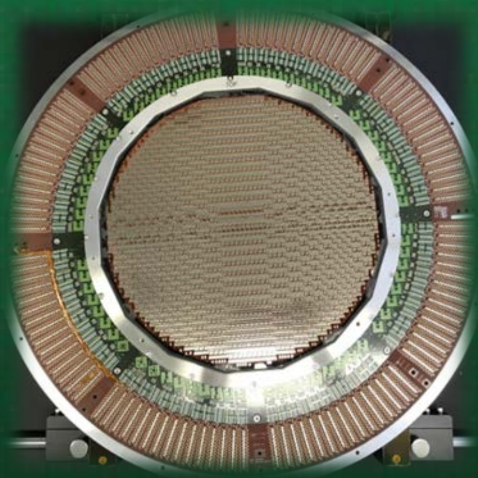
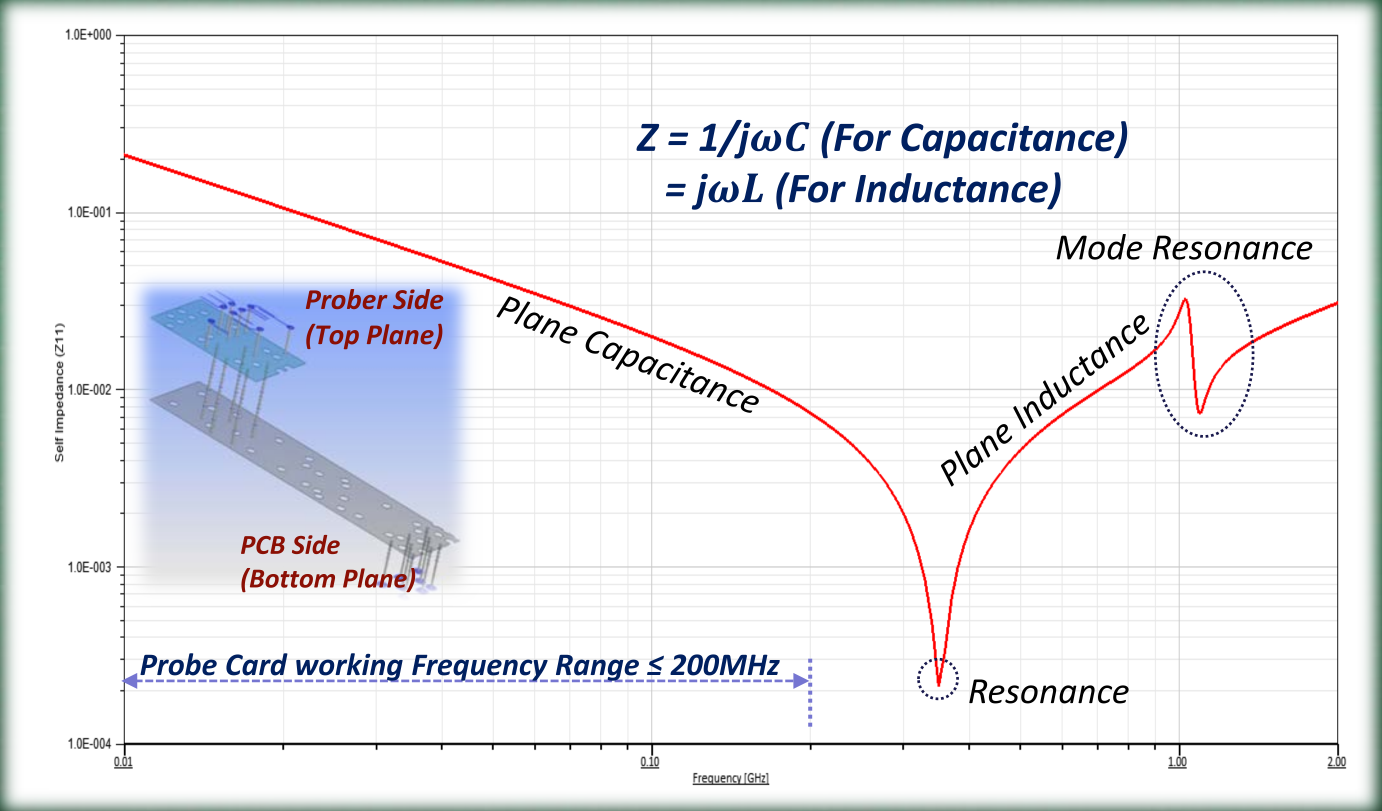


Fig. Probe Card Assembly

Basic Study for Power Integrity

- *Power Impedance Characteristics on Space Transformer (w/o De-cap)*



- ✓ *STF Power Plane (Top/Bottom)*
- ✓ *Power Impedance without De-capacitor*
- ✓ *Similar Characteristics like De-capacitor*
- ✓ *Plane Capacitor and Plane Inductor*

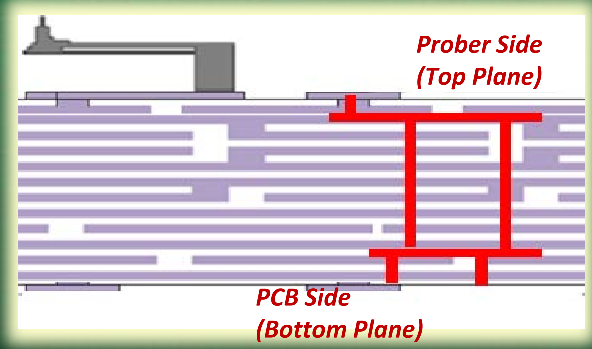


Fig. Side View of PDN on Probe Card

Basic Study for Power Integrity

- *Decoupling Capacitor and Target Impedance*

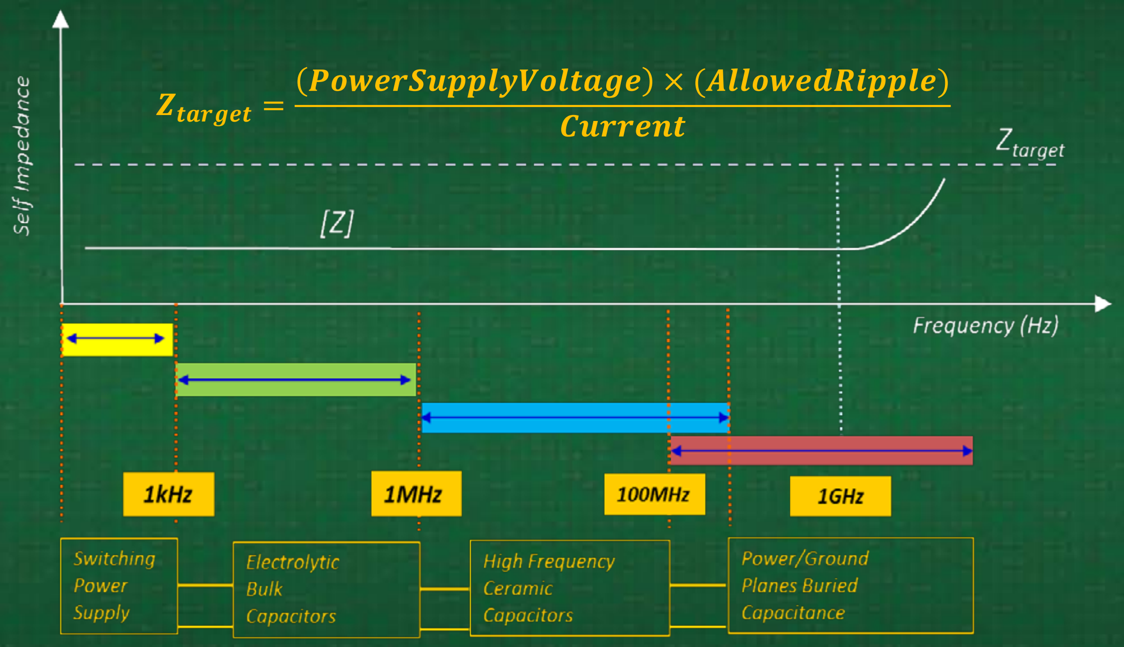
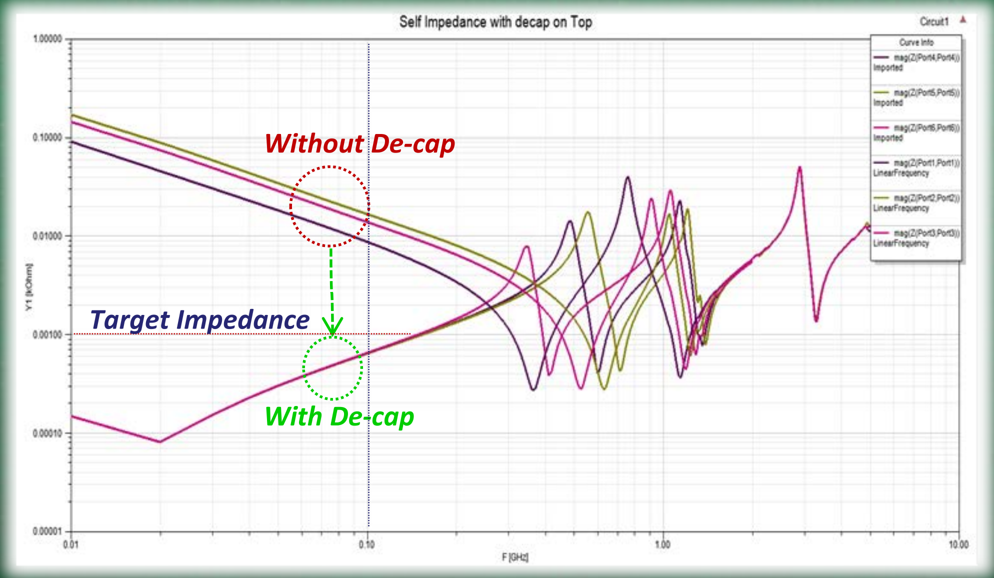


Fig. Target Impedance with Decoupling Capacitor

Example) $Vdd = 1V$, ΔI = 50mA , Voltage Tolerance 5%

$$Z_{target} = \frac{1 \times 0.05V}{50mA} = 1\ \Omega$$



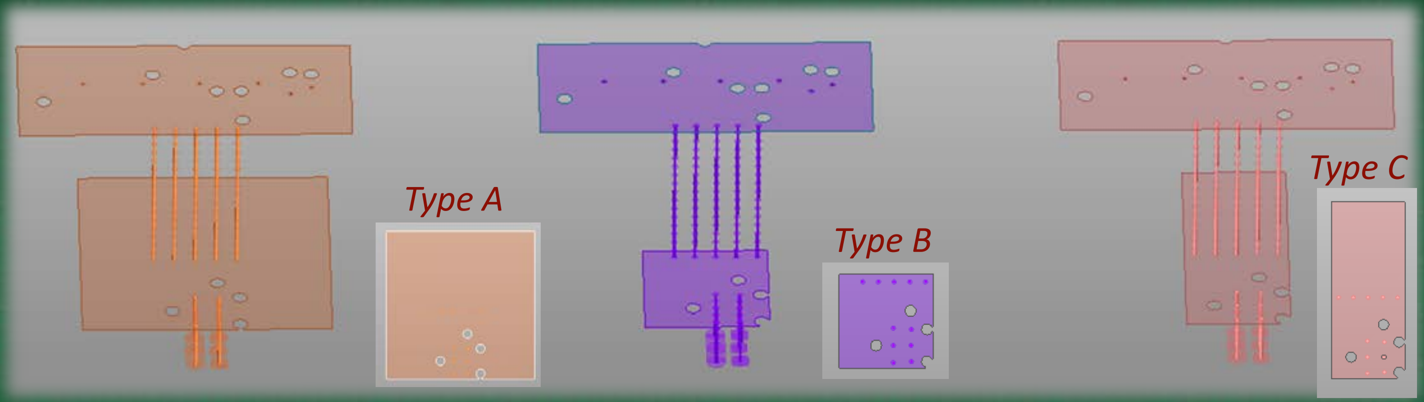
✓ Various of De-capacitors have own Characteristics at Frequency.

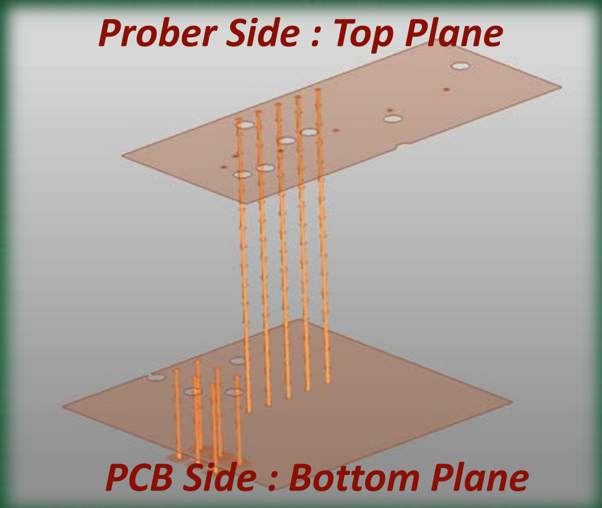
✓ Target Impedance is the ratio of Voltage to Current.

✓ Low Impedance implies Large Capacitance and Low Inductance.

Power Integrity on Probe Card

- *Impedance Analysis for Different Size of Power Plane on Space Transformer*





Top Power Plane / Bottom Power Plane

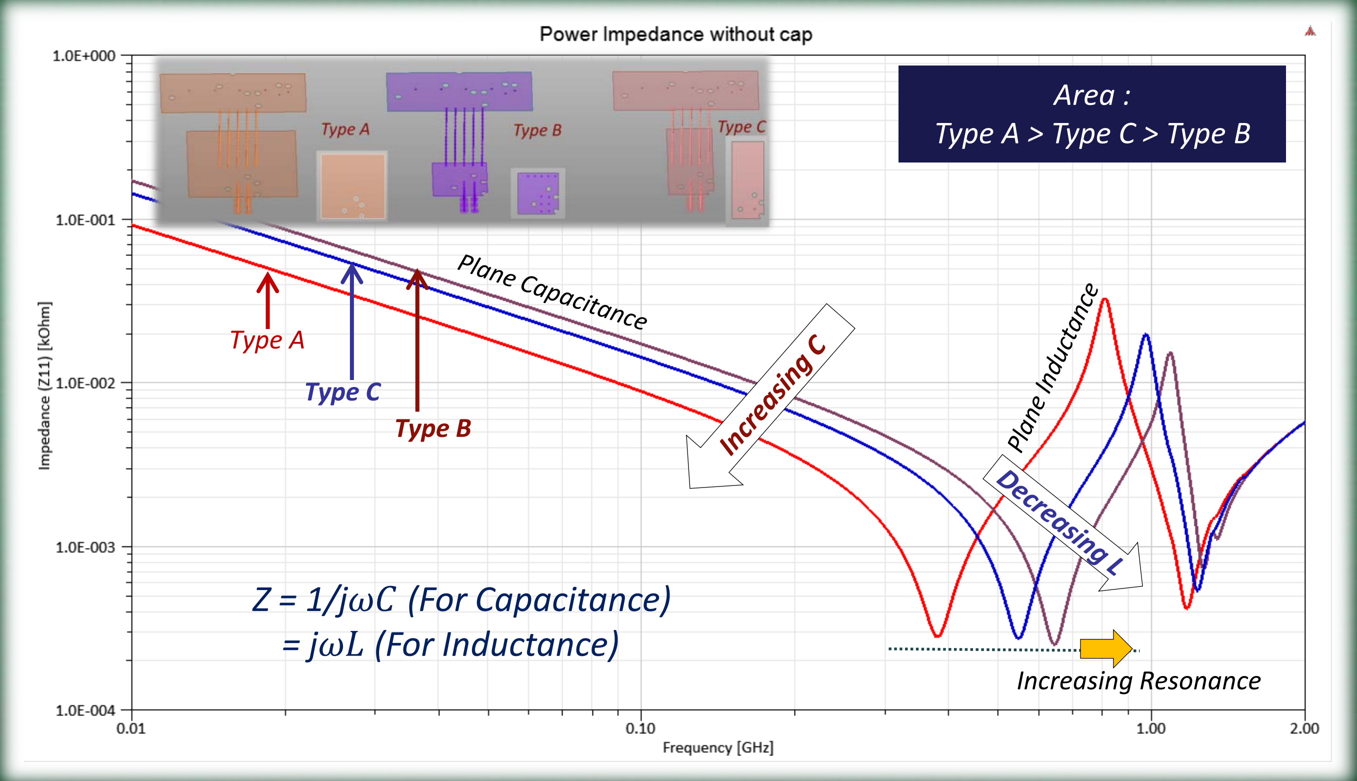
Type A	Type B	Type C
▪ Top Plane Size : 16mm x 16mm ▪ Bottom Plane Size : 12 mm x 12 mm	▪ Top Plane Size : 16mm x 16mm ▪ Bottom Plane Size : 6 mm x 6 mm	▪ Top Plane Size : 16mm x 16mm ▪ Bottom Plane Size : 6 mm x 12 mm

✓ *Impedance Analysis for Different Size of Bottom Power Plane*

✓ *Analysis for Plane Capacitance and Plane Inductance*

Power Integrity on Probe Card

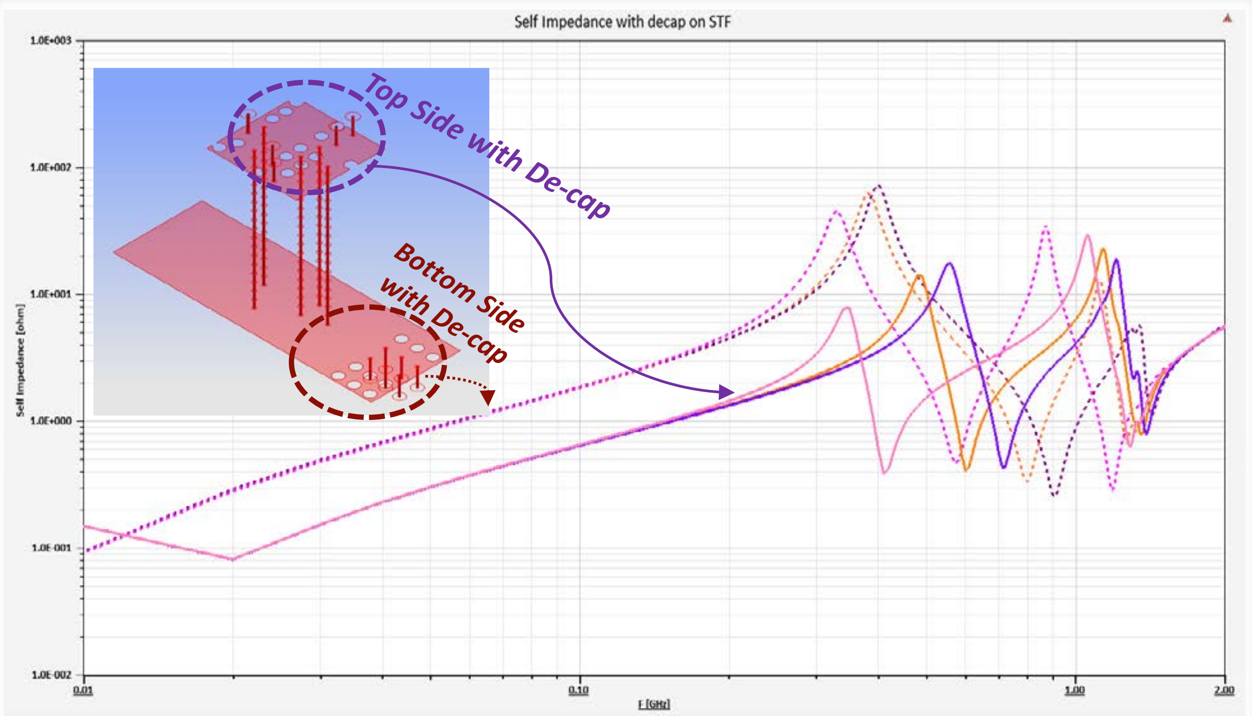
- *Impedance Analysis for Different Size of Power Plane on Space Transformer (w/o De-cap)*



- ✓ *As Power Plane Size is large, the Plane Capacitance is increasing.*
- ✓ *As Power Plane Size is small, the Plane Inductance is decreasing.*
- ✓ *As Power Plane Size is small, the Resonance is increasing.*

Power Integrity on Probe Card

- *Impedance Analysis for Different Size of Power Plane on Space Transformer (with De-cap)*



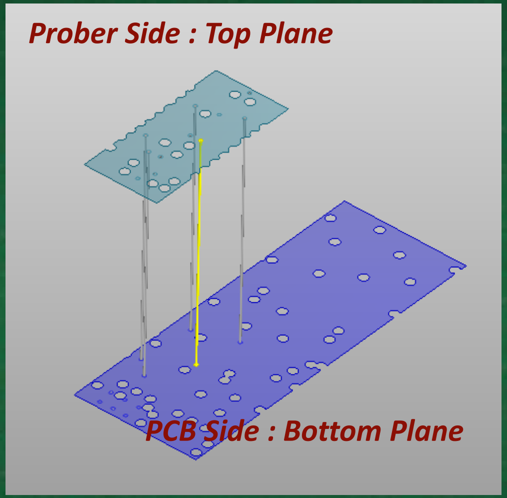
[The Effect of Decoupling Capacitor]

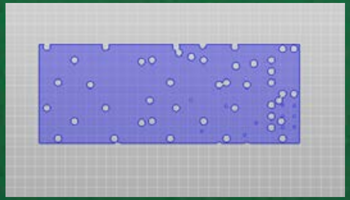
- ✓ *Lower Impedance between Power and Ground Reference Planes.*
- ✓ *Reduce/Eliminate Plane resonances.*
- ✓ *The Power Impedance depends on the Position.*
- ✓ *Top side of De-cap is much more Effective than Bottom side of De-cap.*

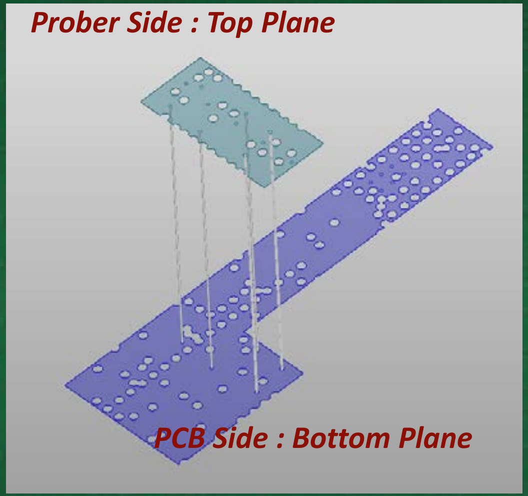
- ✓ *De-cap can make Low impedance at Working Frequency Regardless of Plane Size.*

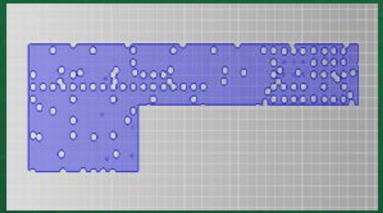
Power Integrity on Probe Card

- Impedance Analysis for Different Shape of Power Plane on Space Transformer









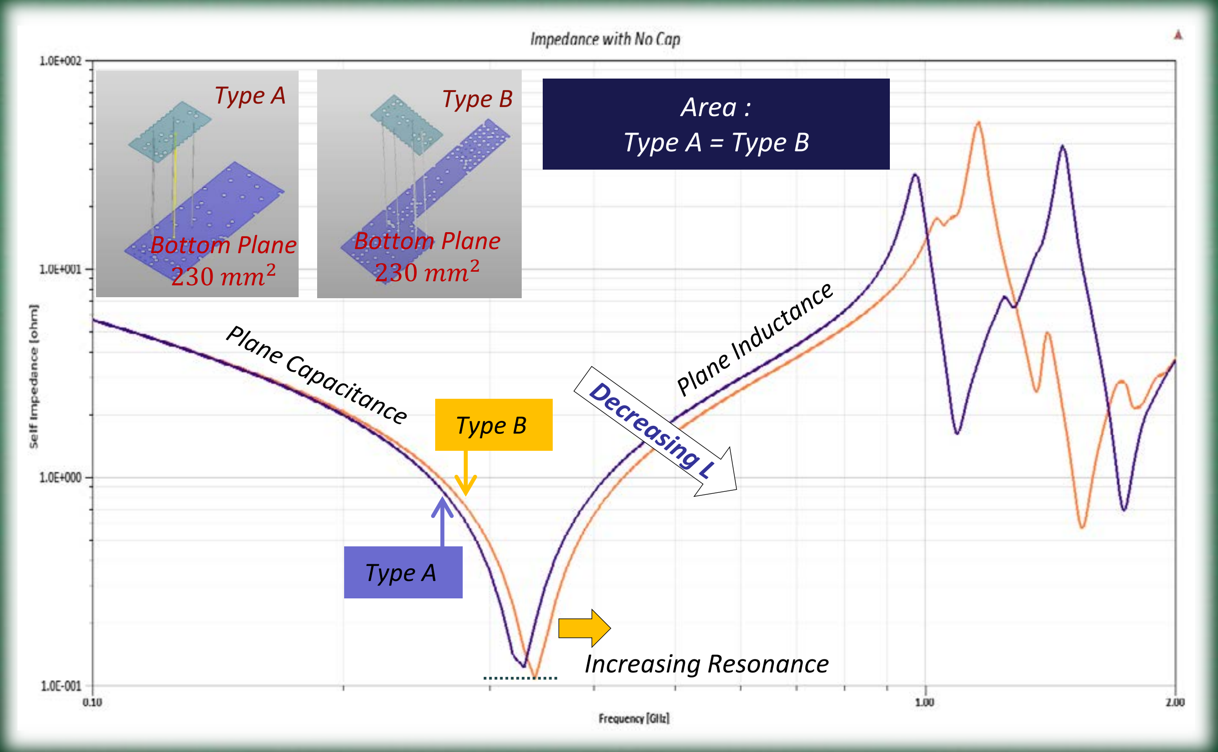
- Impedance Analysis for Different Shape of Bottom Power Plane
- Analysis for Plane Capacitance and Plane Inductance

■ Top Power Plane / Bottom Power Plane

Type A	Type B
▪ Power Top Plane Area : 64 mm^2 ▪ Power Bottom Plane Area : 230 mm^2	▪ Power Top Plane Area : 64 mm^2 ▪ Power Bottom Plane Area : 230 mm^2

Power Integrity on Probe Card

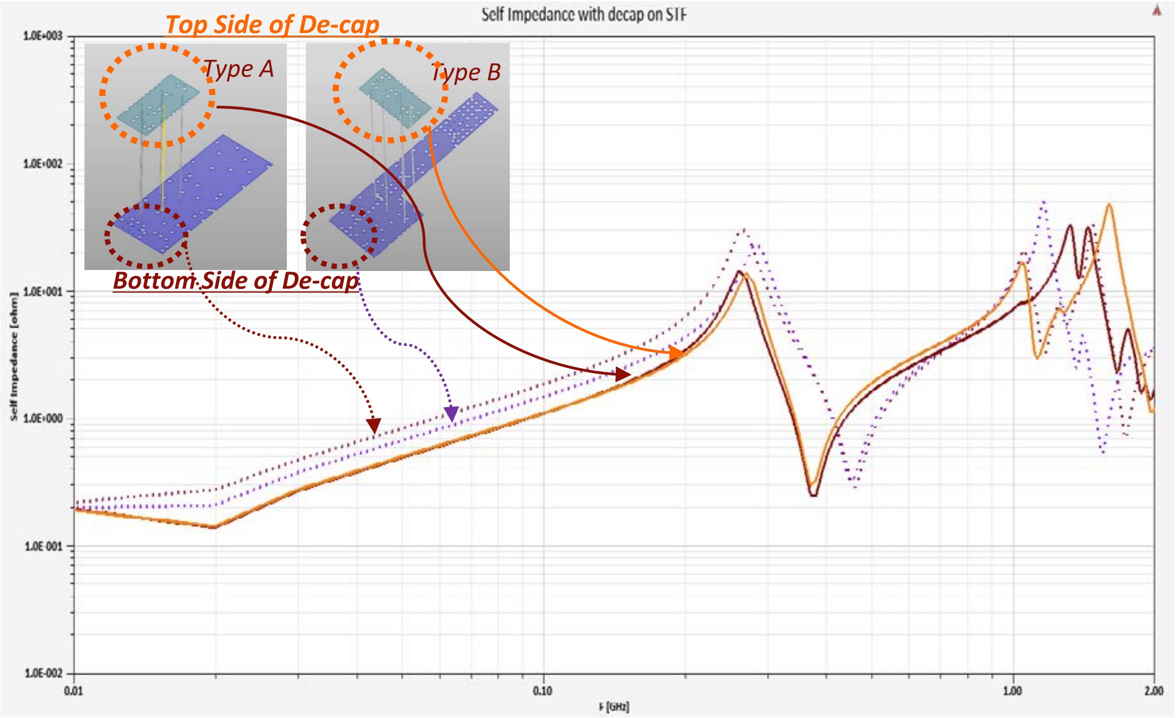
- *Impedance Analysis for Different Shape of Power Plane on Space Transformer (w/o De-cap)*



- ✓ *For Different Shape of Power Plane, these have similar Plane Capacitance.*
- ✓ *Plane Inductance have a little differences between these 2 cases.*
- ✓ *The Resonance is Increasing slightly.*

Power Integrity on Probe Card

- *Impedance Analysis for Different Shape of Power Plane on Space Transformer (with De-cap)*



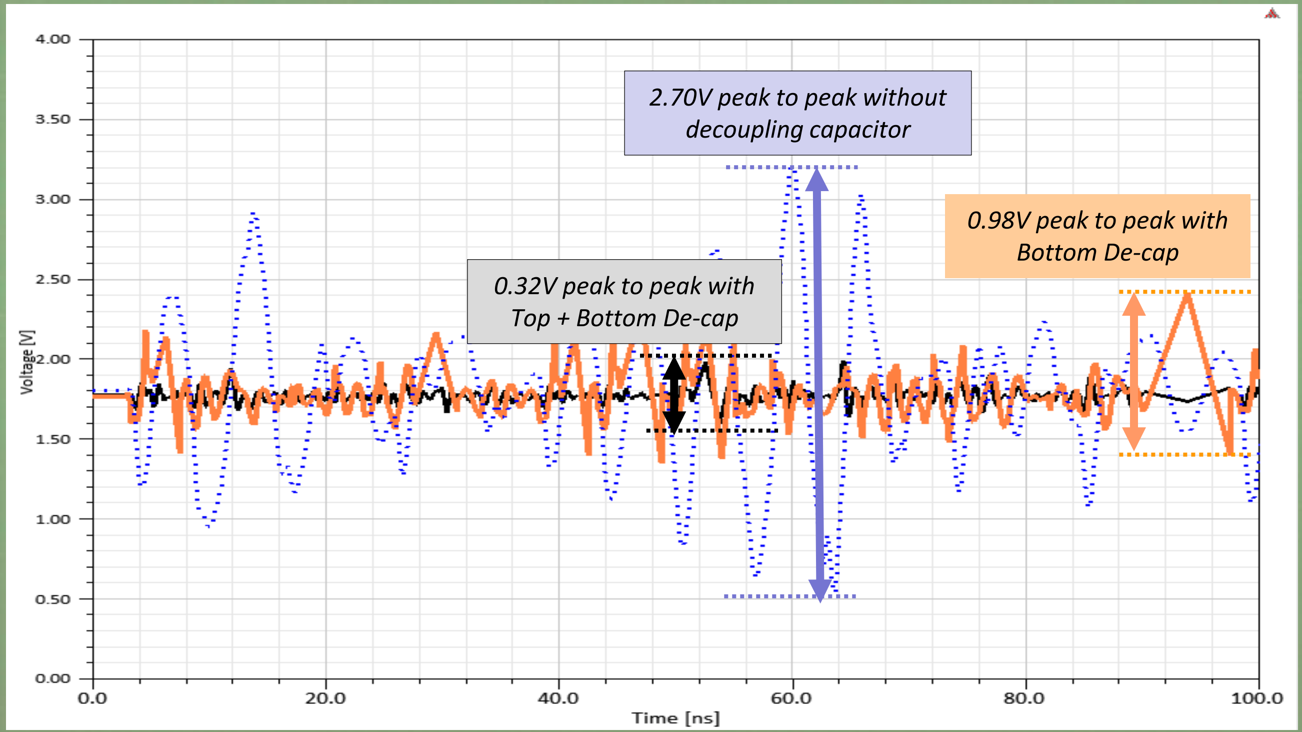
[The Effect of Decoupling Capacitor]

- ✓ *Lower Impedance between Power and Ground Reference Planes.*
- ✓ *Reduce/Eliminate Plane resonances.*
- ✓ *The Power Impedance depends on the Position.*
- ✓ *Top side of De-cap is much more Effective than Bottom side of De-cap.*

➢ *De-cap can make Low Impedance at working Frequency Regardless of Plane Shape.*

Power Integrity on Probe Card

• *Decoupling Capacitor Effect of SSN Voltage on Space Transformer*



[Simulation Conditions]

- ✓ DRAM DDR2 IBIS Model
- ✓ Time Domain Analysis
- ✓ Decoupling Capacitor Effect depends on Position.
- ➢ De-cap decreased Voltage Fluctuation and Noise as changing De-cap Position.

- Simultaneous Switching Noise (SSN)

$$\Delta V = L\frac{\Delta I}{\Delta t}$$

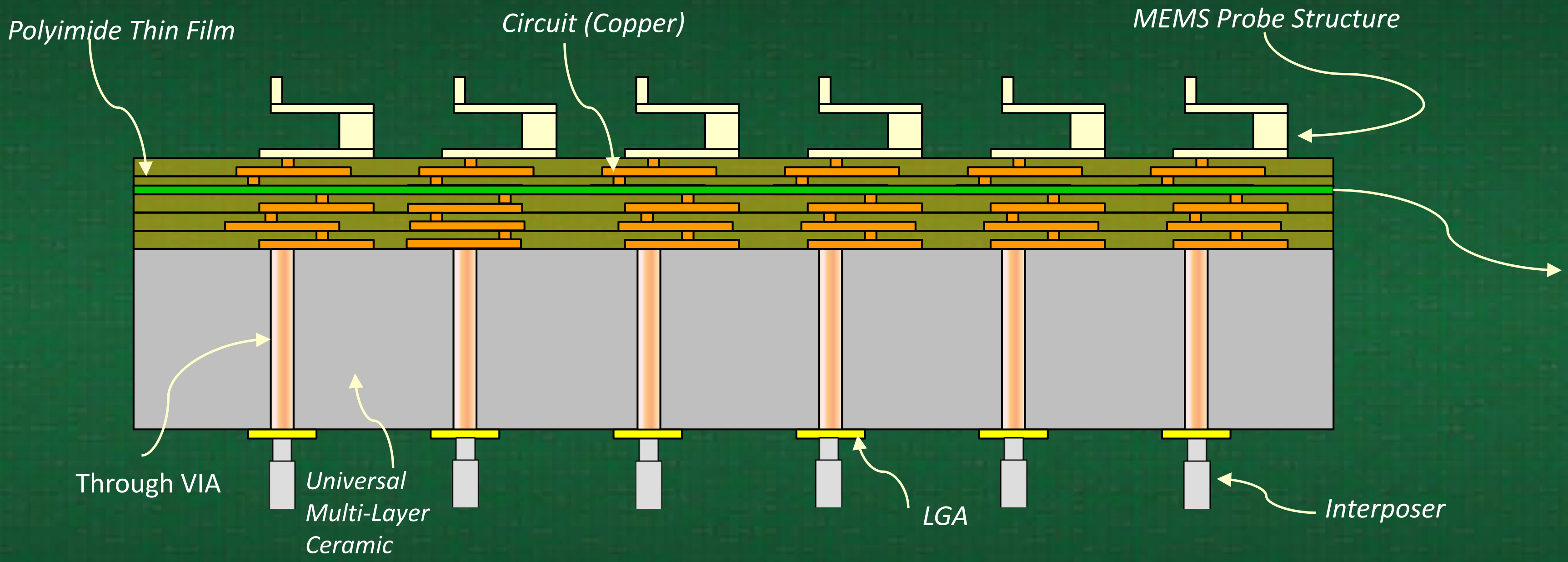
: ΔI : Increase of Maximum Power (Current)

: Δt : Increase of Clock Frequency

- SSN cause by Simultaneous Switching Output Buffers

Power Integrity on Probe Card

- *Space Transformer Circuit Design Concept on Polyimide Thin Film*



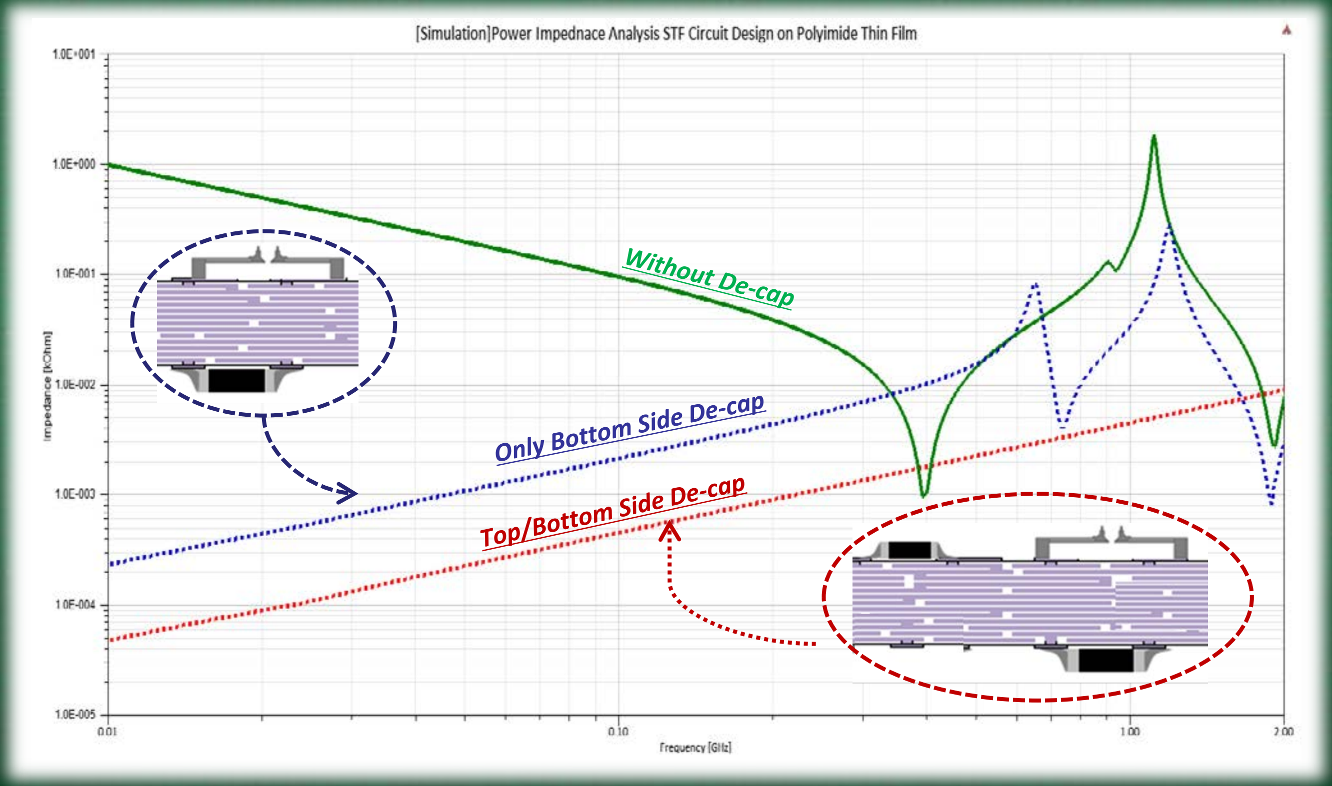
Signal / Power / Ground Layer

1. *Signal Impedance 50 ohm*
2. *Low Power Impedance*

- *STF Consists of Universal Multi-Layer Ceramic and Polyimide Thin Film.*
- *Circuit Design on Polyimide Thin Film is made by MEMS Process.*
- *Probe Structure is built up by 3D MEMS (Layer by Layer)*

Power Integrity on Probe Card

- PDN Impedance characteristics on Space Transformer (with Polyimide)



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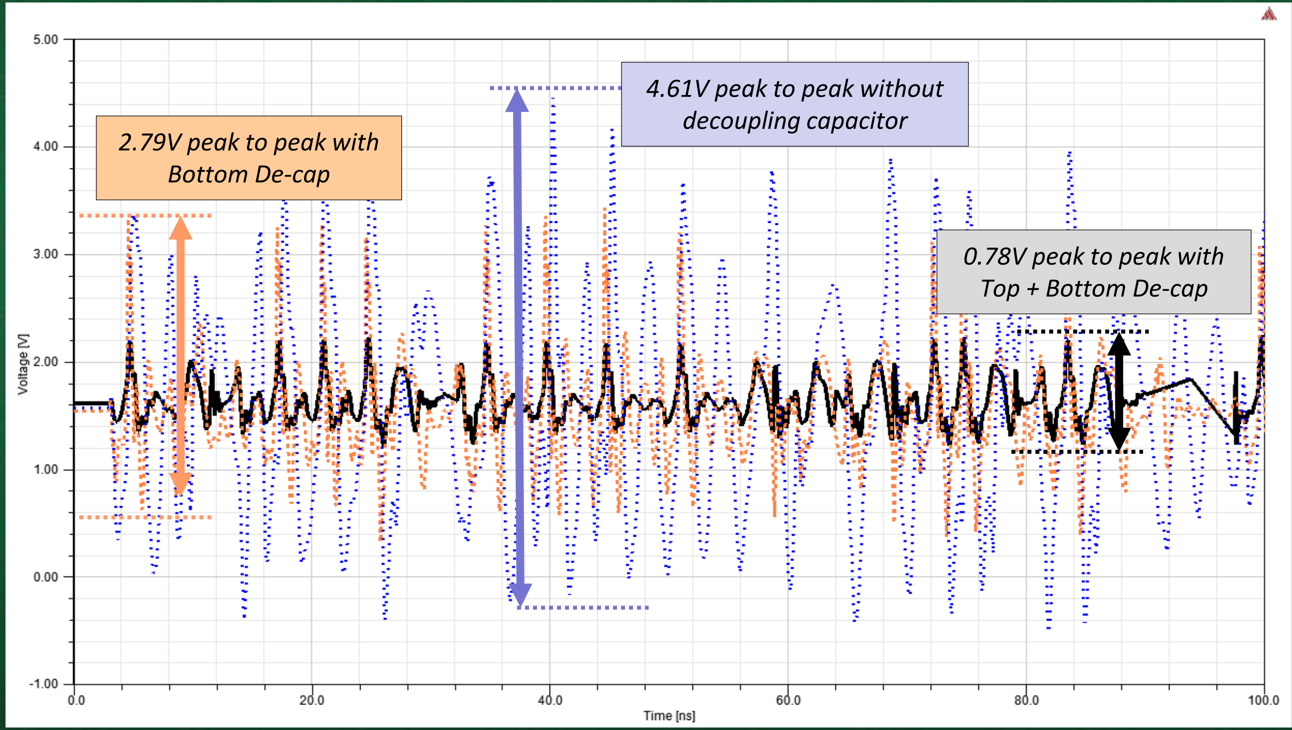
Power Integrity on Probe Card

- *Decoupling Capacitor Effect of SSN Voltage on Space Transformer (with Polyimide)*



[Simulation Conditions]

- ✓ DRAM DDR2 IBIS Model
- ✓ Time Domain Analysis
- ✓ Decoupling Capacitor Effect depends on Position.
- ➢ De-cap decreased Voltage Fluctuation and Noise as changing De-cap Position.

- Simultaneous Switching Noise (SSN)

$$\Delta V = L\frac{\Delta I}{\Delta t}$$

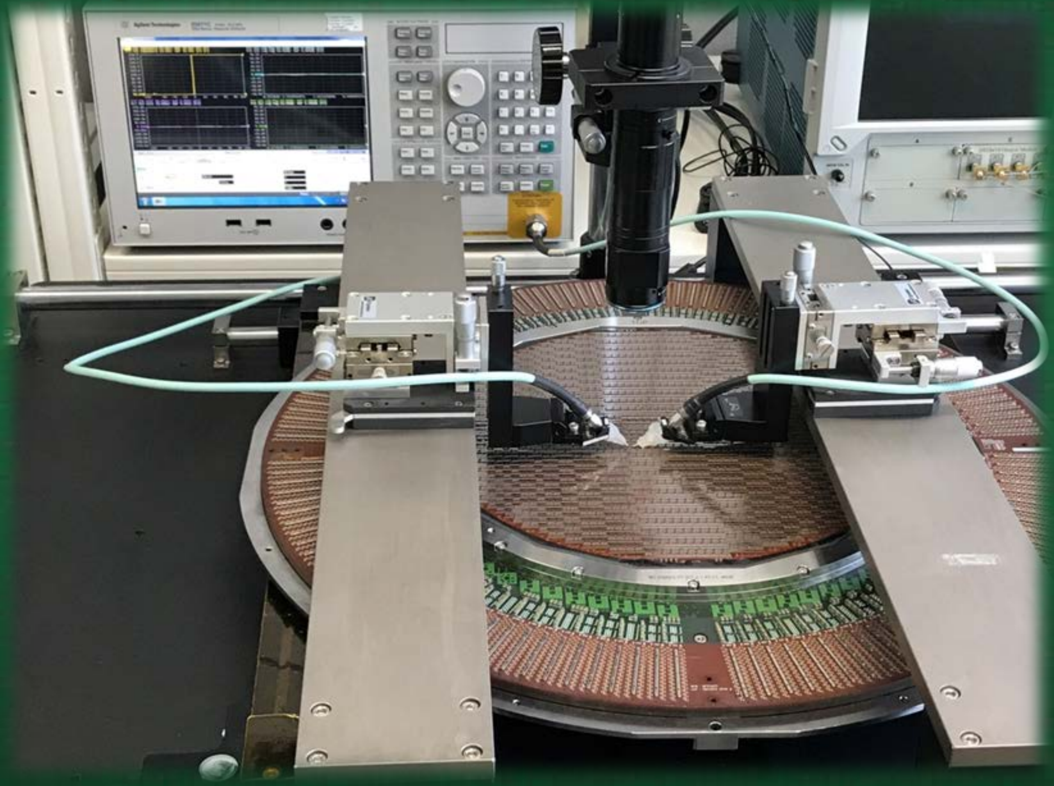
: ΔI : Increase of Maximum Power (Current)

: Δt : Increase of Clock Frequency

- To Reduce SSN, Inductance needs to be Controlled.

Power Integrity on Probe Card

- *Measurement Setup to Analyze Power Impedance on Probe Card*

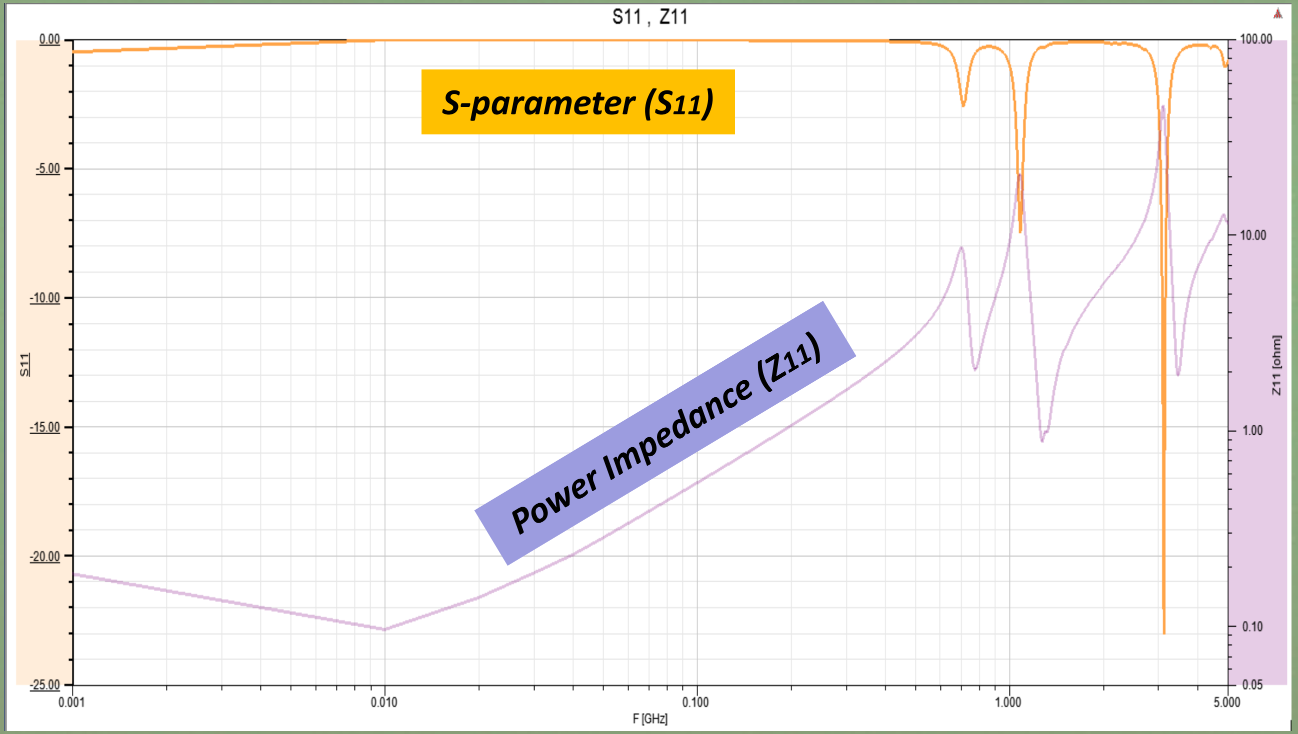


- ✓ *Vector Network Analyzer (≤8GHz)*
- ✓ *RF Probe (≤15GHz)*
- ✓ *Probe Station (2-Dimension)*
- ✓ *Microscope (x20)*
- ✓ *Probe Card (PCB+STF Assembly)*

➢ *S-parameter → Z-parameter (Z11)*

Power Integrity on Probe Card

- *Relationship between S-parameter and Z-parameter*



- ✓ *Reverse Pattern of 2 parameters between Resonance and Impedance*
- ✓ *Resonance makes High Impedance*
- ✓ *S-parameter (S_{11}) → Z-parameter (Z_{11})*

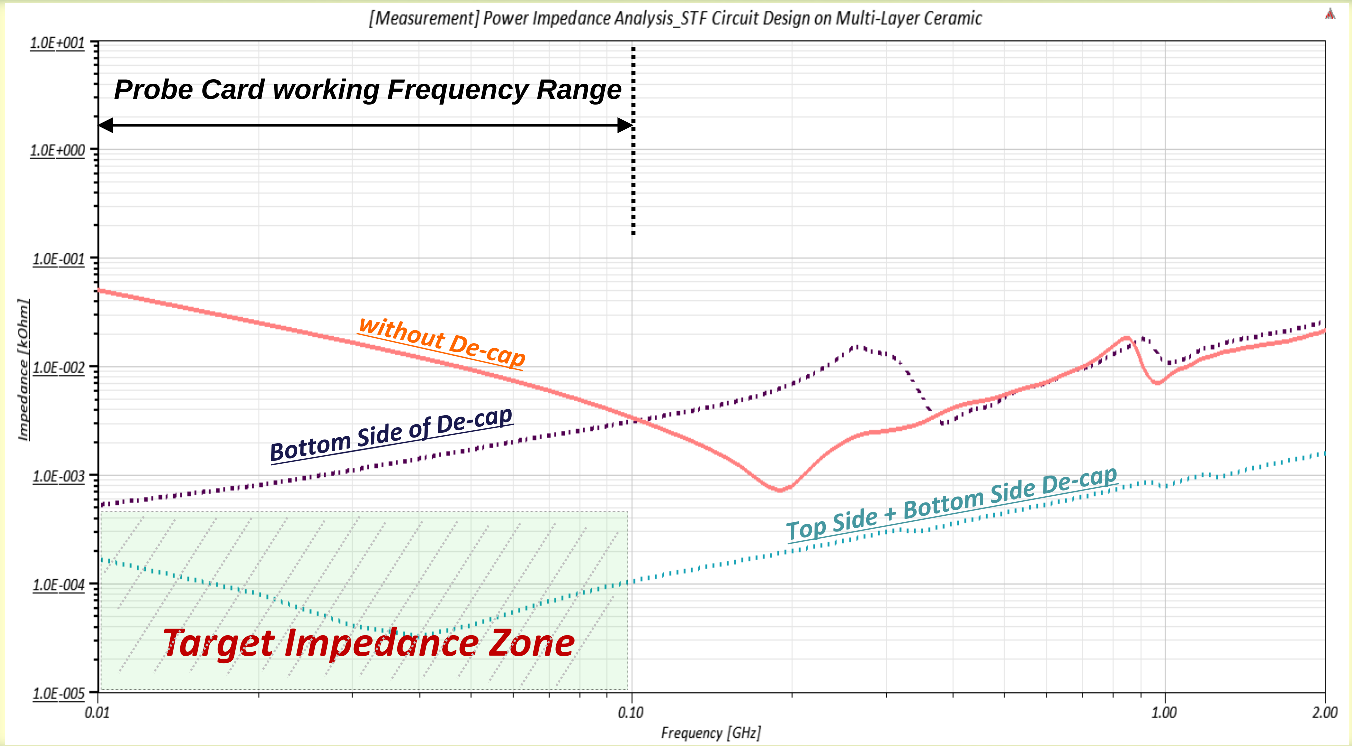
➢ ***Self Impedance (Input Impedance)***

Z_{11} ➔ **Dominant**

$$Z_{11} = \frac{[(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}]}{[(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}]} Z_0$$

Power Integrity on Probe Card

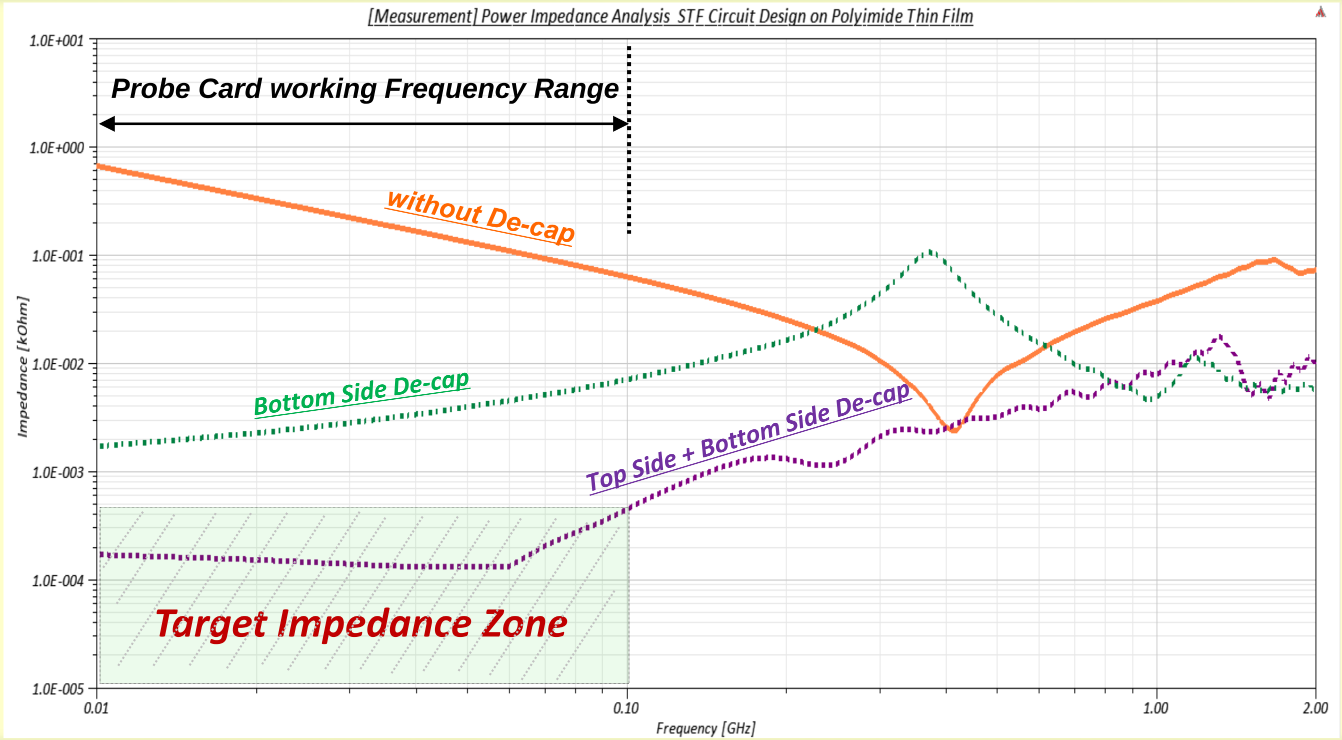
- *[Measurement] Power Impedance Analysis on Space Transformer (w/o Polyimide)*



- ✓ *De-cap can make Low Impedance at working Frequency Regardless of Plane Size or Shape.*
- ✓ *Large number of De-caps affect Resonance and Impedance.*
- ✓ *Matching Target Impedance is available for placing De-cap on Top and Bottom side.*

Power Integrity on Probe Card

- *[Measurement] Power Impedance Analysis on Space Transformer (with Polyimide)*



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- ✓ *Large number of De-caps affect Resonance and Impedance.*
- ✓ *Matching Target Impedance is available for placing De-cap on Top and Bottom side.*

SUMMARY

- ✓ *Basic Study for **Power Impedance** on Space Transformer has been performed.*
- ✓ ***Power Integrity** has been analyzed both Normal Space Transformer and Polyimide Space Transformer using method of Simulation and Measurement.*
- ✓ *Satisfaction for **Target Impedance** with Decoupling Capacitors which Impedance depends on position and Top Size of De-cap is much more effective for Lowering Impedance.*

FUTURE WORKS

- ✓ ***The Electrical Characteristics*** *for Probe Card Circuit designed by Polyimide + Multi-Layer Ceramic (Called it 'Hybrid type space transformer').*

- ➢ *Could have many Issues because of large number of discontinuity points from Multi-Layer Ceramic to Polyimide Circuit.*

  *- Analysis of **Signal Integrity** (Impedance, Eye-Diagram, Crosstalk…)*

  *- Analysis of **Power Integrity** (Power Impedance, Target Impedance, SSN…)*

Acknowledgements

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- *SANG-KYU YOO*
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- *YONG-HO CHO*
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- *HUN-SOO KIM*
- *SUNG-WOONG LEE*

- *JONG-GWAN YOOK*
- *HO-SUNG LEE*

Thanks for Your Attention !