SWTW 2-0-1-7

SW Test Workshop

Semiconductor Wafer Test Workshop

# A Full-Automatic Test System for Characterizing Large-Array Fine-Pitch Micro-Bump Probe Cards

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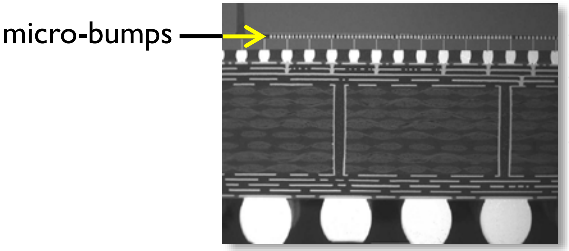
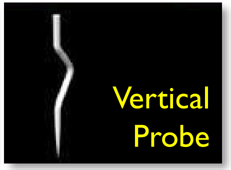
# Direct Micro-Bump Probing

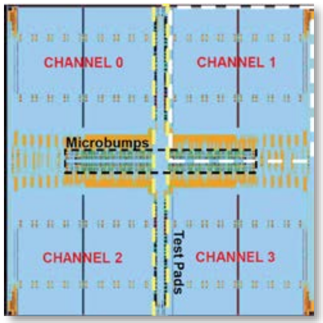


[Xilinx, 3D-TEST'12]

- Functional interconnects of 3D-stacked dies are formed by large arrays of fine-pitch micro-bumps
- Impossible to probe with conventional probe technology
  - Cantilever probes : cannot handle arbitrary arrays
  - Vertical probes : cannot handle the fine pitch



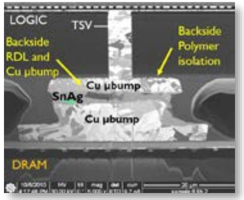
- Options for pre-bond test
  1. Skip pre-bond test: poor compound stack yield; higher cost
  2. Dedicated pre-bond probe pads: extra design, area, test time, post-bond load; and micro-bumps remain untested
  3. Use advanced probe technology to probe micro-bumps



[Samsung, ISSCC'11]

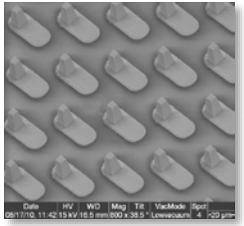
# Related Prior Work

- **SWTW’11**: Marinissen et al. *(imec + Cascade Microtech)*
  Imec and Cascade started collaboration, defined probe targets



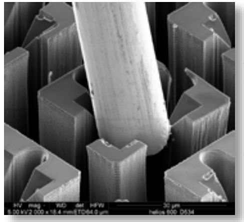
[SWTW’11]

- **ITC’11**: Smith et al. *(Cascade Microtech + imec)*
  First collaboration results, mainly on probe technology



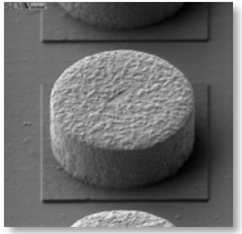
[ITC’11]

- **SWTW’13**: Böhm et al. *(Feinmetall + Team Nanotec + imec + FH + CM)*
  Silicon crown tips, embedded in vertical probe card with TSVs
  Most Inspirational Presentation Award, but no product follow-up



[SWTW’13]

- **ITC’14**: Marinissen et al. *(imec + Cascade Microtech + TU Delft)*
  - WIO1-1Bank: good $R_C$; no impact on bond yield; cost-effective
  - But... (i) only 1 Bank and (ii) only daisy-chains of 30 micro-bumps



[ITC’14]

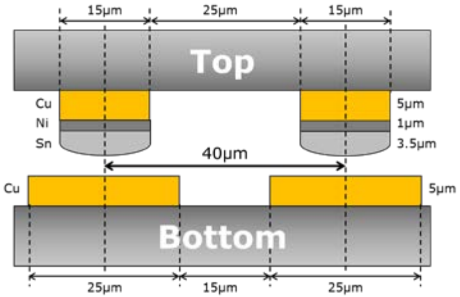
# Presentation Overview

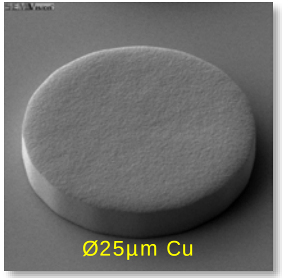
1. Introduction
2. Wide-I/O Micro-Bump Arrays
3. Vortex-2 Test System
4. Probe Technology
5. Test System Software
6. Experimental Results
7. Test Cost Comparison
8. Conclusion

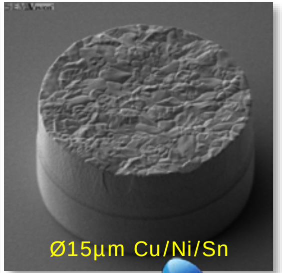
# What Do We Want To Probe?

## Micro-Bump Probe Targets

- imec's PoR @40µm pitch
- Today's advanced industry practice

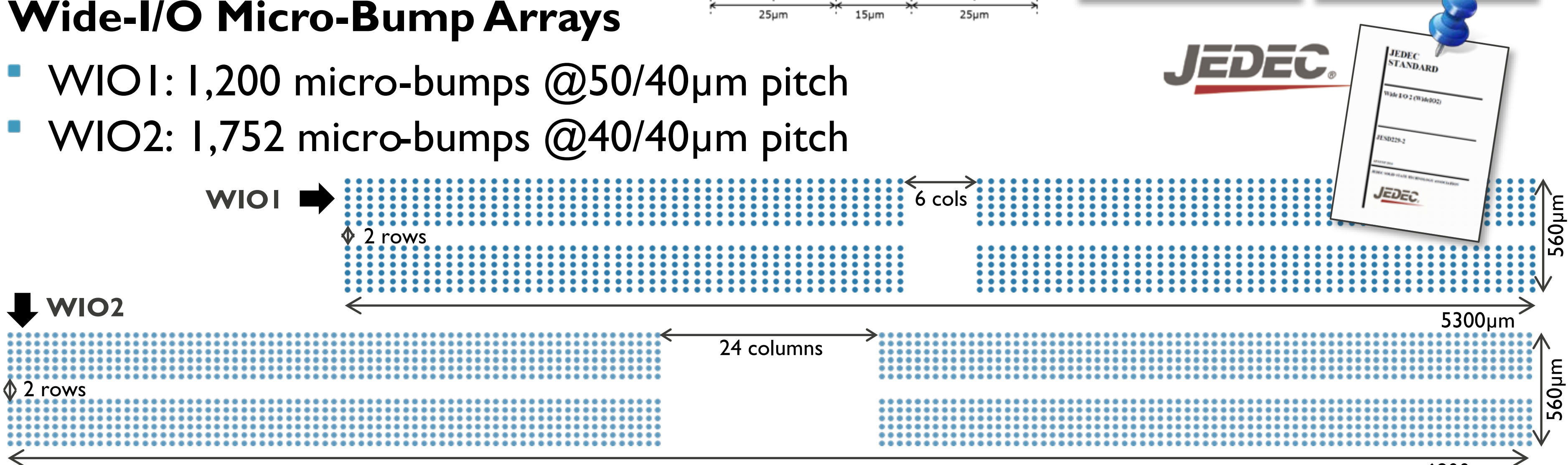






## Wide-I/O Micro-Bump Arrays

- WIO1: 1,200 micro-bumps @50/40µm pitch
- WIO2: 1,752 micro-bumps @40/40µm pitch



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# Vortex-2 Test System

**Vortex-2/2**

- micro-bump probing
- parametric testing

**MHU**

wafer
loader

**Vortex-2/1**

- low-leakage parametric testing

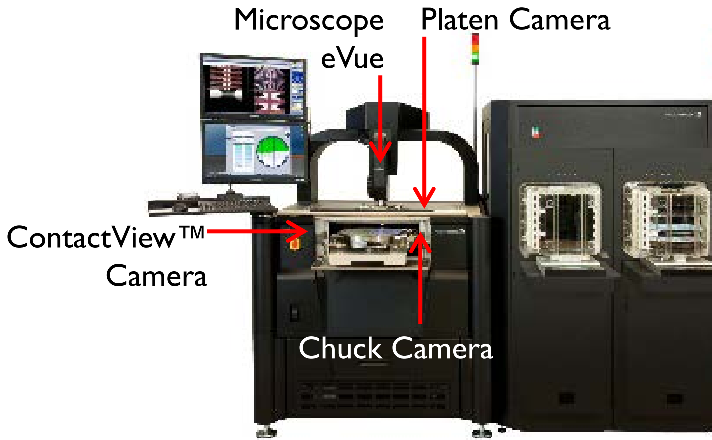
# Vortex-2: In-Line in imec's Fab-2

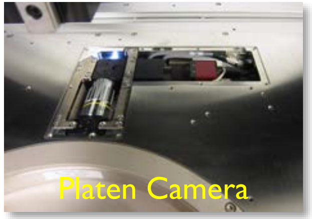
# Cascade Microtech CM300 Probe Station

- **Wafer Handling**
  - Full-automatic wafer loader (200/300mm)
  - Manual loading of tape frames
- **Thermal Control System**: -60...+200 °C
- **Four Cameras**

  ~~(1) eVue~~ ⬇ (3) Chuck ⬆

  (2) Platen ⬇ (4) ContactView™ ➡
- **Microscope Bridge Removed for Test Head**
  - Probe alignment with Platen and Chuck cameras only
  - Chuck needs to move between ‘Align’ and ‘Probe’ positions

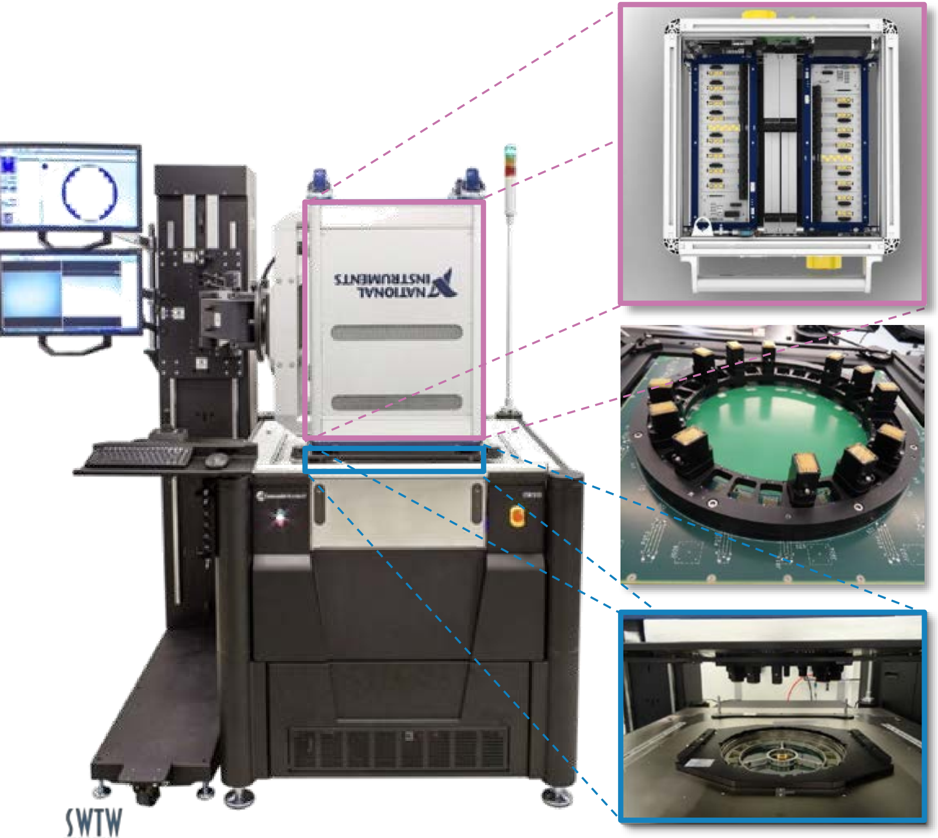


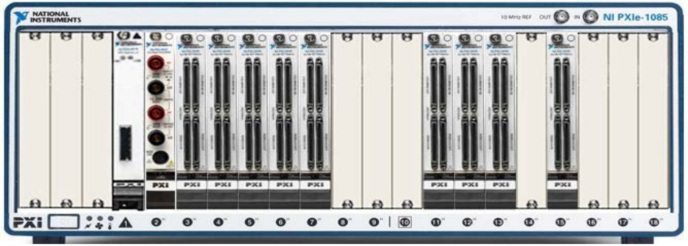

Platen Camera


Chuck Camera

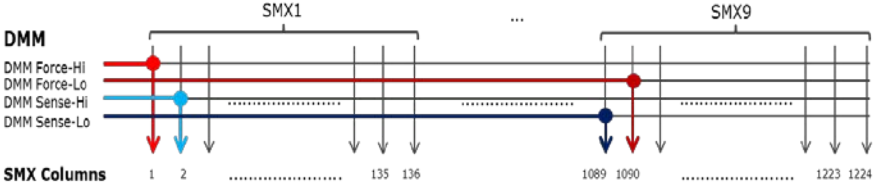

Test Head Docking

# National Instruments Semiconductor Test System



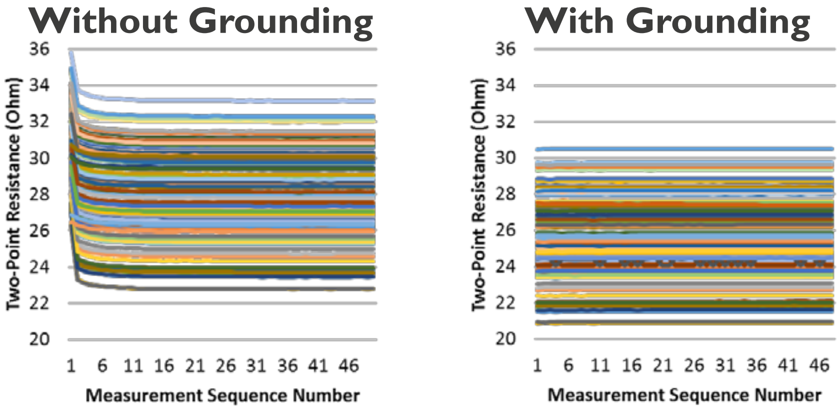


- PXI Rack: programmable Switch Matrix
  - 4 input rows driven by DMM
  - 9×136 = 1,224 output columns
- Two - and four-point *R* measurements
  - $R_{max}$ = 1,000 Ω @100 meas/second

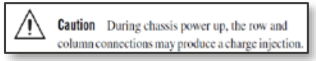


# Grounding the FET-Based Switch Matrix

- Wide-I/O Switch Matrix is composed of nine concatenated switch modules
  - 9×(4×136)= 4 rows × 1,224 columns
- NI's PXI-2535 FET-based SMX
  - Benefits
    - Low cost and unlimited life-time
    - All 544 switches can be "on"
  - Drawbacks
    - Significant leakage current
    - Charge injection during power-up



- NI knows issue (manual, website*), but leaves fix to user
  - We suggested programmable GND as feature in new NI SMX modules
- For now, we implemented aprog'able GND from probe card into SMX



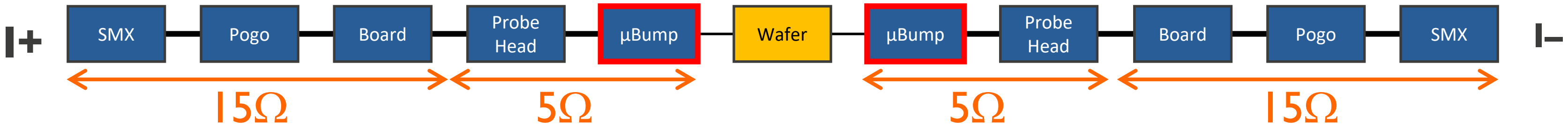
⚠ **Caution** During chassis power up, the row and column connections may produce a charge injection.

* NI website "Why do I get Incorrect Measurements when using the PXI-2535 or PXI-2536?"

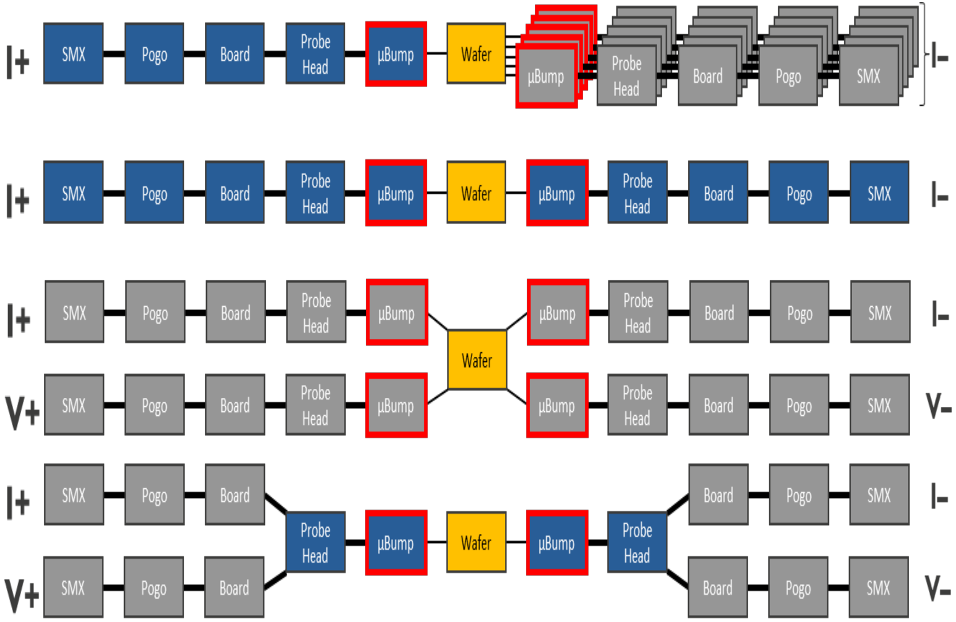
3.VORTEX-2 TEST SYSTEM

# Measurement Routines and Parasitics

▨ = excluded
🟦 = test system
🟨 = wafer
🟥 = probed



1. **Probe-Check** $R_{\text{parasitic}} \approx 20\Omega$
   - All probes shorted
2. **Two-Point** $R_{\text{parasitic}} \approx 40\Omega$
   - Micro-bump daisy-chain
3. **Four-Point** $R_{\text{parasitic}} \approx 0\Omega$
   - Requires four probed micro-bumps
4. **Pseudo Four-Point** $R_{\text{parasitic}} \approx 10\Omega$
   - Requires two channels per probe tip



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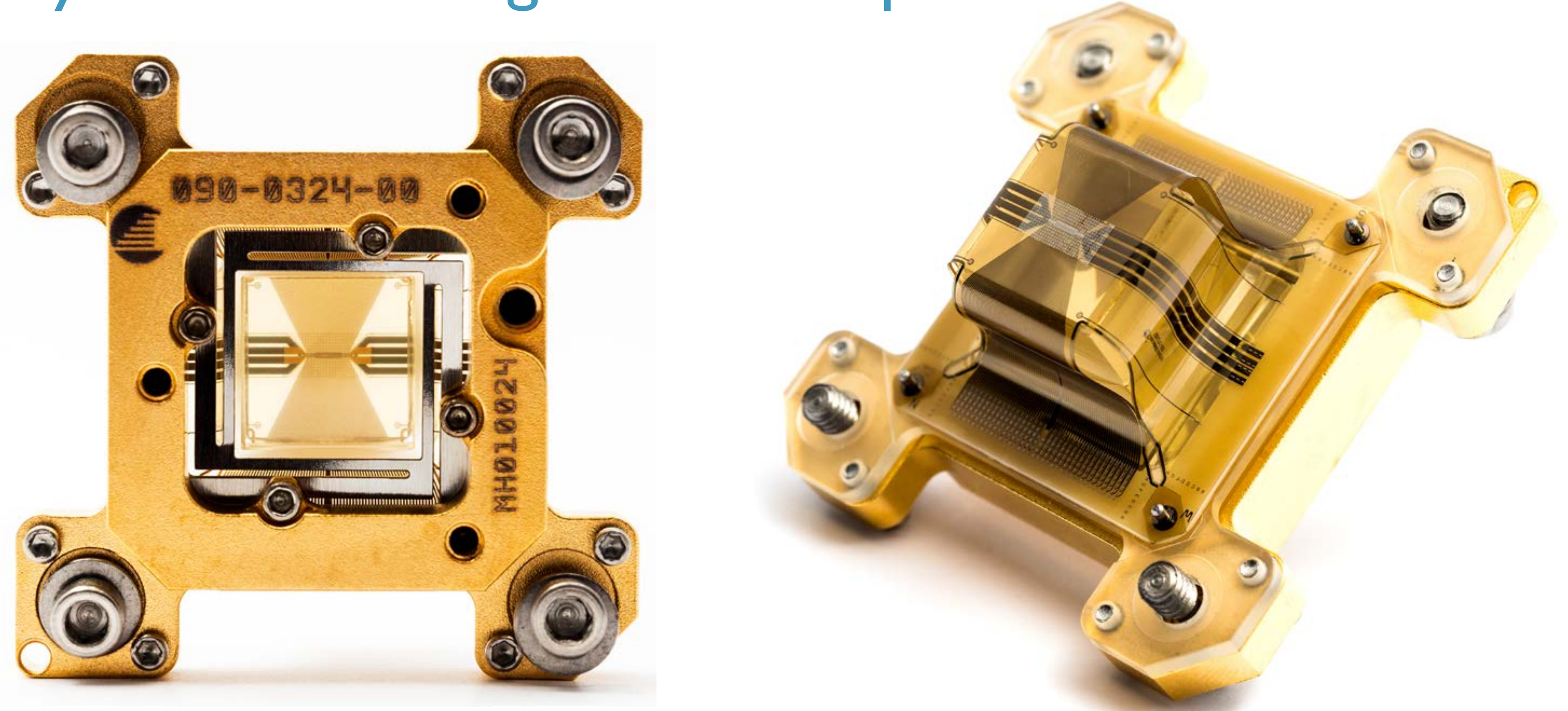
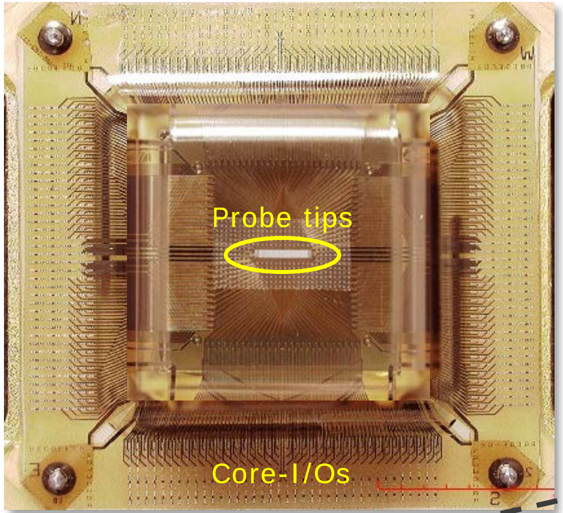
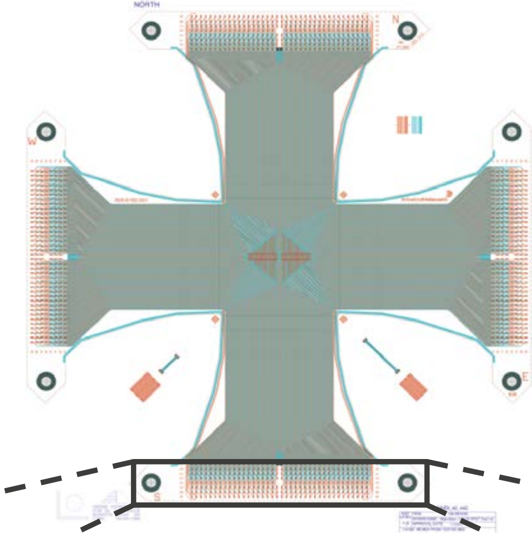
# Pyramid® Rocking Beam Interposer Probe Cores



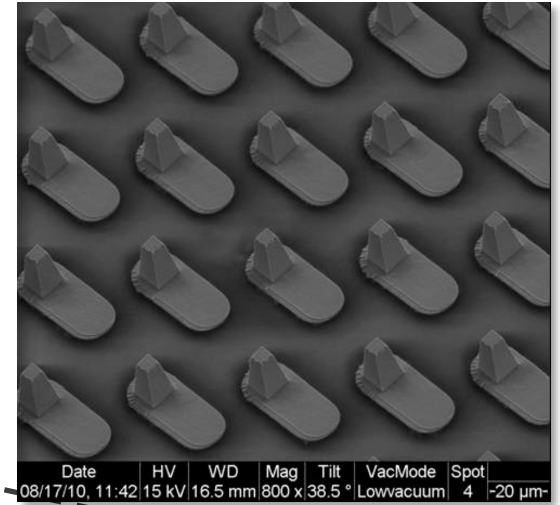
# From Core-I/O to Probe Tip



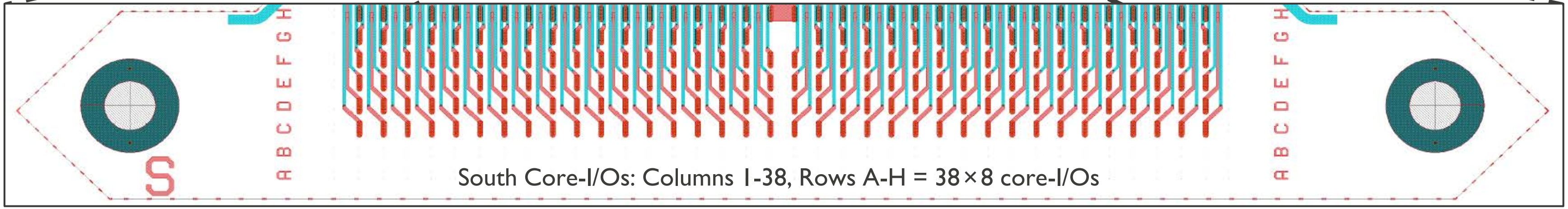
Pyramid Probe® RBI MSI-HD Probe Core with $4 \times (38 \times 8) = 1{,}216$ core-I/Os



Probe Core space transformer layout from core-I/Os to probe tips; $R_{parasitic} \approx 5\ \Omega$



RBI MEMS-type probe tips; micro-scrub with force ≤1 gf/tip with tip heel of $6 \times 1\ \mu m^2$



South Core-I/Os: Columns 1-38, Rows A-H = $38 \times 8$ core-I/Os

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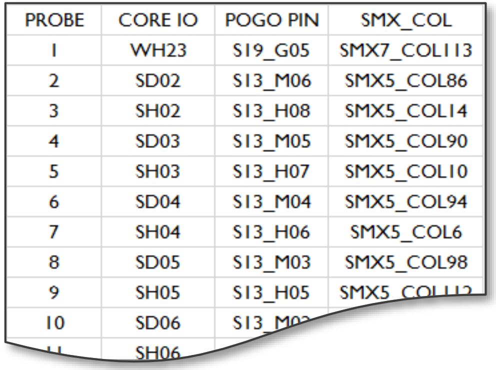
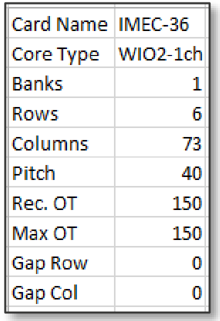
# Automatic Test Generation Inputs

- **Test System Description:** look-up table
  - Per line : probe number; core-I/O; pogo block/pin; switch matrix/column
  - Example: 3; `SH02`; `S13_H08`; `SMX5_COL14`



| PROBE | CORE IO | POGO PIN | SMX_COL |
|---|---|---|---|
| 1 | WH23 | S19_G05 | SMX7_COL113 |
| 2 | SD02 | S13_M06 | SMX5_COL86 |
| 3 | SH02 | S13_H08 | SMX5_COL14 |
| 4 | SD03 | S13_M05 | SMX5_COL90 |
| 5 | SH03 | S13_H07 | SMX5_COL10 |
| 6 | SD04 | S13_M04 | SMX5_COL94 |
| 7 | SH04 | S13_H06 | SMX5_COL6 |
| 8 | SD05 | S13_M03 | SMX5_COL98 |
| 9 | SH05 | S13_H05 | SMX5_COL112 |
| 10 | SD06 | S13_M0 | |
| 11 | SH06 | | |

- **Probe Core Description**
  - Key parameters, incl. probes layout and recommended/max OT

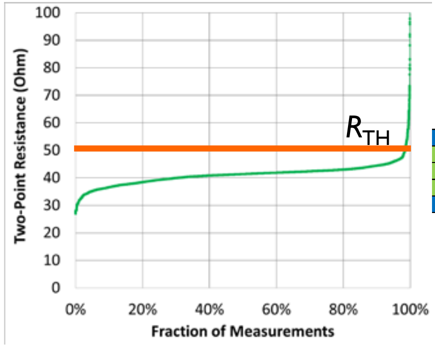


| | |
|---|---|
| Card Name | IMEC-36 |
| Core Type | WIO2-1ch |
| Banks | 1 |
| Rows | 6 |
| Columns | 73 |
| Pitch | 40 |
| Rec. OT | 150 |
| Max OT | 150 |
| Gap Row | 0 |
| Gap Col | 0 |

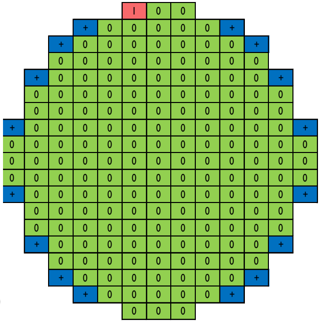
# Many Test Results: Data Abstraction & Visualization

- Individual and aggregate results
- $R_{MAX}$ fixed by meas.mnt range
- $R_{TH}$ determined with CDF plot

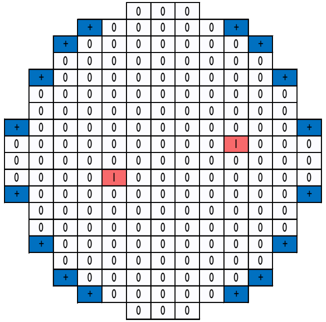
**CDF Plot**



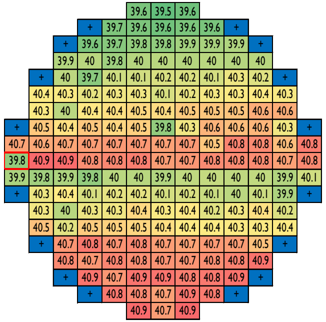
**Wafer Maps**



**#Opens**: $R > R_{MAX}$

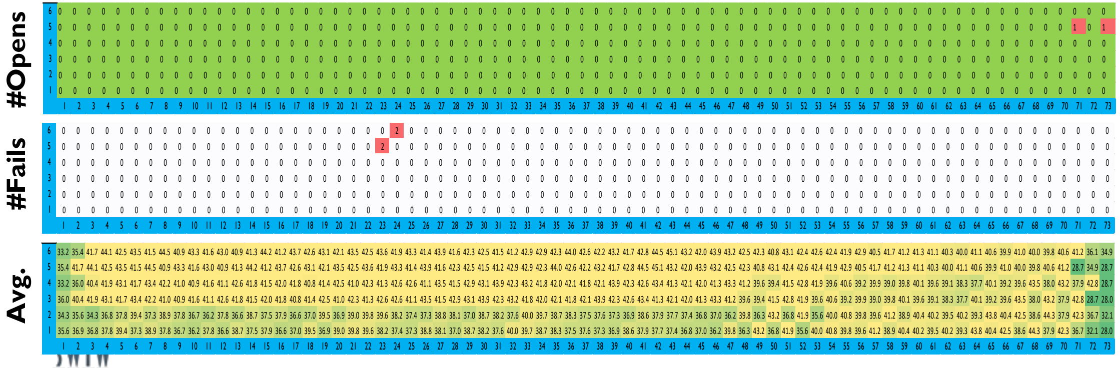


**#Fails**: $R_{TH} < R \leq R_{MAX}$

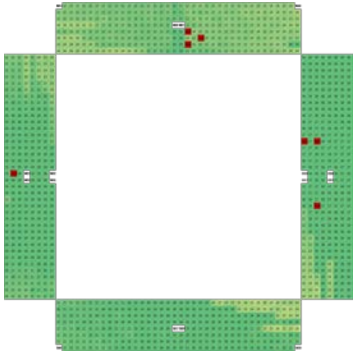


**Average**: $R_{AVG}$

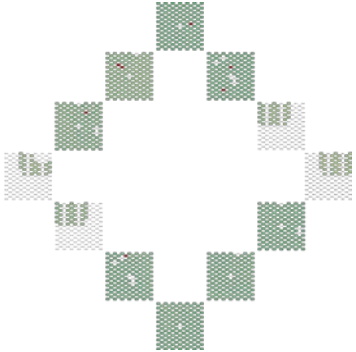
**Probe Maps**



**Core-I/O Map**



**Pogo-Pin Map**



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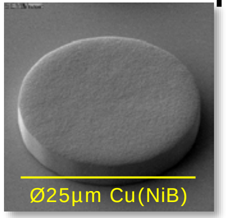
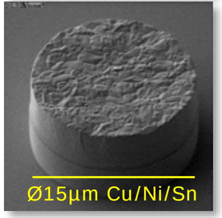
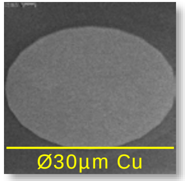
# imec Test Chip Designs with Micro-Bumps

## BMB: Blanket Micro-Bump

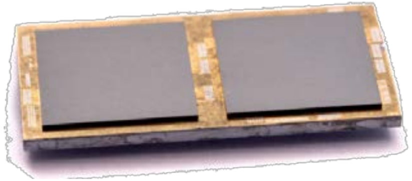
- All micro-bumps shorted by blanket Cu
  - Arrays: 50/50µm pitch, WIO1, WIO2
  - Banks with 0/1/2 dummy rings
- 9,421,272 functional micro-bumps/wafer


Ø25µm Cu(NiB)


Ø15µm Cu/Ni/Sn


Ø30µm Cu

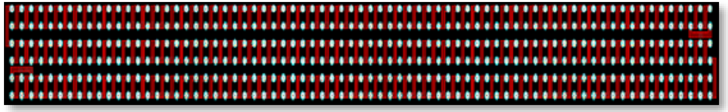
## Vesuvius-2.5D

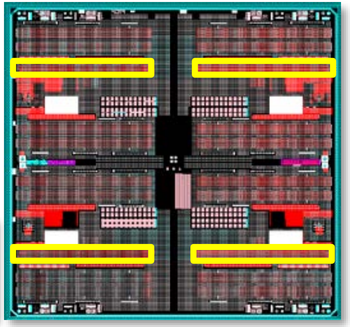


- WIO1: 1,200 bumps
- 40 daisy-chains of 30 micro-bumps each

## PTCU/W: Processing Test Chips

- WIO2 -1bank: 438 micro-bumps
- Embedded micro-bumps: zero height
- Micro-bumps pairwise connected through M1 in diagonal fashion



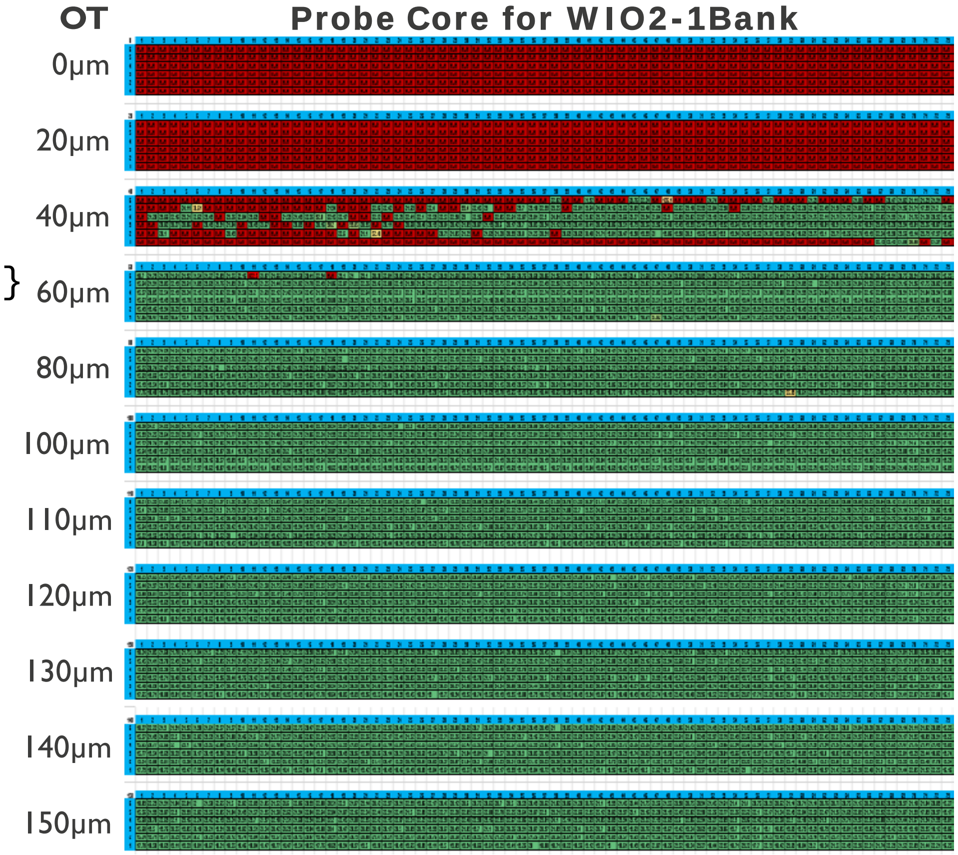


# Incoming Inspection on Blanket Wafer

- Increase over-travel from 0 to $OT_{max}$
- Perform 'Probe Check' routine:

```
for all probes $p \in P$ do {
    two-point $R$ measurement $p$ vs. $P \setminus \{p\}$
}
```

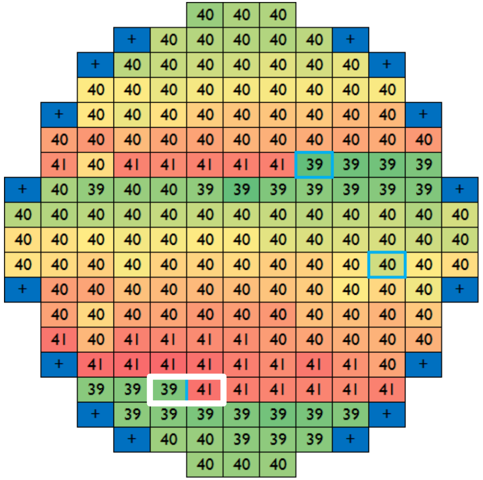
- Determine
  - Open probes, if any: $R > R_{MAX}$
  - FtL: First-to-Last OT; here 40µm
  - Recommended OT; here 100µm
    - Too low: poor contact
    - Too high: reduced lifetime



6. EXPERIMENTAL RESULTS

# Probe Tip Cleaning

- Recommended cleaning set-up
  - Substrate : ITS Probe Lapping Film, 1 µm grit particle size
  - Recipe : 60% of probing over-travel, 10 touch-downs
  - Interval : After 50 touch-downs



| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 40 | 40 | 40 | | | | | |
| | | | + | 40 | 40 | 40 | 40 | 40 | + | | | |
| | | + | 40 | 40 | 40 | 40 | 40 | 40 | 40 | + | | |
| | | 40 | 40 | 40 | 40 | 40 | 40 | 40 | 40 | 40 | | |
| | + | 40 | 40 | 40 | 40 | 40 | 40 | 40 | 40 | 40 | + | |
| | 40 | 40 | 40 | 40 | 40 | 40 | 40 | 40 | 40 | 40 | 40 | |
| | 41 | 40 | 41 | 41 | 41 | 41 | 41 | 39 | 39 | 39 | 39 | |
| + | 40 | 39 | 40 | 40 | 39 | 39 | 39 | 39 | 39 | 39 | 39 | + |
| 40 | 40 | 40 | 40 | 40 | 40 | 40 | 40 | 40 | 40 | 40 | 40 | 40 |
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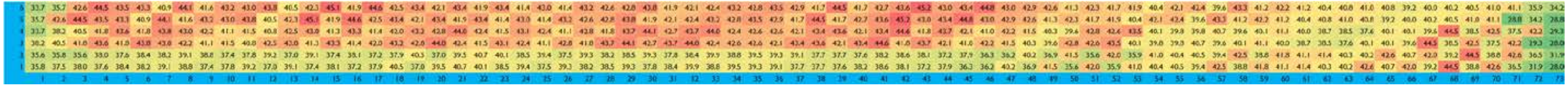
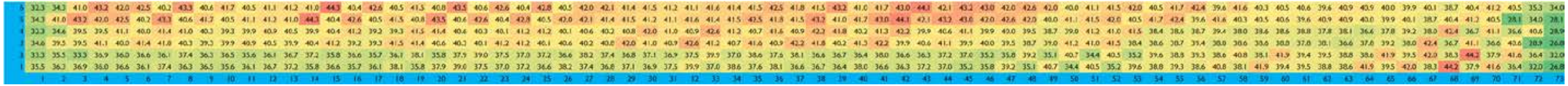
| + | 40 | 40 | 40 | 40 | 40 | 40 | 40 | 40 | 40 | 40 | 40 | + |
| | 40 | 40 | 40 | 40 | 40 | 40 | 40 | 40 | 40 | 40 | 40 | |
| | 41 | 40 | 41 | 41 | 41 | 41 | 40 | 40 | 40 | 40 | 40 | |
| | + | 41 | 41 | 41 | 41 | 41 | 41 | 41 | 41 | 40 | + | |
| | | 39 | 39 | 39 | 41 | 41 | 41 | 41 | 41 | 41 | | |
| | | + | 39 | 39 | 39 | 39 | 39 | 39 | 39 | + | | |
| | | | + | 40 | 40 | 39 | 39 | 39 | + | | | |
| | | | | | 40 | 40 | 40 | | | | | |

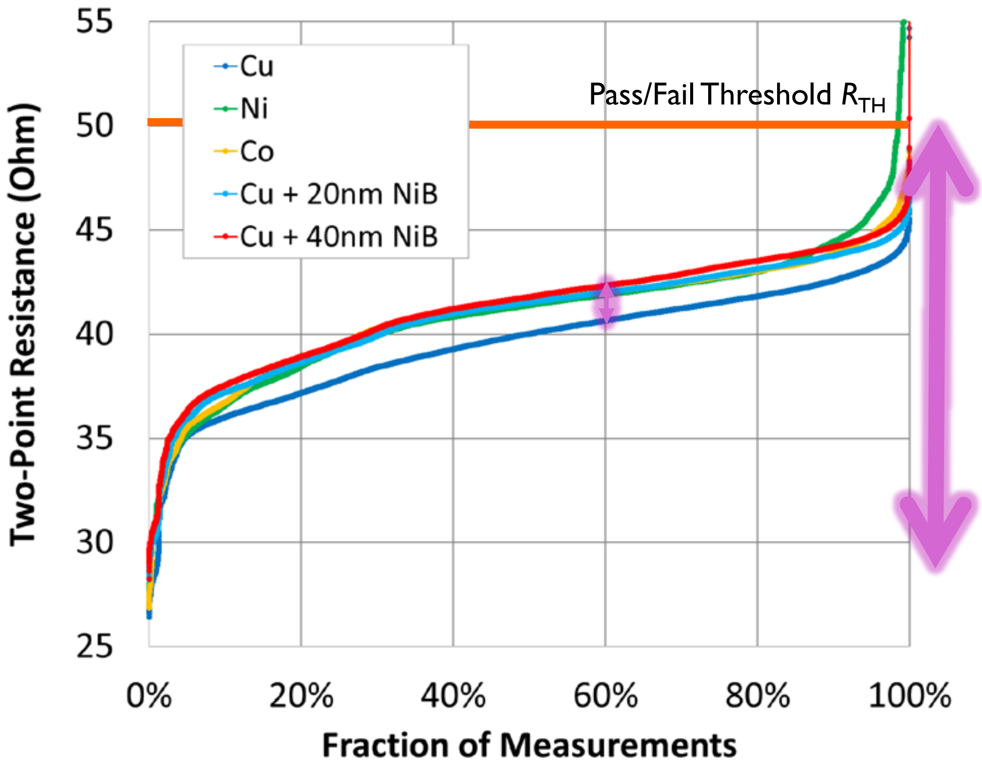
**Before Tip Cleaning**



**After Tip Cleaning**



# Contact Resistance Dependent on Bump Metallurgy

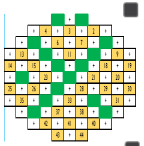


- Sample size: 20,900 – 37,620 measurements per wafer
- Pass/Fail threshold $R_{TH}$ set at 50 $\Omega$
- Large variation: due to parasitic *R* in test system and probe core
- Small variation: micro-bump metallurgy
  - D05: Cu
  - D09: Ni
  - D02: Co
  - D14: Cu +20nm NiB
  - D09: Cu +40nm NiB

# Probe-To-Pad Alignment (PTPA) Accuracy

- **PTPA Accuracy**: determined by (1) probe station and (2) probe core
  - Measure probe-mark errors in all four corners of micro-bump array

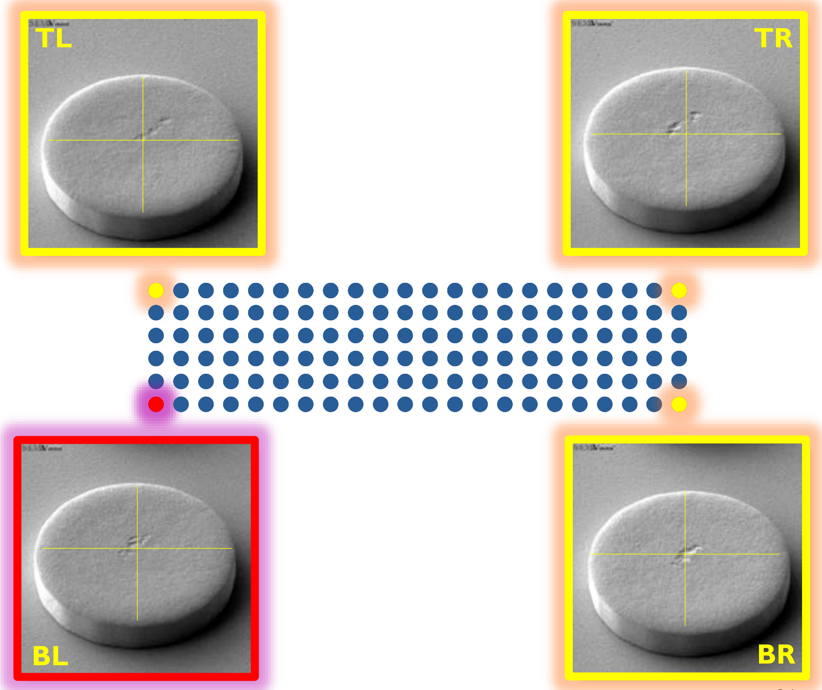
## 1. Probe Station Accuracy



- Equals error of BL probe mark, as BL tip is main probe training location
- Error is chuck-position dependent

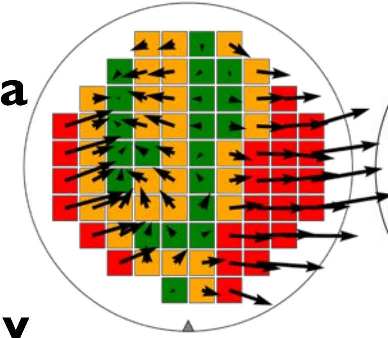
## 2. Probe Core Accuracy

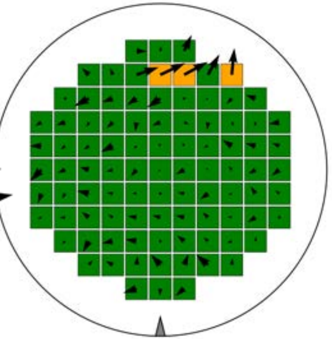
- Translate errors such that BL= (0,0)
- Errors other corners due to probe core
- These errors are chuck-pos independent

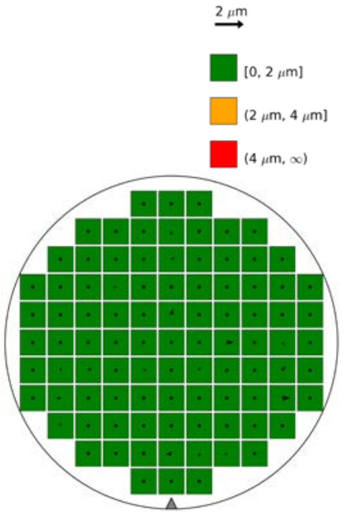


# Probe Station's PTPA Results

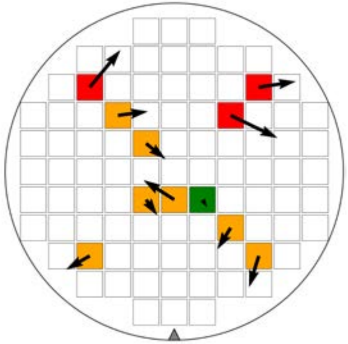
- **Cannot Use Top-View Camera**
  - No microscope bridge
  - Probe cores 'non see-through'
- **Platen + Chuck Cameras Only**
  - 'Align' ↔ 'Probe': chuck moves
  - Rely on Compensation Matrix
- Compensation Matrix recalibrated in Jan and May 2017
- **Thermal Control** required for accurate PTPA

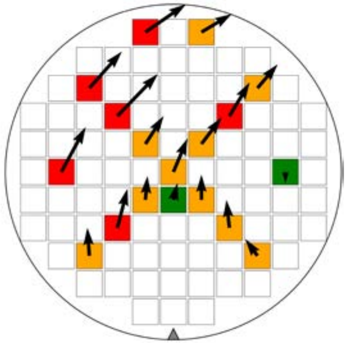

Stage Test Platen Cam
Before Service

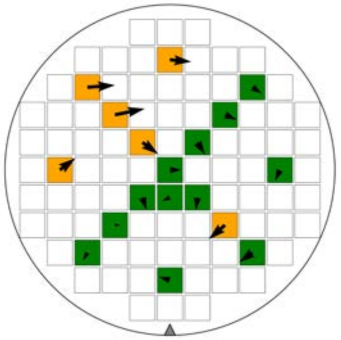

Stage Test Platen Cam
After Service Jan. 2017



Stage Test Platen Cam
After Service May 2017


PTPA @T=22°C
Before Service


PTPA @T=32°C
After Service Jan. 2017


PTPA @T=22°C
After Service Jan. 2017

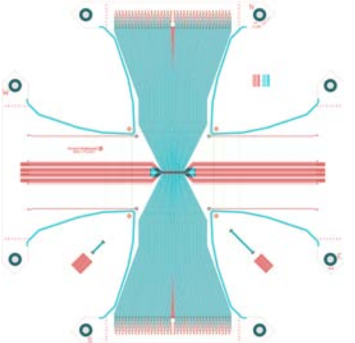
# Probe Cores' Grid Accuracy Results

**Legend**

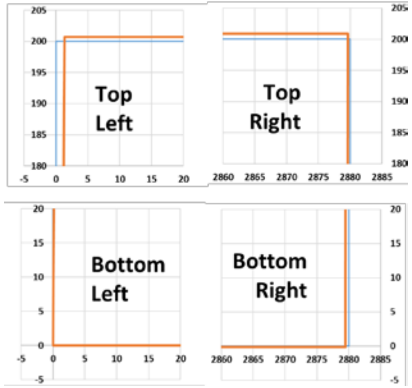
— = Ideal

— = Actual

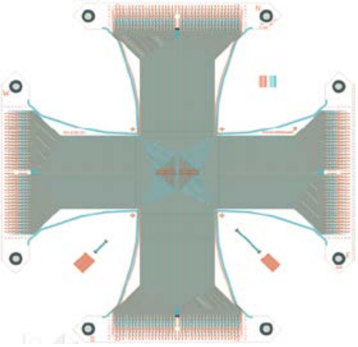
- **WIO2-1Bank**



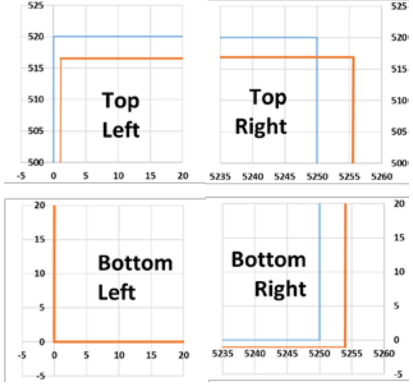
| Corner | Ideal (µm) | | Actual (µm) | | Error (µm) | | Relative Error | |
|---|---|---|---|---|---|---|---|---|
| | x | y | x | y | x | y | x | y |
| BL | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00% | 0.00% |
| BR | 2880.00 | 0.00 | 2879.47 | -0.12 | -0.53 | -0.12 | -0.02% | +0.06% |
| TR | 2880.00 | 200.00 | 2879.61 | 200.88 | -0.39 | 0.88 | -0.01% | +0.44% |
| TL | 0.00 | 200.00 | 1.33 | 200.71 | 1.33 | 0.71 | -0.05% | +0.35% |



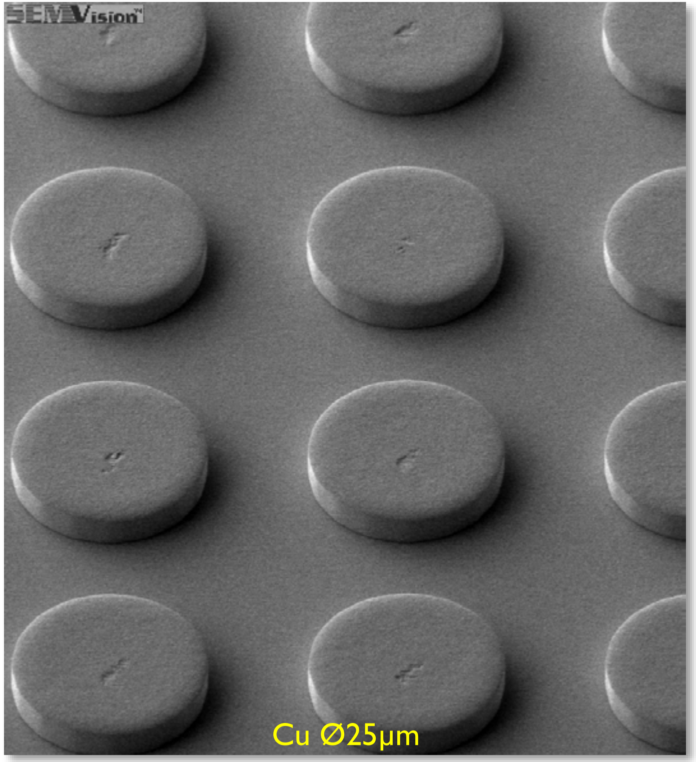
- **WIO1-4Bank**

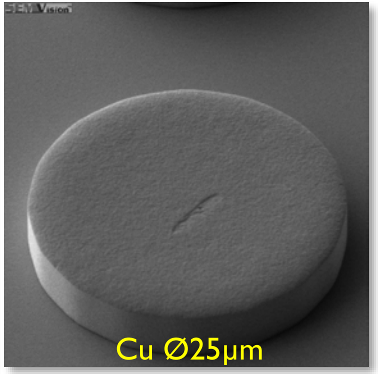


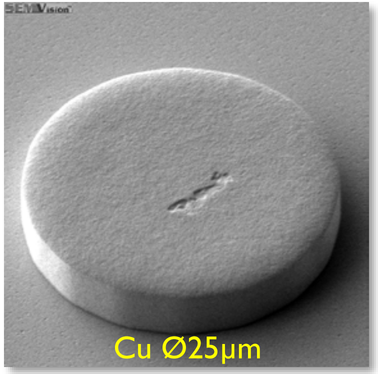
| Corner | Ideal (µm) | | Actual (µm) | | Error (µm) | | Relative Error | |
|---|---|---|---|---|---|---|---|---|
| | x | y | x | y | x | y | x | y |
| BL | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00 | 0.00% | 0.00% |
| BR | 5250.00 | 0.00 | 5253.93 | -0.99 | 3.93 | -0.99 | 0.07% | -0.19% |
| TR | 5250.00 | 520.00 | 5255.65 | 516.86 | 5.65 | -3.14 | 0.11% | -0.60% |
| TL | 0.00 | 520.00 | 1.13 | 516.58 | 1.13 | -3.42 | 0.02 % | -0.66% |

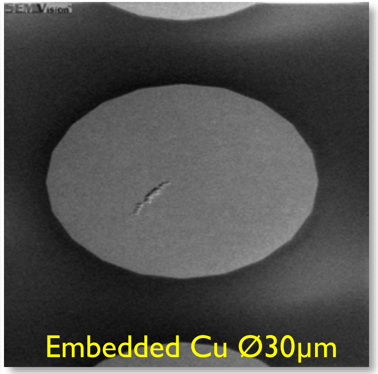


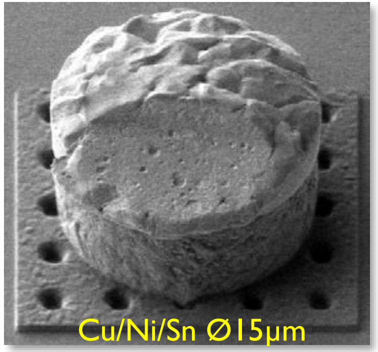
# Probe Marks on Various Micro-Bumps at 40µm Pitch

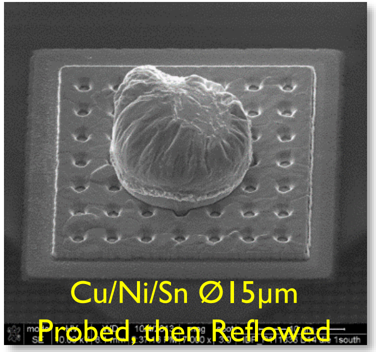

Cu Ø25µm

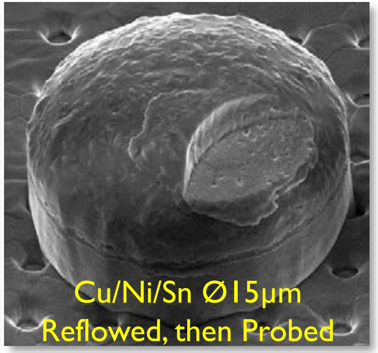

Cu Ø25µm


Cu Ø25µm


Embedded Cu Ø30µm


Cu/Ni/Sn Ø15µm


Cu/Ni/Sn Ø15µm
Probed, then Reflowed


Cu/Ni/Sn Ø15µm
Reflowed, then Probed

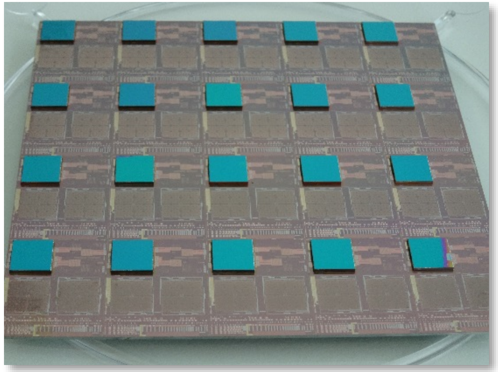
6. EXPERIMENTAL RESULTS

# Probe Mark Impact on Stack Interconnect Yield

- **Probe Marks**
  - On Cu, Co, Ni: very small
  - On Sn: can be reflowed away

| WIO1 Bank | A | B | C | D |
|---|---|---|---|---|
| Top die probed | ✗ | √ | √ | ✗ |
| Bottom die probed | √ | √ | ✗ | ✗ |
| Interconnect yield | 100% | 100% | 100% | 100% |
| DC resistance $R_{dc}$ | 32.0Ω | 42.4Ω | 45.0Ω | 33.1Ω |

Vesuvius-2.5D D2W stacks



| Ch. | DC | Stack 1 | Stack 2 | Stack 3 | Stack 4 | Stack 5 | Stack 6 | Stack 7 | Stack 8 |
|---|---|---|---|---|---|---|---|---|---|
| A | 1 | 24.8 | 25.2 | 25.7 | 29.3 | 31.7 | 34.7 | 38.7 | 30.9 |
| A | 2 | 29.7 | 36.6 | 37.6 | 41.0 | 40.6 | 106.0 | 34.7 | 35.2 |
| A | 3 | 24.7 | 25.7 | 27.0 | 30.5 | 25.2 | 25.2 | 26.3 | 30.1 |
| A | 4 | 25.8 | 26.4 | 27.4 | 27.6 | 26.9 | 27.2 | 27.6 | 26.9 |
| A | 5 | 24.0 | 23.7 | 25.0 | 25.0 | 24.1 | 26.5 | 28.1 | 28.1 |
| A | 6 | 29.4 | 29.1 | 30.3 | 32.3 | 30.5 | 33.5 | 33.7 | 33.7 |
| A | 7 | 26.8 | 28.1 | 27.7 | 27.6 | 28.0 | 27.2 | 27.9 | 27.6 |
| A | 8 | 30.4 | 29.9 | 32.9 | 32.1 | 32.0 | 32.4 | 32.1 | 31.9 |
| A | 9 | 38.2 | 35.2 | 40.6 | 39.1 | 46.3 | 42.2 | 41.6 | 42.4 |
| A | 10 | 34.3 | 30.1 | 33.3 | 33.3 | 33.5 | 35.2 | 34.7 | 37.2 |
| B | 1 | 36.3 | 26.4 | 39.3 | 39.4 | 43.0 | 46.0 | 53.7 | 42.0 |
| B | 2 | 51.3 | 31.2 | 44.4 | 50.3 | 51.4 | 53.1 | 47.3 | 46.9 |
| B | 3 | 35.8 | 37.6 | 38.7 | 40.4 | 36.8 | 36.8 | 37.5 | 37.3 |
| B | 4 | 36.8 | 38.0 | 39.2 | 39.6 | 38.3 | 39.0 | 39.5 | 38.6 |
| B | 5 | 35.3 | 34.9 | 36.5 | 36.5 | 35.9 | 36.6 | 38.7 | 36.8 |
| B | 6 | 40.4 | 40.2 | 43.4 | 44.1 | 42.2 | 44.0 | 44.8 | 44.4 |
| B | 7 | 37.9 | 39.8 | 39.6 | 39.3 | 39.1 | 38.7 | 39.8 | 39.3 |
| B | 8 | 41.5 | 41.5 | 44.9 | 44.2 | 43.6 | 43.8 | 44.5 | 43.4 |
| B | 9 | 48.2 | 47.9 | 51.8 | 51.5 | 53.7 | 54.3 | 52.9 | 53.5 |
| B | 10 | 51.1 | 41.8 | 44.6 | 46.1 | 46.9 | 51.3 | 46.3 | 45.1 |
| C | 1 | 58.4 | 51.8 | 78.6 | 73.5 | 59.4 | 98.9 | 56.0 | 52.2 |
| C | 2 | 46.5 | 43.2 | 44.6 | 47.4 | 48.0 | 49.7 | 49.4 | 46.4 |
| C | 3 | 40.0 | 37.7 | 41.3 | 41.1 | 41.3 | 41.1 | 42.7 | 38.9 |
| C | 4 | 45.1 | 44.7 | 49.1 | 48.2 | 50.7 | 51.1 | 50.0 | 49.5 |
| C | 5 | 41.0 | 39.6 | 43.4 | 42.6 | 42.1 | 41.7 | 42.4 | 41.5 |
| C | 6 | 37.5 | 38.5 | 38.8 | 38.8 | 38.7 | 38.4 | 39.0 | 38.4 |
| C | 7 | 41.1 | 41.0 | 42.9 | 43.6 | 48.5 | 44.8 | 45.3 | 45.2 |
| C | 8 | 36.9 | 37.1 | 38.5 | 38.2 | 44.5 | 38.1 | 40.1 | 38.4 |
| C | 9 | 40.0 | 41.0 | 42.7 | 42.4 | 41.7 | 41.9 | 42.4 | 41.8 |
| C | 10 | 40.2 | 42.7 | 42.5 | 45.3 | 45.8 | 40.8 | 41.5 | 40.6 |
| D | 1 | 38.4 | 53.4 | 67.0 | 64.5 | 53.4 | 62.3 | 47.8 | 41.4 |
| D | 2 | 32.4 | 29.7 | 32.4 | 35.4 | 36.9 | 35.2 | 35.9 | 34.6 |
| D | 3 | 29.5 | 26.9 | 29.2 | 29.0 | 29.9 | 30.8 | 29.5 | 31.6 |
| D | 4 | 30.8 | 33.4 | 38.0 | 37.5 | 38.3 | 39.6 | 38.3 | 38.5 |
| D | 5 | 29.8 | 29.5 | 31.2 | 30.7 | 40.4 | 30.2 | 30.5 | 30.4 |
| D | 6 | 26.1 | 26.2 | 27.0 | 27.9 | 26.6 | 26.6 | 27.1 | 26.9 |
| D | 7 | 30.1 | 30.7 | 30.9 | 31.8 | 31.2 | 33.0 | 34.7 | 33.8 |
| D | 8 | 25.7 | 25.5 | 26.7 | 26.5 | 26.7 | 26.5 | 27.5 | 27.4 |
| D | 9 | 29.5 | 29.7 | 30.7 | 31.0 | 29.7 | 30.6 | 30.4 | 30.2 |
| D | 10 | 28.8 | 30.0 | 31.1 | 30.7 | 30.5 | 30.9 | 29.9 | 29.1 |

- **Experiment on Vesuvius-2.5D with WIO1-4Banks**
  - Probed per bank in all four combinations of top/bottom die yes/no probed prior to stacking
  - No impact on stack interconnect yield observed

[ Marinissen et al. – ITC'14]

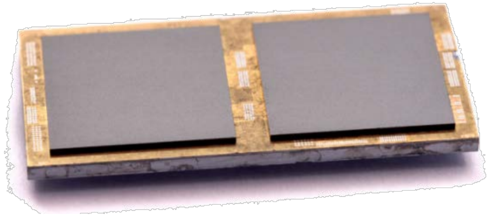
# Presentation Overview

1. Introduction
2. Wide-I/O Micro-Bump Arrays
3. Vortex-2 Test System
4. Probe Technology
5. Test System Software
6. Experimental Results
7. Test Cost Comparison
8. Conclusion

# Cost Modeling for Single-Site Testing

## Cost Comparison

- Case: Vesuvius-2.5D
- Two active dies on top of passive interposer



## Three Scenarios

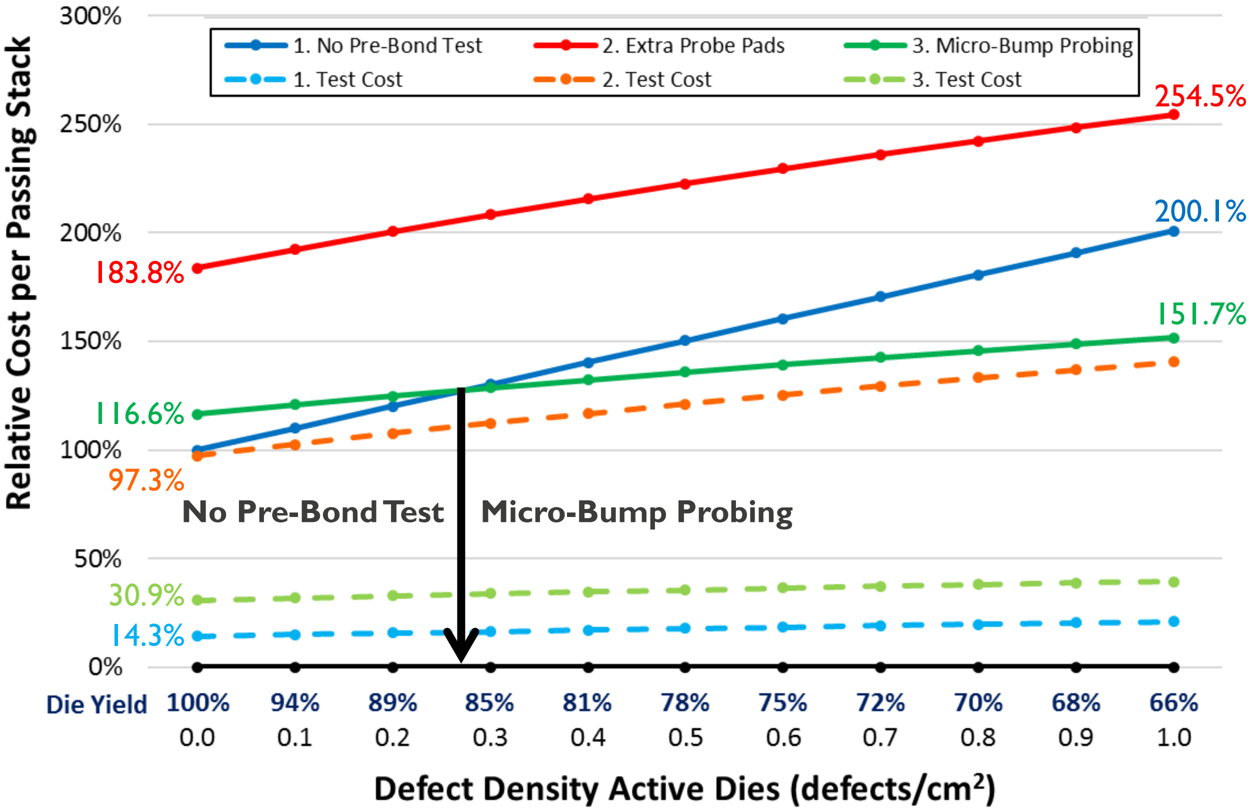
1. No pre-bond test 🟦
2. Extra pre-bond pads 🟥
3. Micro-bump probing 🟩

| Parameter | Inter-poser | 1. No Pre-Bond | 2. Extra Pads | 3. Bump Probe |
|---|---|---|---|---|
| | | Dies 1+2 | Dies 1+2 | Dies 1+2 |
| Pre-bond test contacts / die | n.a. | n.a. | only 120 | 1,200 |
| 300mm wafer cost | $ 700 | $ 3,000 | $ 3,000 | $ 3,000 |
| Die area | 200 mm$^2$ | 65.61 mm$^2$ | 66.61 mm$^2$ | 65.61 mm$^2$ |
| Gross die / wafer | 302 | 968 | 953 | 968 |
| Defect density | 0.1 /cm$^2$ | **0.0-1.0** /cm$^2$ | **0.0-1.0** /cm$^2$ | **0.0-1.0** /cm$^2$ |
| Die yield | 84.52% | 100-65.76% | 100-65.48% | 100-65.76% |
| Pre-bond fault coverage | n.a. | 0% | 99% | 99% |
| Pre-bond test time / die | n.a. | 0 s | 100 s | 10 s |
| Pre-bond probe card cost / die | n.a. | 0 | 0 | $ 0.50 |
| Pre-bond test cost/die | n.a. | $ 0.00 | $ 5.00 | $ 1.00 |
| Stack interconnect yield | 100% | 99% | 99% | 98% ? |
| Final fault coverage | 100% | 99% | 99% | 99% |
| Final test time / die | 1 s | 10 s | 10 s | 10 s |

# 3D-COSTAR Cost Modeling Results

1. **No Pre-Bond Test** 🟦
   Only acceptable if pre-bond die yield is high
2. **Extra Pre-Bond Pads** 🟥
   10× test time increase ⇒ test significant cost-add
3. **Micro-Bump Probing** 🟩
   expensive advanced probe card is minor overall cost contributor

No difference in product quality due to Final Test!



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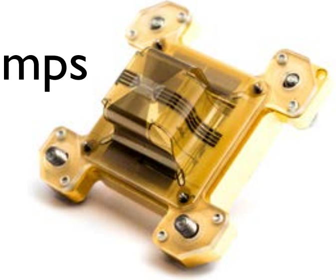
8. CONCLUSION

# Summary

- Unique system for large-array fine-pitch micro-bump probing based on Cascade Microtech CM300
  - At imec routinely used for micro-bump arrays @40/50µm pitch
  - Temperature control and good calibration required
  - PTPA ≤ ±2.5µm: appears sufficient even for 20µm-pitch micro-bumps



- Cascade Microtech Pyramid® RBI probe cards/cores
  - Advanced MEMS-based thin-film probe technology
  - Large arrays down to 40µm pitch
  - Contact resistance 0.1-2.0Ω; parasitic resistance in space transformer ~5Ω
  - Low force ⇒ Limited probe mark ⇒ No impact on stacking yield observed

# Challenges and Solutions for Micro-Bump Probing

| Challenges | Solutions |
|---|---|
| **a. Small Pitch and Diameter**<br>- Pitch = 40μm → 20μm | - Advanced MEMS-type probe cards<br>- Accurate, thermally-stable prober |
| **b. Large Micro-Bump Arrays**<br>- WIO1=1200; WIO2=1752; HBM2=4258 | - Large #channels; hard-docking<br>- Automated data visualization |
| **c. Proper Electrical Contact**<br>- Contact resistance $R_c \le 5\ \Omega$ | - Parasitics, over-travel, tip cleaning<br>- Dependent on bump metallurgy |
| **d. Probe Marks on Micro-Bumps**<br>- No negative impact on stack yield | - Low-force probe cards<br>- Reflow for soft Sn micro-bumps |
| **e. Cost of Test**<br>- Economically feasible | - Advanced probes are expensive<br>- But alternatives are more expensive |

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**Delft University of Technology** *(the Netherlands)*

Said Hamdioui, Mottaqiallah Taouil

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