SW Test Workshop
Semiconductor Wafer Test Workshop

Production Level On-Wafer Probe of Multi-Channel 77 GHz Radar Transceiver Chipset

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NXP Semiconductors

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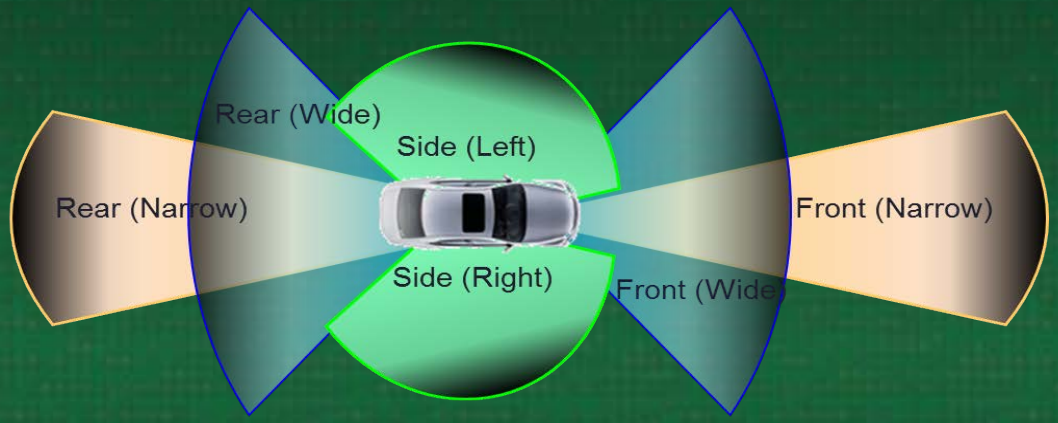
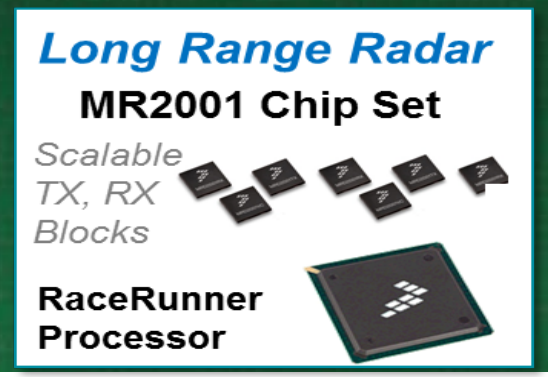
Product Line – MR2001

Applications



- ✓ **Increasing applications for radar**
  - Value added Parking solutions
  - Pedestrian Detection
  - Cross Traffic Alert
- ✓ **Increasing performance with small size**
  - Transition 24 GHz → 77 GHz: improved resolution
- ✓ **Increasing attach rate per car**
  - Radar initially for safety emergency braking
  - Now moving to corner sensors, "cocoon radar"

Product Line



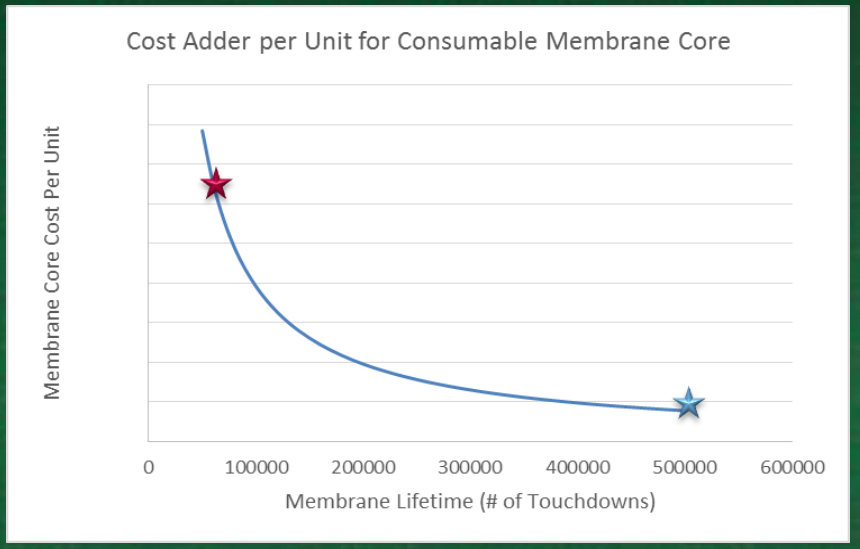
Features	Benefits
Scalable to Four Tx and 12 Rx Channels	Enables single radar platform with electronic beam steering over wide field of view, supporting LRR, MRR and SRR applications for budget to luxury vehicles
Integrated Rx BB Filter and VGA	Saves system BOM cost
Optimized for Radar Processor MPC577xK	Receiver path optimization with MPC577xK, including unique built-in system test features. Ensures the best receiver sensitivity required for excellent detection accuracy
Advanced Packaging Technology	Easiest to use, handle and manufacture for customers. Ensures highest performance and minimum signal interference on the customer PCB
Low Power Consumption of 2.5 W for the Total Transceiver. Best phase noise < -85 dBc/Hz at 100 kHz offset	Low power consumption saves energy and heat. Best phase noise enables precise discrimination of objects for automatic cruise control, blind spot detection, lane departure warning and pedestrian detection

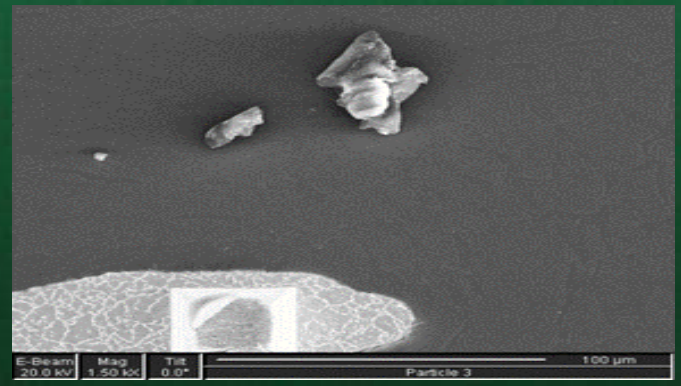
Test Strategy

- **Constraints**
  - **MR2001 Product Line contains minimal DFT or BIST circuitry**
  - **First packaged 38/76 GHz product line produced by NXP (formerly Freescale)**
  - **Historical cost of test dominated previous product COGS**
    - CPU Test Time
    - Hardware (RFIC membrane consumption; setup cost; labor)
- **Objectives**
  - **Lowest cost of test, AT SPEED 38 GHz & 76-77 GHz, possible**
  - **Turnkey probe solution that supported three unique devices (1 Tx; 1 Rx; 1 VCO)**
  - **Standard semiconductor ATE / Prober platform being leveraged across the company**
  - **Process flow compatible with Automotive Qualified Probe Floors**

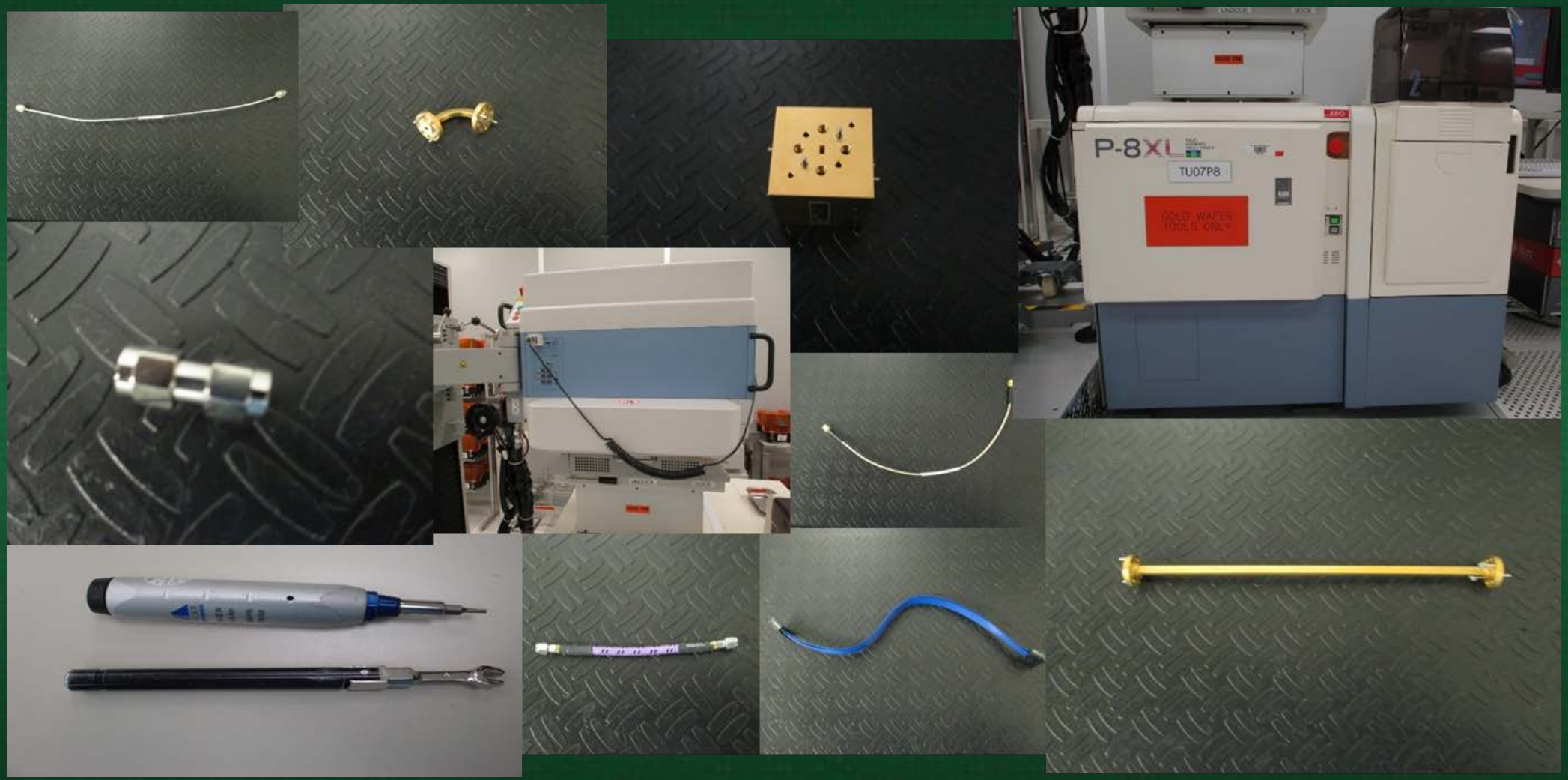
Primary Cost Drivers

- Setup Time between Production Runs
- Labor Skill Level
- Core Cost / Lifetime
  - Wear Rate of Tip
- DUT Pad Construction and Material
- Polish Pad Medium / Material / Handling
- Cleanliness of Process
- PROCEDURES DRIVE COSTS DOWN



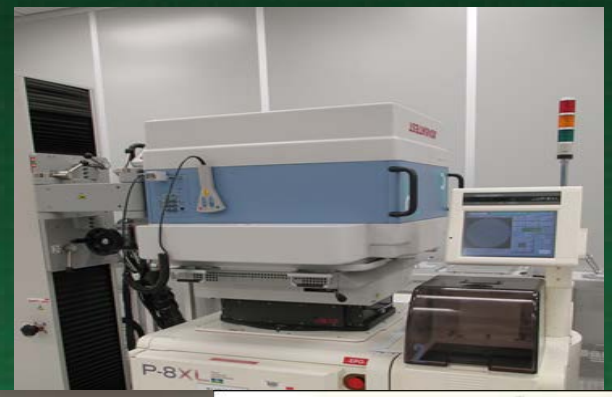


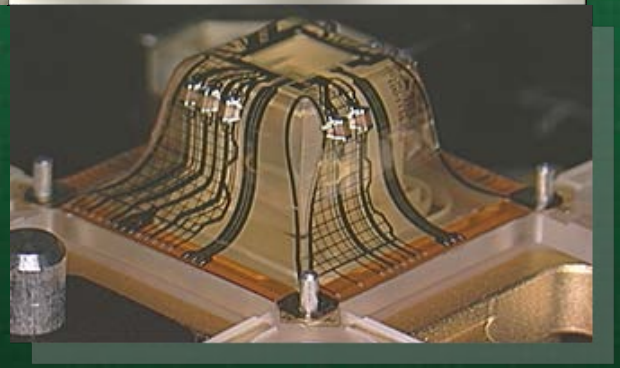
First Prototype System



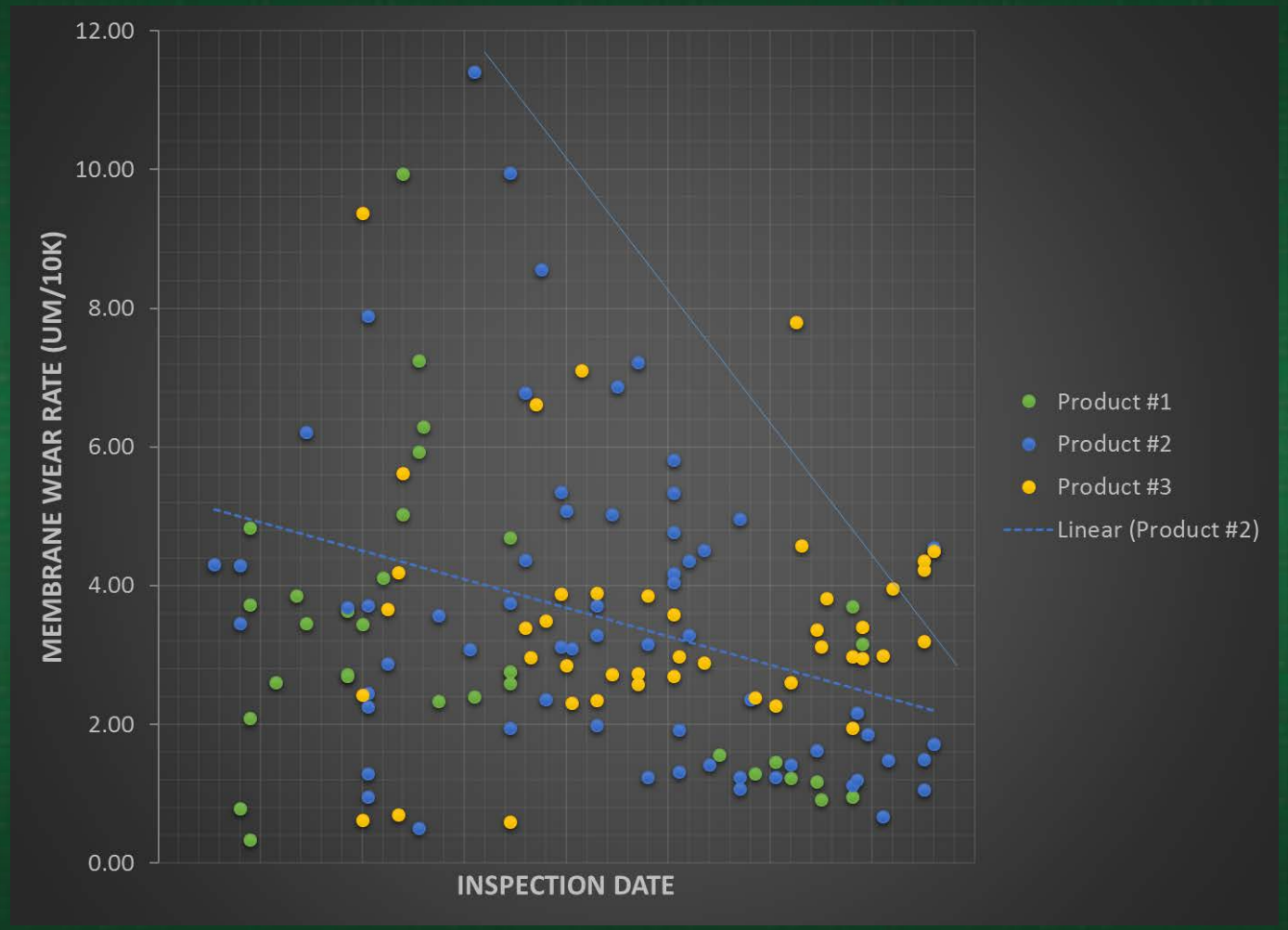
Hardware Selection

- ATE - Advantest 9300 PSRF w/ MMW Device Interface
- Tel Precio Nano Wafer Prober with J750 Head Plate and SACC Ring
- Universal Hard Dock (UHD), SACC Ring, and Probe Card Docking Ring Co-Developed with Vendor
- Probe Card Developed by Cascade
- Probe Technology - Cascade Membrane RFIC
- Standard Off the Shelf Millimeter Wave Components



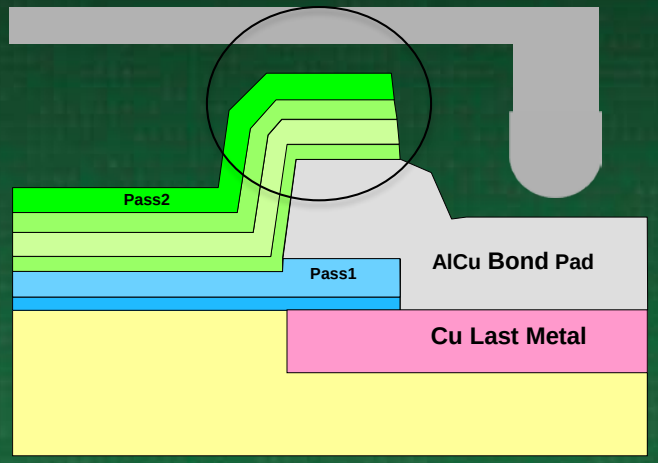


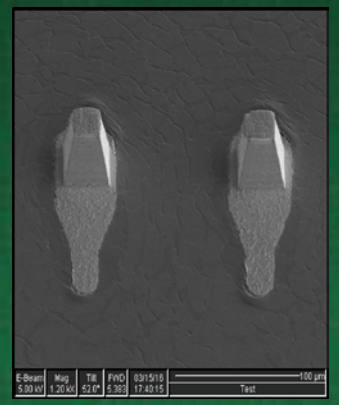
Membrane Wear Rates



- Primary Drivers
  - Probe Temperature
  - Polish Medium
  - Polish Frequency
  - Overdrive
    - On Pad - DUT
    - On Polish Pad

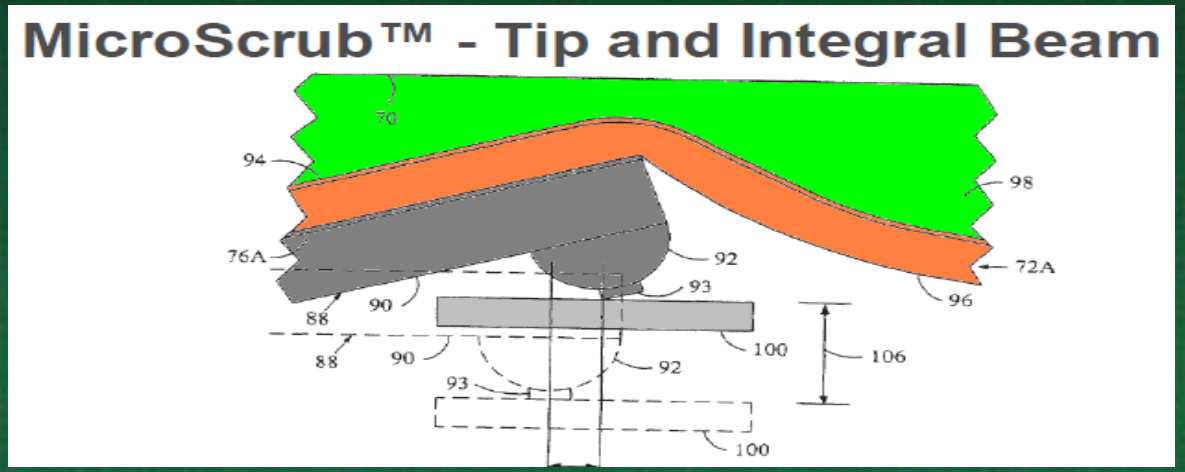
Cascade Membrane Dynamics





- Deflection
  - 10 µm of permanent deflection (beam slope) is equal to the end of life recommendation.
    - Larger values observed from high temp use
  - MicroScrub or “beam slope”
  - Probably larger after more use
  - Larger at higher temperature
  - Depends an tip and beam geometry
- Membrane berm
  - Varies from core to core
  - Probably bigger at overtravel
- Passivation thickness
  - The least variation

Deflection	10 µm
Berm	5 µm
Passivation	+ 4 µm
Clearance Min	19 µm



MicroScrub™ is a Registered Trademark of Cascade Microtech

To avoid passivation damaged:
Manufacturing must control minimum clearance by defining and executing on criteria to discontinue use of membrane before risk of passivation damage increases

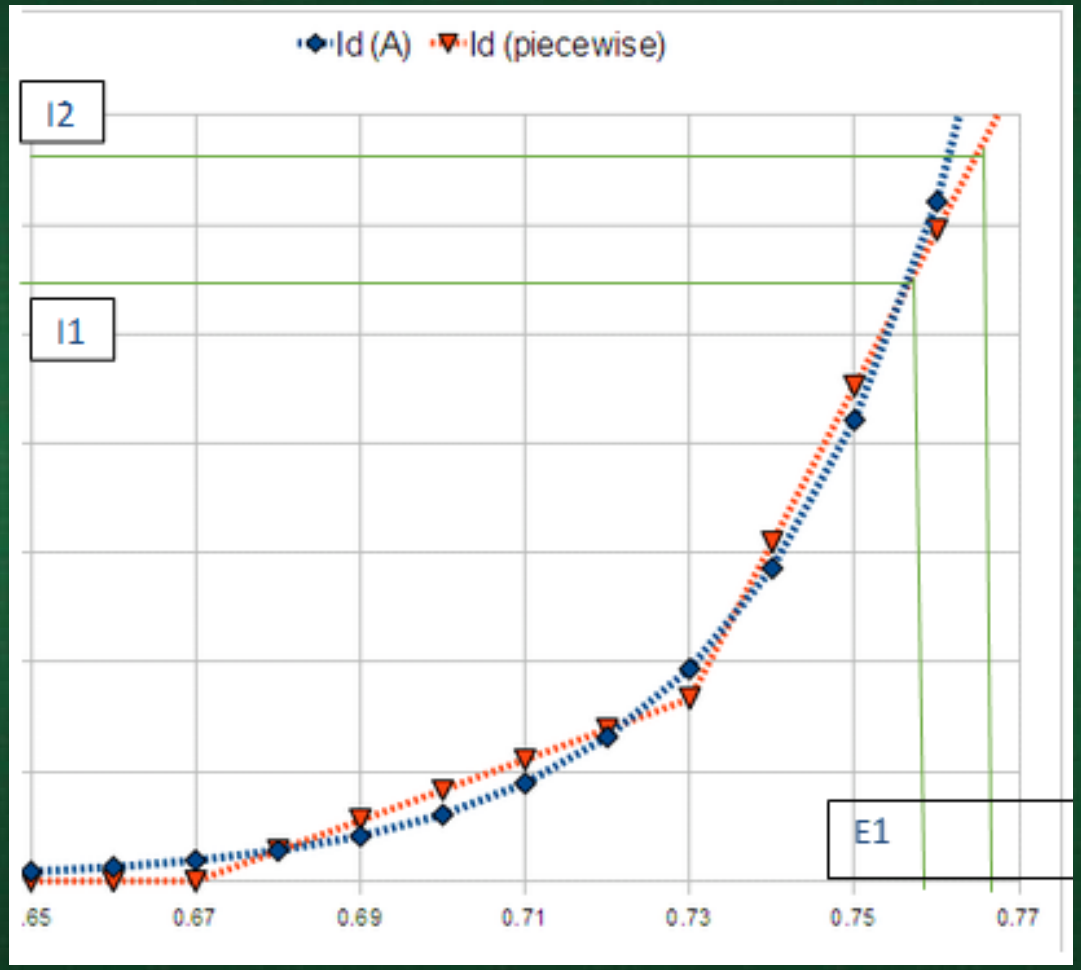
Theory of Contact Resistance Test

Force I1 and measure E1

Force I2and measure E2

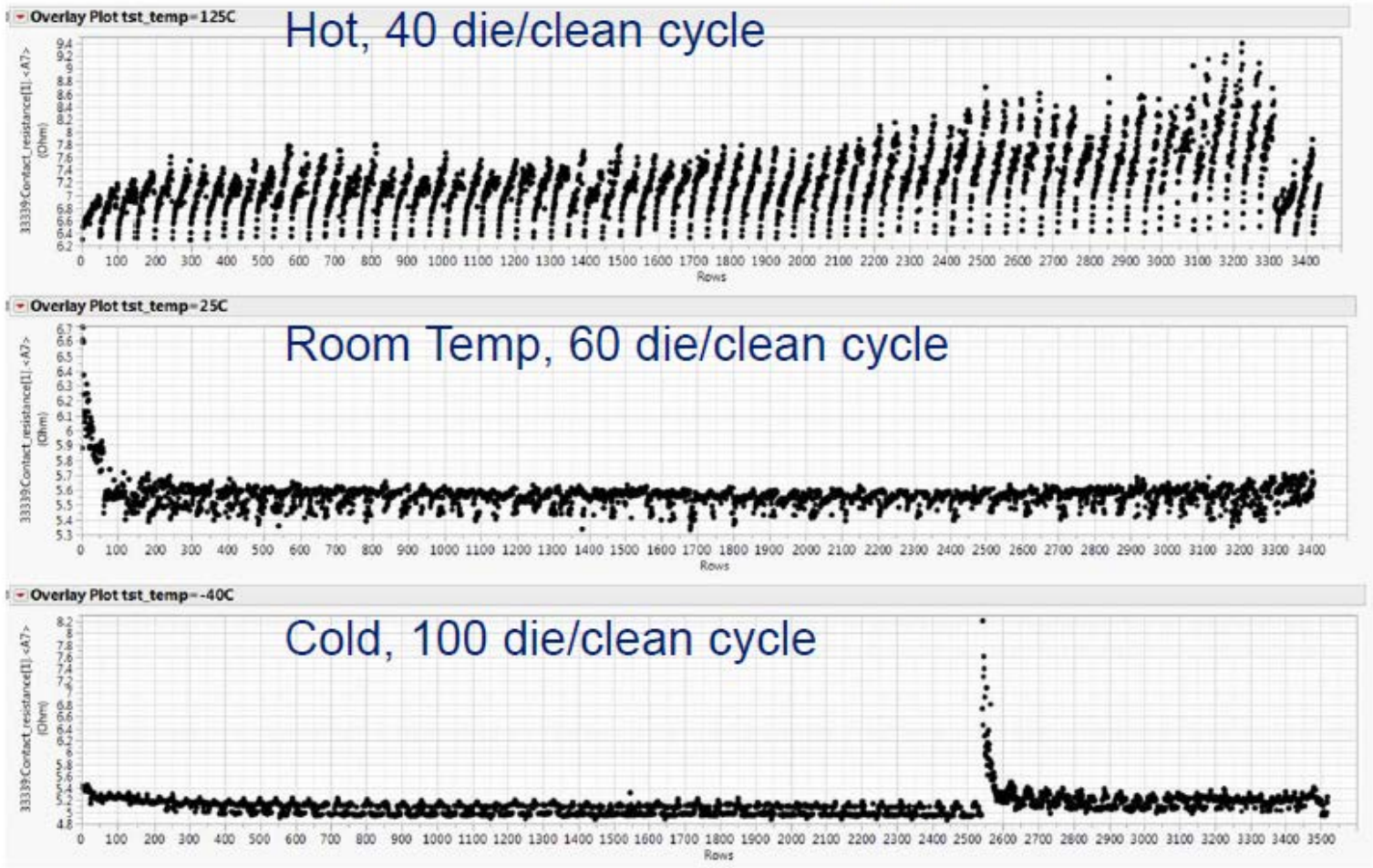
CRES= (E2-E1)/(I2-I1)

Within receiver design, there are 12 individual pins we can monitor via the PS1600 card



Electrical Performance Trends

- CRES Demonstrates Instability at 125 C

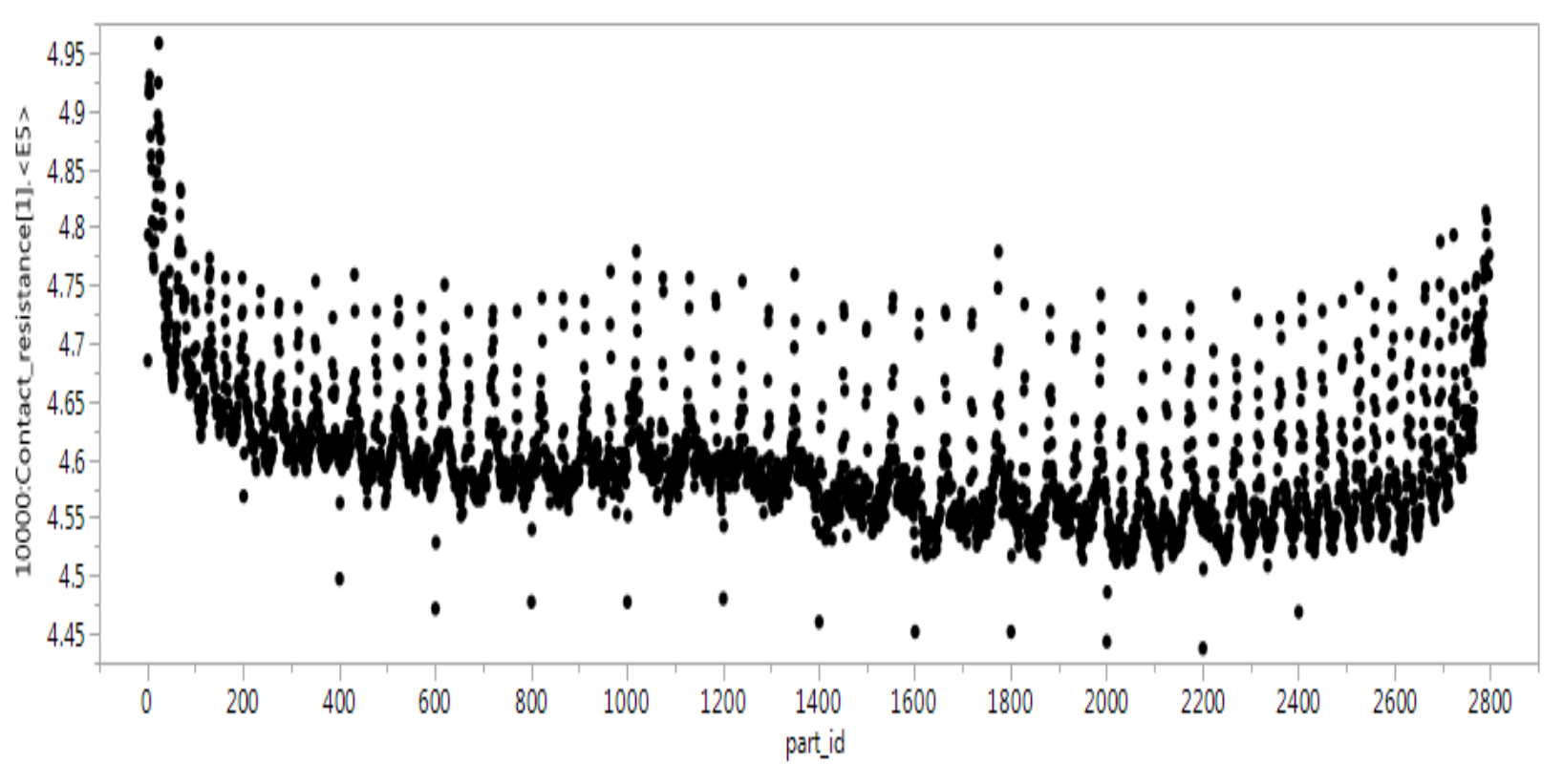


A) Recovery polish event reduced CRES

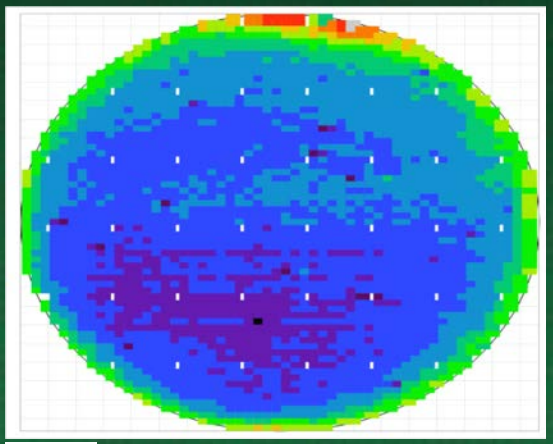
B) New membranes all show a small “wear in “ period. No impact on RF measurements.

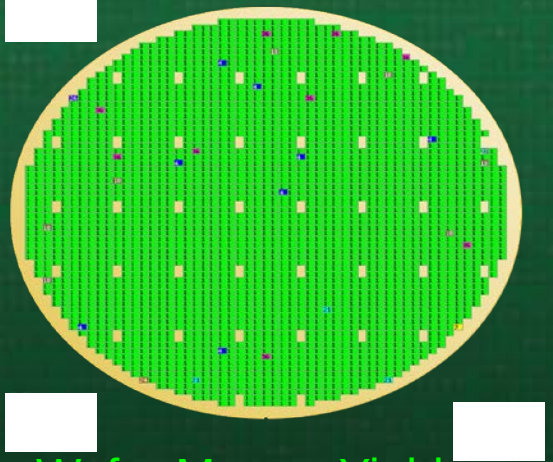
C) Possible build-up / debris on probe tip.

CRES at -40C



Wafer Map -> CRES



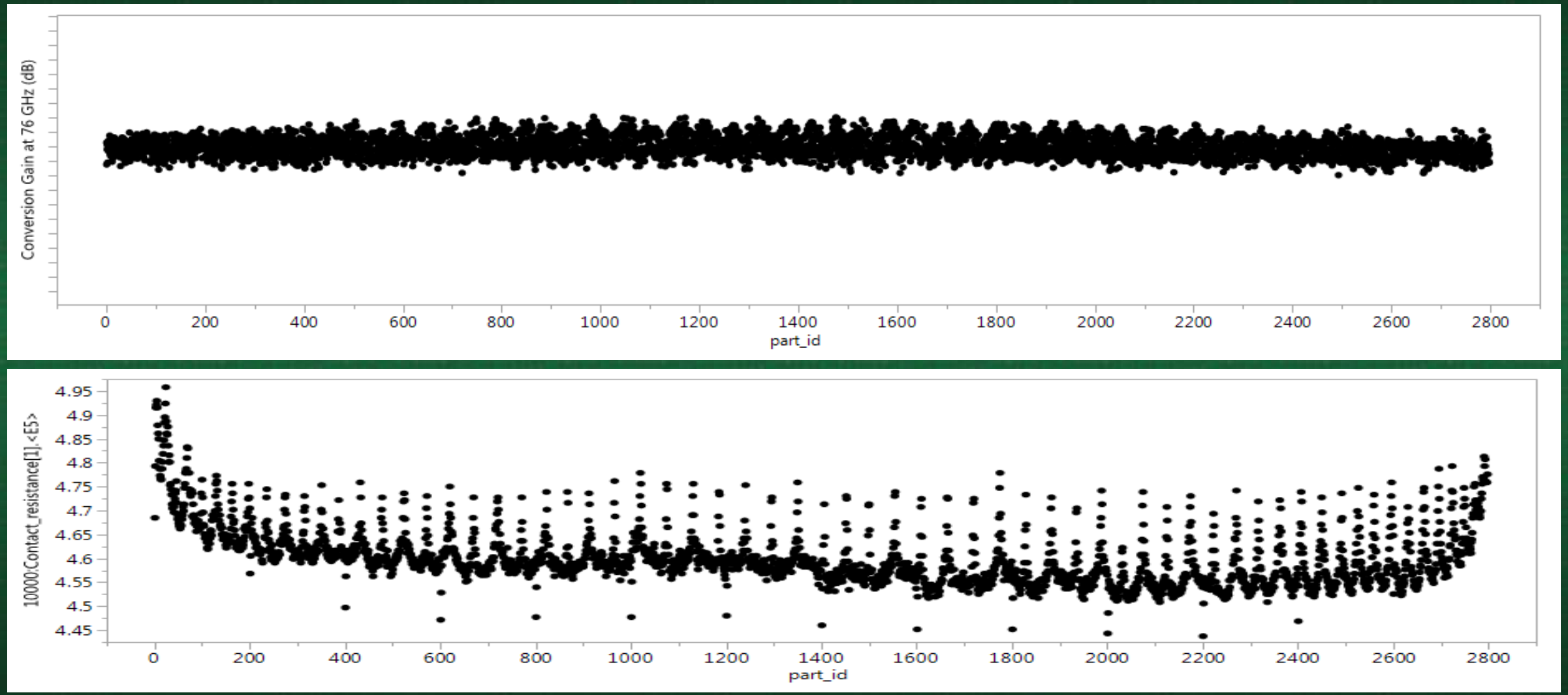


Wafer Map -> Yield

Measured contact resistance drops after polish cycle

- Polish cycle occurs off wafer on auxiliary chuck
- Membrane is in ambient, but not direct contact with wafer at temperature

Receiver Gain Stability



Production MMW Testing

- **The Universal Hard Dock allows manufacturing the ability to change the products running without engineering involvement saving time and engineering resources**
- **Time savings of 2x for changeover between products**
- **Contact resistance tests are able to monitor quality of core performance**
- **Future of MMW Testing**
  - Parallelism
  - Future product complexity dictates supplemental roll as cost of test begins to be dominated by the digital functions of the chip
  - DFT / BIST likely to dominate wafer level probe as more digital functions are integrated into the chip
  - MMW Testing shifts to Probe on Ball or in a Handler/Contactor based system to guarantee product MMW performance

Thank You!

- **Thank you to the following individuals**

  - SW Test Committee for selecting this paper to present
  - SW Test attendees as without attendees you have no conference
  - Jeff Finder (NXP) for taking vacation during SW Test and not able to attend. He also had the confidence in me to present this paper