



SW Test Workshop
Semiconductor Wafer Test Workshop

New Inspection Solution for Probing Technology



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PTI Taiwan

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Overview

- **Background / Introduction**
- **Inspection Solution for Probing Technology**
 - (1) In Line Inspection Solution : AOI / Prober
 - (2) Off Line Inspection Solution : Probe Card AOI / 3DMS
- **Future Work for the Inspection Solutions**
- **Conclusions**
- **Acknowledgement**

**“ To Be , or not to Be :
That is a Question! ”**

Probing Inspection

Background: Cost is Key!



(1) Usually, Test Hourly Rate not include Full Inspection Cost!

Test Cost just cover minimum inspection investment!

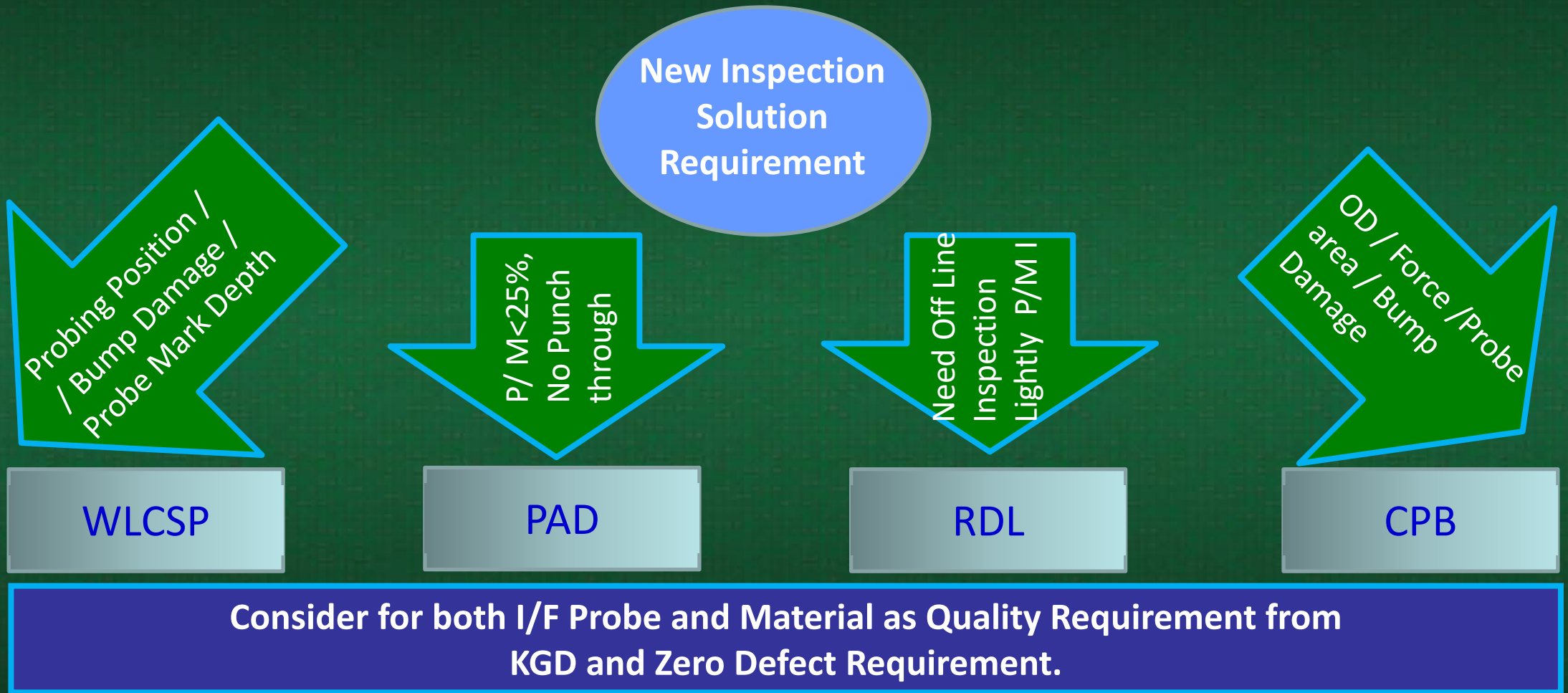
**(2) The Inspection Technology must cover the Probing Quality Control as
KGD / Zero Defect Business!**

**(3) Reasonable Inspection cost could keep driving Probing Technology Continue
Improvement Progress and DFM!**

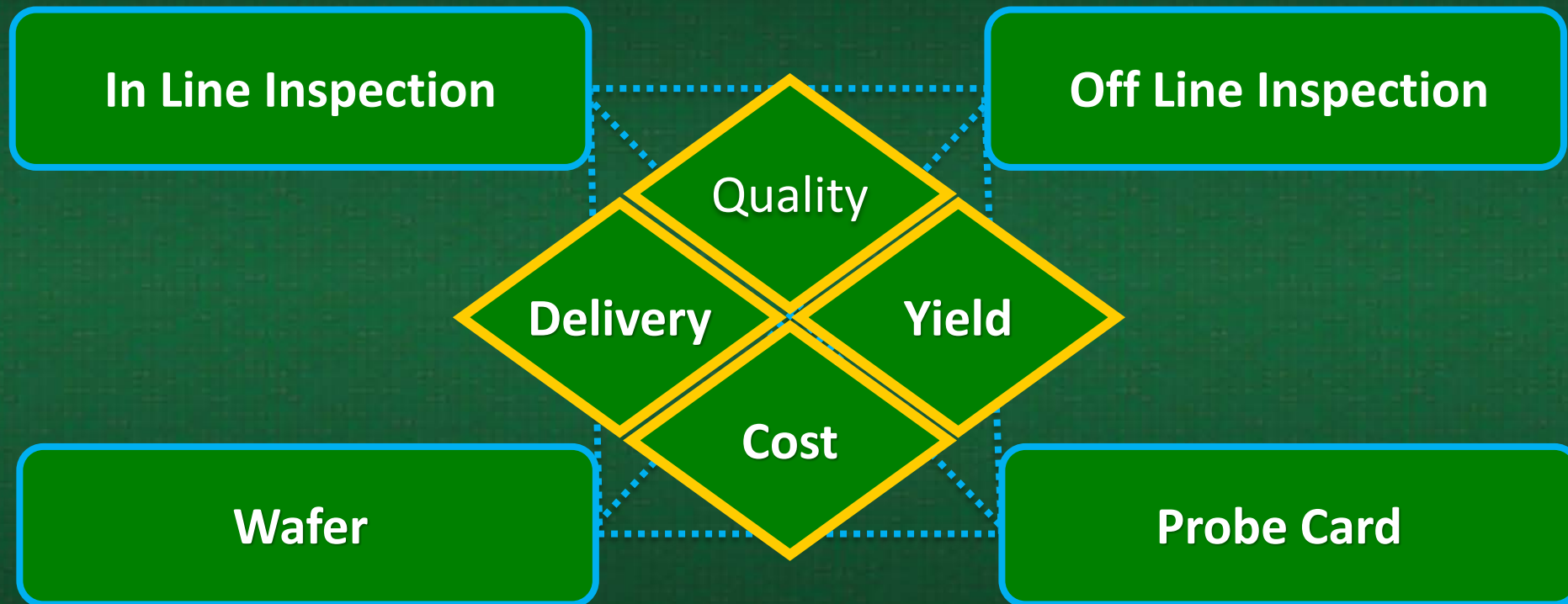
Introduction: New Inspection Solution for Probing Technology

- **The Probe and Probe Mark Quality Control were Key Issues for Wafer Level Package Probing Technology. How to measure the Probe and Probe Marks from in-line and off-line tools will discuss at this presentation.**
- **We development the new tools for probe card /probe mark inspection. New tools provide more efficiency data for clearly engineering information and related setup issues.**
- **We believe the New Inspection Solution could more helpful from user and supplier and improve the probing technology. Will share relate information with partners .**

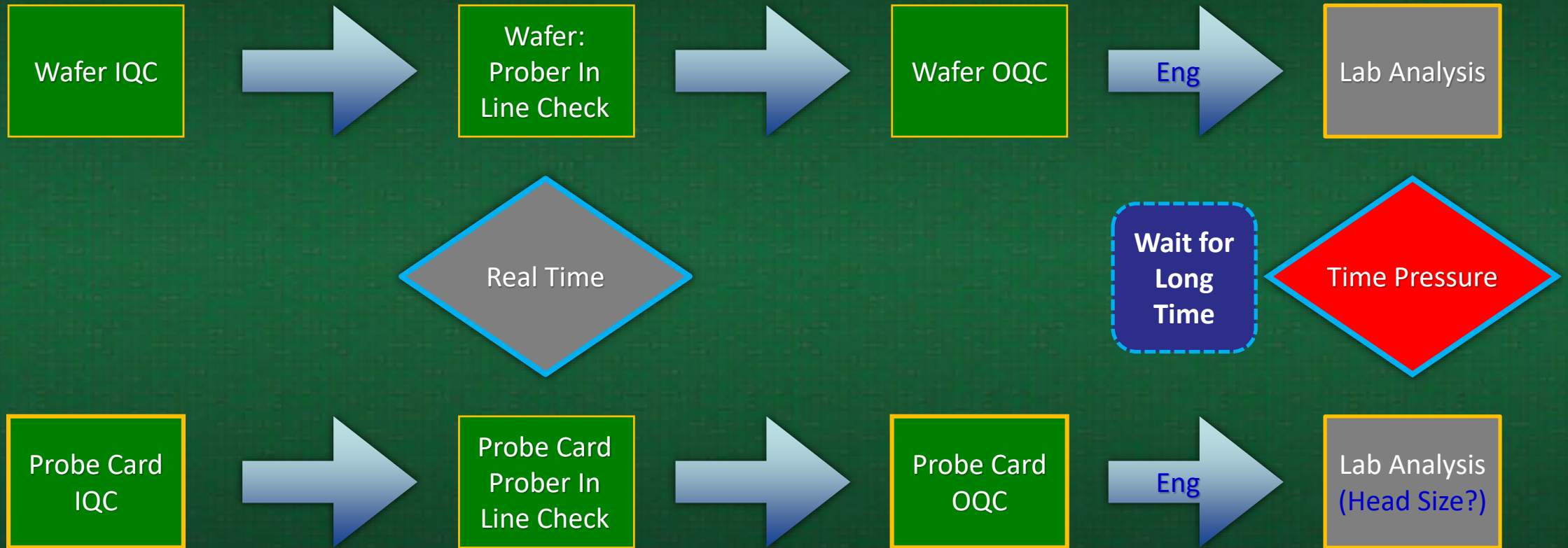
Why Need Inspection for WLP Probing Technology



Inspection Requirement in Probing Technology



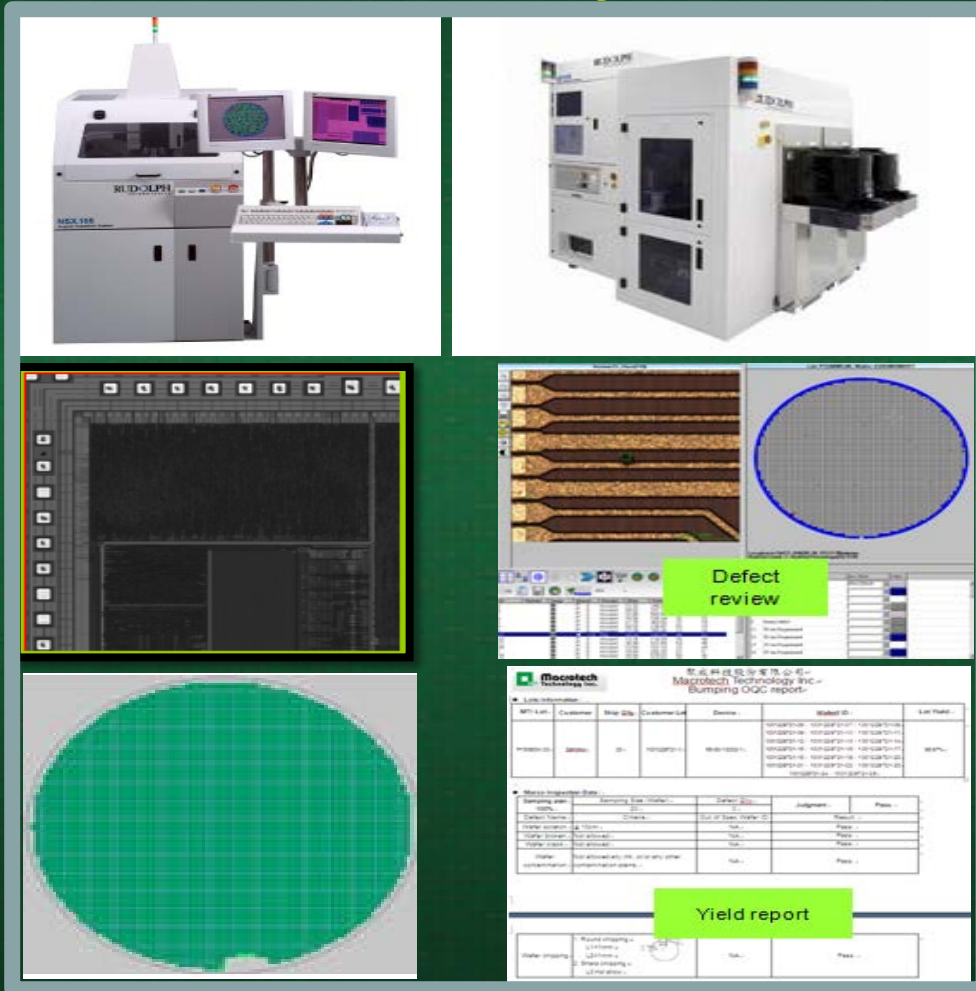
Wafer and Probe Card Inspection Process Flow






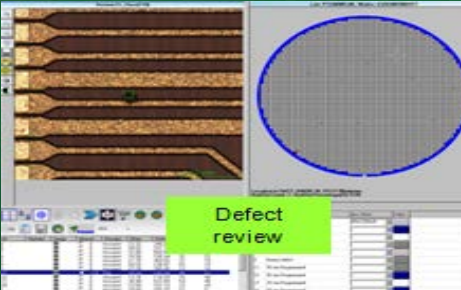
(1) In Line Inspection Solution-AOI & Prober

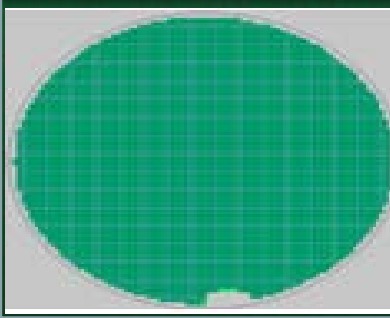

• Wafer AOI Analysis

◆ Prober PMI Analysis











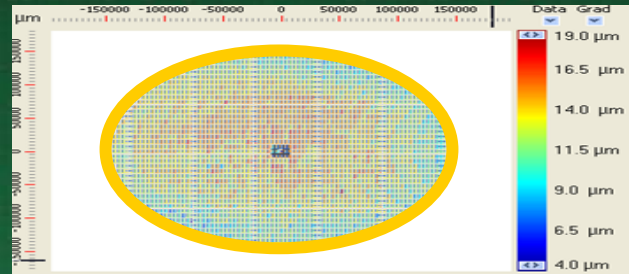
Device Name: 0828-Normal				
Time	Index size	Sampling die Coordinates		
	X	Y	X	Y
1			18	24
2			24	24
3	8.3268	7.0008	18	28
4			24	28

Total pads	Start time	End Time	Total Time
18	12:33:48.838	12:33:58.487	00:00:10.648
18	12:34:02.008	12:34:12.837	00:00:10.831
18	12:34:16.347	12:34:26.887	00:00:10.340
18	12:34:28.401	12:34:38.828	00:00:10.425

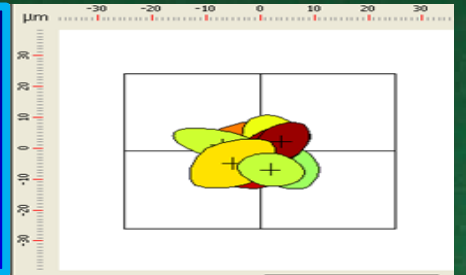
AOI Probe Mark Analysis for 2 TD Probe card Set Up :

KGD Challenges : 2TD P/C for Probe Mark Area and Keep Out Control

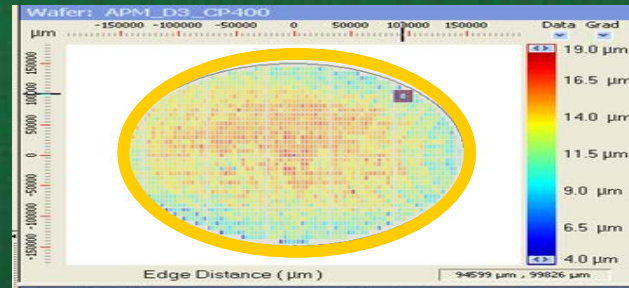
Wafer center is under control



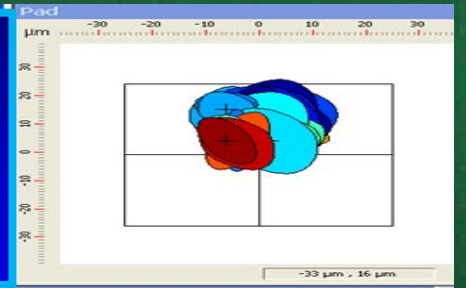
Probe Mark A/A <25%
Production P/M Keep Out
>5um



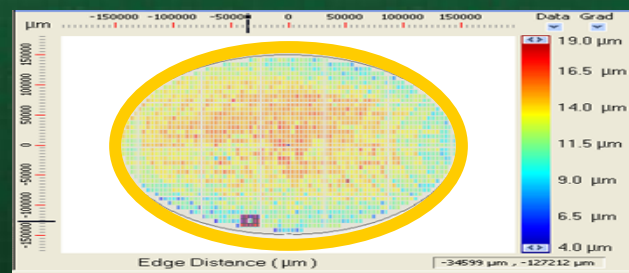
Wafer edge get Worst need
special Set Up



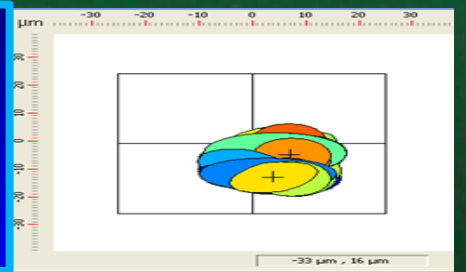
Production P/M Keep Out
<5um
(Vender only ensure Off
Line Check @RT >5um)



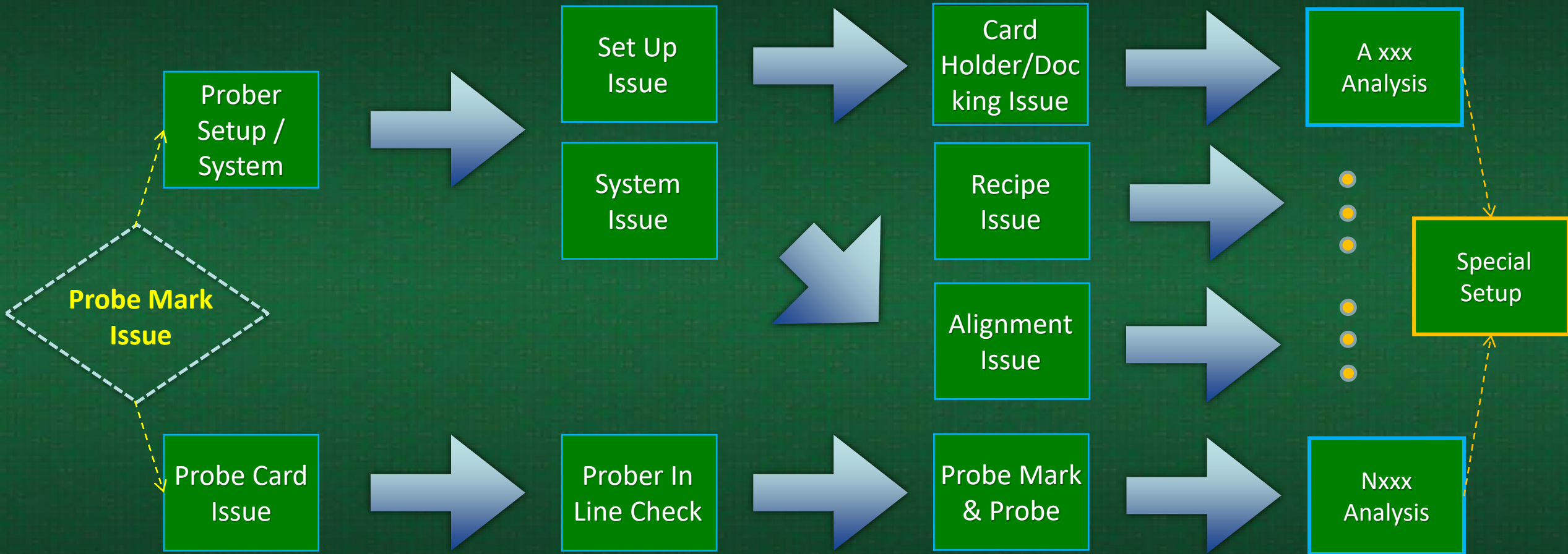
Probe Mark Shift in Spec but
the means get shift



Probe Mark A/A <25%
Production P/M Keep Out
>5um

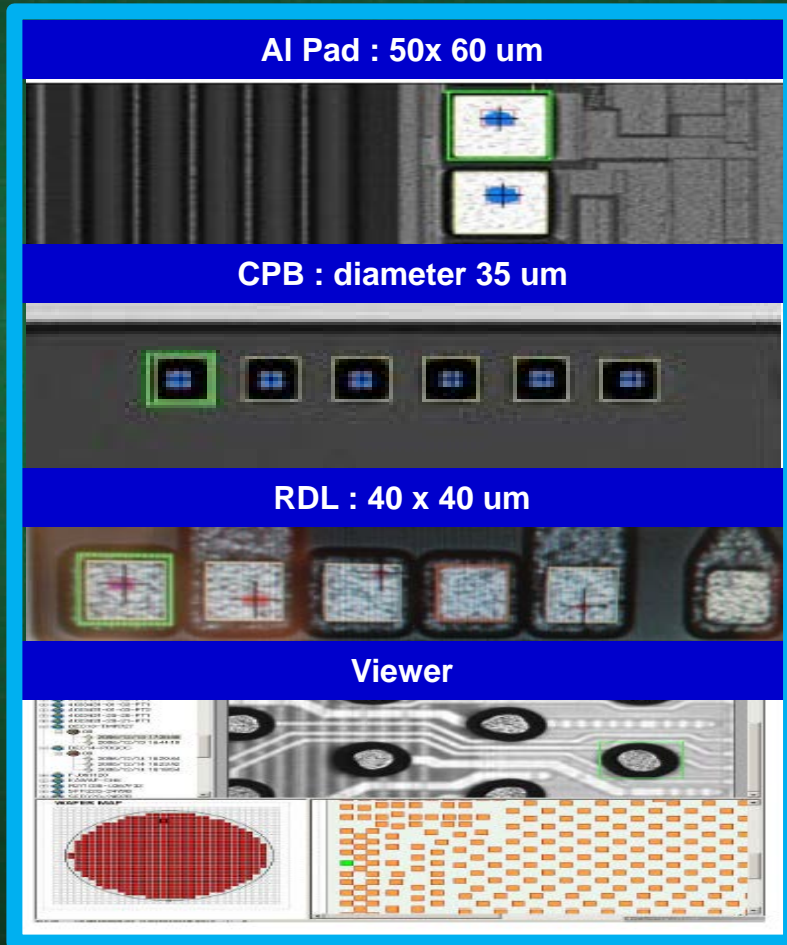


More Data to Analysis

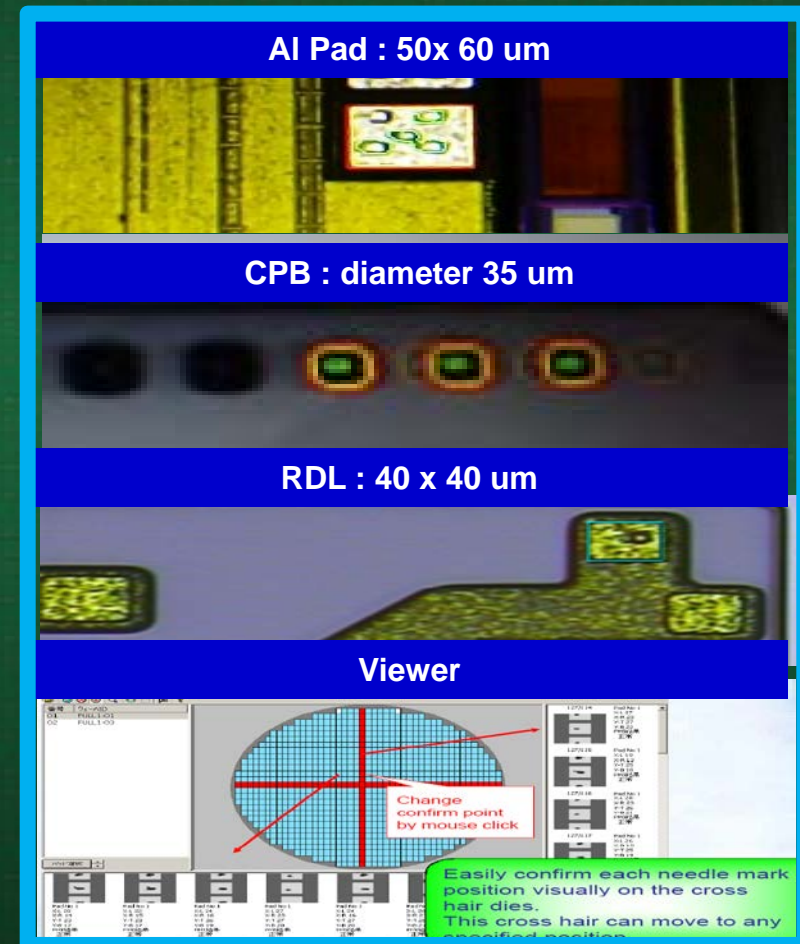


Prober PMI Technology

◆ TEL Precio -PADSi

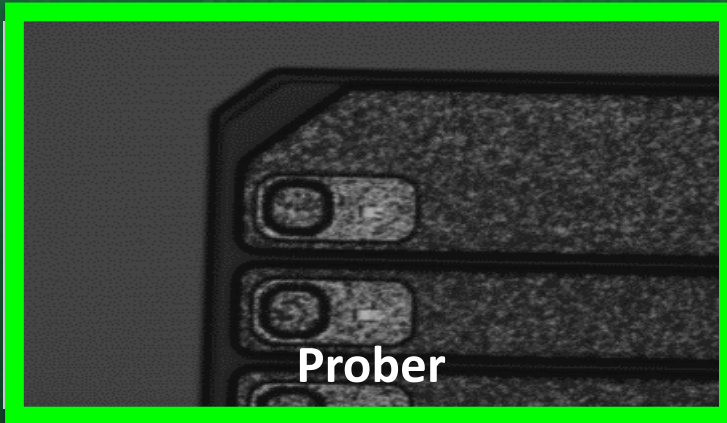
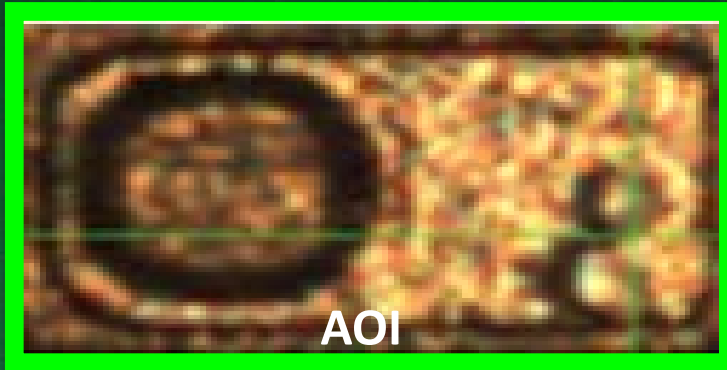


◆ Accretech UF-3000 –Fast PMI



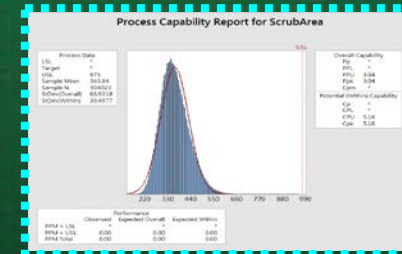
In Line Challenge: AOI and Prober for RDL

Probe mark Inspection



[Issue]:

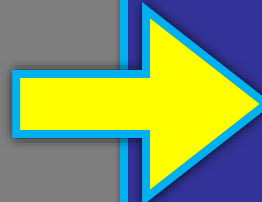
1. Customer Spec: Not allow probing out of RDL Pad.
2. AOI and Prober both can detect the Probe Mark under the RDL Pad or Not. But could not identify the Clearly P/M size with OD!
That will hard to check the setup issue!
3. Probe mark Inspection Analysis Technology still need vender support to development.



(2)Off Line Check Solution : AOI / 3DMS Technology

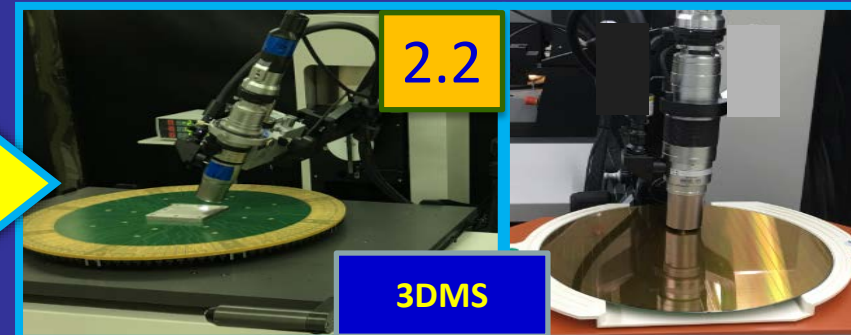
Past

Thinking

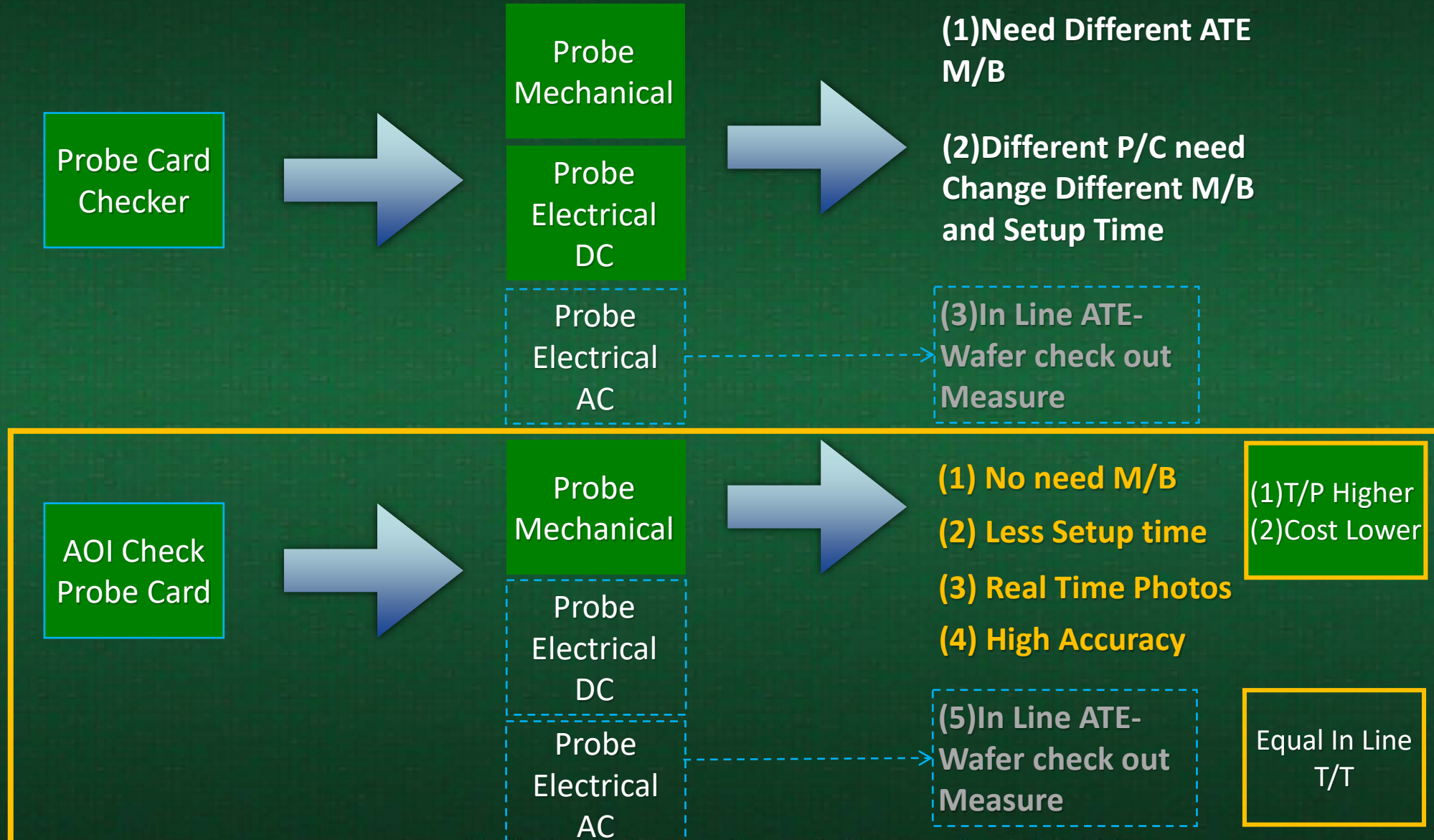


NEW

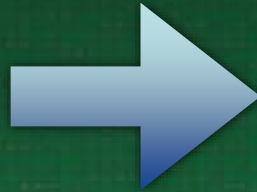
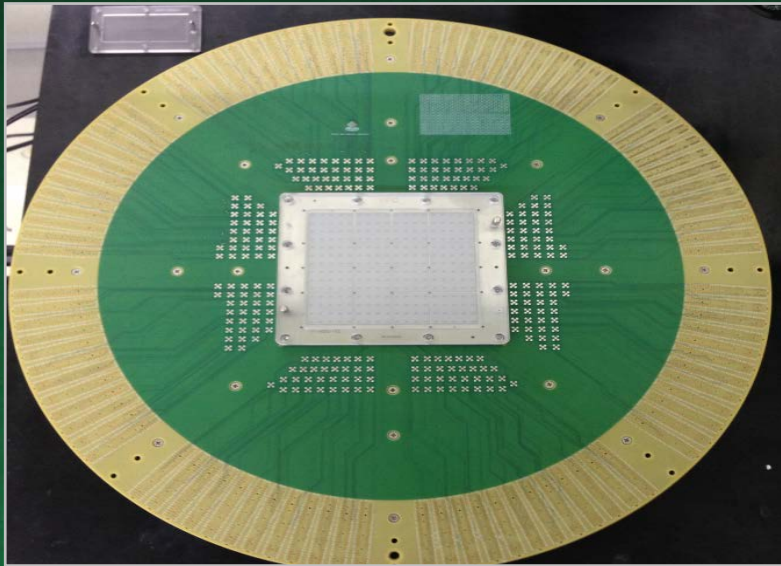
Thinking



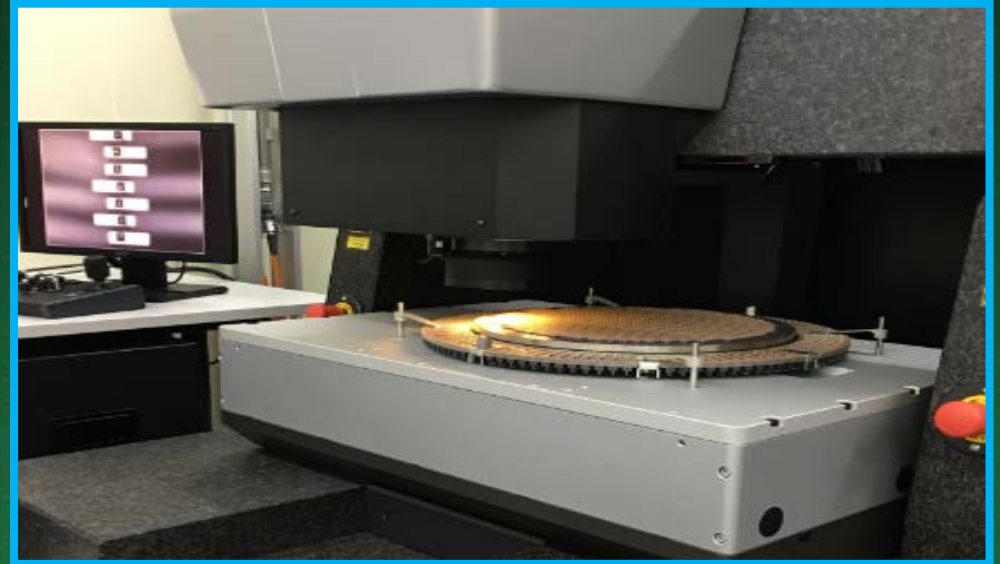
(2.1)AOI System Development Concept for Probe Card



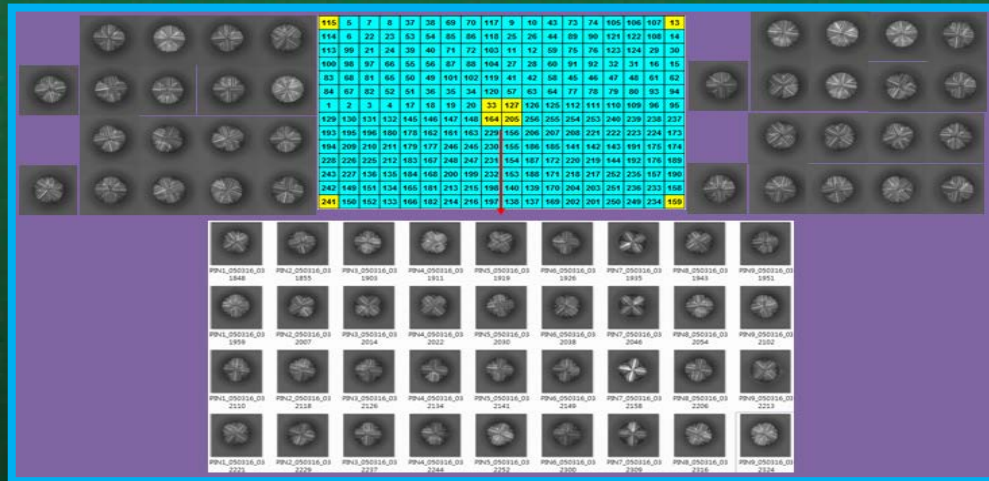
(2.1) Probe card Measurement _ AOI Solution



- (1) No Limited for Exist ATE P/C
- (2) High T/P
- (3) High Accuracy



Probe Pictures



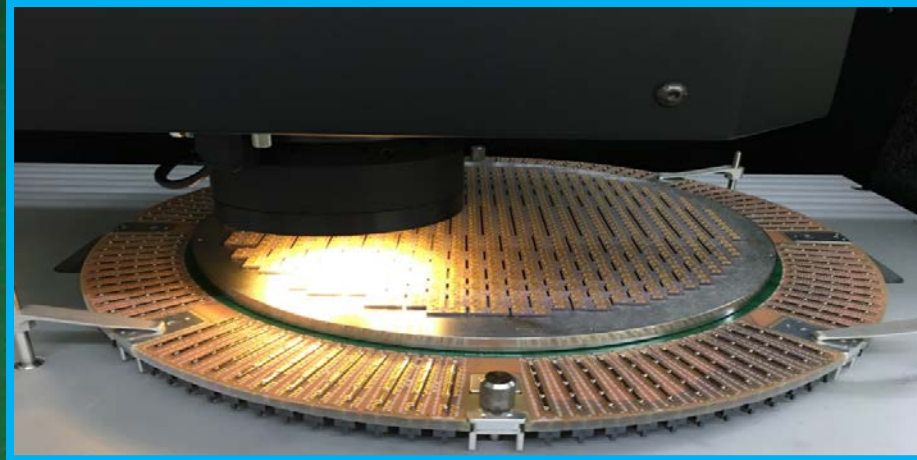
Probes (X,Y,Z) / Probe Head Data



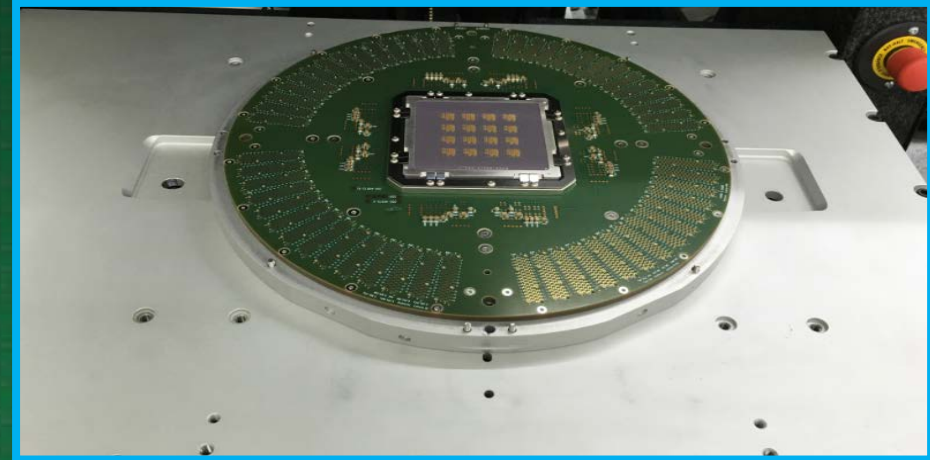
Probe Cards AOI Checker Solution

No Need Any Mother Board

T5377s-Full Contact Card



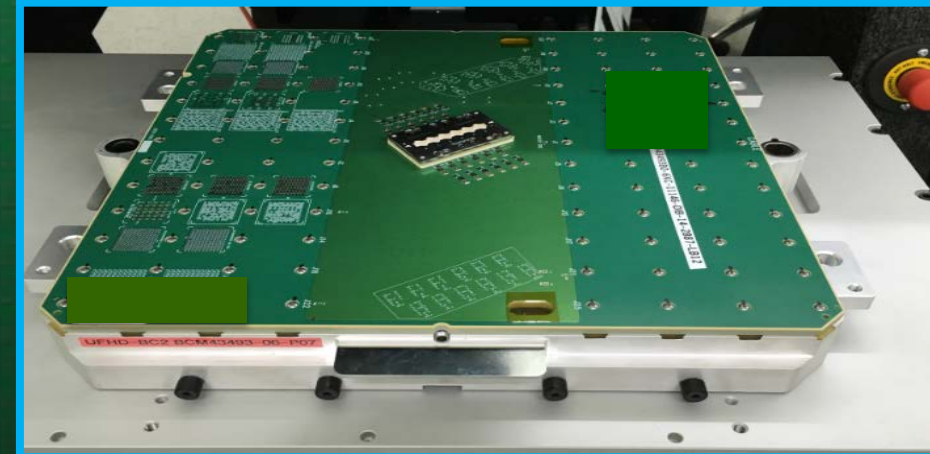
T5593 KGD Card



93K-DD Card



uFlex-DD Card

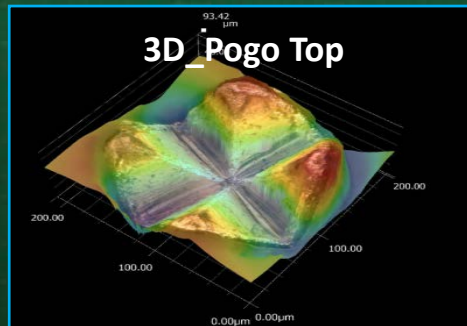
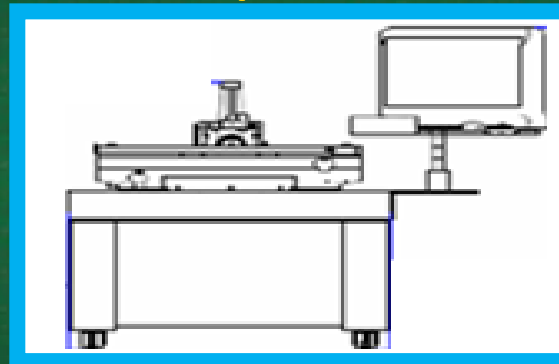
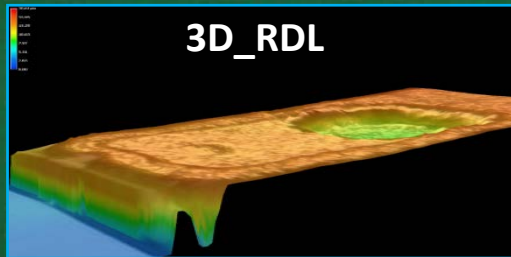
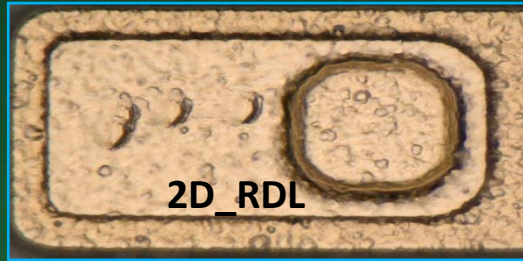


2016 SWTW :

Trying make 3D Microscope for WLP / Probe card

Engineering Analysis

Development for
Wafer and Probe card
Inspection

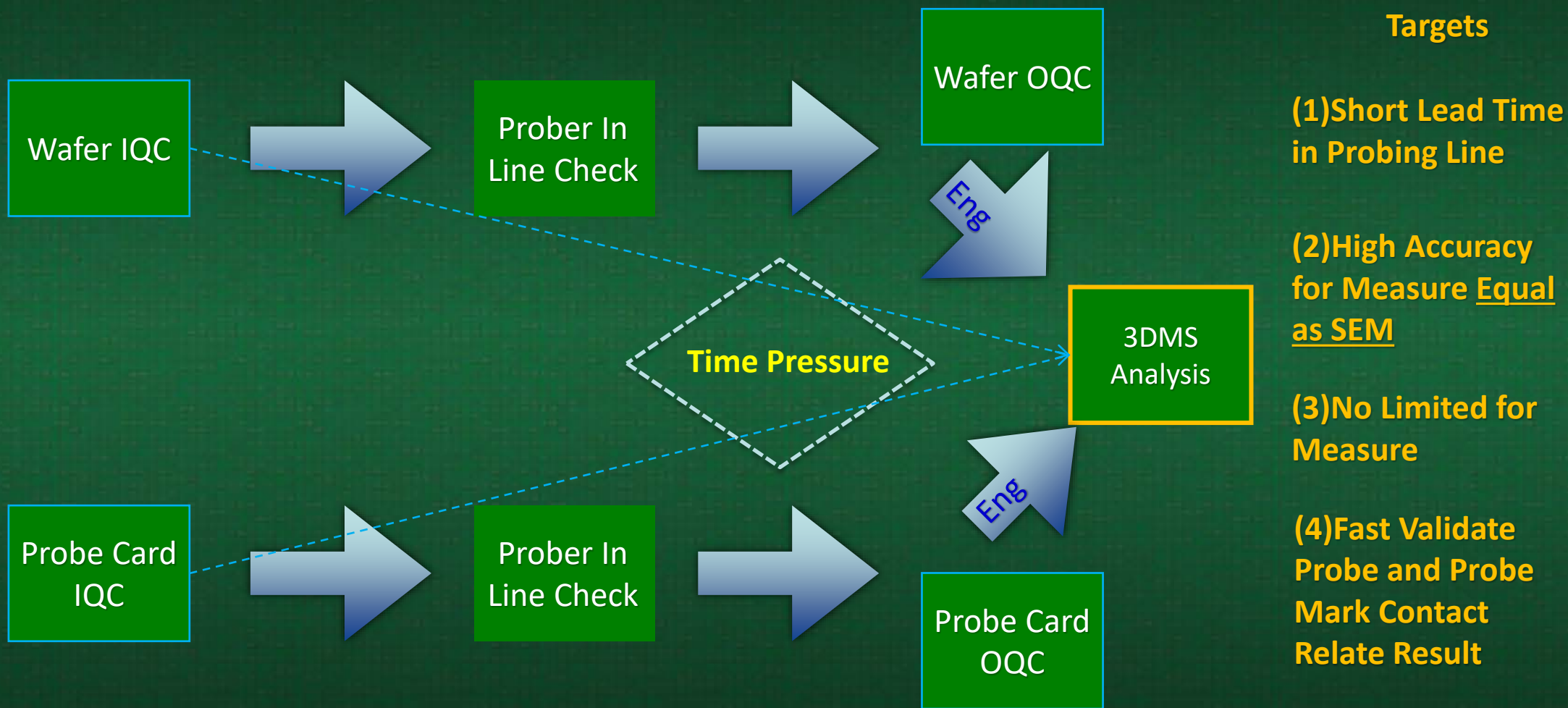


- (1) Try & Error for CIP
- (2) Need more times to develop this system

- (1) No Limited for Measure
- (2) High Accuracy like SEM

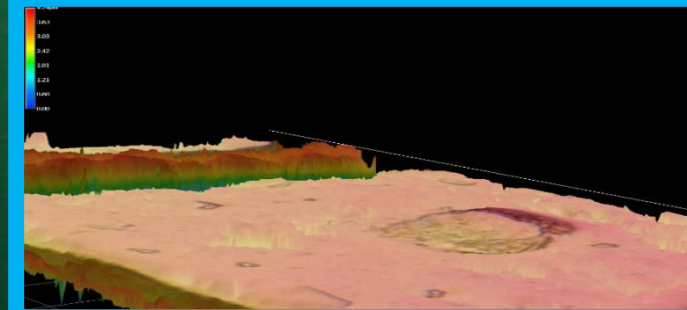
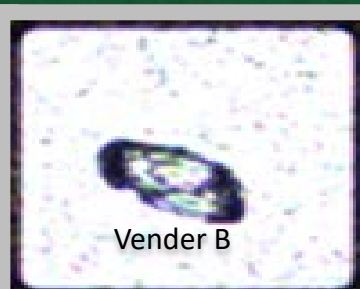
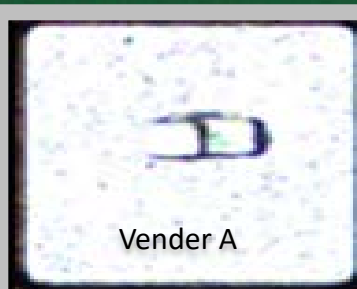
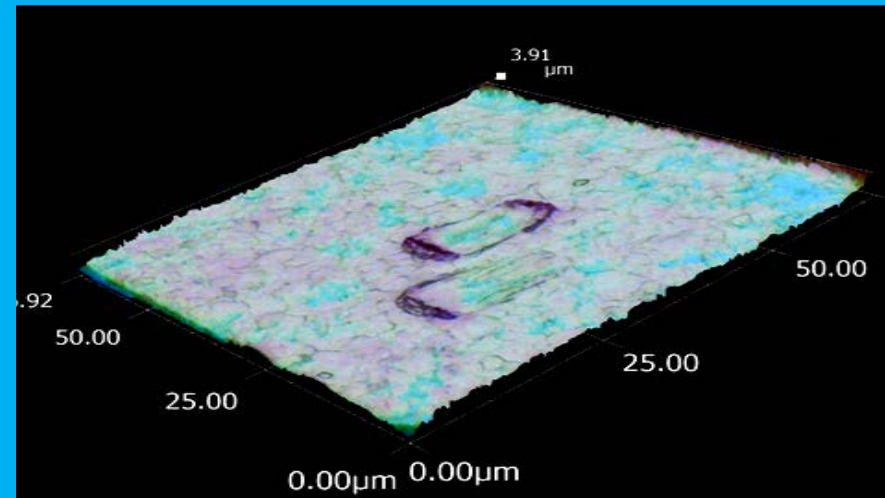
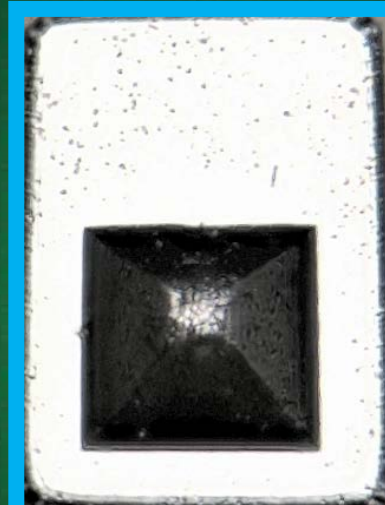
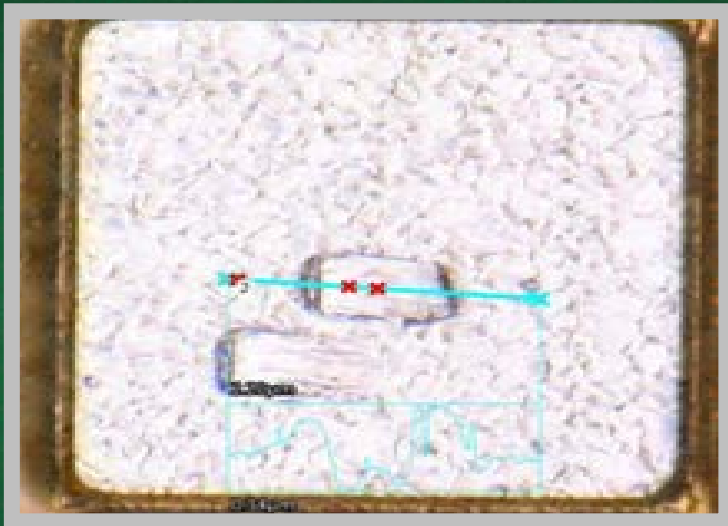


(2.2) New Inspection System Development Concept for Probe Card and Wafer



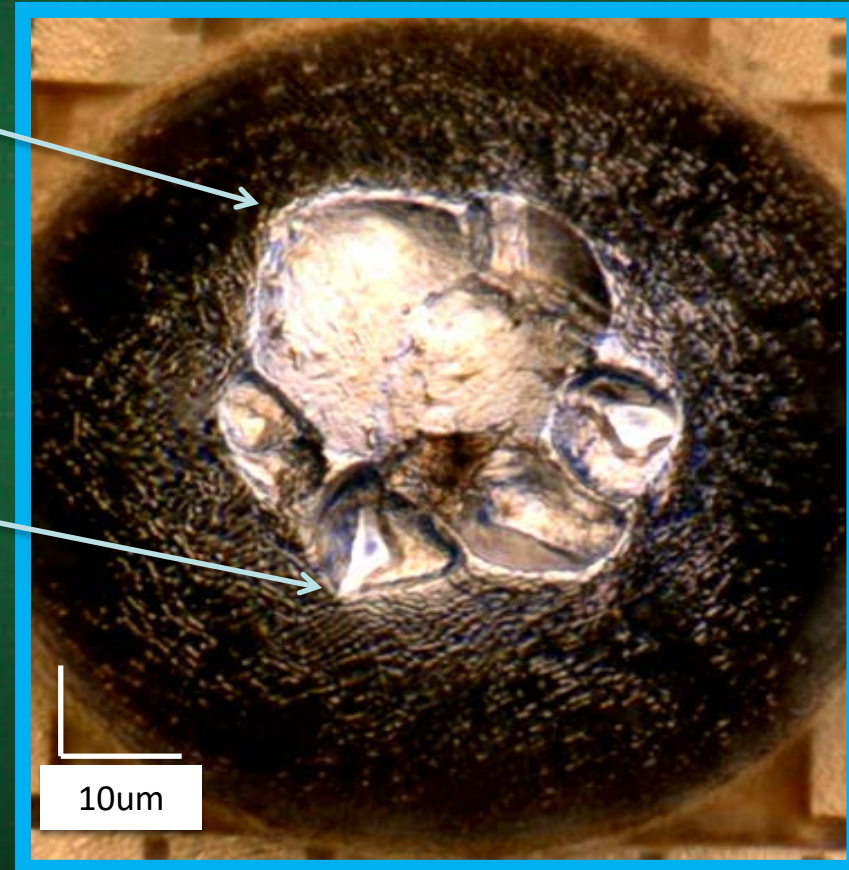
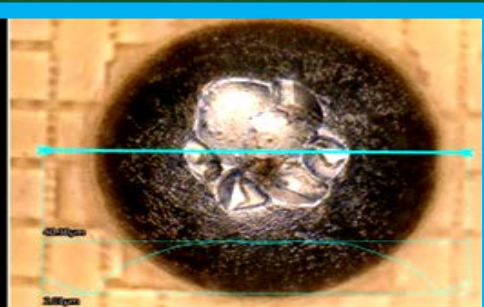
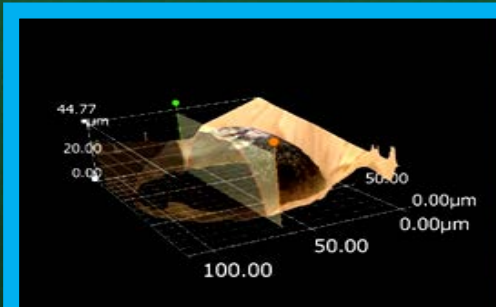
2D/3DMS for Al Pad Probe mark

◆ 2DMS: Probe Mark Inspection ◆ 3DMS: Probe Tip / Probe Mark Depth



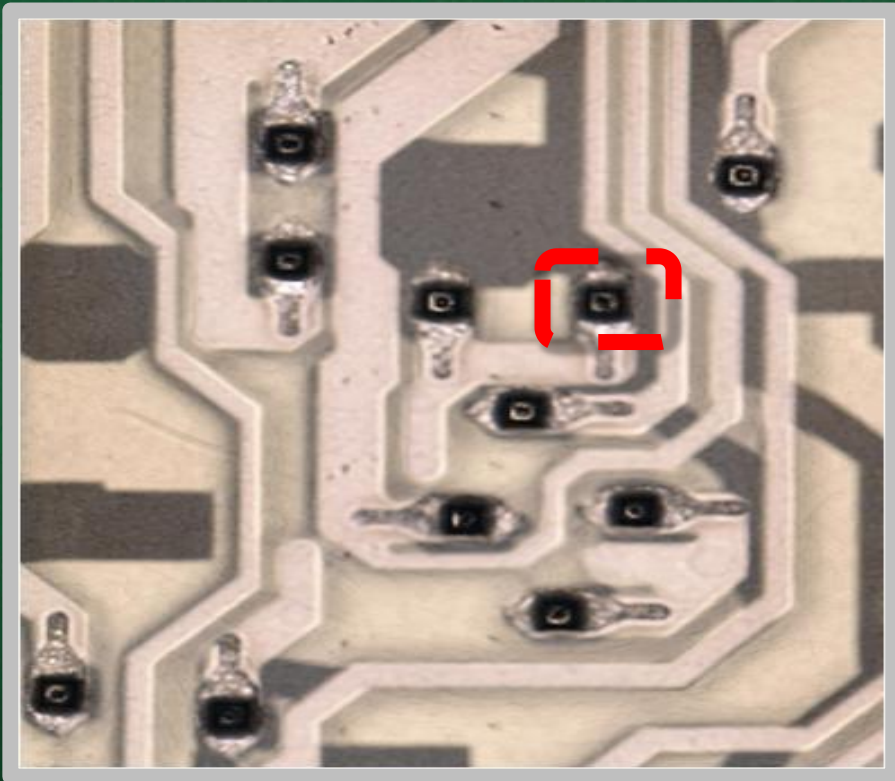
3DMS check for Probe and Bump

- Probe tip – Geometry / Debris
- Probe Depth Measurement

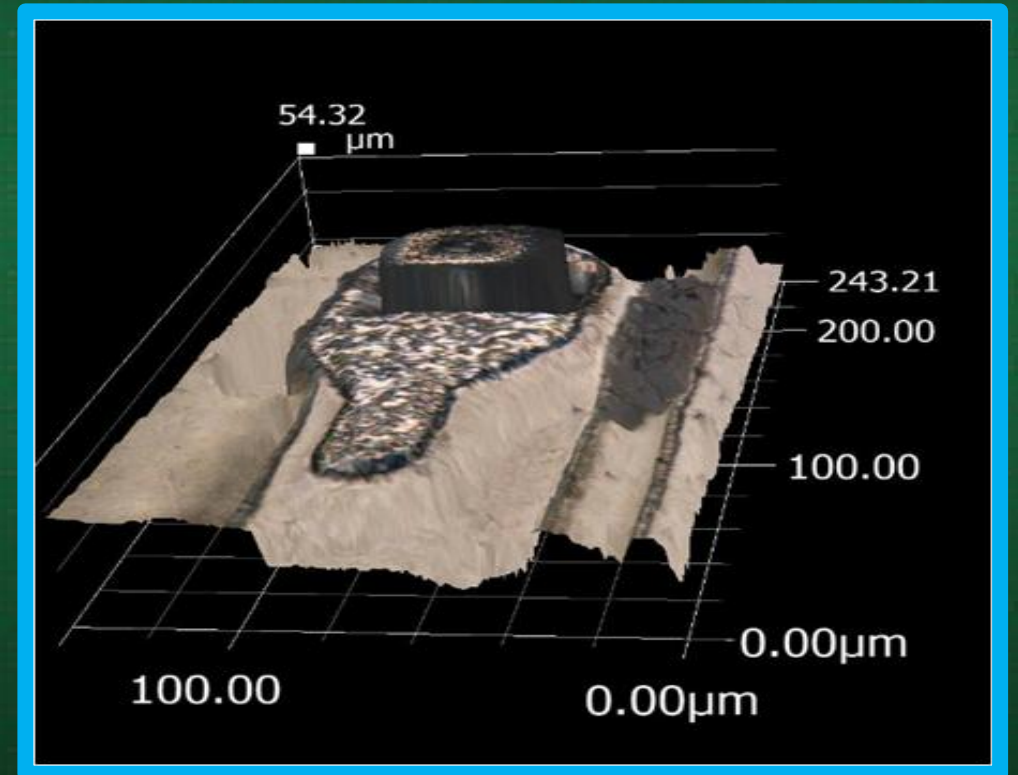


2D/3DMS finding for Probe Lifetime

- 2DMS- Probe Diameter/ Height- Probe Wearing Issue



- 3DMS-New Finding- + Membrane Structure Issue



3DMS for All P/Cs and Devices for Engineering Analysis Capability

P/C Type



uFlex P/C



T537X P/C

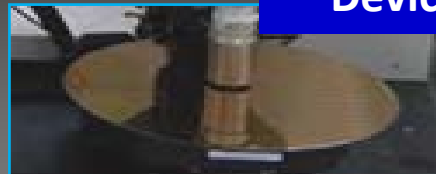


93K P/C

Flexible for Different Type P/Cs and Devices



Devices

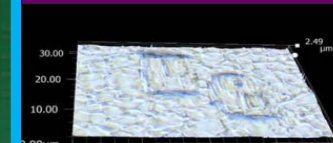


300mm Wafer

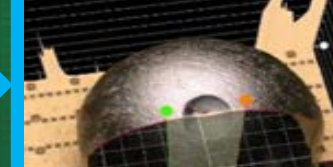


Sub Panel

Contact I/F



PAD



WLCSP



CPB



RDL



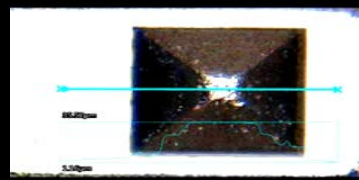
Probe Type



Membrane Probe

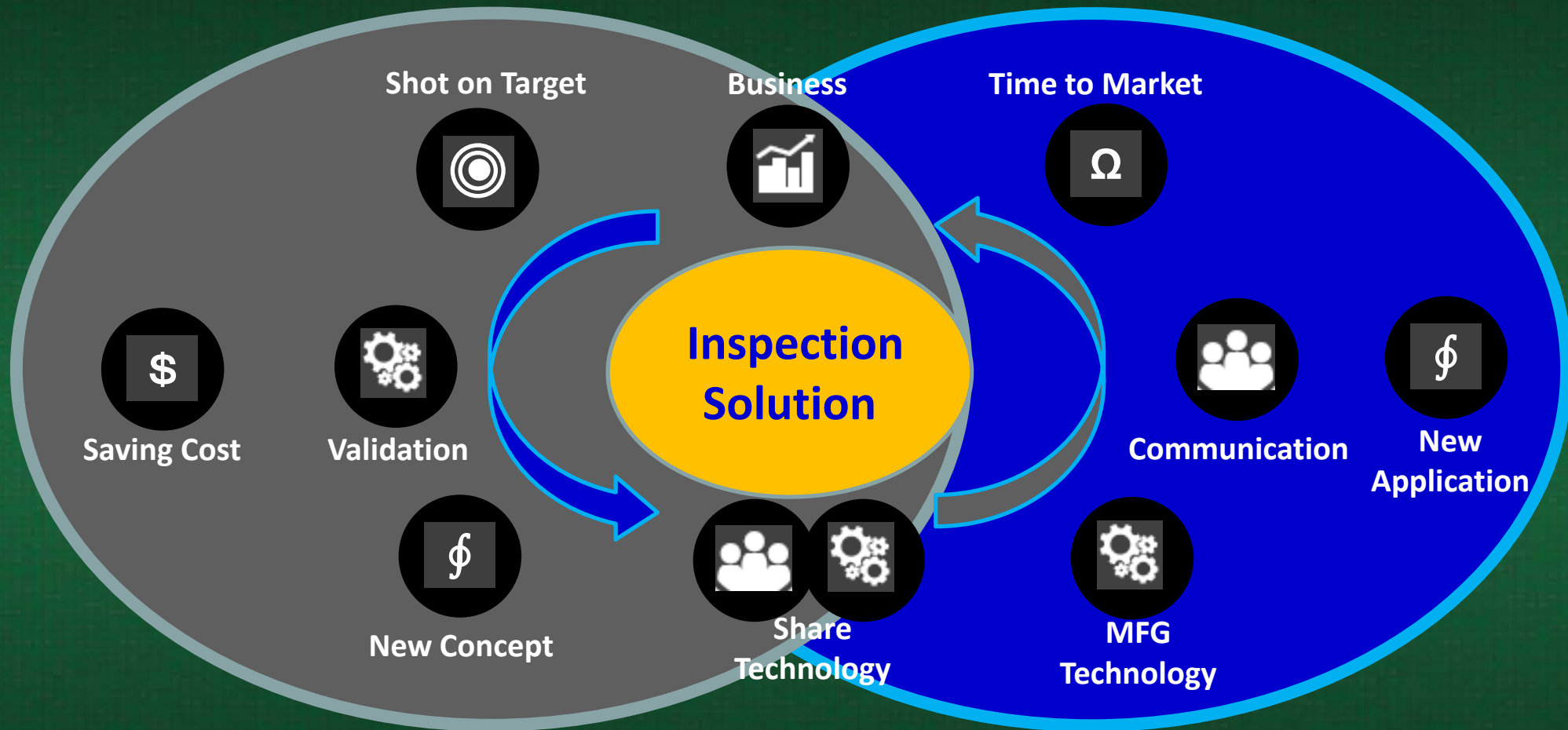


Pogo Probe



MEMS Probe

Conclusion



Build up the new working model for Customer Service & Probe suppliers! Helpful for Next Step Development!

Future Work:

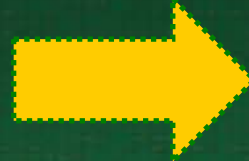
AOI New Function for WLP Probe mark Analysis

CPB

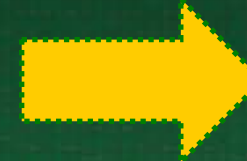
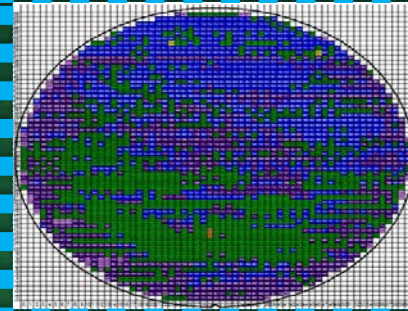
RDL

WLCSP

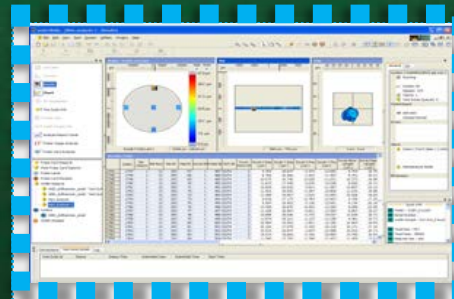
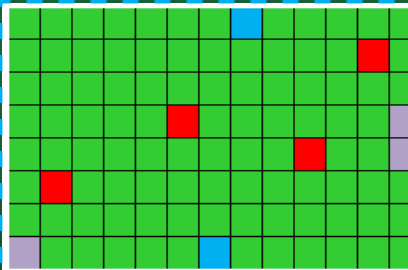
uBump



AOI /3DMS
Probing
Result
Analysis

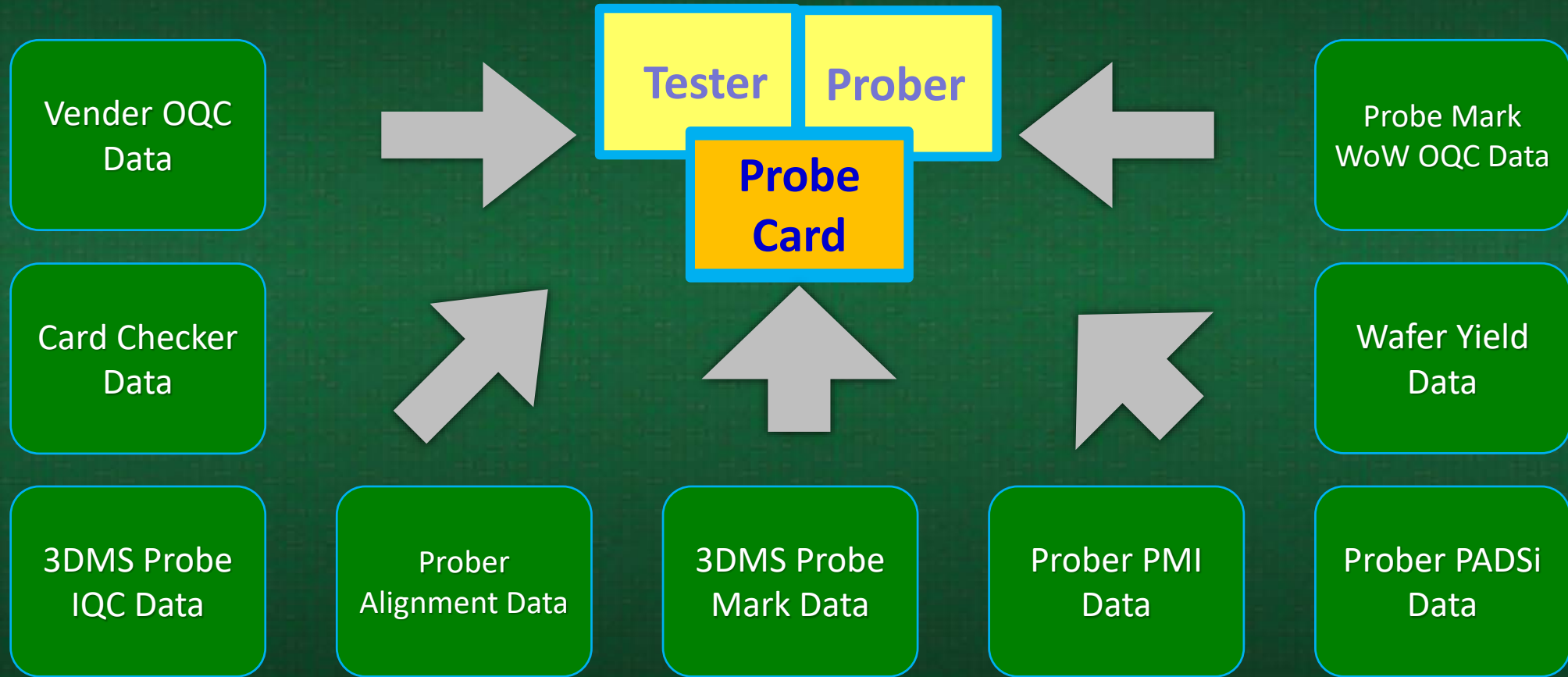


User /
Customer
Expect
Data



WLP I/F Shrink Trend Roadmap ,
Development Big Data to
analysis :
(1) Prober Performance
(2) Probe card Performance
(3) Validate New Probing
Technology

Future Work: Many Data Streams for Big Data



Acknowledgments

We would like to thank PTI colleagues support for this presentation.

(1) Henry Tseng

(2) Allan Ku

(3) James Hsieh

Also thanks suppliers fully support this project.

(1) Taiwan Local Suppliers

(2) Accretech / Rudolph / TEL

Thank you!