SW Test Workshop

Semiconductor Wafer Test Workshop

Device Interface Challenges of the Next Decade

TERADYNE

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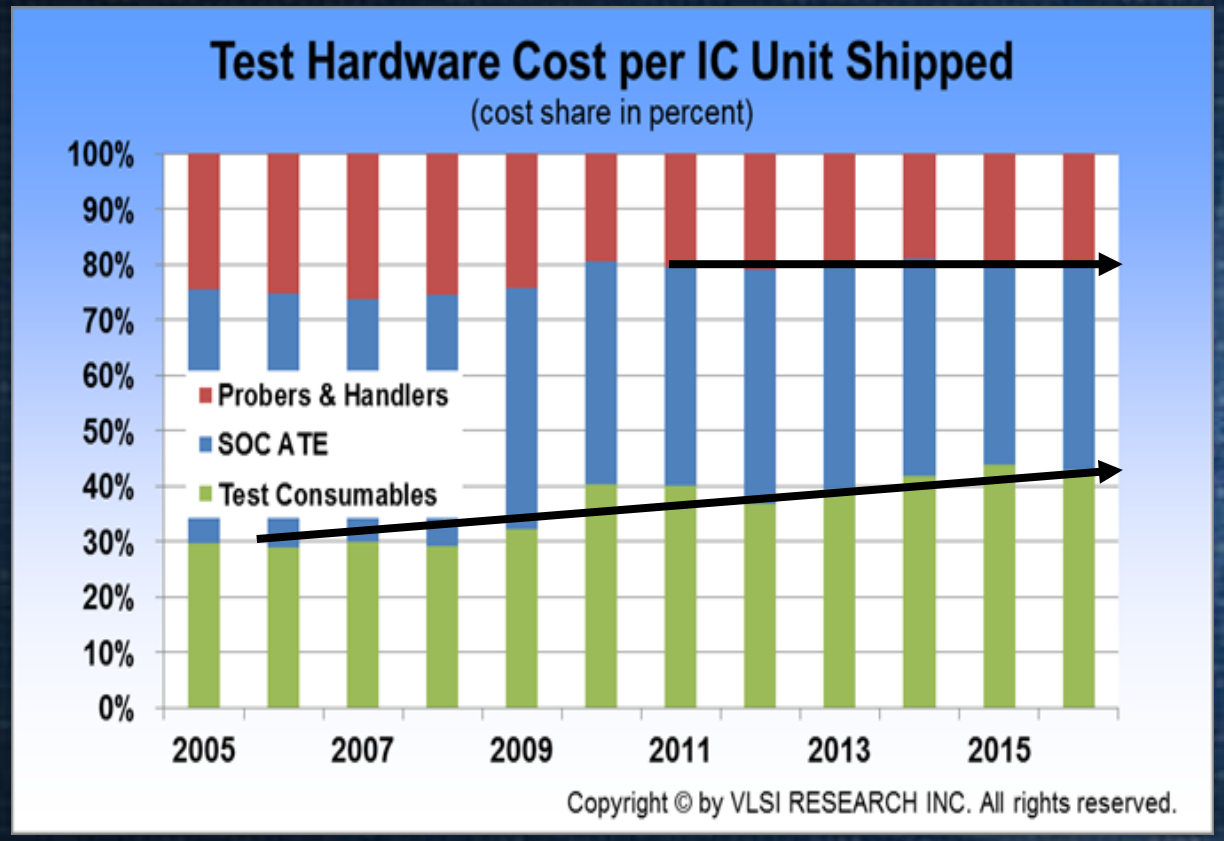
Outline

- Situation today
- End market drivers
- Importance of Time to Market & Time to Volume
- Density: I/O, power, and components
- “Sub-micron scale” Device Interface paradigm

Device Interface Challenges (today)



Handler/Prober Cost % → Flat

ATE Equipment Cost % ↘ Decreasing

Test Consumables Cost % ↗ Increasing

Consumable spend = Tester spend!

Device interface complexity doubles every 4 years

- Decreasing pin pitch
- More pins, more components
- Higher performance: electrical & mechanical
- In the same area or larger

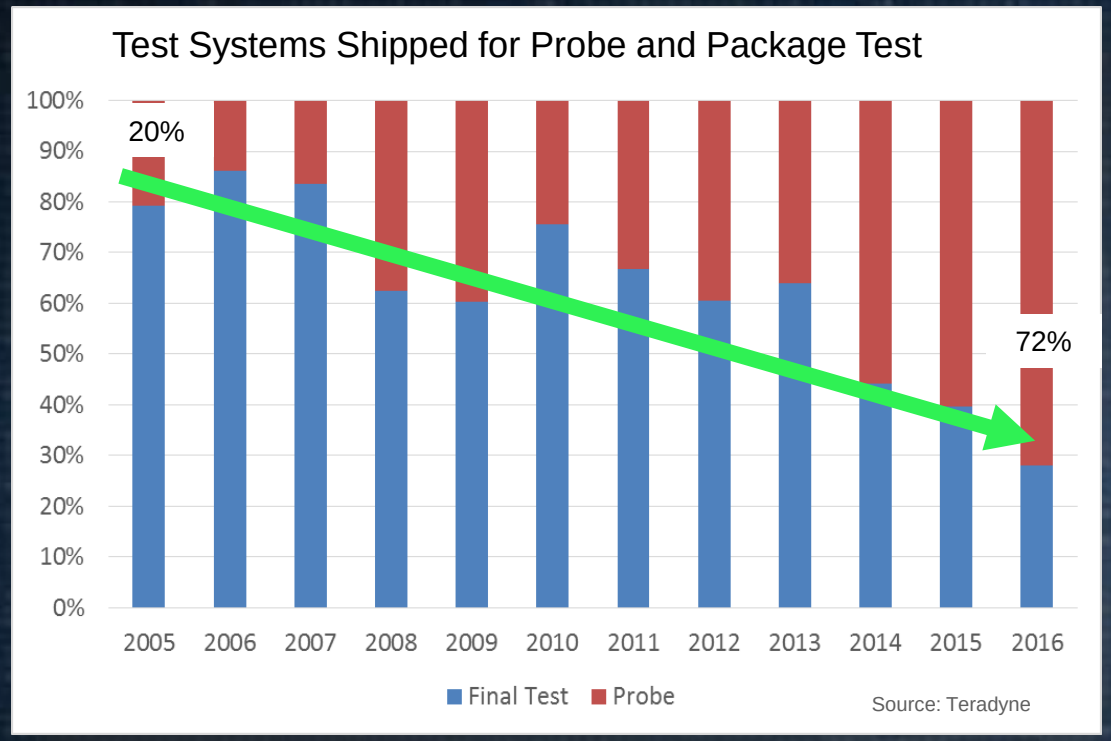
Site count limitations emerging

- Touchdown efficiency @ wafer sort decreasing
- Handler limitations @ final test

Declining DIB execution metrics

- Defect density limits scaling
- Poor yields with new materials and processes
- Long leadtime – longer than time to make silicon wafers!

Transition to More Probe Test

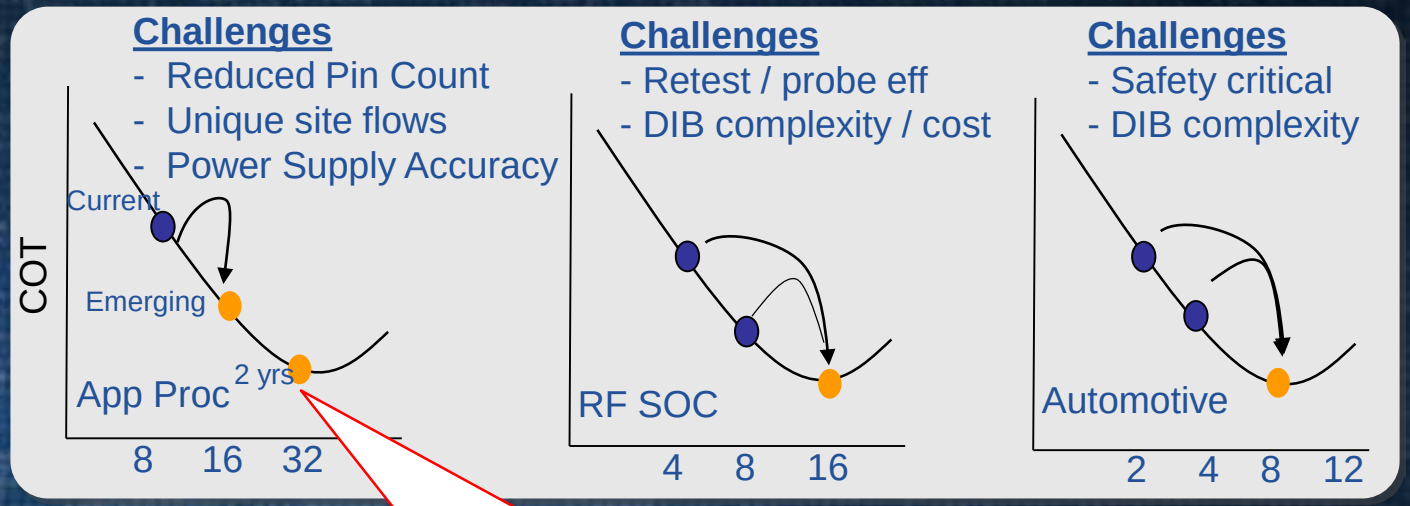


- Greater % of Complex SOC ATE is sold for Probe test
- Most AP and PMIC devices are trimmed at probe
- Multi-chip packaging (logic + memory) economics require KGD
- Major drivers are cost reduction (final test insertions to Probe) or size (chip scale packaging)

Wafer Level Packaging

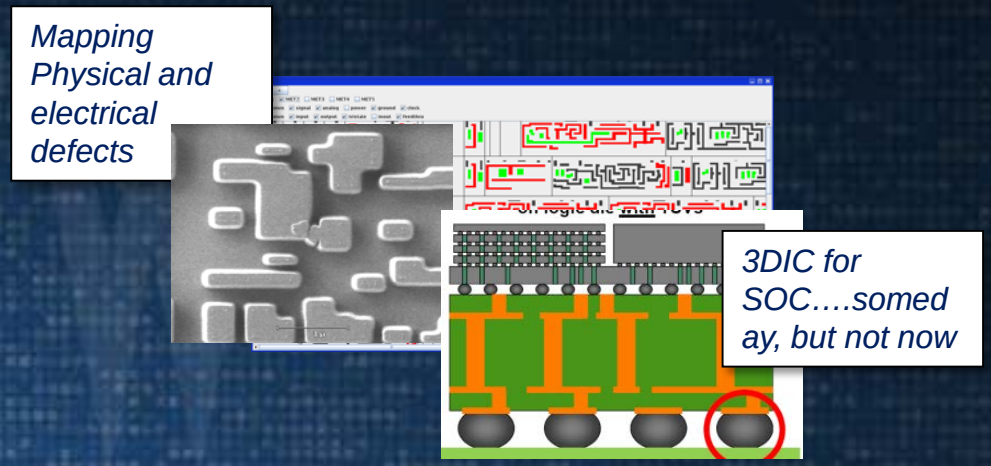
Complexity Inflection Point

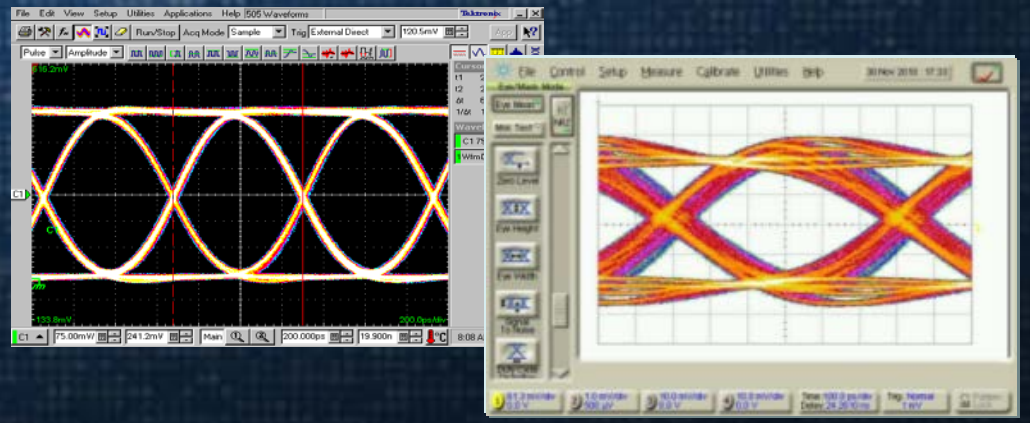
- **IO density problem – lots of great tester resources, but how do I get them to the DUT?**
- **Dimensions of the problem:**
  - **DUT area I/O & power density**
  - **Performance vs density**
  - **Process scaling**
  - **Speed of execution**
- **“It is a system problem at the test cell level”**



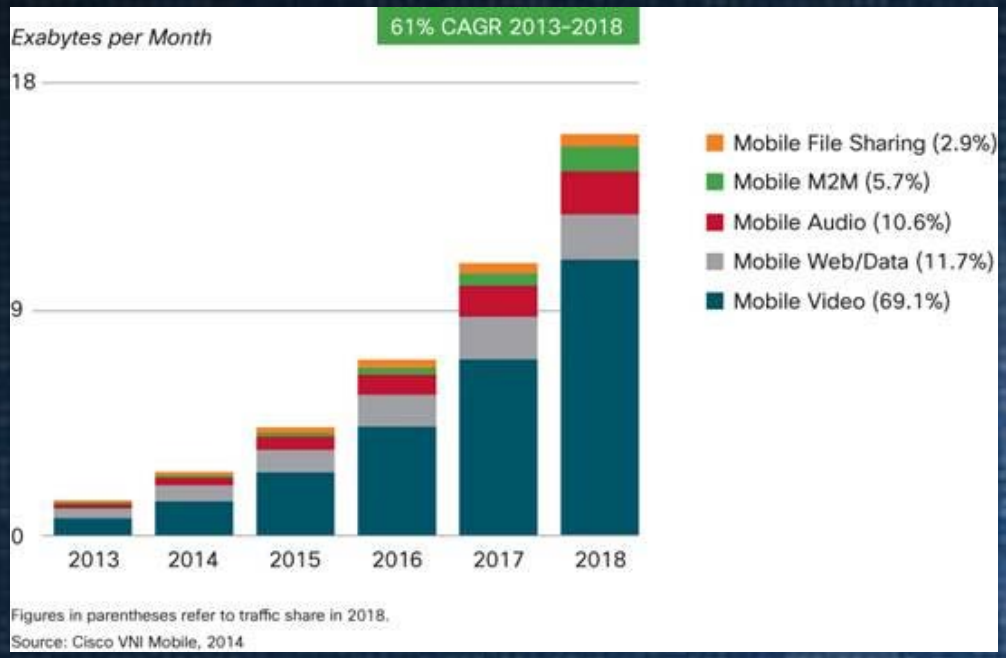
Mobile Processor Trends

- **More Cores, More Gates ➔ More I/O & power pins**
  - Test Times increasing ~ 10 to 20% per year just due to device complexity
  - Increasing parallelism is typically the counter, but worsening TDE is eating up gains.
- **Cost per transistor is not going down fast enough, driving multi-die packages**
- **Increased challenges with high speed IO**
  - DDR Interfaces as fast or faster than traditional PC memory
  - High Speed Serial Tests
  - DFT will get more difficult at higher speeds

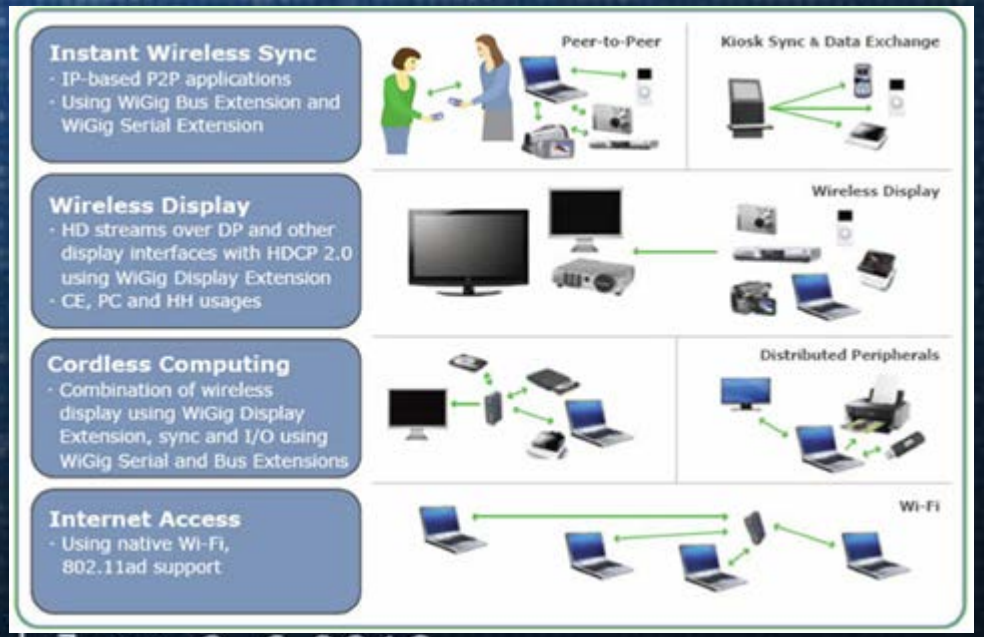




Wireless (RF & mmWave) Trends

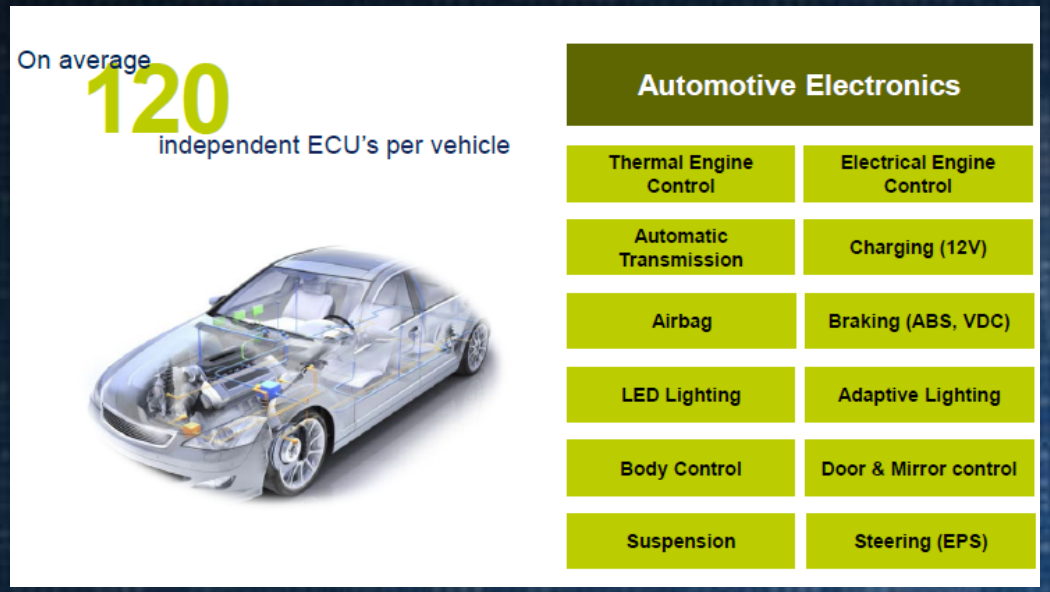


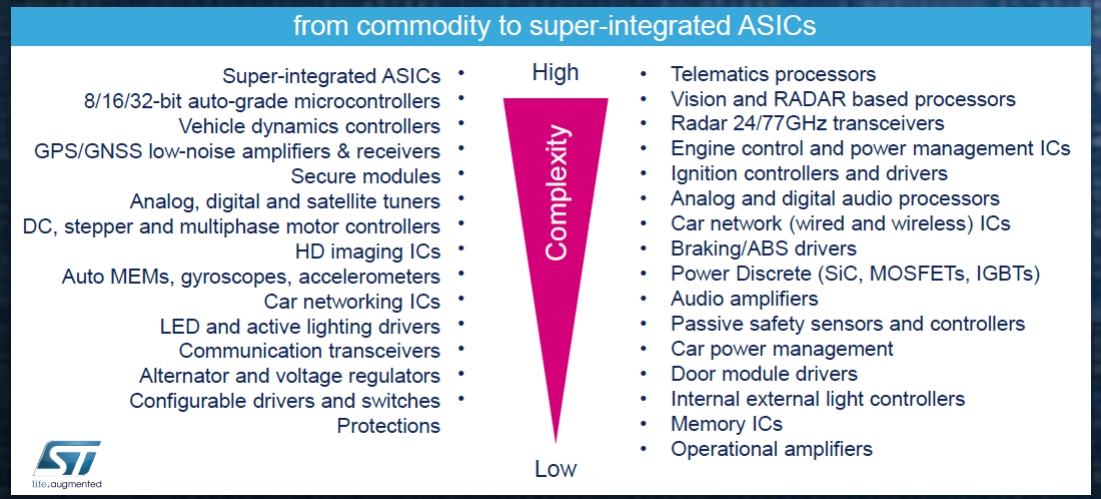
- **Increase Demand for Higher Data Rate & Connectivity**
  - Overall mobile data traffic is expected to grow at a 61% CAGR to 15.9 Exabytes per month by 2018
  - MIMO & Carrier Aggregation requiring 2x-3x more active RX & TX device ports
  - Cell and backhaul infrastructure improvements needed to support higher data capacity



- **Expanded use of mmWave for Consumer Applications**
  - Line-of-site data transfer for uncompressed video and infotainment
  - Wireless “Last Mile” (+29GHz and above)
  - Auto Radar (+72 GHZ)

Automotive Trends





Improvement in emissions, performance, and safety are due largely to advances in semiconductor technology

High performance semiconductor products have made their way to the car:

- Vehicles are a "rolling supercomputer"
- Automotive reliability adds at speed tri-temp testing (-40 to +150C) and more….

New electrical components bring new device interface requirements:

- Packaging & handling: power modules
- High voltage: +1kV
- High current: +1kA

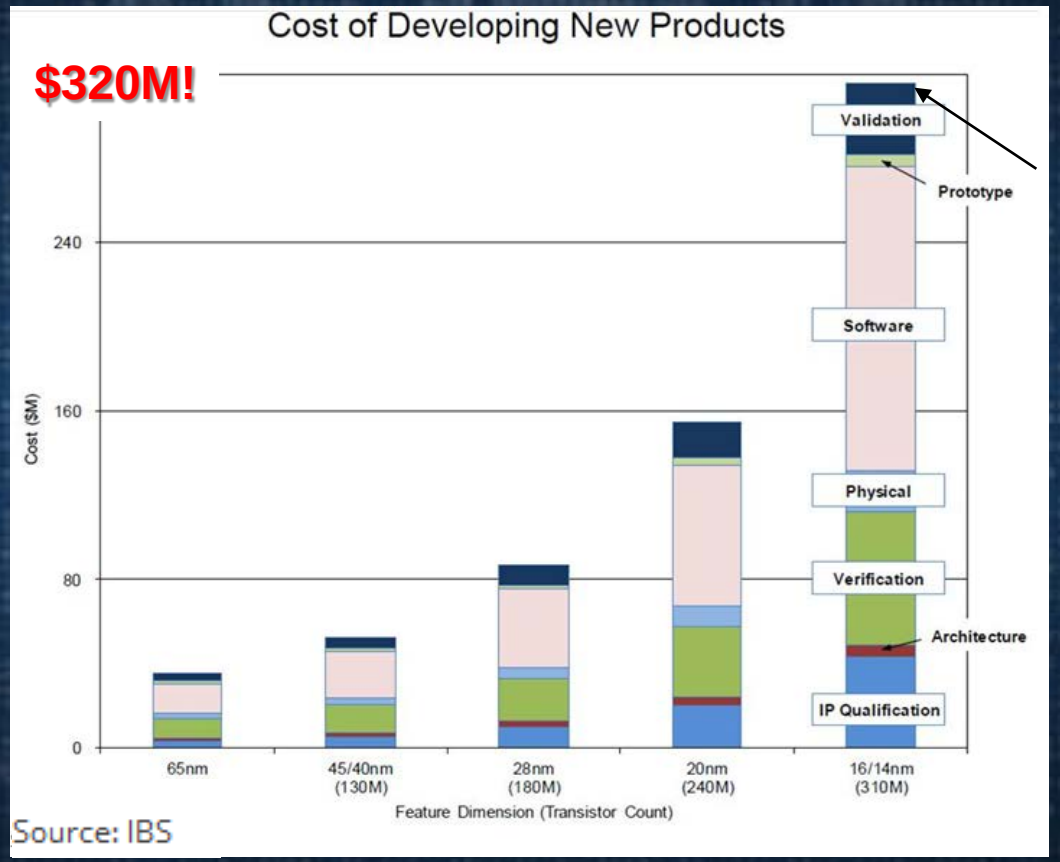
Product safety and reliability take on significant role in ATE applications

- Power ratings can hurt or kill people if not properly safe-guarded or fail.

IC Development Costs – Time to Market

Time to Market & Time to Volume requires:

- **First pass device interface NPI success: functional and full performance**
- **OTD at +95%**
- **Manufacturing leadtime matching first silicon run time, generally 21 to 28 days from silicon tapeout to wafer out**

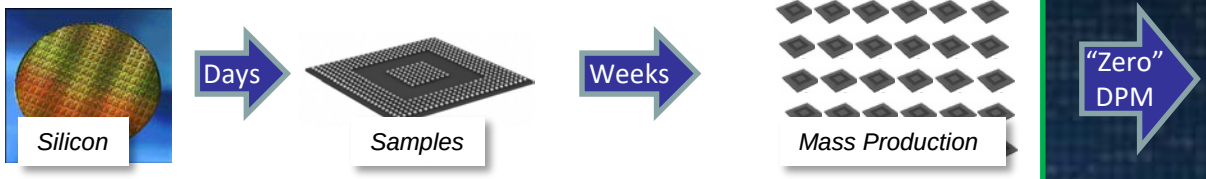


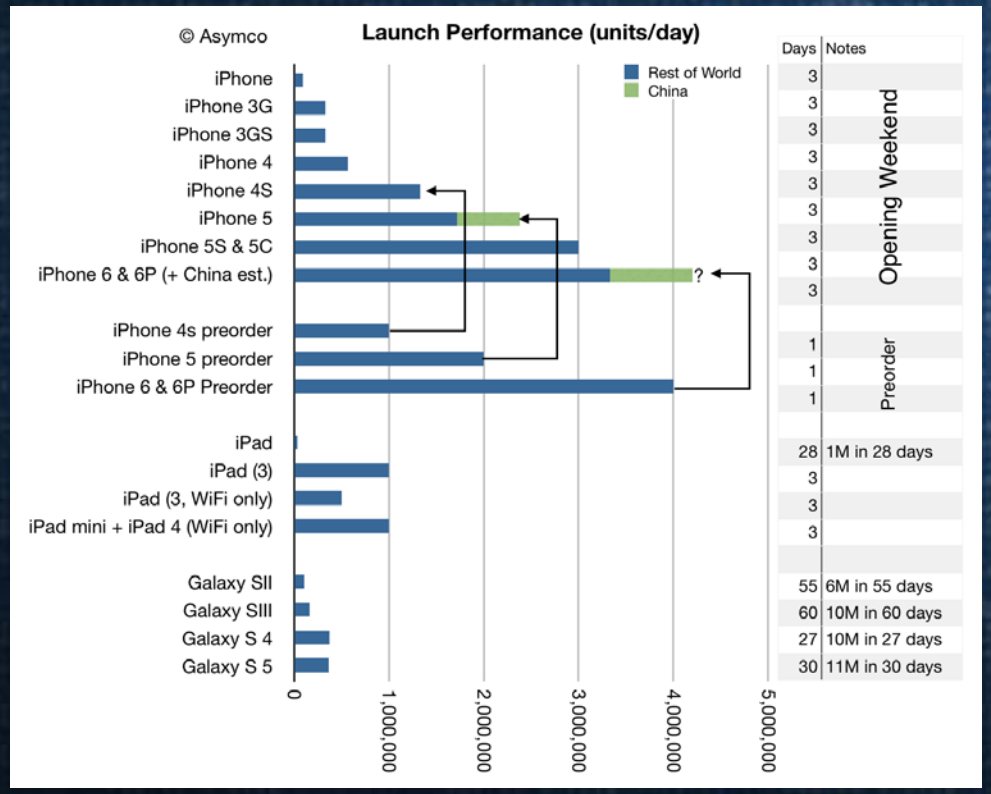
Cost of Test Development (<1%)

Risk mitigation cost to ensure first pass NPI success (leadtime, OTD, quality) has high leverage to maximize return to silicon dev expense

Time to Volume

COT is important but getting to market quickly with the best quality is what really counts!



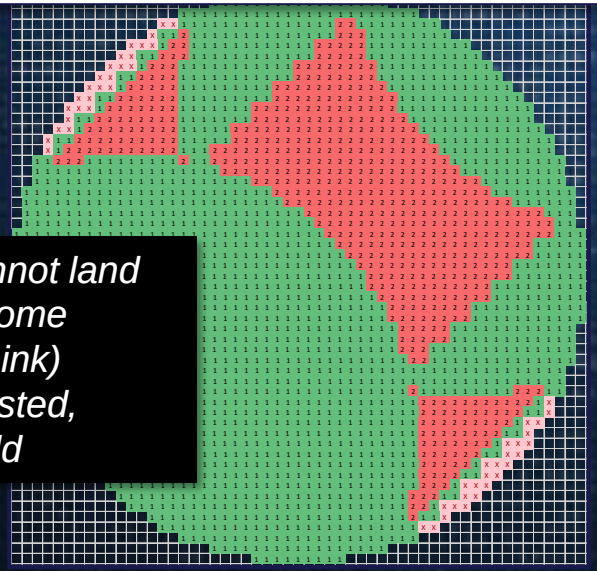


- **Fast Ramps: Essentially full volume from product launch for high profile new products**
- **Must bring up new silicon process at the same time (example: 14nm FinFET)**
- **Yield must be good to reduce cost but defect rate must be extremely low**
- **Device Interface must be perfect on first iteration: functionality & performance**

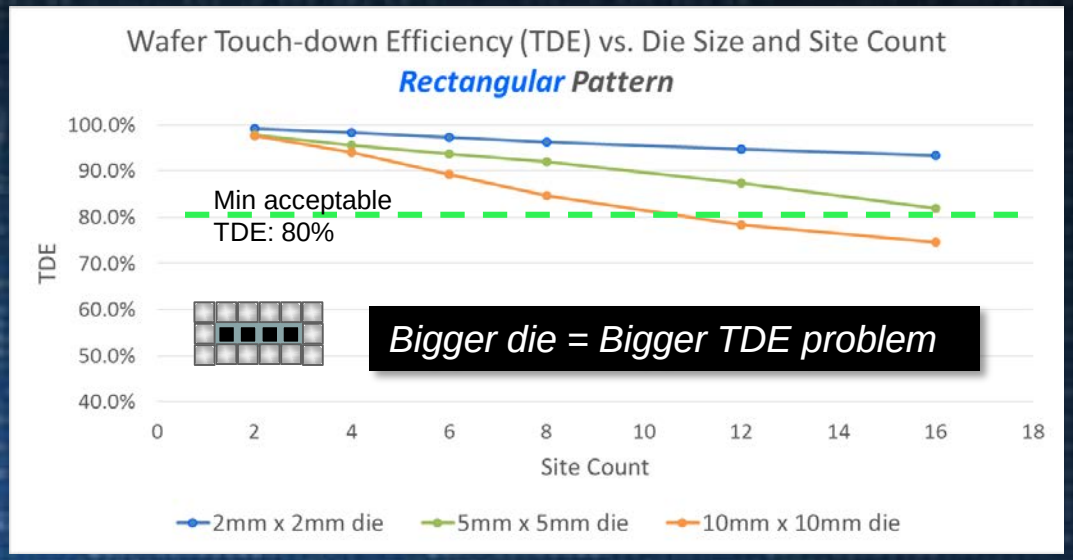
I/O Density – TDE problem

- **Throughput gain by increases in wafer test site count is destroyed by poor touch-down efficiency (TDE)**
- **TDE limited by I/O & power routing density**

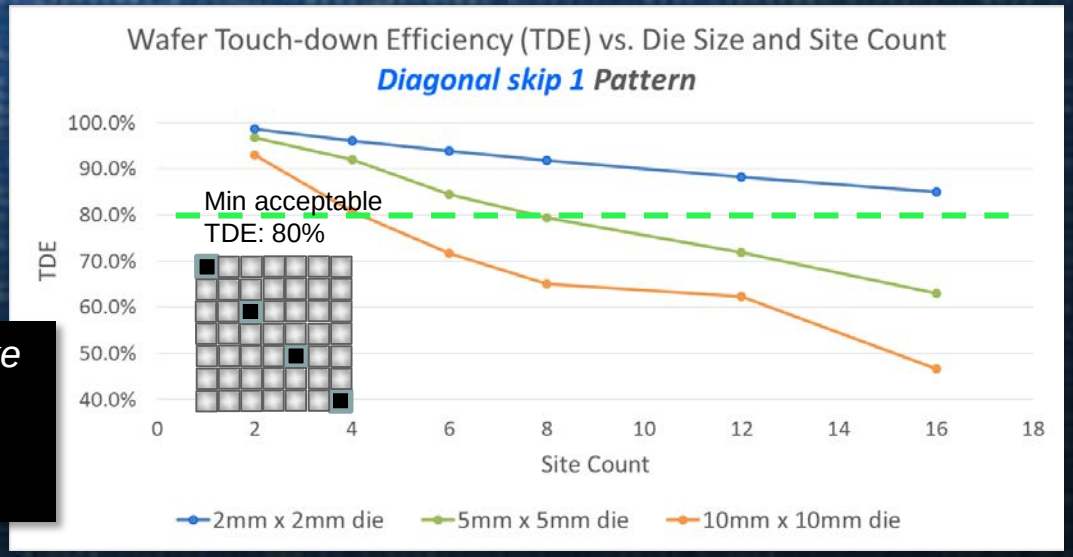
Touchdown pattern, 8 site diagonal 5mm wafer without going off-die



If probes cannot land off the die, some devices (in pink) cannot be tested, reducing yield

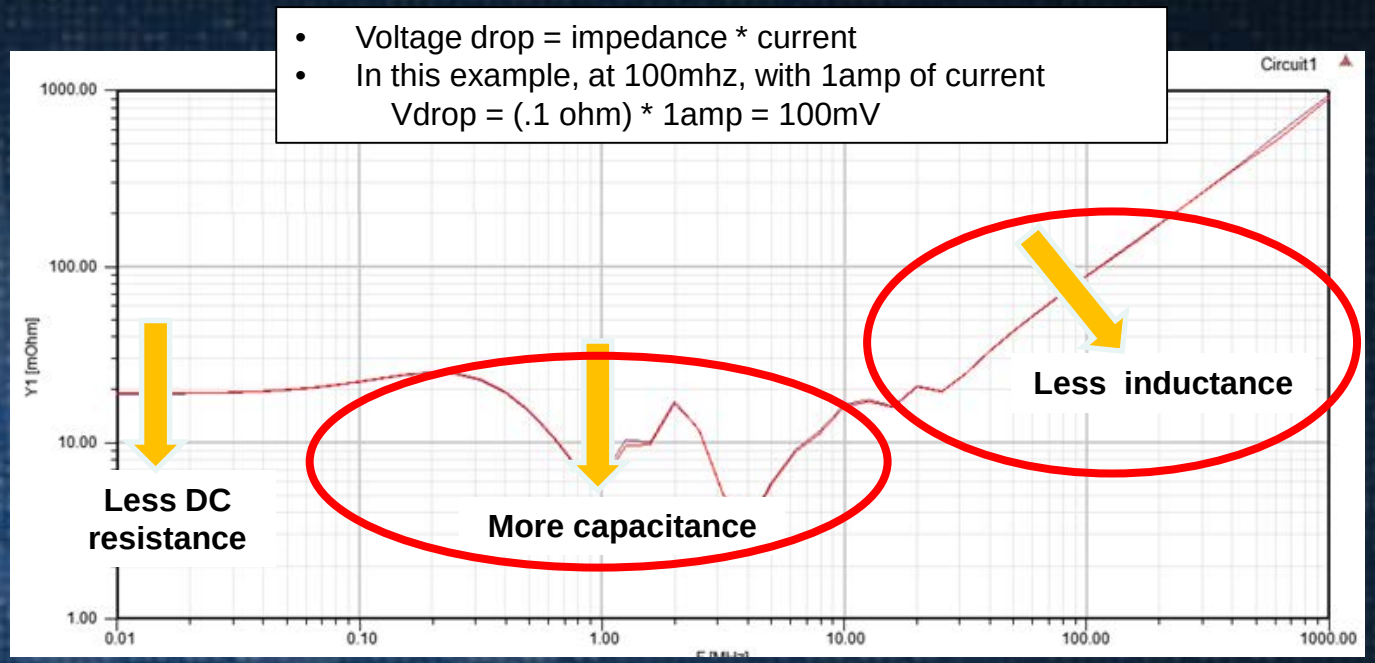


Skipping die to make probe card layout easier makes TDE even worse



Power Density - Power Impedance

- **Many devices need less than 10% voltage drop from nominal power input without impacting yield**
  - Power rails continue to decrease in maximum voltage as transistor size shrinks
  - 900mV (today) ➔ 600-700mV (2020).
  - 90mV droop (today) ➔ 60mV (2020)
- **Number of power rails continues to increase:**
  - App Processor: 20+ rails / DUT
  - Auto MCU: 10+ rails / DUT
  - RF: 8+ rails / DUT
- **Challenges:**
  - Site matching: <2-3% site/site variance
  - Power rail density: ~4 rails / layer (today)
  - Needle / socket pin impedance. Contact technology is limiting performance gains.



	Rails / DUT	Site Count	PCB Layers
AP	20	8	40
Auto MCU	10	16	40
RF	8	16	32
PMIC	20	8	40

+60% of PCB layers and increasing. Already limits site count increases

Component density - yield & diagnostics



AOI

Fault Coverage: 30%*

Limitations: small component (< 0201 body) faults need 10um defect resolution to identify

Flying Probe

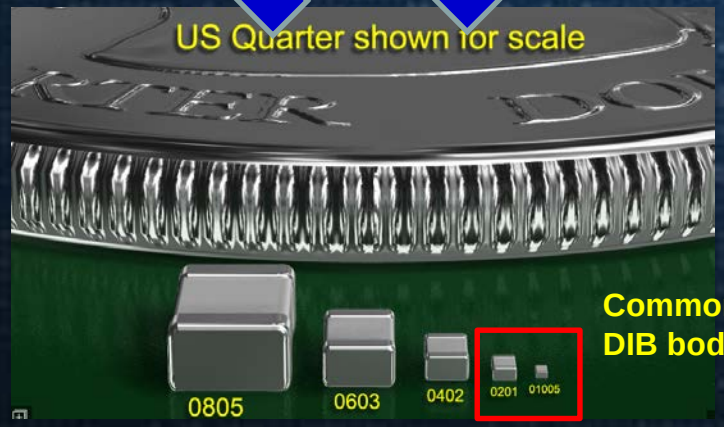
Fault Coverage: 37%*

Limitations: small component (below 0201) cannot be accessed to probe

In Circuit Test

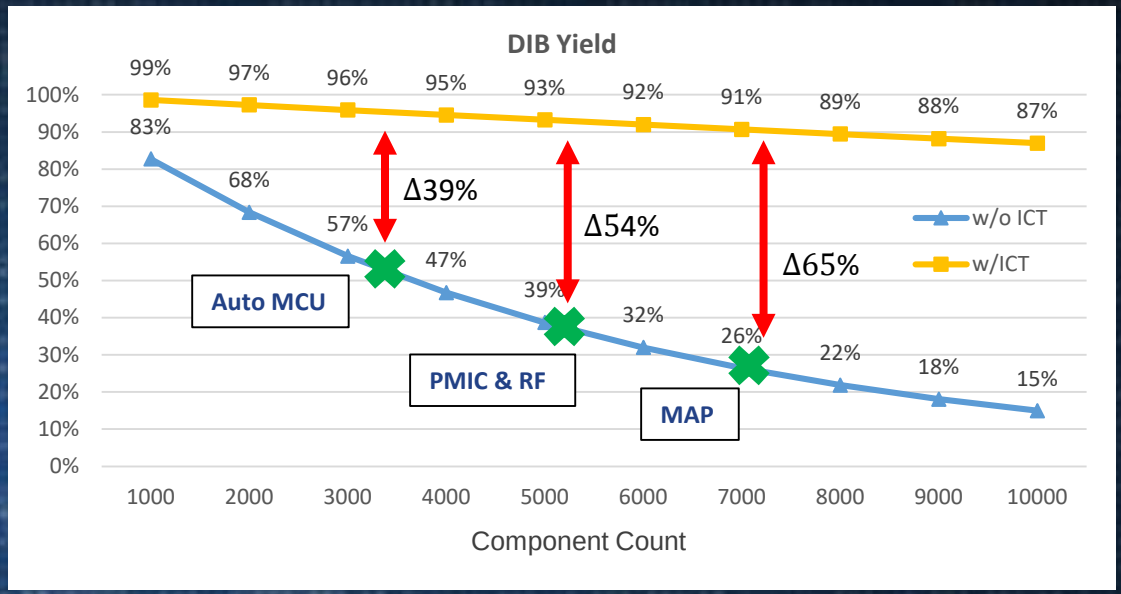
Faults Found: >80%*

Limitations: lead time (>6 wks), cost prohibitive ($+60K) , and intrusive (test point insertion)



Common ATE DIB body sizes

High component count + small body size = poor yield



Assembled DIB / probe card yields impact new silicon bring up time:

- Unknown, random assembly defects are difficult to differentiate from defects in new silicon or test programs.
- Conventional practices (AOI & Flying Probe) have low fault coverage, ICT not feasible for custom DIBs (long lead time, test point insertion)
- Physical defects: DUT area scratches, pad planarity all at micron scale

Component counts will continue to grow

- Application space is fixed, site count will continue to grow
- Application circuits becoming more complex, more like the end application

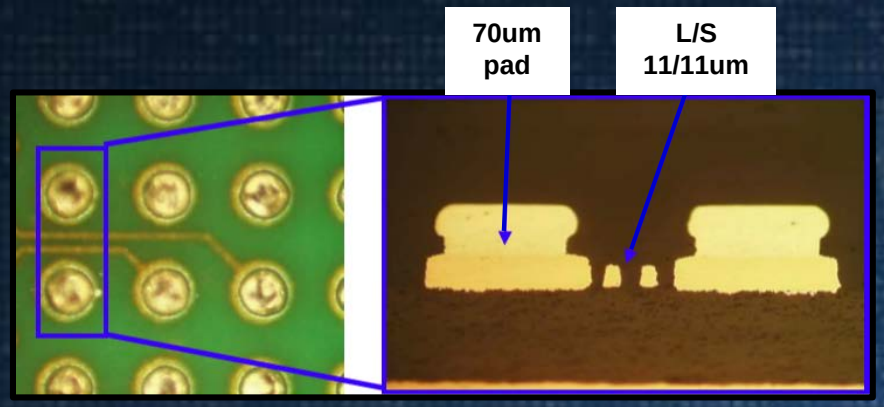
DIB 2028 targets

		2018 (today)	2028 (future)
Pin density	The number of DUT sites and DUT pin count in the same or smaller area drive up the pin area density. **Challenge**: Routing out the signals to the instruments and power supplies becomes increasingly difficult.	4,000 I/O per sq in 80um C4 pitch	16,000 I/O per sq in 40 um C4 pitch
I/O Performance	Increased challenges with high speed I/O (PCIe, DDR Interfaces, mmWave) to support BW intensive end products. **Challenge**: Increasing test standards (signal integrity, eye opening) including safety to insure quality for the end applications.	32 Gbps (dig) 6 GHz (RF) 1 kVA (power)	128 Gbps (dig) +100 GHz (RF) 10 kVA (power)
Power Performance	Device Supplies < 700mV require excellent accuracy. Increasing power rails per DUT consumes high PCB layer count. **Challenge:** Increasing test standards (power impedance curve) to insure quality for the end applications.	4 power rails / layer (PCB) 20mOhm @1MHz 100mOhm @ 100 MHz	16 power rails/layer (PCB) 5mOhm @1MHz 20mOhm @ 100 MHz
Components	Application circuit complexity increases component count per DUT site. **Challenge:** Use of smaller foot print components make diagnosing and repairing defects increasingly difficult to detect and time consuming	70 comp per sq in (0201 body size) 1st time BIN1: 50%	200 comp per sq in (sub-01005 body size) 1st time BIN1: +95%
Execution	Delivery of the device interface from pin-out freeze to wafer out for first probe contact with full performance **Challenge:** Increasing DI complexity increases risk of design or mfg defects. Complex mfg processes take longer.	75% OTD 6 week leadtime	95% OTD 3 week leadtime

Must achieve these targets in combination to best optimize:

- COT reduction
- TTM & TTV
- Test quality

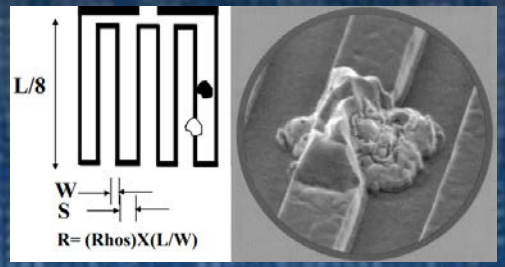
Device Interface at Sub-micron Scale



- Fine pitch DUT area routing escape is an enabler to increase I/O density
- Smaller line / space enables more than one signal to escape on a single layer requiring fewer toal layers
- As pin pitch decreases the L/S becomes smaller, requiring sub-micron scale process capability and control

Defect Density

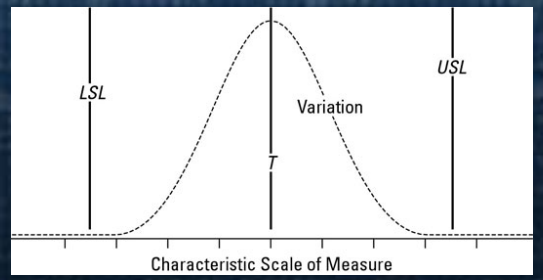
Size and frequency of a random defect that can cause a short / open



- Cleanliness is a function of all critical inputs: people, process, tools.
  - Requires a wholistic yield management system.
- Characterization & testing is required to set process targets and drive continuous improvement
  - DIB TTM & quality standards don't allow experimentation on a live project
- To achieve a viable yield
  - < 0.1 defects / DIB @ 400x400mm
  - A 10um process requires Class 100

Process Capability

The ability of a process to produce output within specification limits



- For a 11/11um L/S feature, to maintain impedance control:
  - +/- 5% = +/- 2.5um
  - To meet a Cpk of 1.67 requires measured std deviation of ***0.5um!***
- L/S control is the outcome of process capability of photo & etch
  - Since the processes are sequential the individual process capability must be even better!

“Sub-micron scale” Device Interface Era

Emerging paradigm: “It is a system problem at the test cell level”

- **Engineer the full path taking into account everything from Instrument to DUT contact**
- **Sustainable pin scaling curve: “2 x 4 scaling” – 2x pins, 2x performance every 4 years**

This paradigm will require a significant change in how designers and suppliers approach the problems:

- **Sub-micron scale resolutions & accuracy enabled by semiconductor class capabilities and processes**
- **Collaboration among industry specialists: ATE, Probe / Handler equipment, manufacturing, socket / probe head, etc.**
- **Major upgrades in engineering skill, discipline, and investment**

People	Process	Tools
• Management • Design: architecture, PI & SI • Process engineering • Quality engineering • Line operators	• Design: concurrency • Materials characterization • Process characterization • Quality management • Business & Operations	• Design: layout, sim, mechanical • Automated process control • Yield/Defect management • Inspection & Diagnostics • Risk management & mitigation