SW Test Workshop

Semiconductor Wafer Test Workshop

Probing solutions and inherent customization to enable advanced copper-based 3D integration schemes

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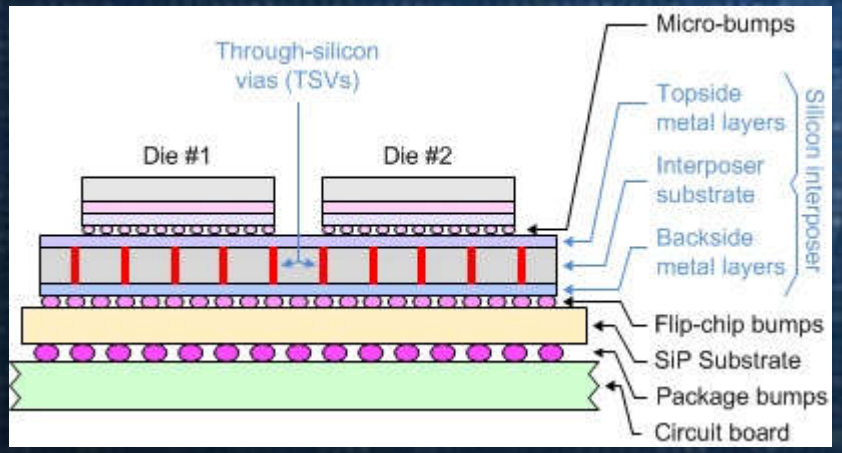
Overview

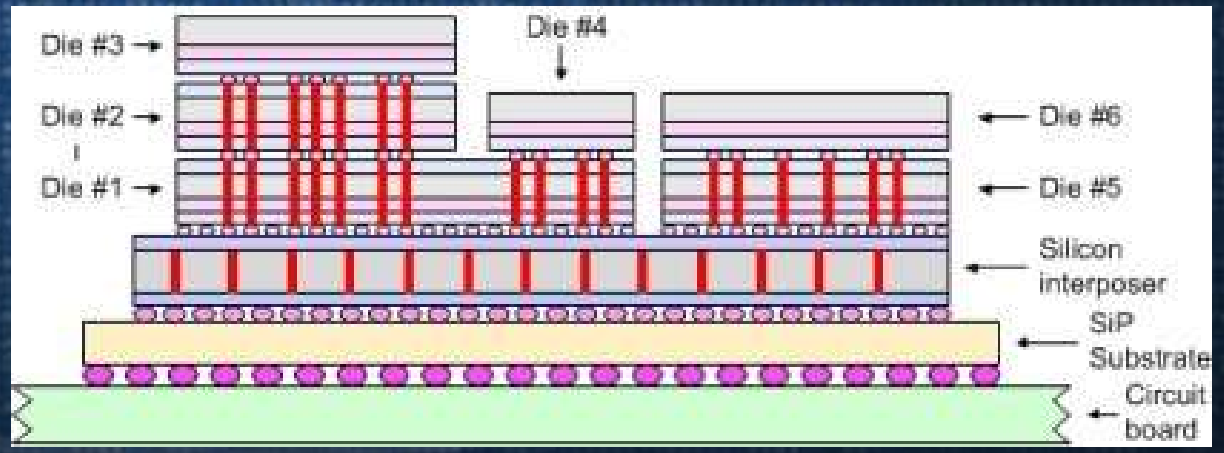
- **Background: Cu probing & Fan-Out Panel-Level Packaging (FOPLP) trends**
- **Probing technology path finding and know-how acquisition on Cu-based applications**
  1) Cu probing: early studies
  2) Processors probing
     - Customer A case study
     - Customer B case study
  3) Wide I/O memories probing
     - IMEC case study
- **Moving to FOPLP, RDL Cu pad probing: SEC case study**
  1) Technology customization
  2) Results of qualification at Customer
- **Lessons learned and future work**

Cu probing trend

- **A general trend can be identified in EWS towards Cu probing**
- **This is one of the key ingredients to allow semiconductor manufacturers to exploit 3D packing architectures with high interconnection density**
  - Main drivers are recent mobile processors and high performance memories



2.5D IC / System in Package using a Si interposer and through-silicon vias (TSVs)



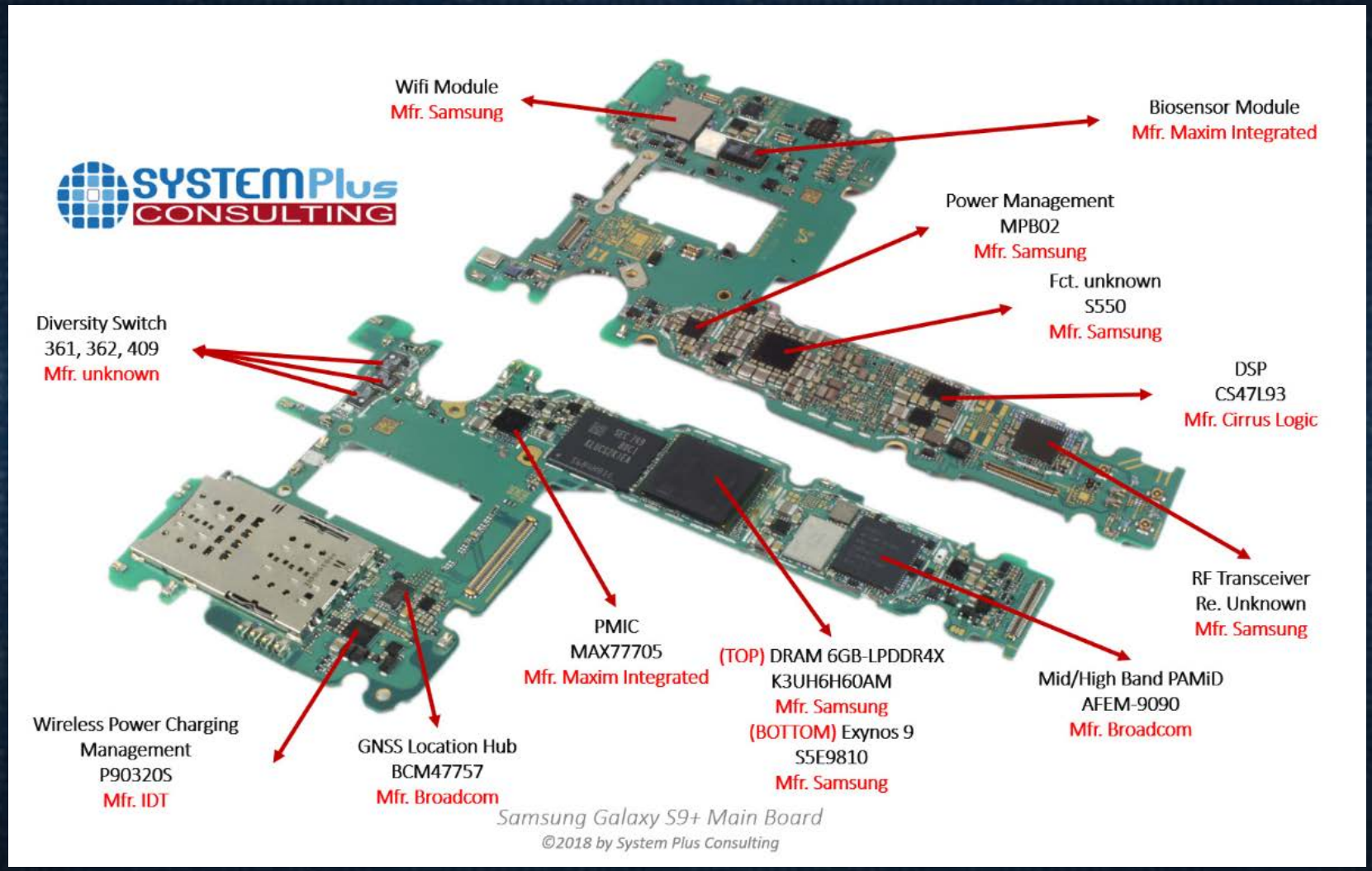
3D IC / System in Package example:
Memory dies stacked and attached to logic die and/or analog/RF die attached to a digital logic die, …

Ref. [1]

3D IC benefits versus 2D IC

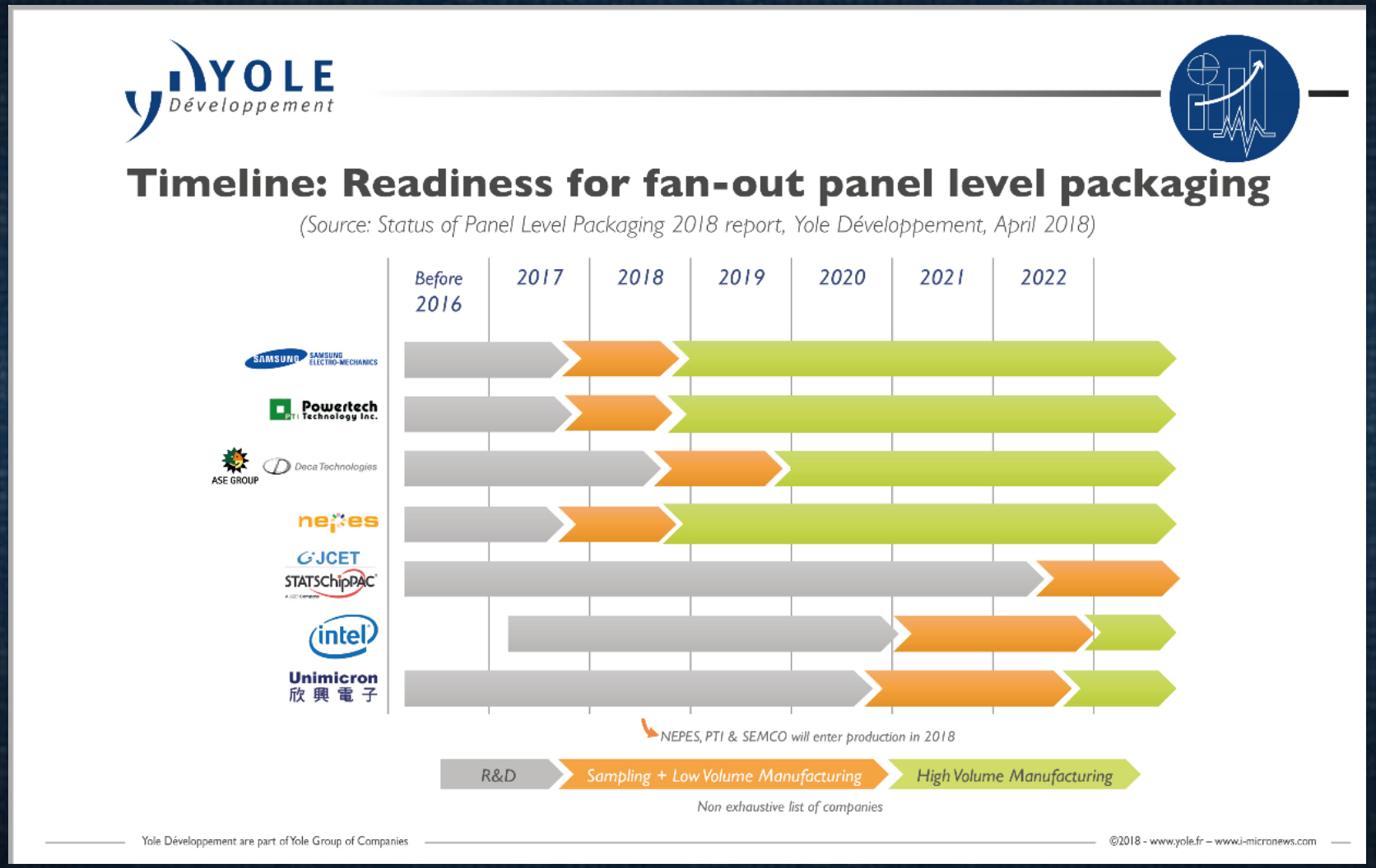
- **Smaller footprint**
  - More functionalities into a small space
- **Shorter interconnect length**
  - Decrease power consumption and power budget
  - Increase bandwidth = high bandwidth memories, parallel access
- **Design freedom**
  - Higher order of connectivity vs. 2D architecture
  - Heterogeneous components can be integrated
- **Cost improvements**
  - Partitioning of large chips into smaller dies for improved yield and testability

Packaging trend in mobile applications



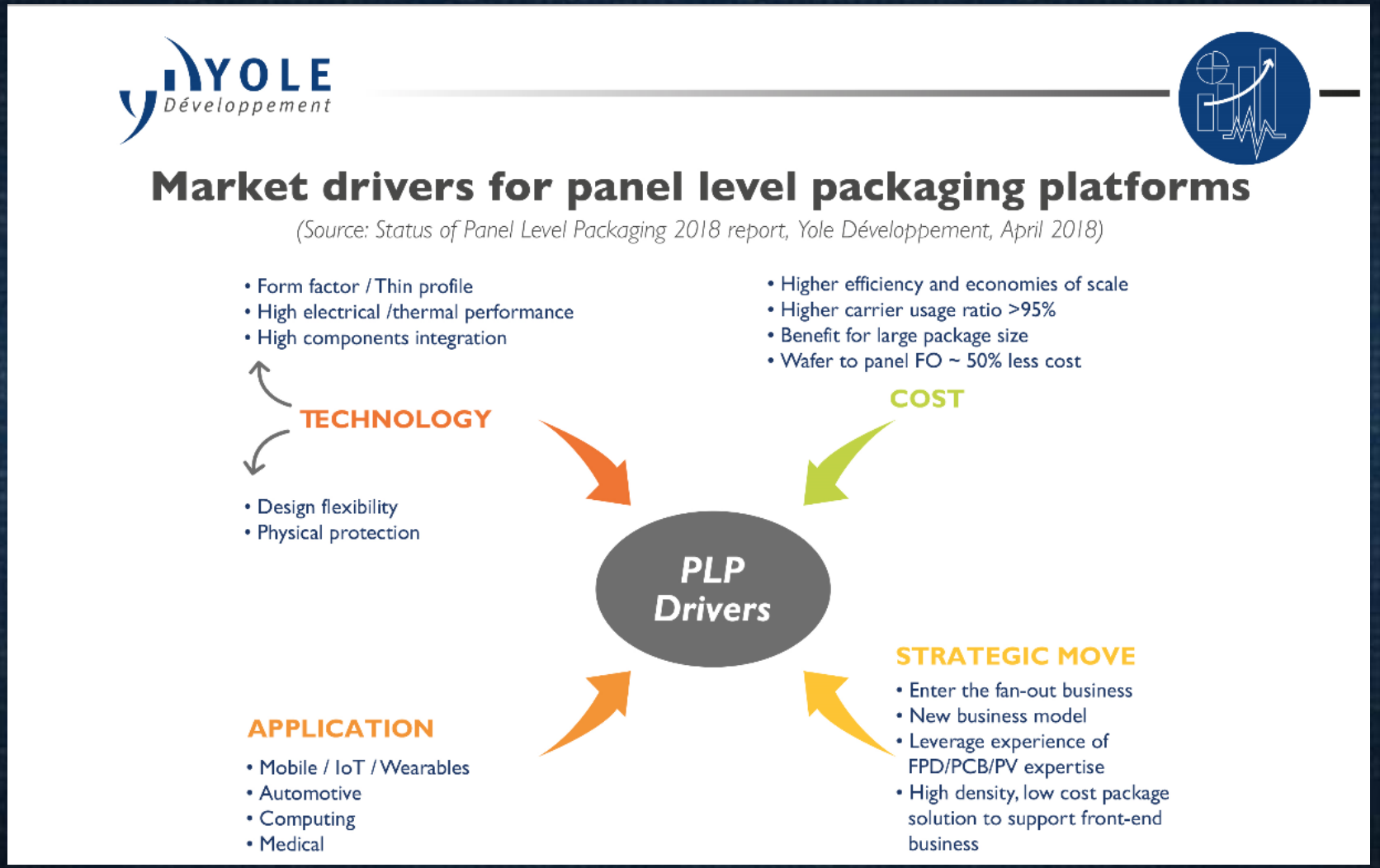
Ref. [2]

Readiness for fan-out panel level packaging



Ref. [3]

Panel level packaging technology drivers

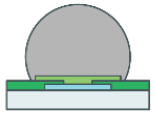
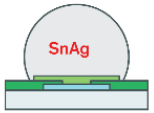
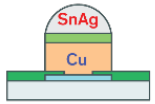
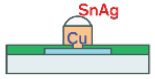


Ref. [3]

Cu-based interconnects

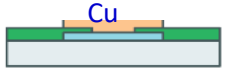
- Reducing solder amounts (finally to zero), Cu-based bumped interconnects gain lower pitch capability and higher current carrying capability
- Cu pad is an interesting option for RDL layer testing

Bumping technology generations:

	SnPb C4 Bump	Pb-Free C4 Bump	Cu Pillar + Pb-free Cap	Cu µ-Pillar + Pb-free Cap
Structure				
Diameter	75 – 200 µm	75 – 150 µm	50 – 100 µm	10 – 30 µm

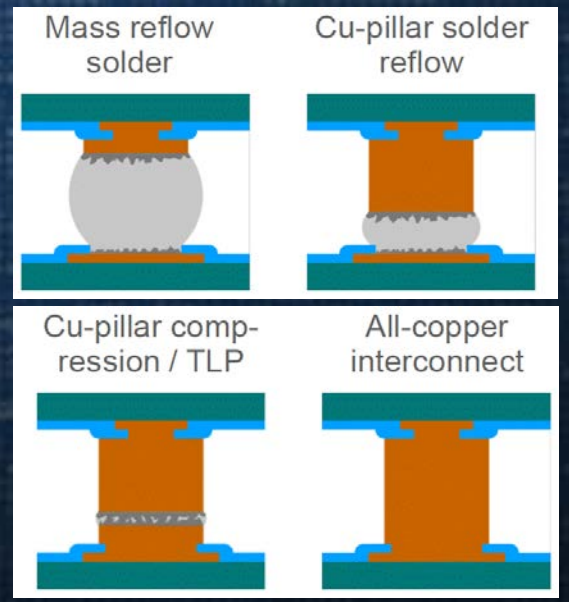
Old Technology → Current Technology → Next-Generation Technology

Pad option:

Cu Pad

50 – 100 µm

Ref. [4]

Roadmap from solder to all-copper interconnects:



Ref. [5]

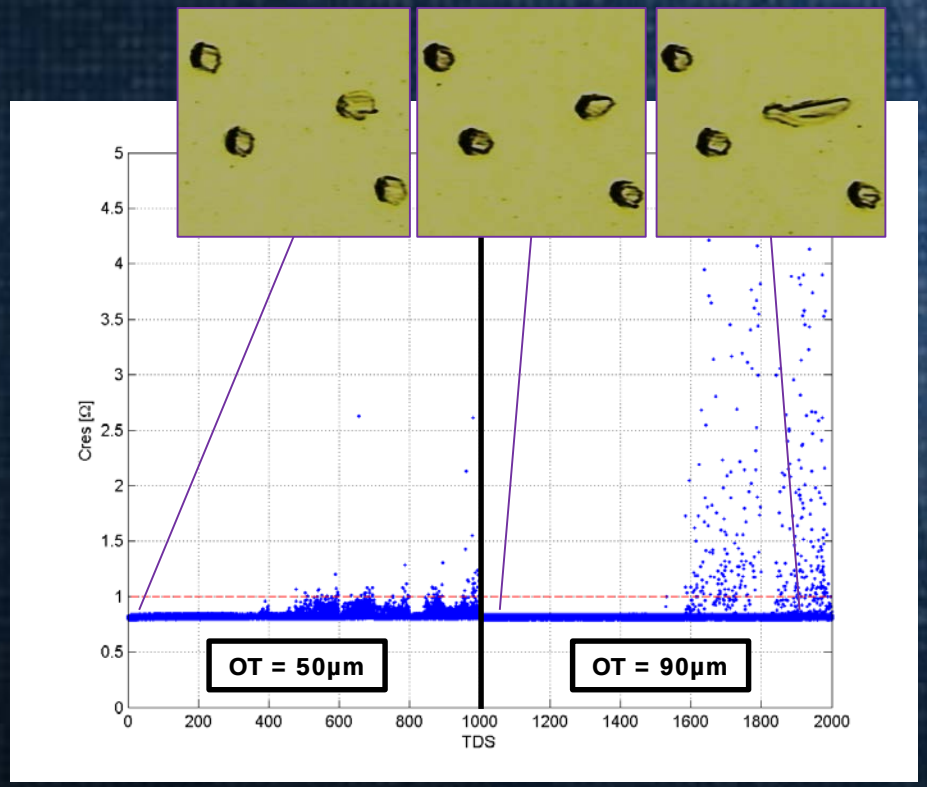
Probing technology requirements

- **Processors probing requires…**
  - High current carrying capability
  - Probing at both RT and Hot
  - Minimum pitch is not critical (≥ 90 µm FA)

- **Wide I/O memories probing requires…**
  - Ultra fine pitch (≤ 50 µm FA)
  - Current carrying capability is not critical

Early studies

- From the beginning, explorative studies on Cu blank wafers showed the importance of tip material and scrub control to guarantee contact stability

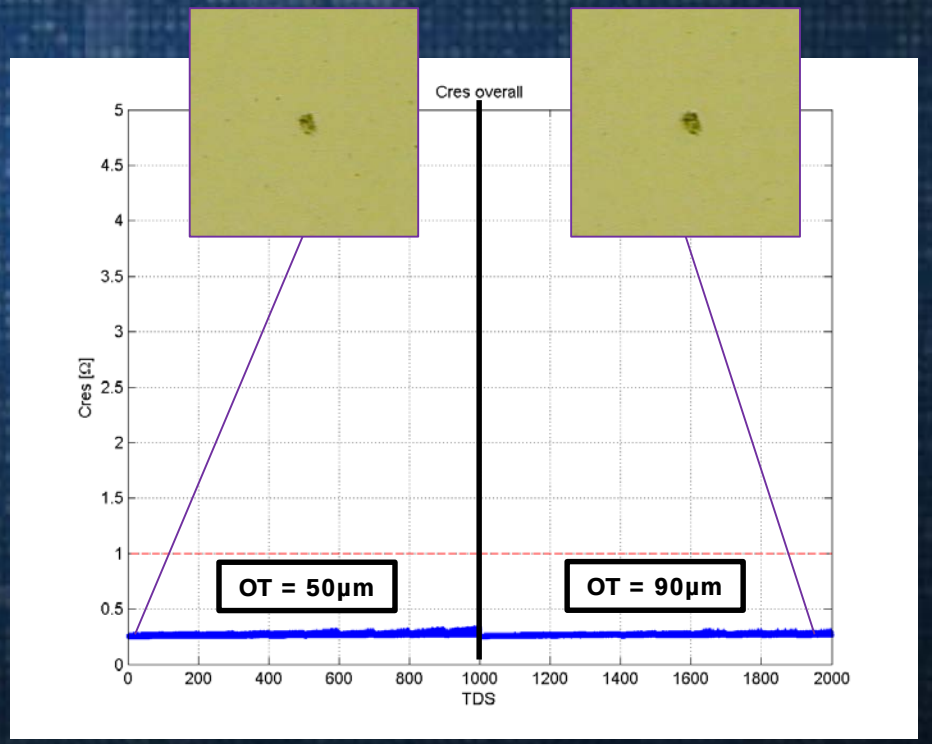


TPEG™
T3 LCR2

Standard mechanics

Pointed tip
LCR2 alloy

Cleaning Frequency = 100



Arianna™
A3 HC

Improved mechanics

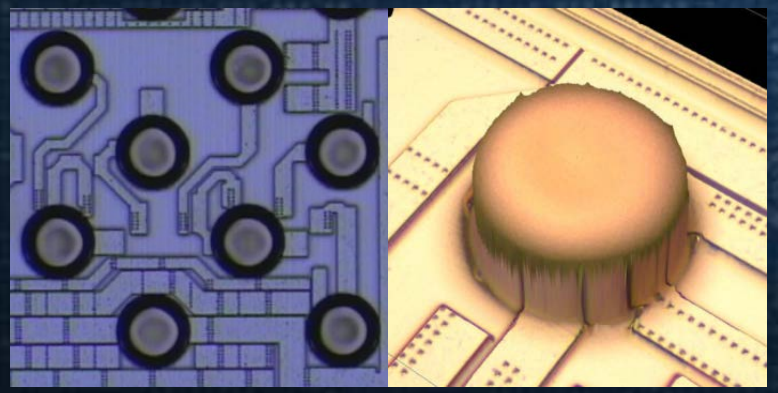
Pointed tip
Customized alloy

Cleaning Frequency = 100

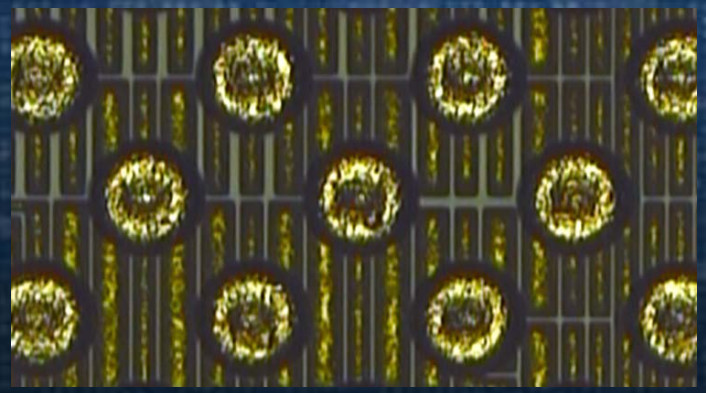
Early studies

- **Looking at Cu surface:**
  - Surface morphology and metallurgy differ largely from Customer to Customer, requiring dedicated customization studies
  - Cu surface (pads, pillars) are more prone to oxidation – or at least the oxide layer is impacting more contact resistance – than Al surface (pads)

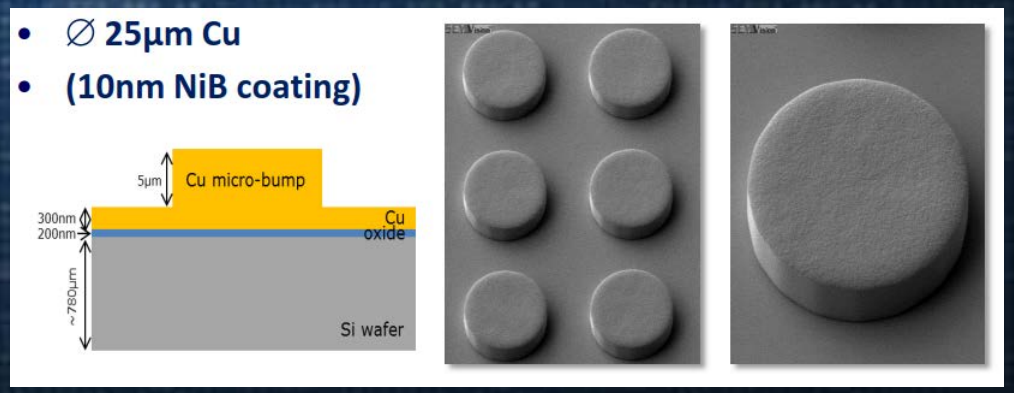
Customer A



Customer B



Customer IMEC (see paper)



Refs. [6,7]

Processor probing

- **Technology development through**
  - Probing technology path finding
  - Customer A case study
  - Customer B case study

Processor probing

Probing technology development

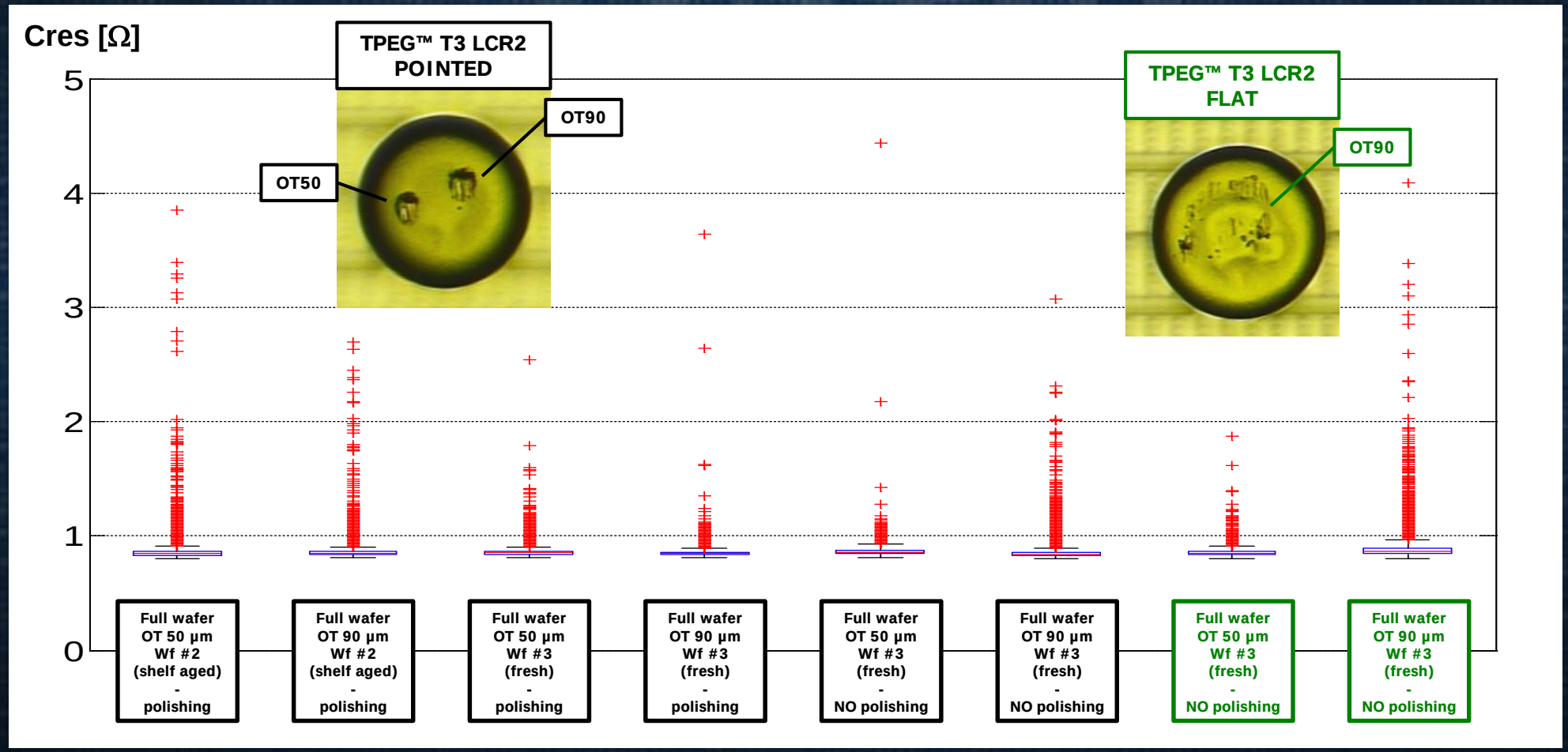
- **TP reference technology is TPEG™ T3 LCR2**
- **Arianna™ A3 HC & Arianna™ AS90 HC are proposed for this application to**
  - Improve contact resistance stability
  - Improve current carrying capability

PARAMETER	TPEG™ T3 LCR2	Arianna™ A3 HC	Arianna™ AS90 HC
Needle diameter	2 mils equivalent	2 mils equivalent	2.4 mils equivalent
X/Y Alignment	±10 µm	±10 µm	±10 µm
Z planarity	Δ 20 µm	Δ 20 µm	Δ 20 µm
Min pitch FA	90 µm	90 µm	90 µm
CCC	500mA	1200 mA	1500 mA

Processor probing

Customer A case study

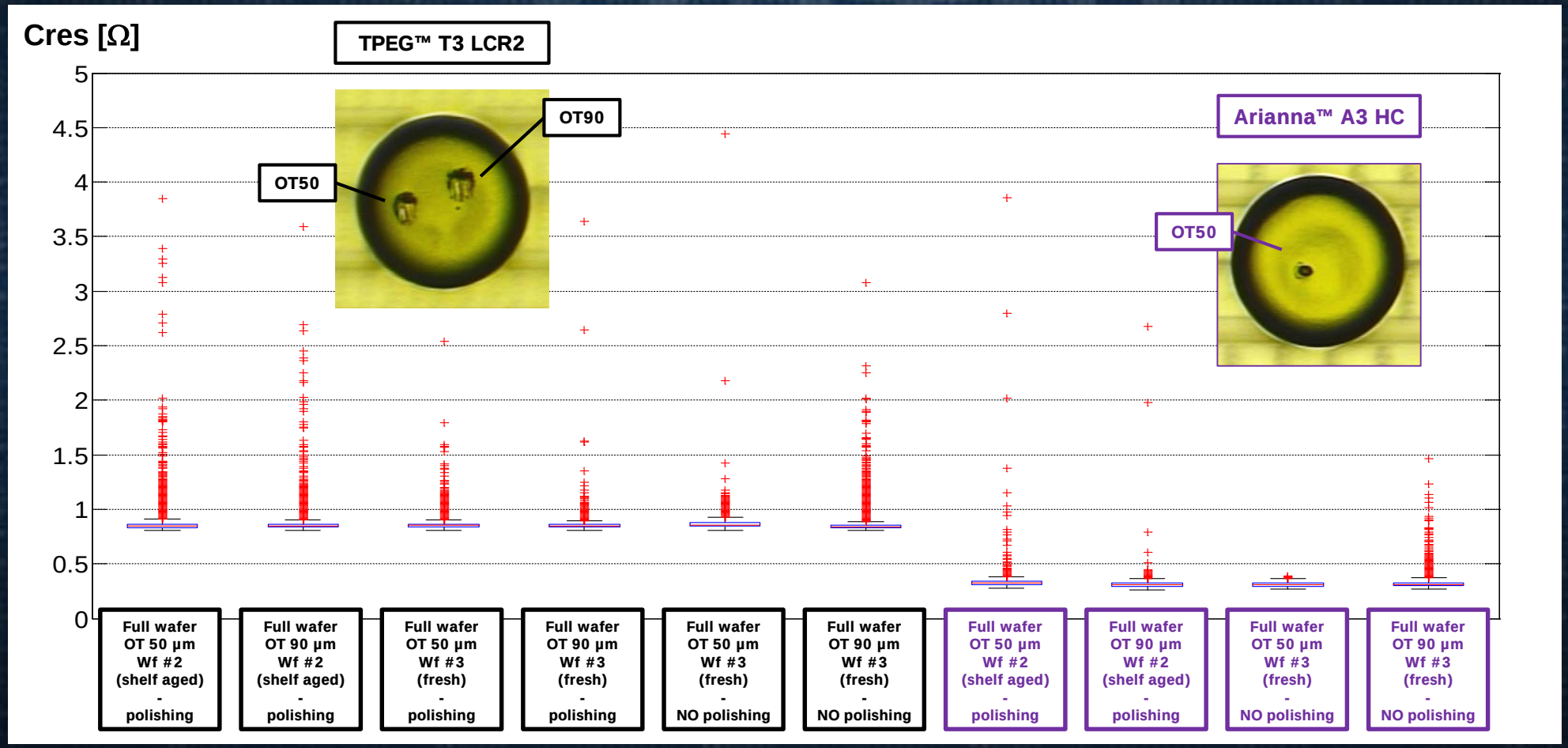
- **TPEG™ T3 LCR2: comparing pointed vs flat tip**



Processor probing

Customer A case study

- **Moving to Customized Tip solution: TPEG™ T3 LCR2 vs Arianna™ A3 HC**



Processor probing

Customer B case study – 1st run

- **Customer required to emulate Cu bump wafer testing as follow:**
  - 3x full wafers with polishing frequency 100, OD = 75µm electrical
  - 4x full wafers no polishing (tot. 1800 PTDs), OD = 75µm electrical
  - Success criterion: maximum Cres Probe Std Dev < 250 mΩ

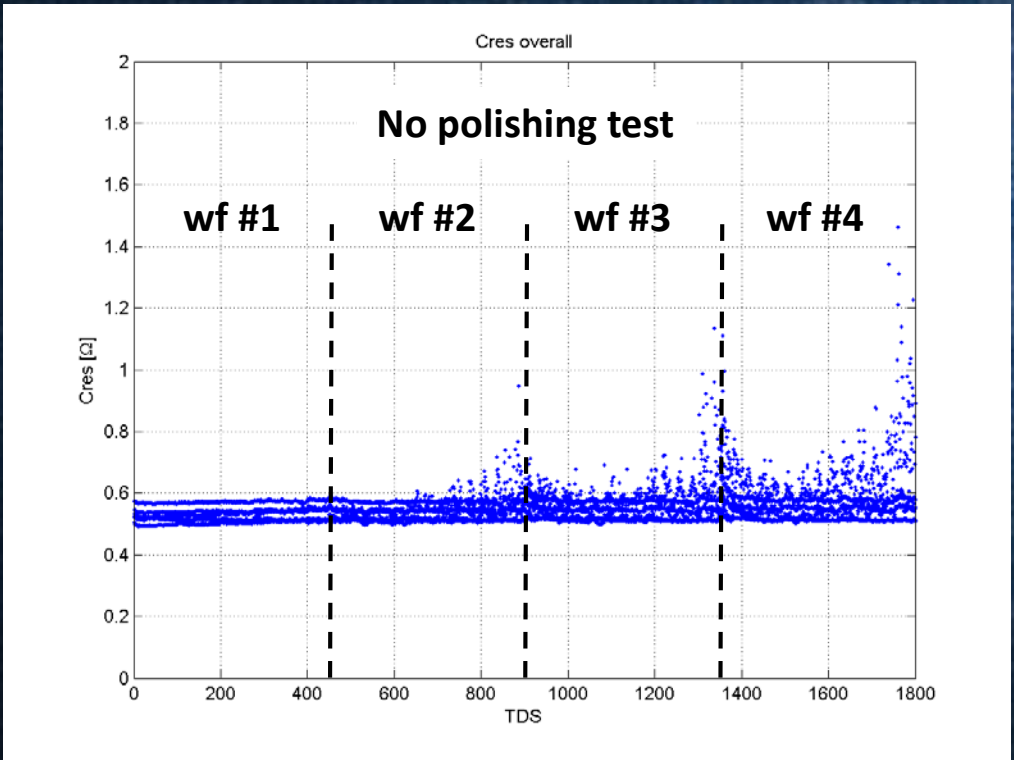
Technology	Tip Option	Scrub Option	Probe count	Max Probe SD polishing	Max Probe SD NO polishing
TPEG™ T3 LCR2	Pointed	Controlled	48	13 mΩ	13 mΩ
TPEG™ T3 LCR2	Flat	Controlled	48	4 mΩ	19 mΩ
Arianna™ A3 HC	Customized	Controlled	48	8 mΩ	6 mΩ
Arianna™ A3 HC	Customized	Standard	48	20 mΩ	87 mΩ

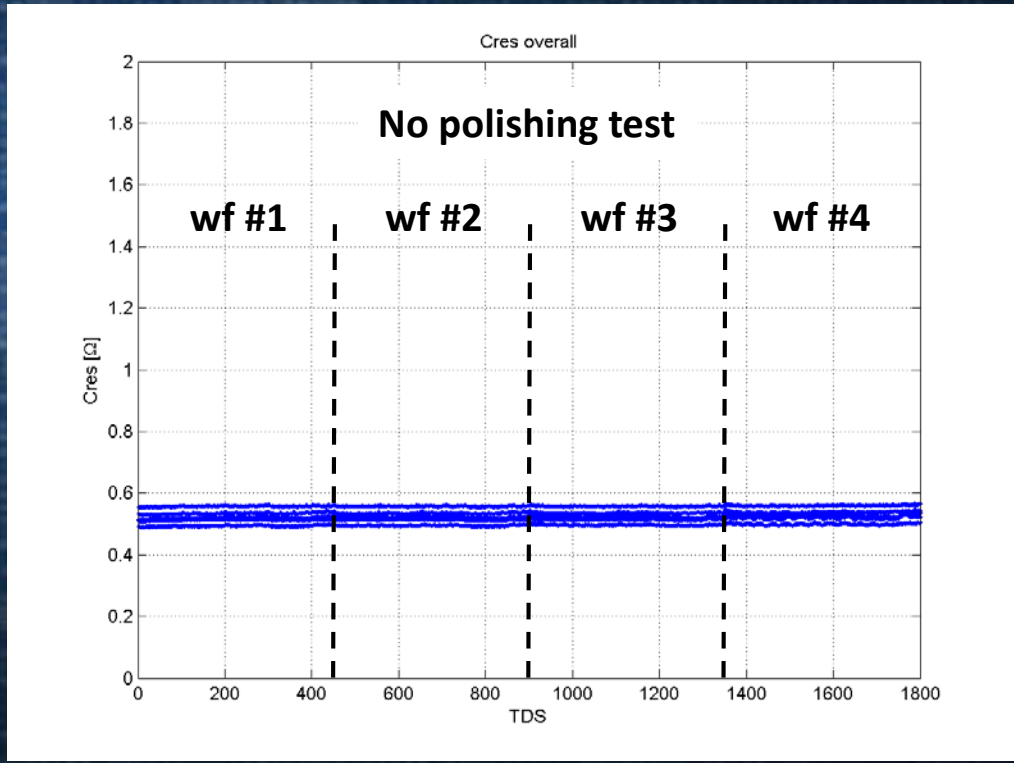
- **Stable electrical contact stability is found for all technologies**
  - Superior performances are confirmed for TP Customized Tip solution with controlled scrub
  - Controlled scrub mechanics is providing a measurable advantage

Processor probing

Customer B case study – 1st run

- **Arianna™ A3 HC, standard scrub**
  - Max Probe SD = 87 mΩ
  - Slight, progressive contact instability
- **Arianna™ A3 HC, controlled scrub**
  - Max Probe SD = 6 mΩ
  - Contact stability maintained



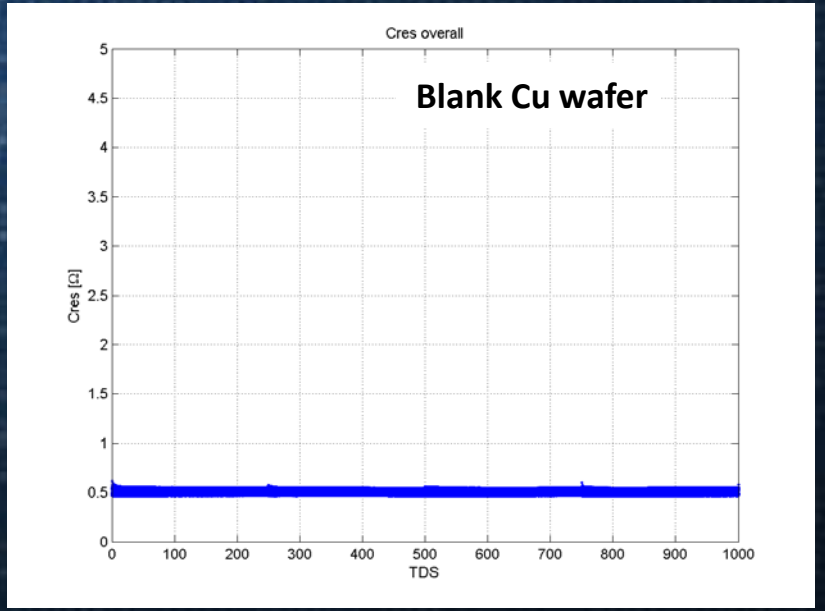


Processor probing

Customer B case study – 2nd run

- **Based on positive results with Arianna™ A3 HC technology, the Customer required to**
  - Further improve current carrying capability
  - Assess stability of electrical performances over entire life span → new evaluation procedure
  - Improve HF performances

- **Technoprobe proposed to move to Arianna™ AS90 HC**
  - Customized tip evaluated on Cu blank, showing high Cres stability
    - Cres ~ 0.5 Ω (including interconnection)
    - Maximum Cres Probe Std Dev = 5 mΩ
    - Total standard deviation (on 48 probes) = 27 mΩ
  - Dedicated tip designs to probe on Customer wafer are developed: Geometry 1 & Geometry 2

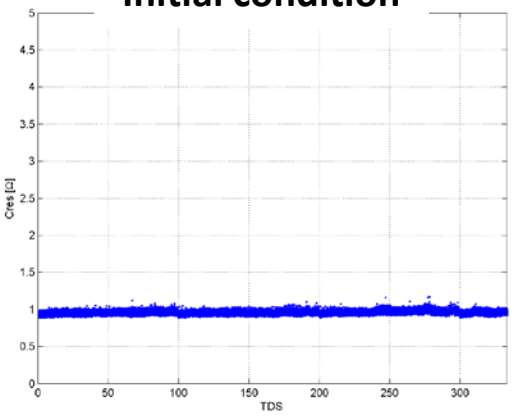
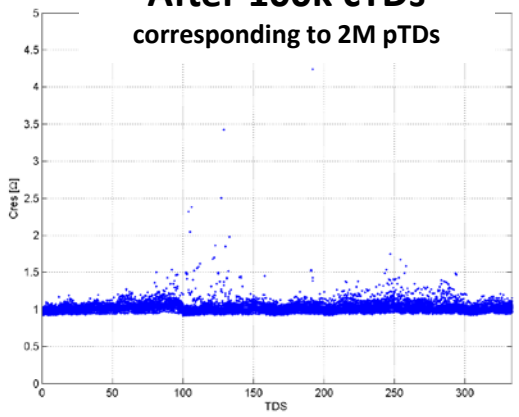
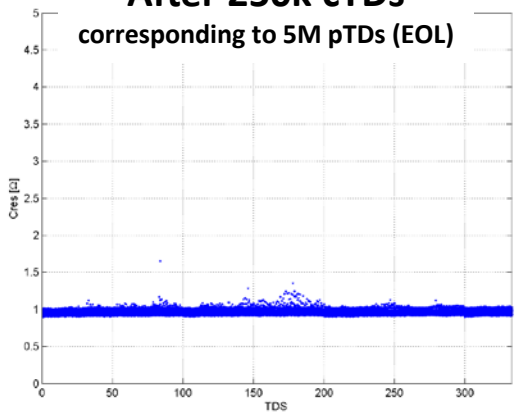
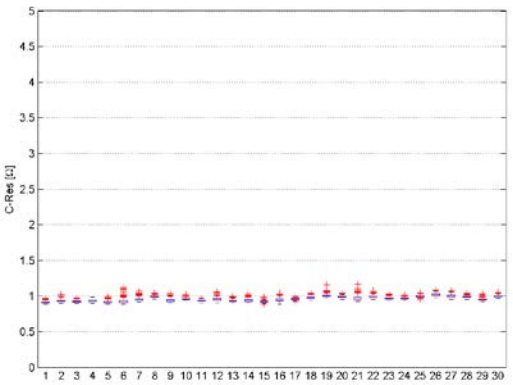
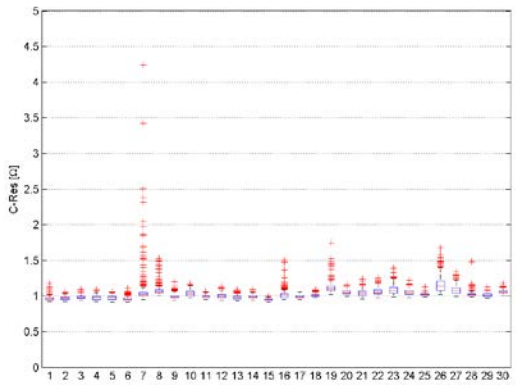
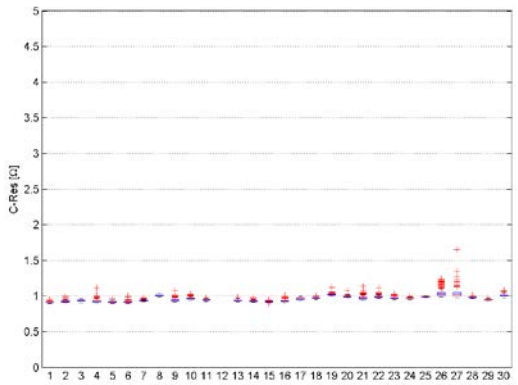


Overall Cres (1000 TDs, cleaning freq 100)

Processor probing

Customer B case study – 2nd run

- **Arianna™ AS90 HC with Geometry 1 – cleaning ageing test**

	Initial condition	After 100k cTDs corresponding to 2M pTDs	After 250k cTDs corresponding to 5M pTDs (EOL)
Overall Cres (full wafer, cln freq 100)			
Single channel Cres boxplot (full wafer, cln freq 100)			

Processor probing

Customer B case study – 2nd run

- **Arianna™ AS90 HC with Geometry 2 – cleaning ageing test**

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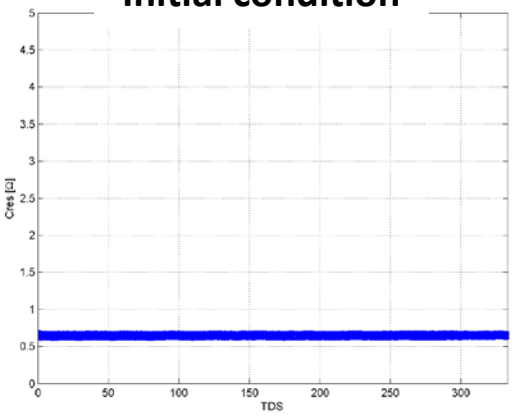
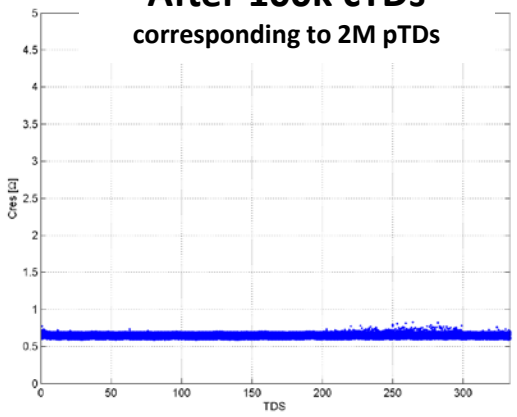
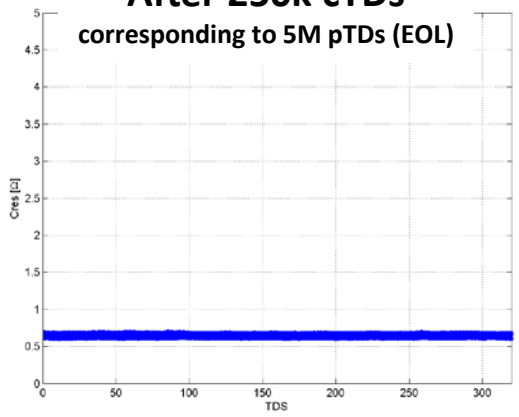
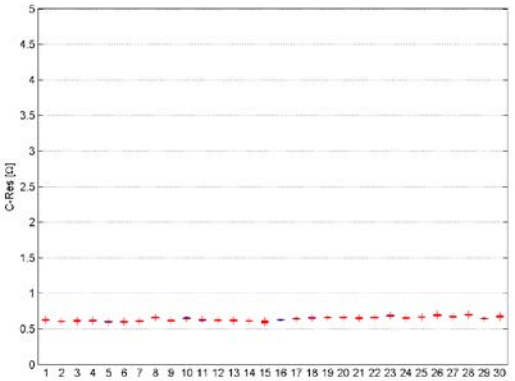
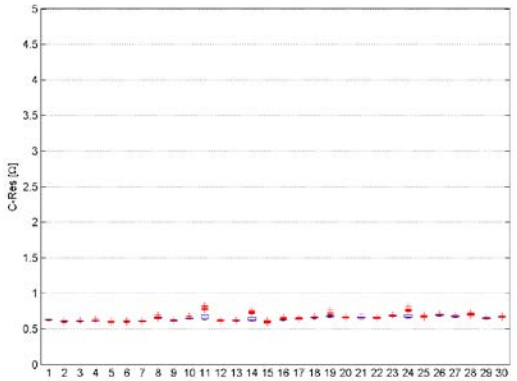
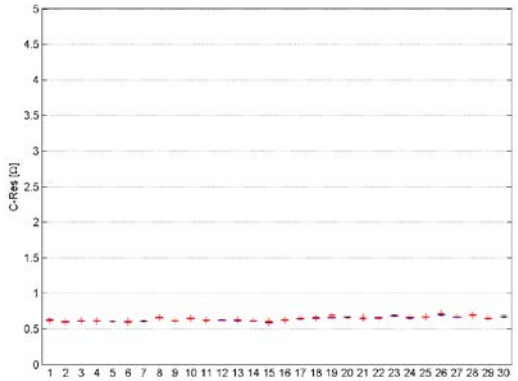
Overall Cres (full wafer, cln freq 100)			
Single channel Cres boxplot (full wafer, cln freq 100)			

Wide I/O memories probing

- **Technology development through**
  - Probing technology path finding
  - IMEC case study (ref.[8] dedicated paper at SWTW 2018 presented by IMEC "Leading-Edge Wide-I/O2 Memory Probing Challenges: TPEG™ MEMS Solution")

Wide I/O memories probing

Probing technology path finding

- **TSV/µ-bump memory dies probing needs ultra-fine pitch FA technologies**
  - TP first solution to address 40µm FA is dated 2010 to provide an engineering level solution (FT 1.0, mechanical manufacturing)
  - As further step, TP applied TPEG™ MEMS concept also to ultra-fine pitch

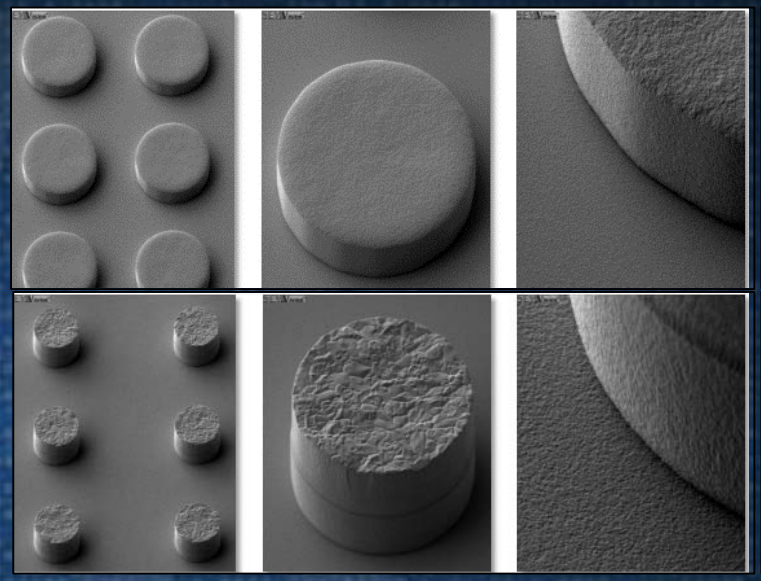
- **TPEG™ MEMS Tx0 probe family was developed**
  - Target application is 60-50-40µm FA probing over Al pads or µ-bumps

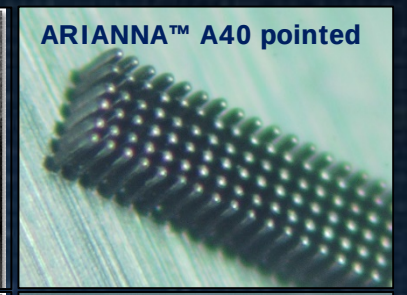
- **Now the respective Arianna™ Ax0 solutions are being introduced**
  - Target application is 60-50-40µm FA probing over Cu pads or µ-pillars

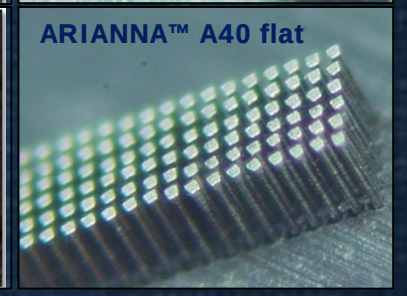
Wide I/O memories probing

Customer IMEC case study

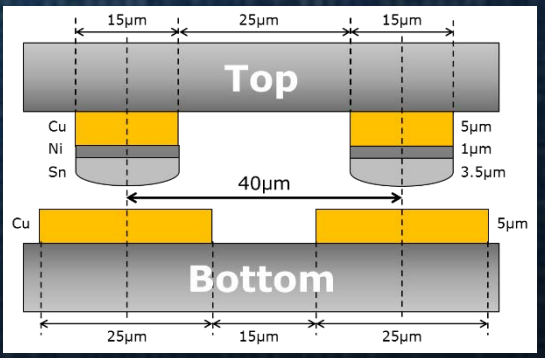
- **IMEC Blanket Micro-Bump wafer**
  - JEDEC Wide I/O 2 (JESD-229/2)
  - Top side: Cu/Ni/Sn ∅ = 15µm
  - Bottom side: Cu (+NiB) ∅ = 25µm
  - Micro-bumps shorted by blanket Cu







- **TP probe card**
  - 73 x 6 probes at 40µm pitch FA
  - Micro-wired space transformer
  - Arianna™ A40 flat probe head for Top side
  - Arianna™ A40 pointed probe head for Bottom side



See Refs. [6,7,9] for details.

SEC case study

Moving to FOPLP, RDL Cu pad probing

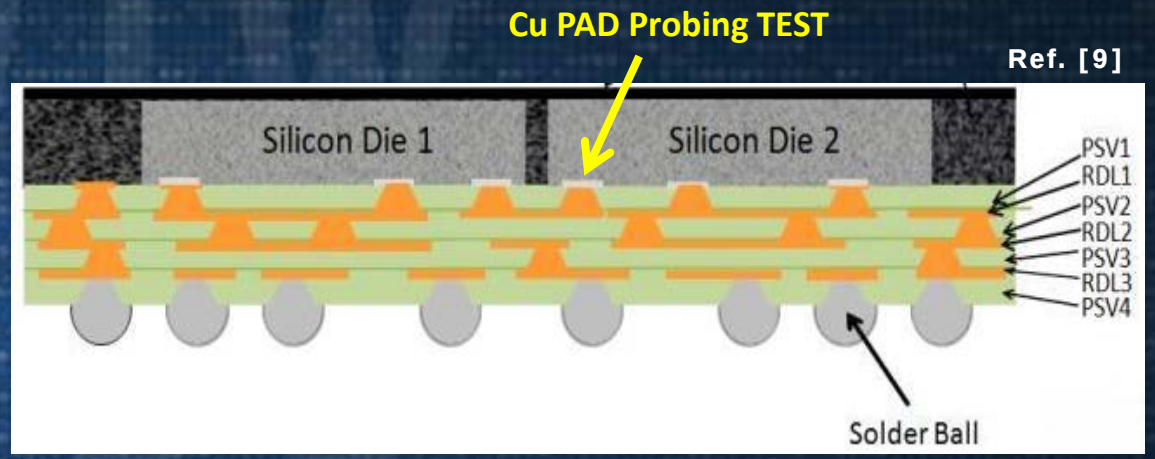
- **All path finding and know-how acquisition efforts allowed Technoprobe to conceive a solution to cope with requirements of FOPLP, Cu pad probing**

- **Specific SEC challenges and requirements drove us to develop a probing technology capable of:**
  - Small pad opening
  - Thin Cu metallization layer
  - Possible irregular pad topography

SEC case study

Technoprobe Technology customization

- **Requirement from SEC is to probe on Cu pads on RDL**
- **Main targets for evaluation:**
  - Same or better electrical contact performances vs. Al pad reference
  - Minimal pad damage to allow safe multiple testing (RT, Cold, Hot)

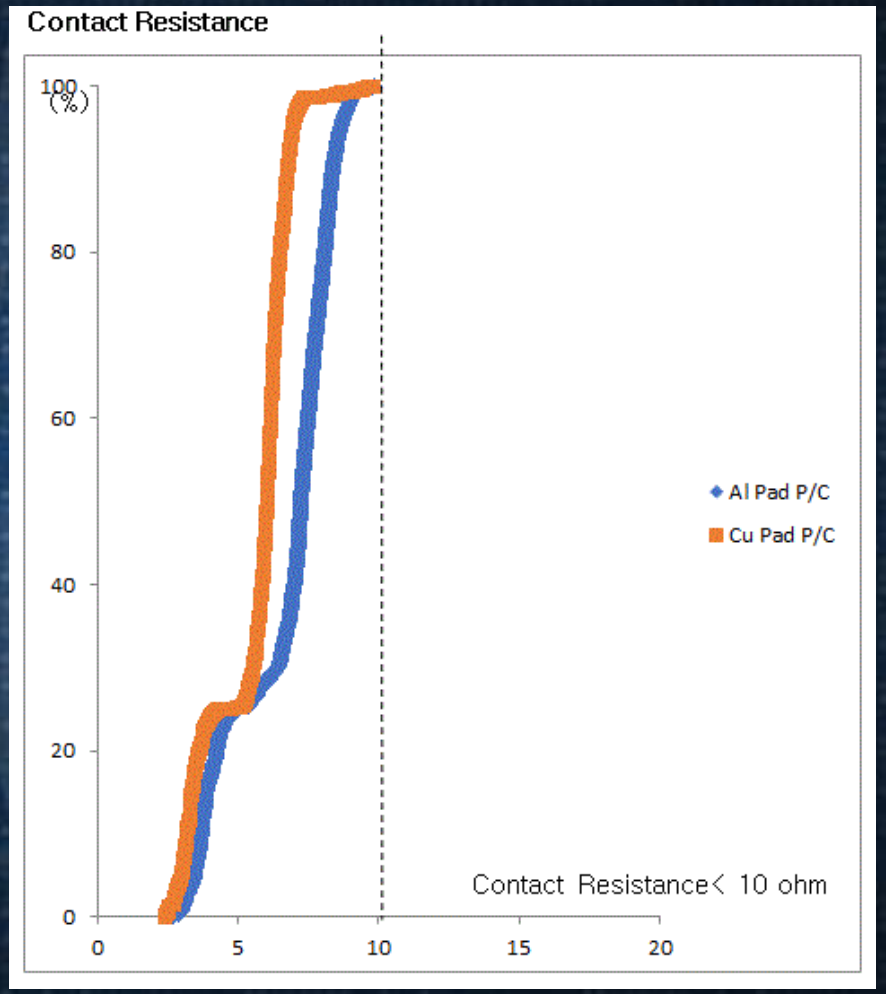


- **Arianna™ AS90 technology with further customized tip geometry and material is selected**
  - Tip Geometry 3 is selected
  - A novel alloy “Type 2” is specifically developed for this application

SEC case study

Results of qualification at Customer

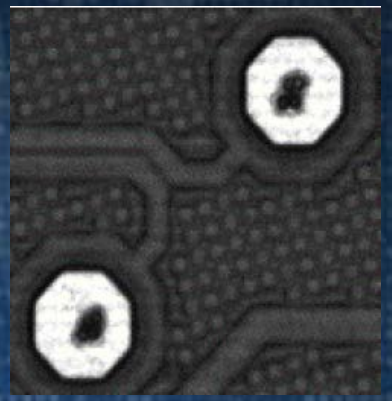
- **Stable Cres is found**
  - Results reported are for full wafer trial run
- **Probing electrical performances are exceeding Al Pad benchmark in terms of**
  - LVCC Margin test
  - DC test
  - DFT(Scan) test
  - Function test
  - Analog test



SEC case study

Results of qualification at Customer

- **Cu pad damage is very limited**
  - Scrub depth is not exceeding 300 nm
  - No delamination issues found



Al pad

Cu pad

- **Based on wear out data from the field, expected lifetime with current cleaning recipe is exceeding 1M probing TDs for RT testing**

SEC case study

Results of qualification at Customer

- **Arianna™ AS90 technology has been qualified by SEC for RT & HT testing and released to mass production**
  - Stable Cres is found with requested scrub mark depth and size
  - This result is achieved by a dedicated customization of probe tip (alloy and geometry)

Lessons learned

- **Cu probing on diverse target structures (pads, pillars, µ-pillars) is gaining momentum driven by processors and high performance memories testing requirements in the evolving 3D packing architectures scenario**

- **Key ingredients implemented by Technoprobe to successfully probe on different Cu structures are**
  - Tip : customized geometry and alloys
  - Scrub control to guarantee contact stability during probing process
  - … and a joint development path between probe card vendors and customers, allowing Technoprobe to verify and further customize probing solution for unprecedented electrical and mechanical performances

Thank you for your attention!

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