SW Test Workshop

Semiconductor Wafer Test Workshop

LEADING-EDGE WIDE-I/O2 MEMORY PROBING CHALLENGES: TPEG™ MEMS SOLUTION

Ferenc Fodor

Erik Jan Marinissen

imec

Leuven, Belgium

Raffaele Vallauri

Daniele Acconcia

TECHNOPROBE

Wafer Probing Technologies

Cernusco Lombardone, Italy

June 3-6, 2018

1. INTRODUCTION
MOTIVATION

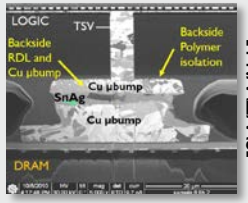
- Unique test system at imec for direct probing of fine-pitch large micro-bumps arrays
  - Advanced probe card characterization
  - Regular pre-/post-bond probing of wafers with micro-bumps
- Four-phase evaluation of Technoprobe probe cards:
  - Phase 1 : Wide-I/O2 **1bank** probe card with TPEG™ T40 tips
  - Phase 2 : Wide-I/O2 **1bank** probe card with ARIANNA™ A40 tips

  Same card
  Different probe heads
  - Phase 3 : Wide-I/O2 **4bank** probe card with TPEG™ T40 tips
  - Phase 4 : Wide-I/O2 **4bank** probe card with ARIANNA™ A40 tips

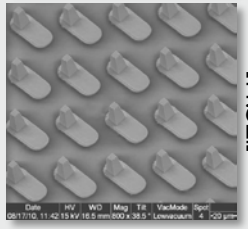
  Same card
  Different probe heads
- Completed so far: phases 1 and 2

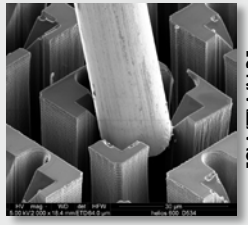
1. INTRODUCTION
RELATED PRIOR WORK

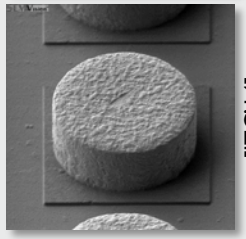
- **SWTW'11**: Marinissen et al. *(imec + Cascade Microtech)*
  - Imec and Cascade started collaboration, defined probe targets
- **ITC'11**: Smith et al. *(Cascade Microtech + imec)*
  - First collaboration results, mainly on probe technology
- **SWTW'13**: Böhm et al. *(Feinmetall + Team Nanotec + imec + FH + CM)*
  - Silicon crown tips, embedded in vertical probe card with TSVs
- **ITC'14**: Marinissen et al. *(imec + Cascade Microtech + TU Delft)*
  - WIO1-1Bank: good R_C; no impact on bond yield; cost-effective
  - But... (i) only 1 Bank and (ii) only daisy-chains of 30 micro-bumps
- **SWTW'17**: Marinissen et al. (*imec + Cascade Microtech*)
- **ITC-Asia'17**: Marinissen et al. (*imec + Cascade Microtech GmbH + FormFactor*)
  - Fully automatic test system for advanced probe card characterization



[SWTW'11]


[ITC'11]


[SWTW'13]


[ITC'14]

OUTLINE

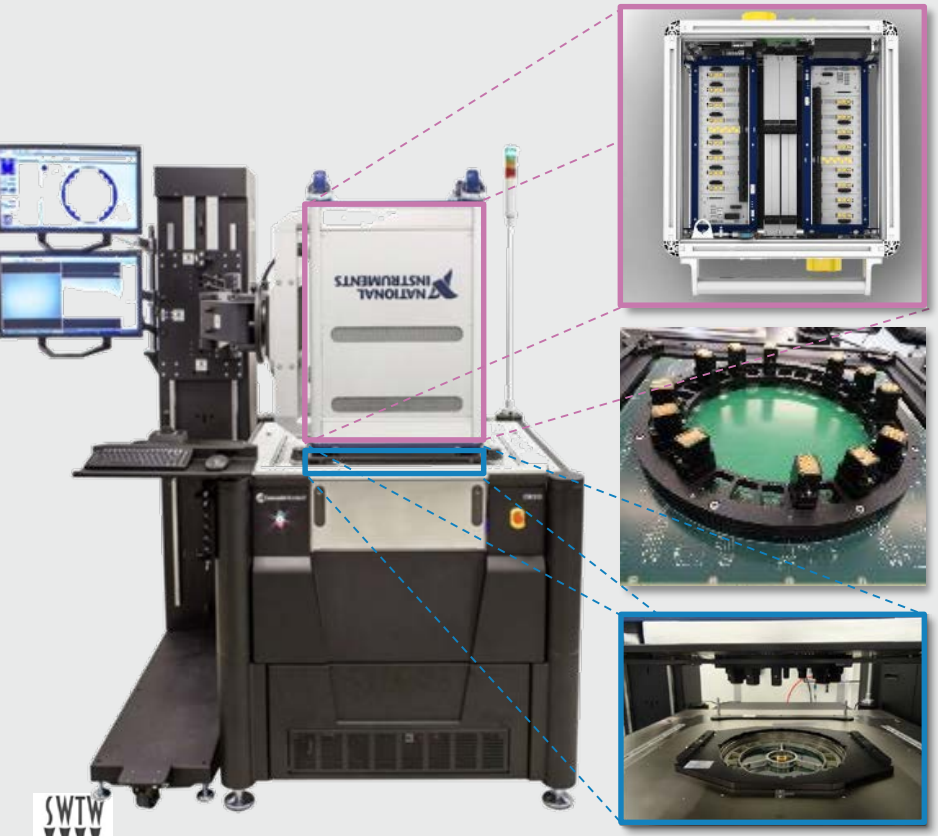
1. Introduction
2. Test Infrastructure
3. imec Test Chips with Micro-Bumps
4. Design of Experiments
5. Probing on Sn Micro-Bumps
6. Probing on Cu Micro-Bumps
7. Conclusion

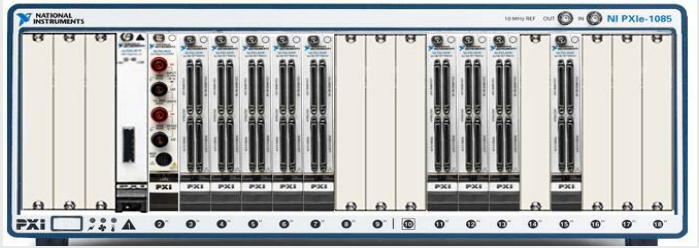
2. TEST INFRASTRUCTURE

2. TEST INFRASTRUCTURE

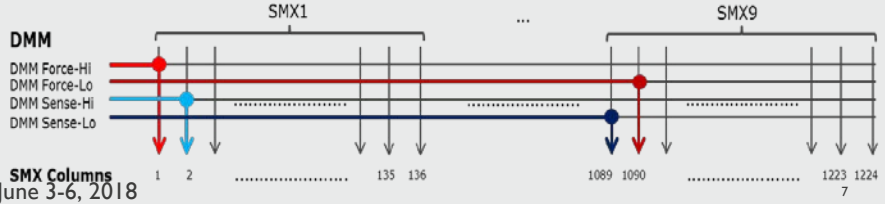
VORTEX 2.2 TEST SYSTEM FOR MICRO-BUMP PROBING

VORTEX 2.2 TEST SYSTEM FOR MICRO-BUMP PROBING

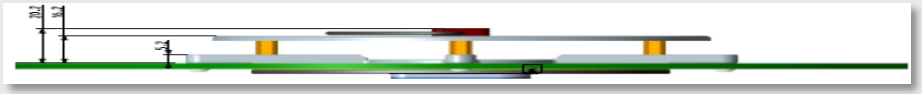




- PXI Rack: programmable Switch Matrix
  - 4 input rows driven by DMM
  - 9×136 = 1,224 output columns
- Two- and four-point *R* measurements
  - R_{max} = 1,000 Ω @100 meas/second
  - $R_{meas} > R_{max}$ ➔ 'NaN' (=open)

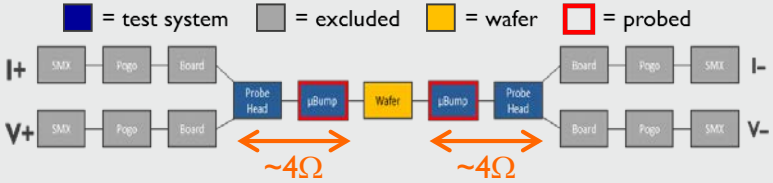


TECHNOPROBE WIDE-I/O2 MEMS PROBE CARDS



Technoprobe Specification

Parameter	TPEG™ T40	ARIANNA™ A40
Needle diameter	1 mil equiv.	1 mil equiv.
Tip shape	Flat (Sn)	Flat (Cu)
Z planarity	Δ10μm*	Δ10μm*
Minimum pitch	40μm full array	40μm full array
Force/tip (at 75μm OT)	1.2 gf/tip	1.2 gf/tip
Pin current (CCC)	250 mA	250 mA



Pseudo four-point measurements

- Two tester channels per probe tip, connected at jumper interface

3. IMEC TEST CHIPS WITH MICRO-BUMPS

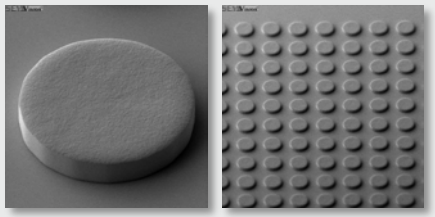
3. IMEC TEST CHIPS WITH MICRO-BUMPS
PROBE CARD CHARACTERIZATION WAFERS

Blanket Micro-Bump Wafer (BMB)

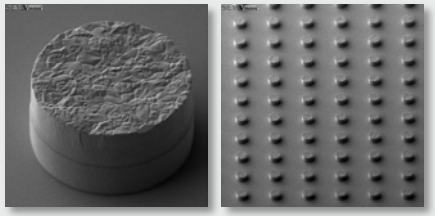
- Only micro-bumps, all shorted

Probe interface:

- Three fine-pitch micro-bump arrays
- Different metallurgies
  - Ø25µm Cu μbumps : 5µm height
  - Ø15µm Cu/Ni/Sn μbumps : 9.5µm height



Ø25µm Cu



Ø15µm Cu/Ni/Sn

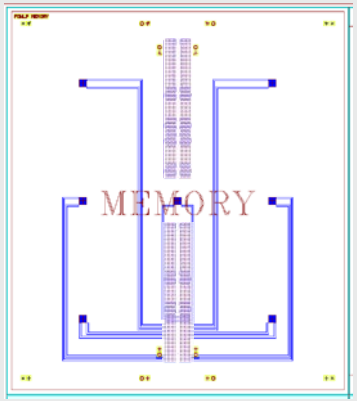
WIO2
@40/40µm
27 arrays

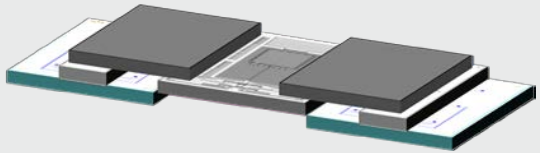
WIO1
@40/50µm
27 arrays

WIO1
@50/50µm
18 arrays

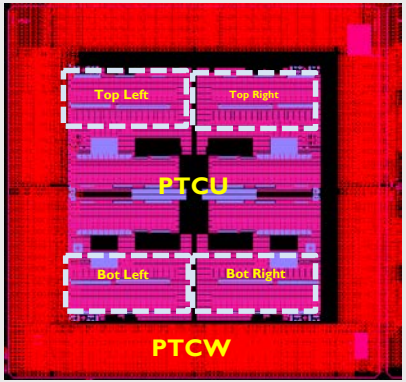
3. IMEC TEST CHIPS WITH MICRO-BUMPS
DEVICE WAFERS

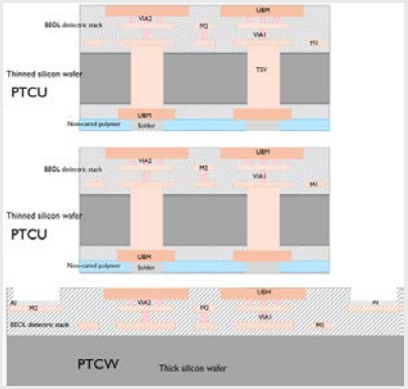
FOWLP Memory





Processing Test Chips 'U' and 'W'





Probe interface:

- WIO2-4banks with Ø15µm Sn micro-bumps
  - Micro-bump height: **9.5µm**
- Technoprobe TPEG™ T40 probe card

Probe interface:

- 4 × WIO2-1bank with Ø30µm Cu micro-bumps
  - Micro-bump height: **0µm** (embedded)
- Technoprobe ARIANNA™ A40 probe card

4. DESIGN OF EXPERIMENTS

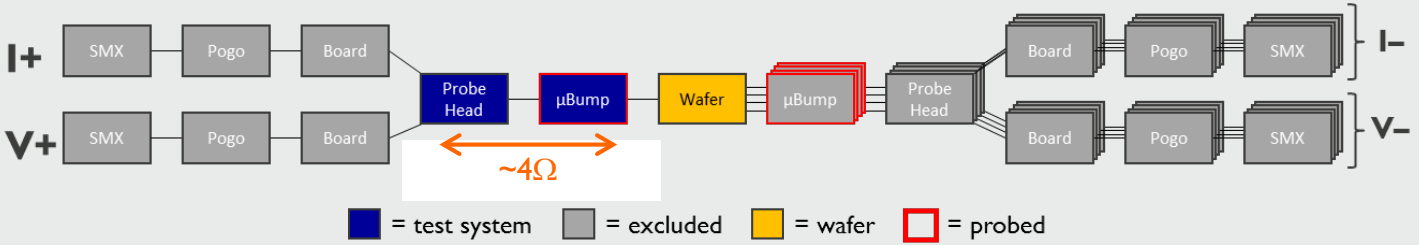
PROBE CARD QUALIFICATION TESTS (1/2)

1. Incoming Inspection on BMB

- Electrical characterization of probe card
- Probe-check measurements at varying over-travels
- Determine first-to-last and long-term suitable over-travel
  - Based on electrical measurements and probe marks

Probe-check routine

- Individually characterizes probe tips
- Measurements include up to 4Ω parasitics
- Measure one probe vs. others ganged
  - Repeat for all probes



PROBE CARD QUALIFICATION TESTS

2. Run-in of Probe Card and Probe Tip Cleaning on BMB

- Creating mileage on the probe card
- Probe-check measurements at selected over-travel
- Determine optimal cleaning interval

Recommended cleaning recipe

- Substrate : 3M / 3µm pink
- Interval : 100 – 500 touch-downs
- Over-travel : 35-50 µm

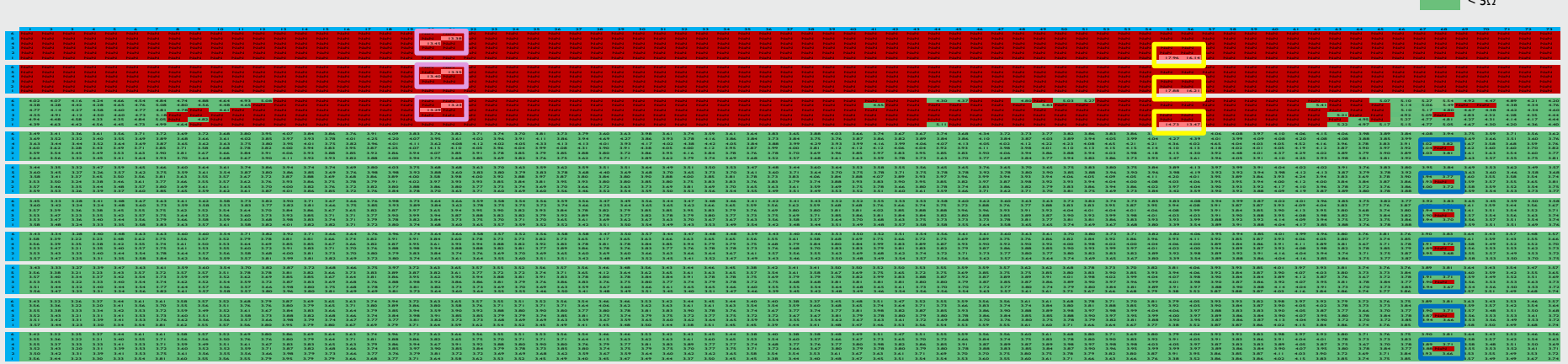
3. Device Wafer Tests

- Use probe card for pre/post-bond testing of device wafers

5. PROBING ON SN MICRO-BUMPS

5. PROBING ON SN MICRO-BUMPS

INCOMING INSPECTION



Over-travel	NaNs	Rmin	Rmax	Rmean
0	434	13.38	17.96	15.11
10	434	13.35	17.88	15.09
20	319	4.02	14.73	4.85
30	1	3.28	4.69	3.87
40	1	3.24	4.40	3.75
50	1	3.23	4.25	3.72
60	1	3.21	4.17	3.71
70	1	3.21	4.16	3.70
80	1	3.20	4.15	3.69
90	1	3.20	4.15	3.69

Identified anomalies:

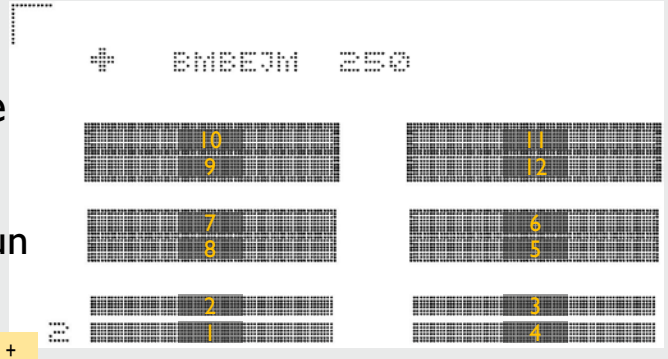
- Permanent SHORT : Probes 239-313
- Temporary SHORT : Probes 55-56
- Permanent OPEN : Probe 214

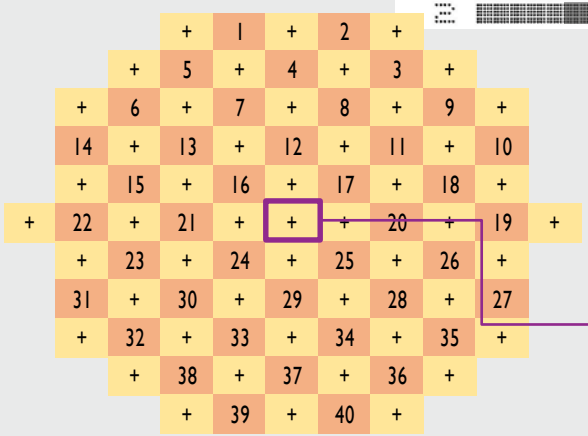
Minimum over-travel: 50µm

RUN-IN OF PROBE CARD

On BMB Wafer

- Check consistency of electrical measurements per probe
- Automatic probing on batches of dies
  - One batch: 40 dies × 12 arrays = 480 touch-downs per run
  - Probing neighboring arrays per die
  - Meandering from North to South





Legend

N — Nth probed die

\+ — Non-probed die

Training die – used for:
- Calibrating PTPA
- Incoming Inspection

Excluded from checkerboard

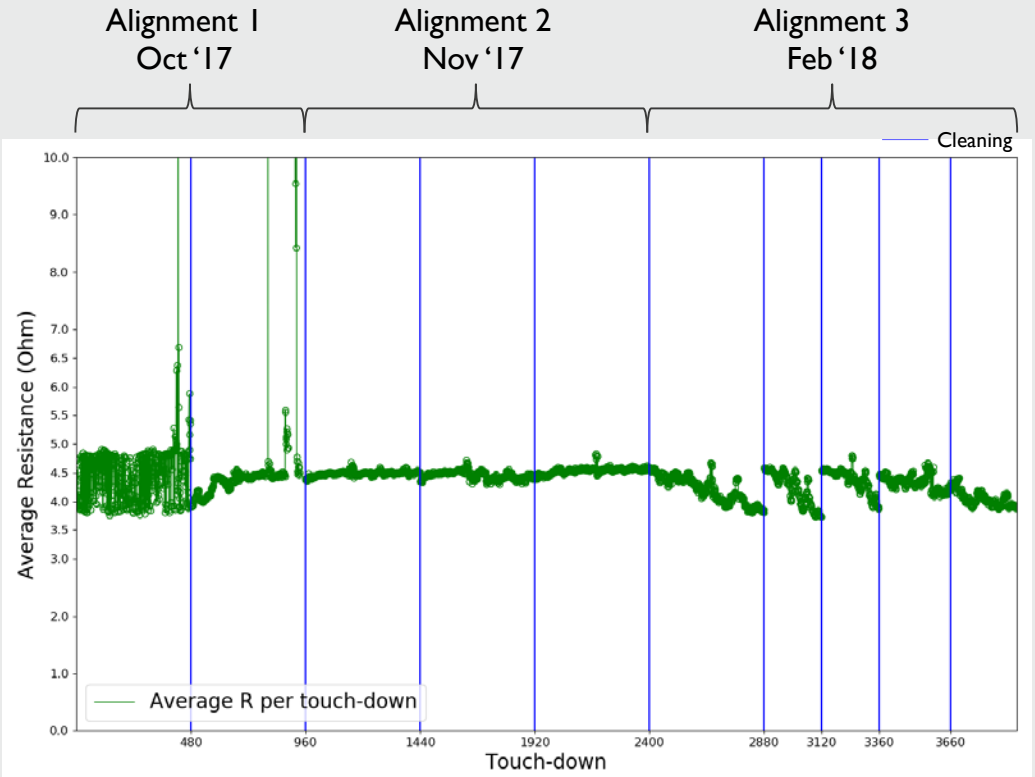
Tip Cleaning

- At varying intervals
  - First after every 480 touch-downs
  - Later after 240 or 300 touch-downs

5. PROBING ON SN MICRO-BUMPS

RUN-IN OF PROBE CARD: ELECTRICAL RESULTS

- Alignment 1
  - Fine-tuning of the test setup
  - Accuracy adjustments
- Alignment 2
  - Normal operating conditions
- Alignment 3
  - Influenced by chuck tilt and low over-travel



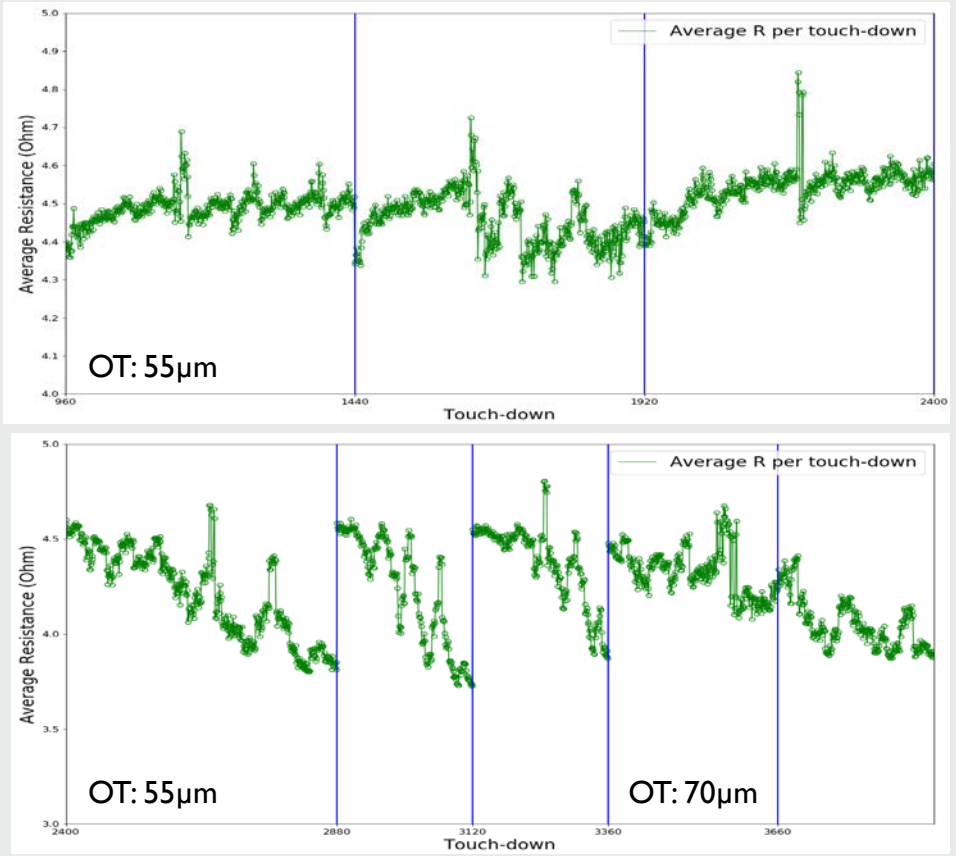
RUN-IN OF PROBE CARD: ALIGNMENTS 2 AND 3

Alignment 2

- Outliers in *R* due to wafer anomalies
- Probe tip cleaning not effective
  - Probes do not get dirty

Alignment 3

- Weaker contact at lower over-travel due to chuck tilt
- Increasing the over-travel flattens *R*-curve



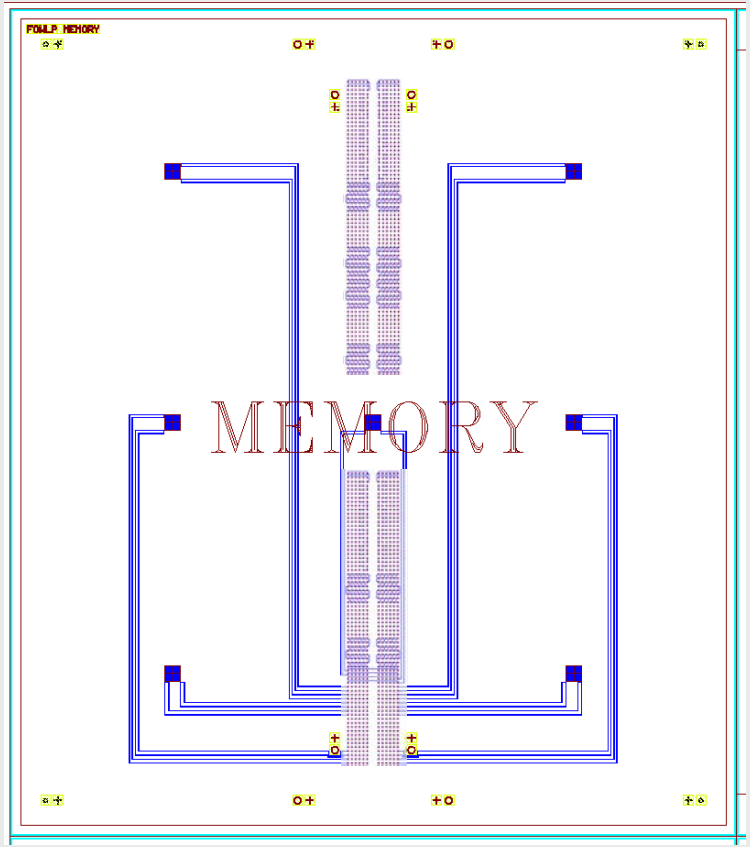
5. PROBING ON SN MICRO-BUMPS
FOWLP MEMORY: DIE DESIGN

Material:

- Fully processed ø300mm wafer, thinned, on tape frame
- 149 Memory dies

Test:

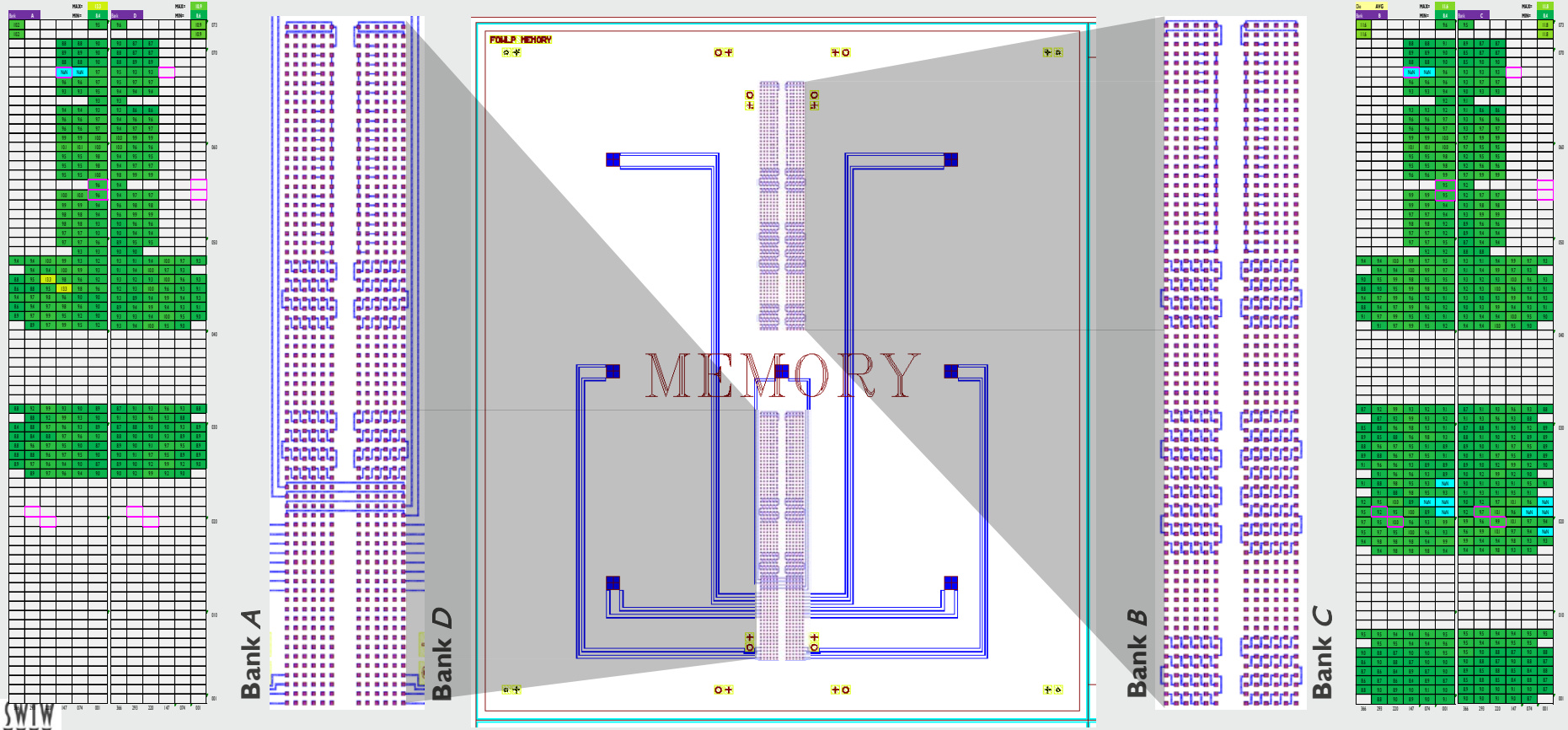
- Pair-wise connected micro-bumps
- 452 measurements / die → 67,348 / wafer
- ~50 minutes test time / wafer
- Measurements include up to 8Ω parasitics



5. PROBING ON SN MICRO-BUMPS

FOWLP MEMORY: DIE DESIGN

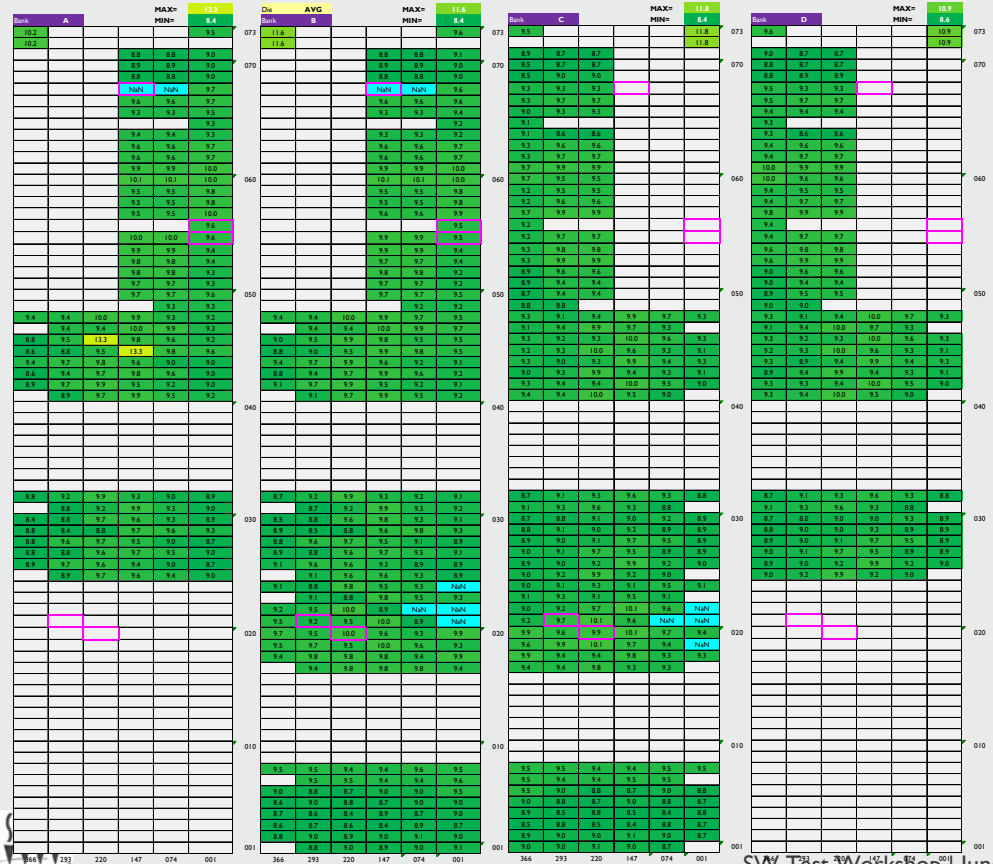
Legend
- = SHORT to neighbor
- = Not connected



5. PROBING ON SN MICRO-BUMPS

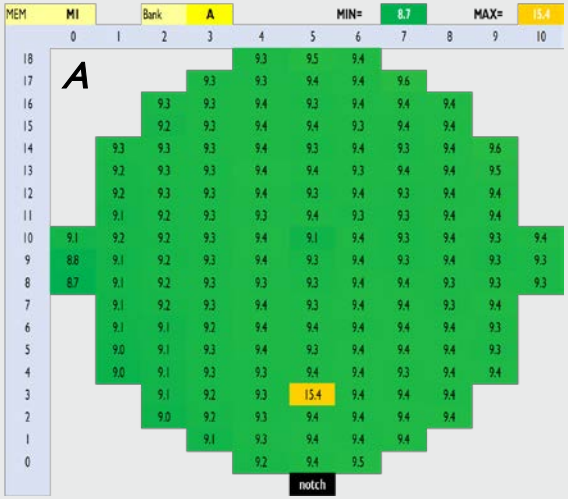
FOWLP 'MEMORY': ELECTRICAL RESULTS

NaN =	NaN	Ohm
MAX Color =	20.0	Ohm
MIN Color =	8.7	Ohm



- Average of all measurements per probe
- Measured resistance as expected!
- Identified one high-ohmic die

➔ exclude from further processing



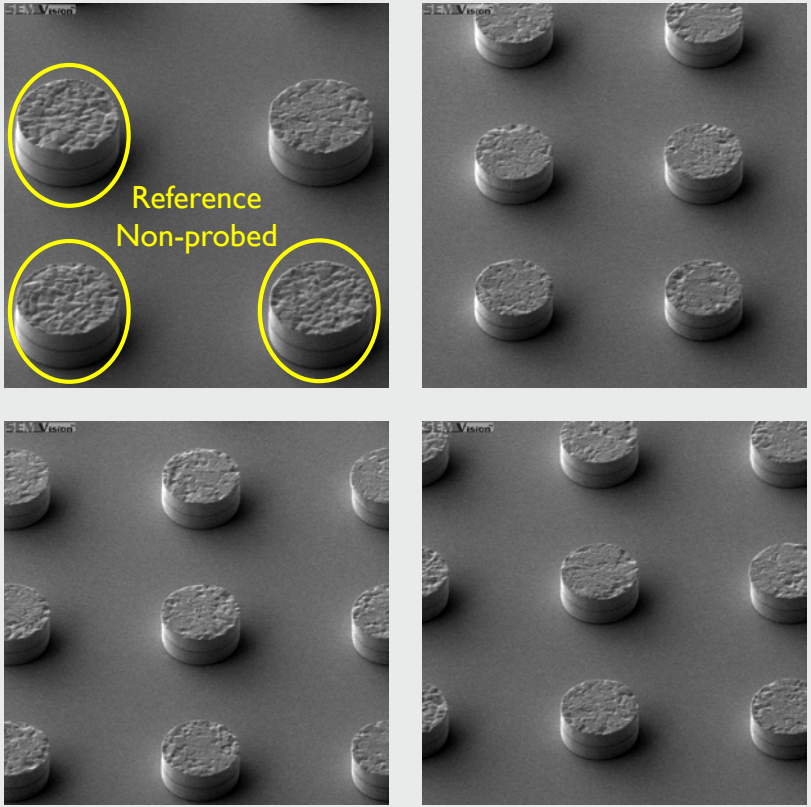
5. PROBING ON SN MICRO-BUMPS

TYPICAL PROBE MARKS

BMB : 9.5µm tall Sn micro-bumps

- Probe diameter : Ø25 µm
- Bump diameter : Ø15 µm

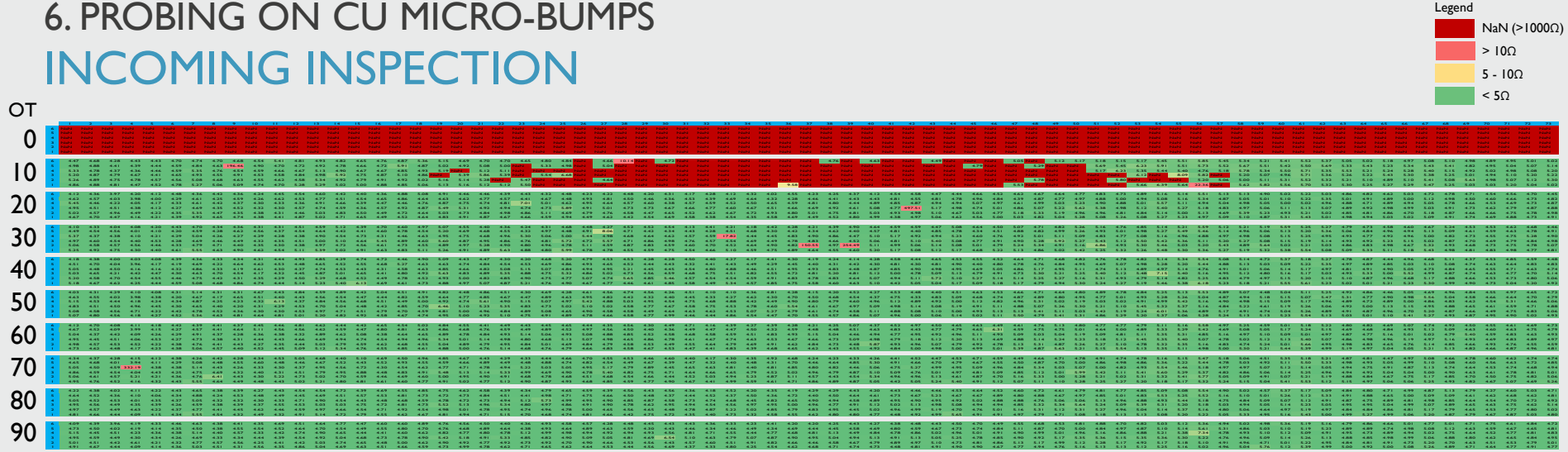
- Probe marks nicely centered
- Uniform marks across whole wafer
- Very light imprints



6. PROBING ON CU MICRO-BUMPS

6. PROBING ON CU MICRO-BUMPS

INCOMING INSPECTION



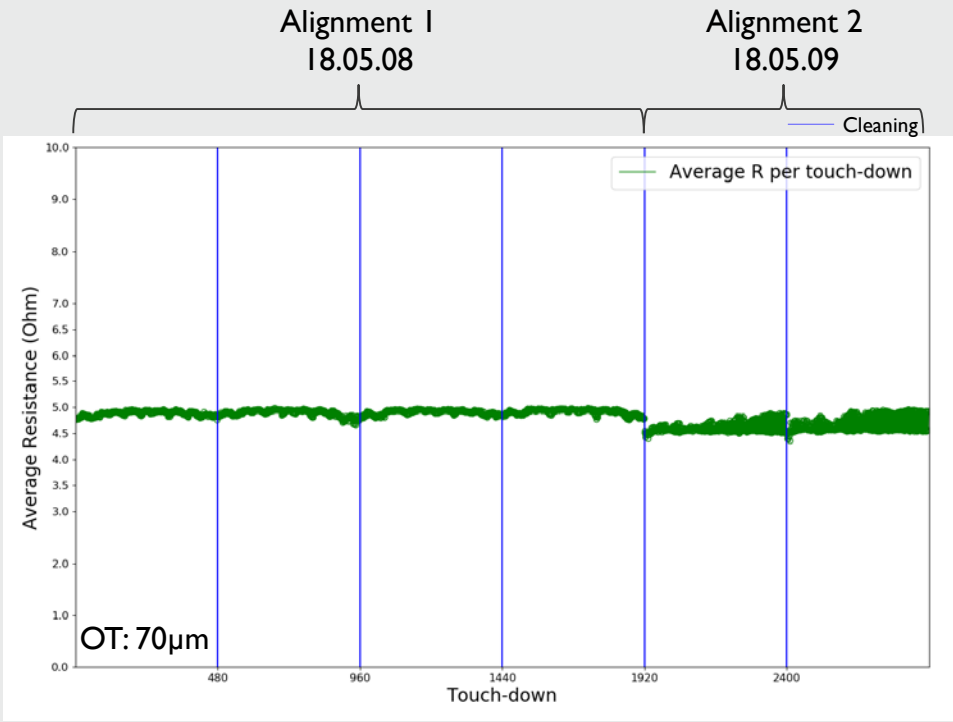
Over-travel	NaNs	Rmin	Rmax	Rmean
0	438	-	-	-
10	157	4.28	196.46	5.20
20	0	3.97	497.51	4.79
30	0	4.01	254.49	4.92
40	0	3.96	7.15	4.79
50	0	3.98	6.46	4.80
60	0	3.99	6.31	4.78
70	0	3.94	332.19	4.85
80	0	4.01	5.73	4.77
90	0	3.96	7.34	4.76

No shorts or opens!

Minimum over-travel: 60µm

RUN-IN OF PROBE CARD: ELECTRICAL RESULTS

- Alignment 1
  - Normal operating conditions
- Alignment 2
  - Measurements influenced by chuck tilt
- Probe tip cleaning not effective
  - Probes do not get dirty



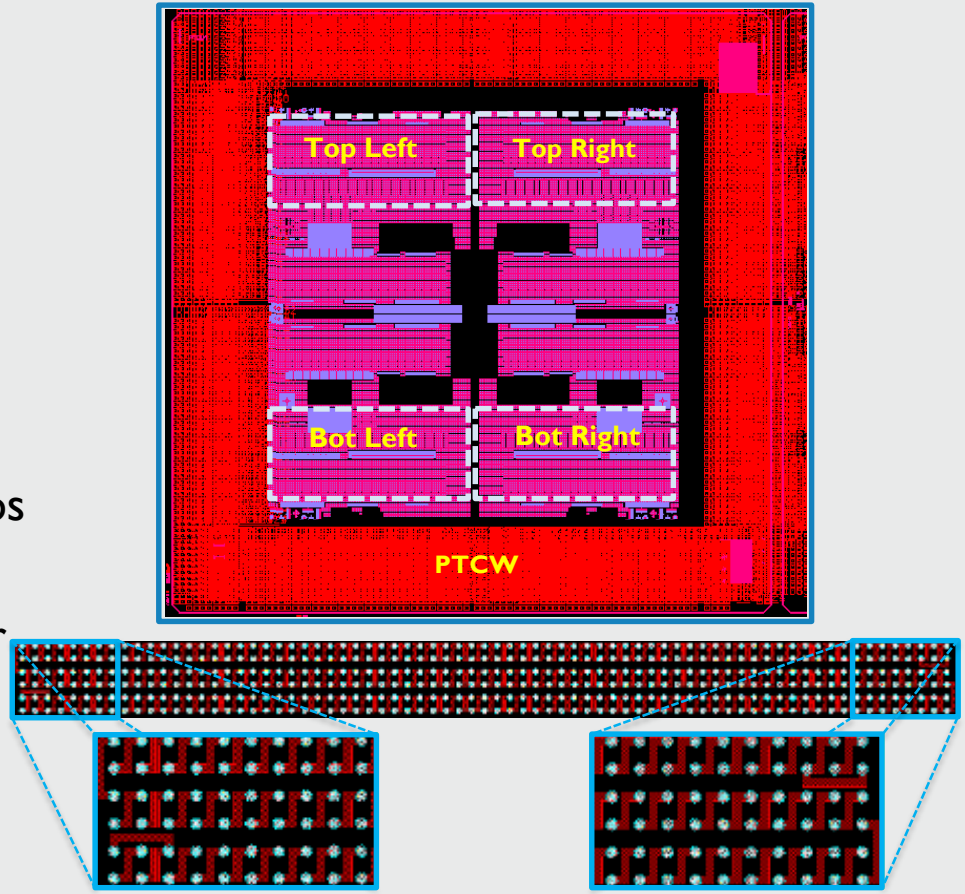
PTCW: DIE DESIGN

Material:

- Fully processed ø300mm wafer
- 275 PTCW dies

Test:

- Pair-wise diagonally-connected micro-bumps
  - Exceptions at corners
- 872 measurements / die → 239,800 / wafer
- ~50 minutes test time / wafer



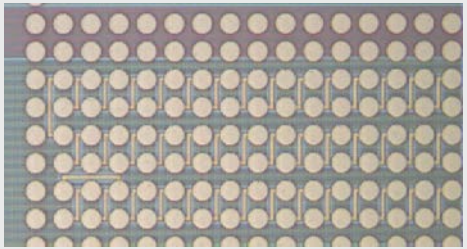
6. PROBING ON CU MICRO-BUMPS
PTCW: ELECTRICAL RESULTS

- Four measurements per probe / die ➔ 1100 measurements per probe / wafer
- Measurements include up to 8Ω parasitics

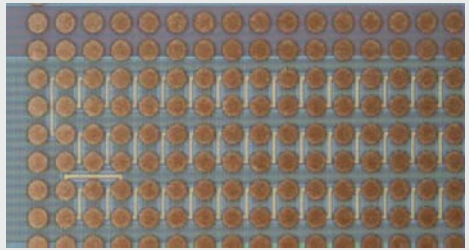
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73
6	11.0	10.5	10.3	11.0	11.3	11.8	12.2	12.7	12.4	13.3	13.2	12.7	13.3	11.0	12.9	11.7	13.3	12.5	14.5	13.3	13.8	11.6	11.2	11.4	10.6	11.5	11.2	10.5	12.3	11.0	12.1	10.8	10.1	10.3	10.1	10.6	10.2	10.5	9.9	10.4	10.7	10.6	10.6	10.5	10.3	10.4	10.5	11.5	10.5	11.1	10.8	10.9	11.2	11.1	11.4	11.8	11.6	11.7	11.4	11.6	11.8	11.5	11.5	12.4	11.3	11.7	11.5	11.7	11.8	11.3	11.1	10.2	10.9
5	11.3	10.5	11.4	10.5	10.6	12.5	13.3	11.3	12.2	13.2	14.0	14.5	11.3	11.4	11.2	14.2	11.6	12.9	13.9	15.8	12.7	11.6	10.2	10.9	12.6	10.5	10.4	12.3	10.8	12.2	11.2	10.9	10.3	9.8	10.3	10.4	10.7	9.9	10.5	10.1	10.5	11.1	10.7	10.1	10.3	10.6	10.7	10.5	11.4	10.6	11.2	10.9	10.8	11.2	11.5	12.0	11.8	11.0	11.7	11.4	11.4	12.4	11.9	10.8	12.8	11.3	10.8	11.9	12.0	11.1	10.9	11.6	10.6
4	12.5	13.5	13.6	11.1	11.6	11.7	13.1	12.2	12.1	12.6	12.2	12.4	13.1	11.9	13.0	10.7	12.1	13.0	12.8	15.5	15.8	15.0	16.2	15.1	14.8	14.7	13.8	13.0	12.4	11.9	12.8	12.6	12.5	13.4	13.1	13.2	12.5	13.4	12.2	12.8	12.5	13.6	12.5	12.7	12.4	12.9	13.6	12.0	14.2	12.7	14.2	13.1	12.0	11.8	11.8	12.2	11.8	12.2	11.9	11.9	13.0	11.5	13.3	12.4	13.1	12.7	13.4	13.6	12.1	11.2	11.1	11.0	10.5
3	15.0	14.5	11.5	12.1	11.4	11.1	12.6	13.6	12.0	12.4	12.6	11.6	12.6	14.4	10.8	12.2	10.7	11.5	15.7	14.7	15.0	17.1	14.8	15.0	15.2	14.2	14.3	13.0	11.5	12.1	12.3	13.1	12.8	12.7	14.0	13.1	12.6	11.8	13.4	12.6	13.1	12.4	13.3	12.5	13.0	12.7	12.4	14.6	11.7	14.5	13.8	12.5	12.1	12.0	12.0	11.5	12.5	12.3	11.8	12.1	12.1	13.2	10.9	13.2	13.0	13.1	14.1	13.3	11.2	11.5	11.9	10.8	12.7
2	15.5	17.2	16.9	14.1	15.8	15.8	16.7	15.3	16.5	14.9	15.3	16.0	17.0	15.6	16.5	15.2	17.4	15.6	22.8	15.6	18.3	14.8	16.6	14.0	18.8	14.4	18.1	15.5	16.1	19.7	15.5	16.2	16.2	15.2	14.8	15.0	13.8	15.0	13.7	13.7	12.3	13.1	12.0	13.8	12.6	13.5	13.0	13.9	13.9	12.9	13.4	11.8	13.4	12.6	13.8	13.1	13.6	13.5	13.6	13.8	14.4	13.6	14.6	12.4	14.6	13.2	14.3	12.6	13.7	14.2	13.1	16.5	11.2
1	20.6	19.7	13.1	18.0	14.7	14.2	15.9	19.8	15.6	13.1	14.8	17.8	16.6	15.4	14.7	17.4	16.0	18.5	15.3	22.6	15.6	17.2	14.1	18.3	14.0	18.8	14.6	16.7	16.6	15.0	20.4	16.2	15.3	15.8	15.1	14.6	14.7	12.7	14.7	14.0	13.0	11.6	13.3	12.2	14.0	13.0	13.4	13.2	13.7	14.0	12.3	13.5	11.7	13.2	13.0	13.3	13.3	14.2	13.9	13.4	13.9	14.8	12.6	15.3	12.4	14.2	13.8	13.1	11.9	14.9	15.4	12.2	19.0

Average *R* per tip across full wafer

- Measured resistance higher than expected
  - Oxidation of Cu micro-bumps



Reference



Heavily oxidized micro-bumps

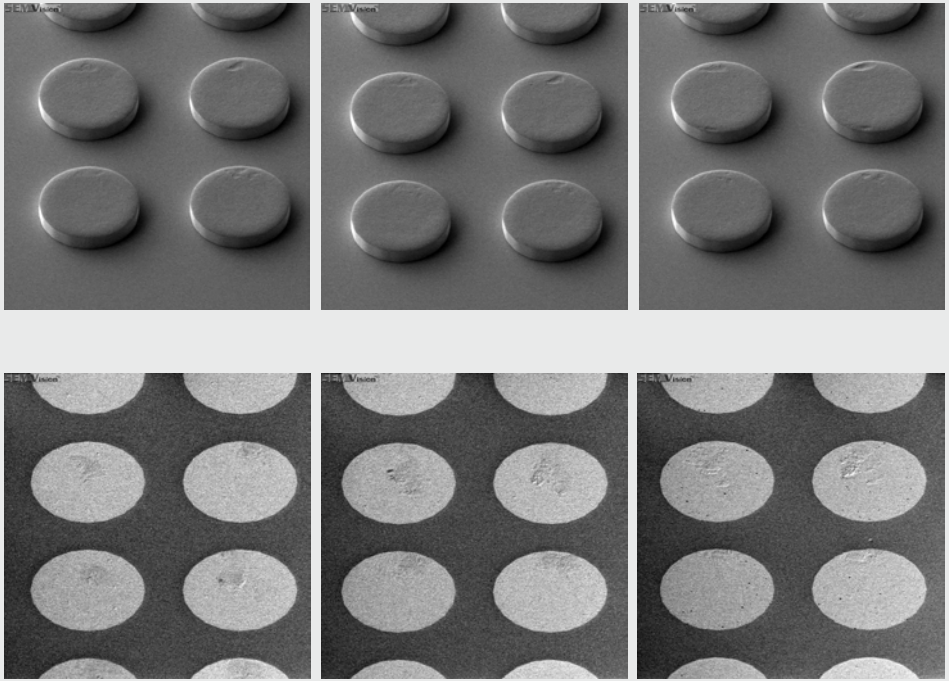
TYPICAL PROBE MARKS

BMB : 5µm tall Cu micro-bumps

- Probe marks on North of *µ*bump
- Uniform marks across whole wafer
- Light imprints

PTCW : Embedded Cu micro-bumps

- Corrected alignment → centered marks
- Light probe imprints



7. CONCLUSION

SUMMARY

- Successfully evaluated two WIO2-1bank probe cards from Technoprobe
  - Stable electrical results
  - Light probe marks
  - No effect of probe tip cleaning, as probes did not get dirty

Probing on Sn micro-bumps

- Technoprobe's TPEG™ T40 probes
- Well-suited for Sn probing
- Probe card to be routinely used in imec

Probing on Cu micro-bumps

- Technoprobe's ARIANNA™ A40 probes
- Well-suited for Cu probing

Future Work

- Continue evaluation with Wide-I/O2-4bank probe cards