



**SW Test Workshop**  
Semiconductor Wafer Test Workshop

***Micro burn-in techniques  
at wafer-level test  
to implement cost effective solutions***



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June 3-6, 2018

# Agenda

1. Melexis Company Overview
2. Automotive Safety Requirements & Burn In
3. Wafer Level micro Burn In (WL $\mu$ BI) Concept
4. TPEG(TM) MEMS T1 LCR2 Vertical Probe Head
5. Characterization, Simulation & System Setup
6. Evaluation Criteria & Achievements
7. Conclusions & Future Work

# Melexis supplies worldwide > 1.3 billion ICs with an average of 10 ICs / car

## Sense & Drive

- ✔ Position
- ✔ Latch & Switch
- ✔ Current
- ✔ Speed
- ✔ BLDC/DC Motor Drivers
- ✔ Fan Drivers
- ✔ Gate Drivers



## Sense & Light

- ✔ Pressure / TPMS
- ✔ Temperature / FIR
- ✔ Light / Rain-Light
- ✔ Gesture / Active Light / 3D ToF
- ✔ Sensors Interface IC
- ✔ LIN RGB Drivers

# Melexis Facilities & Locations



## Sales & Applications

Belgium – Tessenderlo  
Greater China – Shanghai, Shenzhen, Taipei  
France – Paris  
Germany – Erfurt  
Italy  
Japan – Yokohama  
South Korea – Seoul  
USA – Detroit

## Manufacturing

Belgium – Ieper  
Bulgaria – Sofia  
France – Corbeil-Essonnes  
Germany – Erfurt  
Malaysia – Kuching

## Research & Development

Belgium – Ieper, Tessenderlo	Philippines – Manila
Bulgaria – Sofia	Switzerland – Bevaix
France – Grasse, Paris	Ukraine – Kiev
Germany – Erfurt, Dresden	USA – Nashua



# Agenda

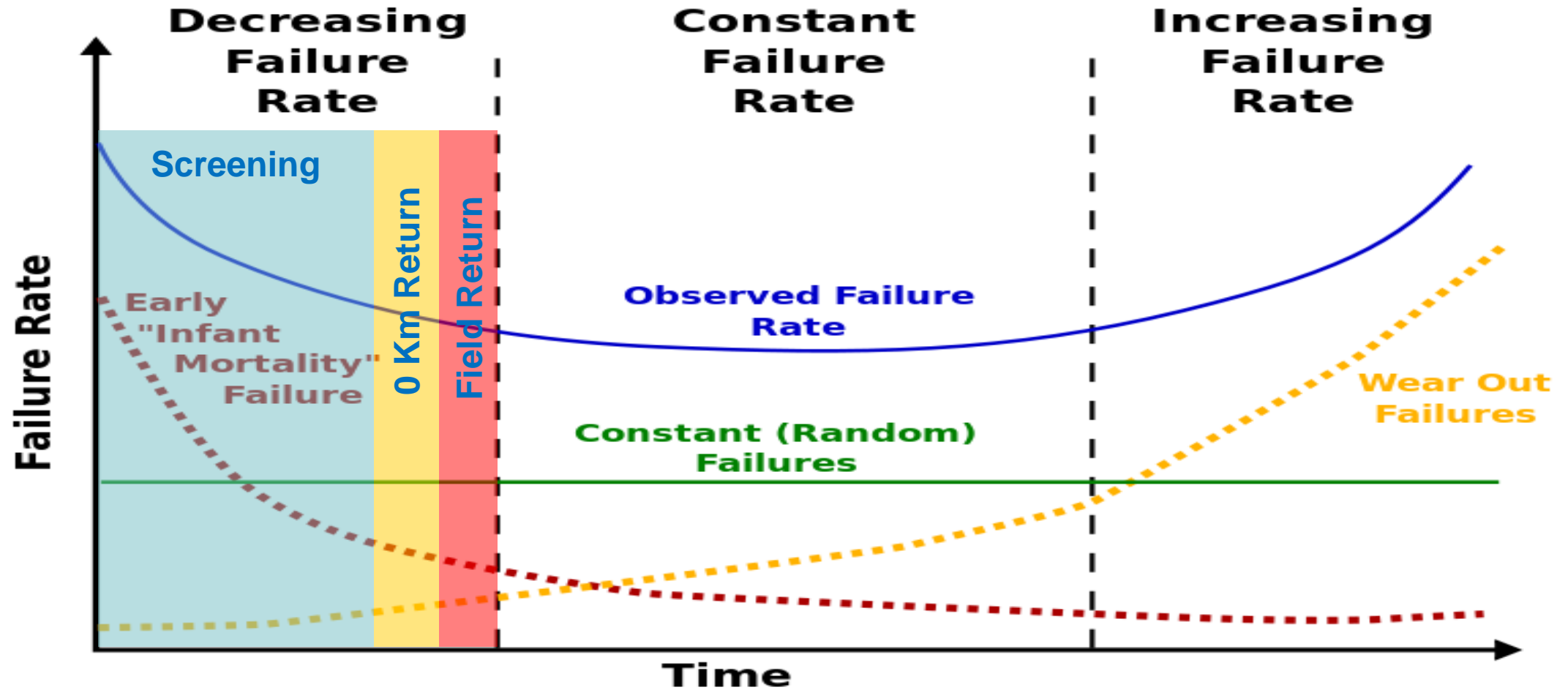
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# Automotive Safety Requirements

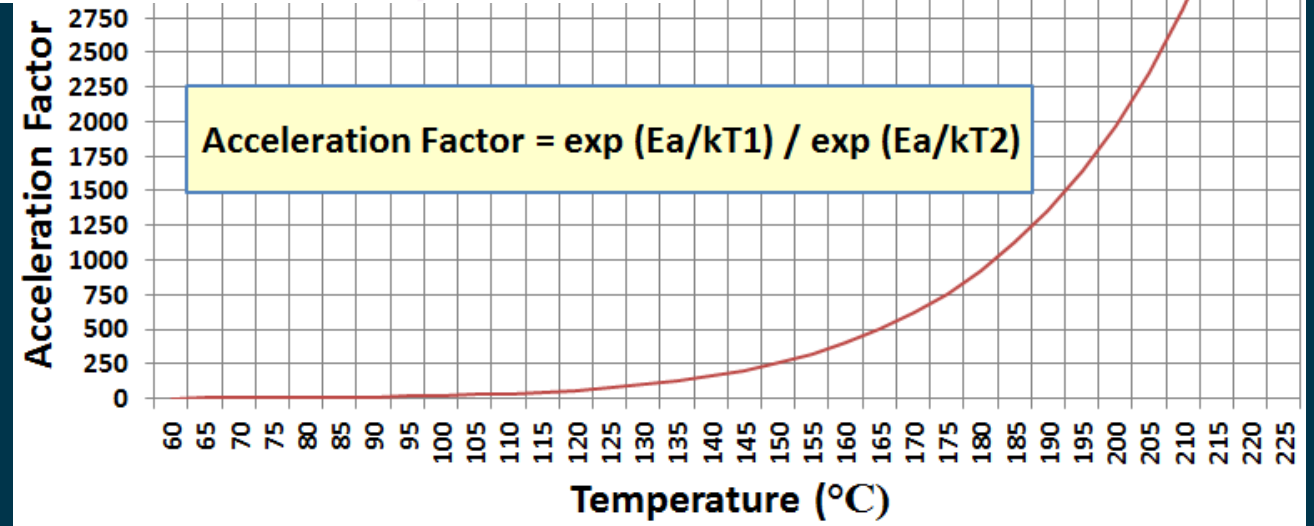
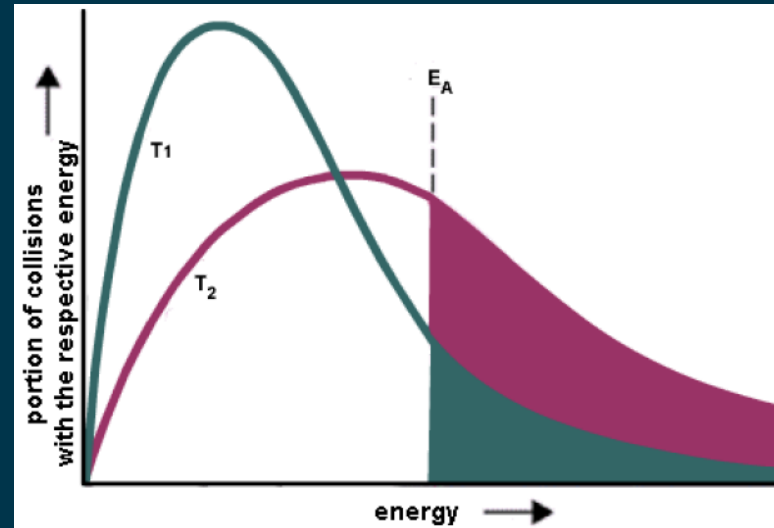
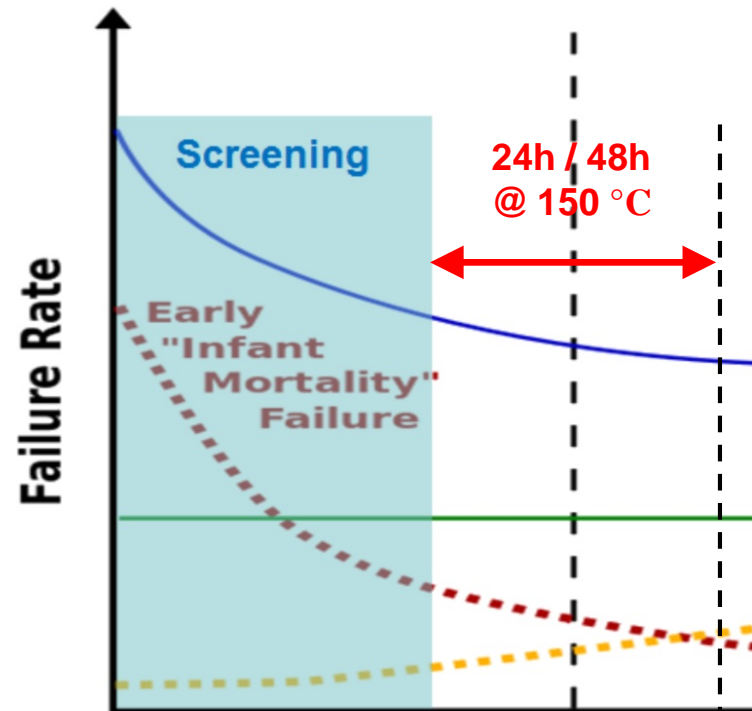
- Prevent 75% of early life failure at customer side
- Focus on digital failures without redesign
- Low impact on supply chain lead-time

→ Only available solution: ***“Burn-In”***

# Burn In Concept



# Burn In Concept





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# Wafer Level *micro* Burn In (WL $\mu$ BI)

## Test requirements:

- Stress all devices with enhanced test capability
- Multi-site testing at the wafer level (for efficient throughput)
- Tests at high temperature
  - High temperature capability and materials (chuck, prober, probe card with stiffener)

## Challenges:

- Stability of the prober and probe card (test-cell) for high temperature
  - Stable Cres, probe-to-pad alignment and minimal pad damage
- Limit effect on supply chain lead time

# Wafer Level *micro* Burn In (WL $\mu$ BI)

$$\text{Acceleration factor} = \exp(E_a/kT_1) / \exp(E_a/kT_2)$$

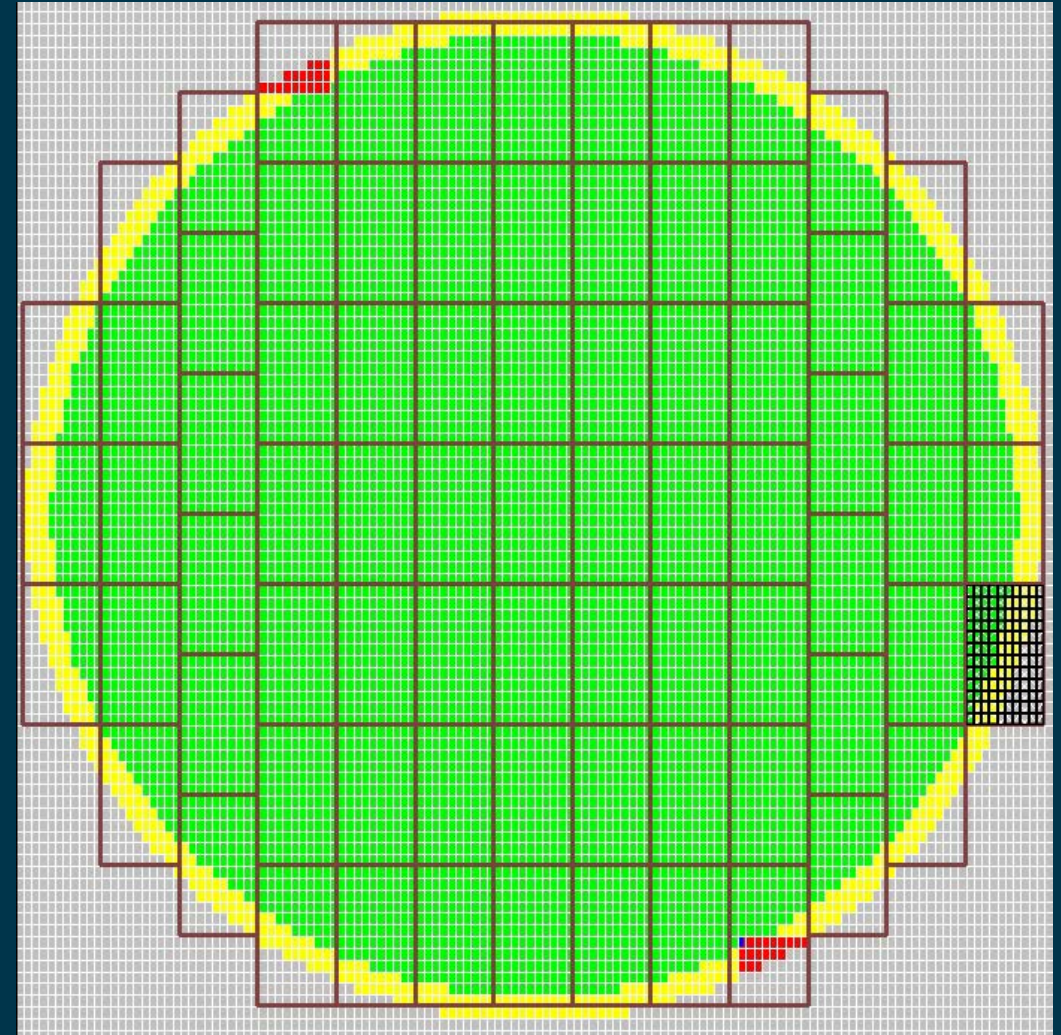
Practical use temperature (T1) = 55°C = 328.15 K

Accelerated test temperature (T2) = **175 °C** = 448.15 K

Activation energy ( $E_a$ ) = 0.7 eV

Boltzmann constant (k) =  $8.6171 \cdot 10^{-5}$  eV/K

**Acceleration factor = 756.43**

[illegible]

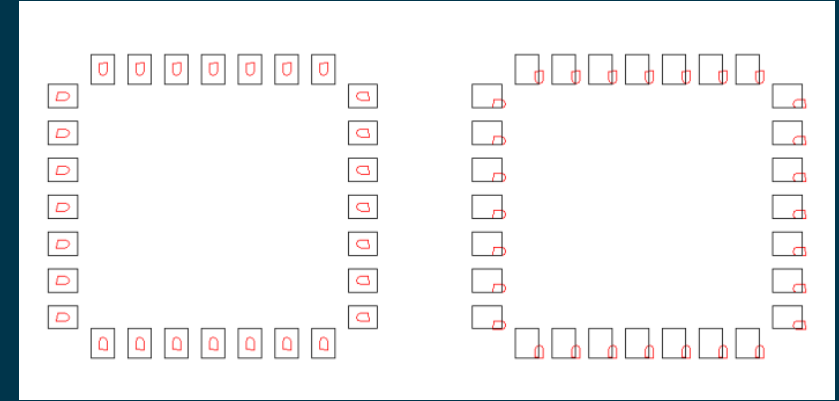
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# Wafer Probing @ Very High Temperature Background

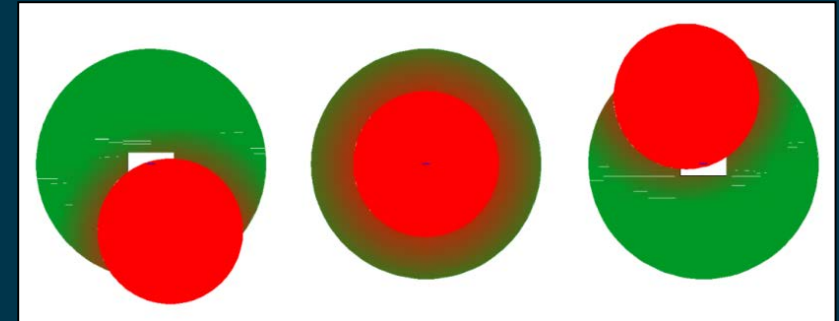
## Challenges of probing in temperature:

- CTE mismatch
- Prober constraints
- PCB thermal gradient



## Issues:

- XY misalignment
- Probe head Z displacement



In red the hot chuck  
In green the PCB

# Concept

**Probe card design needs to consider all materials/mechanical constraints at high temperature trying to mitigate:**

- CTE mismatches
- Thermal gradients

**Probe card for hot temp test needs:**

- Enhanced mechanical structure to test at high temperature
- Dedicated probing technologies to address stable contact

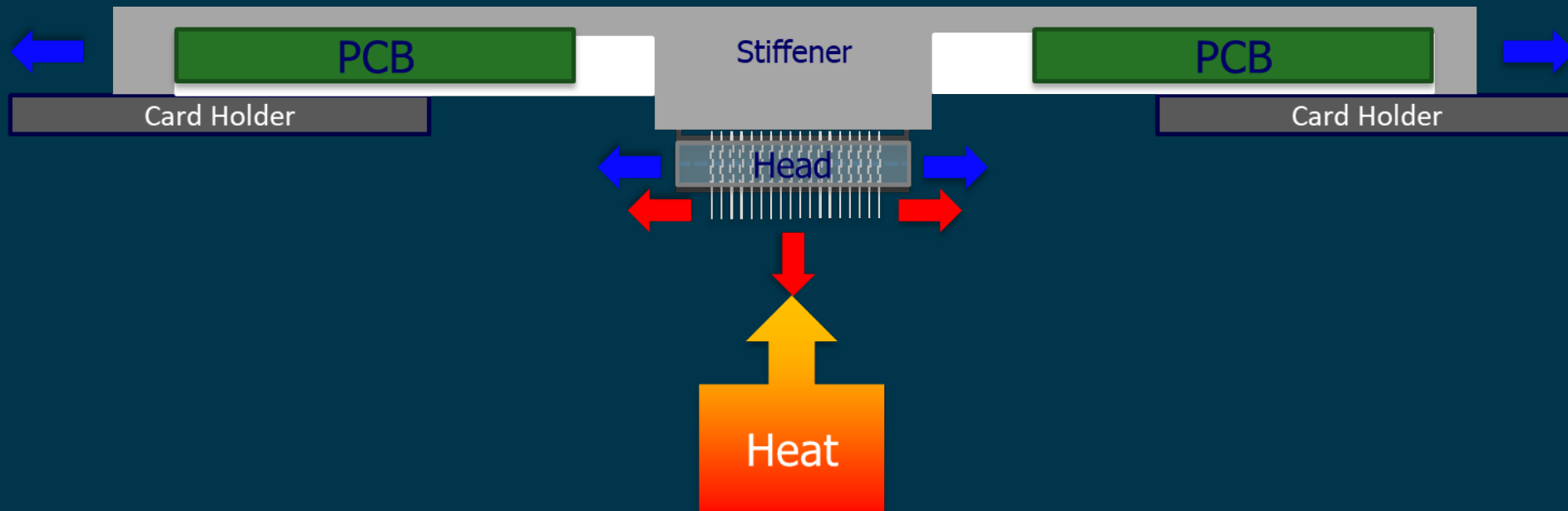
**Characterization data on proofed concept hardware**



# Enhanced Mechanical Structure

## Enhanced mechanical structure to test at high temperature:

- Large stiffener: best configuration is when PC stiffener is larger than PCB and it lands directly on proper PC holder
- High probe depth to increase PCB distance from heat source (chuck)

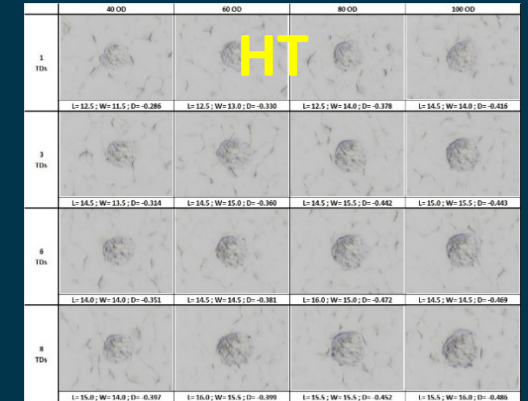
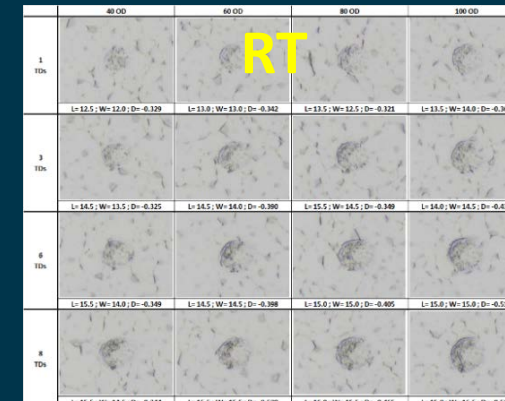
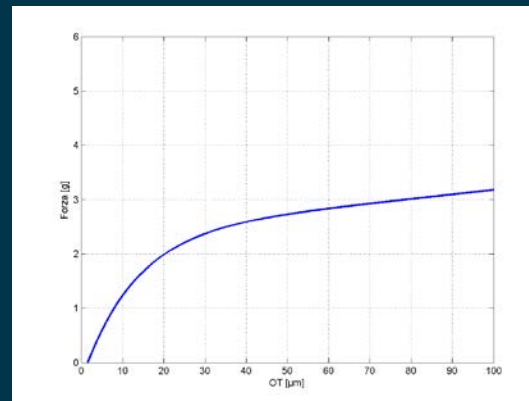
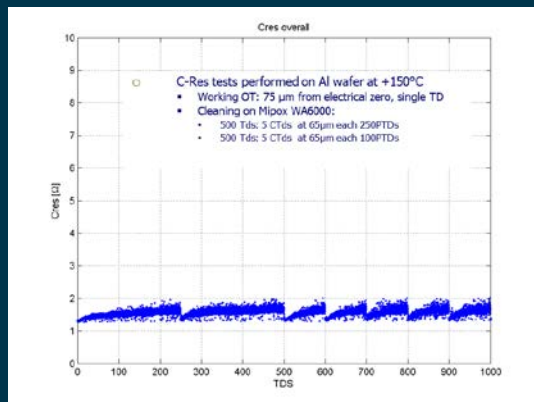


# Dedicated Probing Technologies

## TPEG™ MEMS T1 LCR2 Vertical Probe Head:

- Has been characterized for high temperature  
!! Test up to 200 ° C !!
- Stable Cres over time at high temperature
- Stable force over high temperature
- Stable probe marks over high temperature

PARAMETER	TPEG™ MEMS T1
Needle diameter	Less than 1,5 mils equivalent
Max pin count	> 20.000 pins
X, Y alignment accuracy and Z planarity	X,Y: $\pm 8 \mu\text{m}$ ; Z plan: $\Delta 20 \mu\text{m}$
Min pitch and configuration	55 $\mu\text{m}$ linear configuration
Pin Current (CCC @RT)	410 mA
Force (at 3 mils OT)	3 g



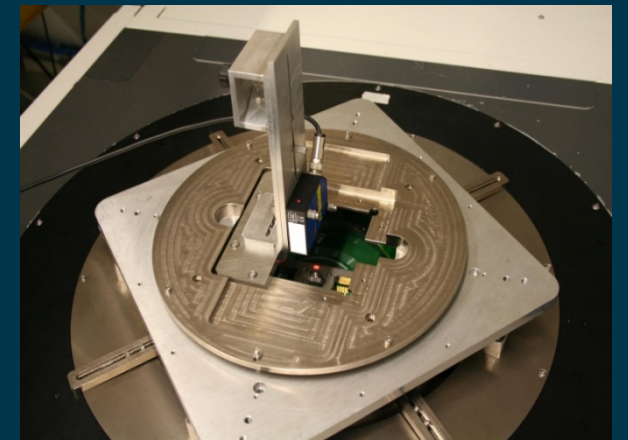
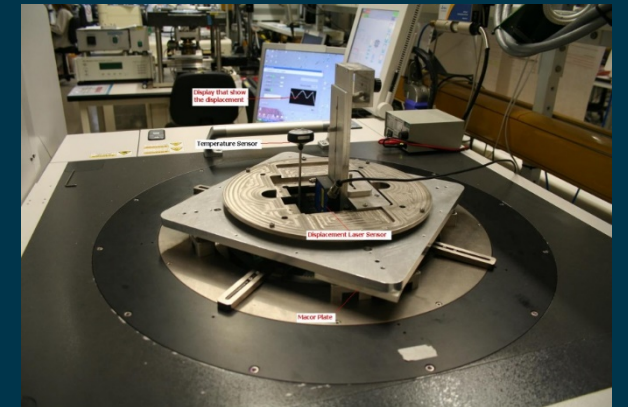
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# Characterization

## Technoprobe's ultra high temperature solution:

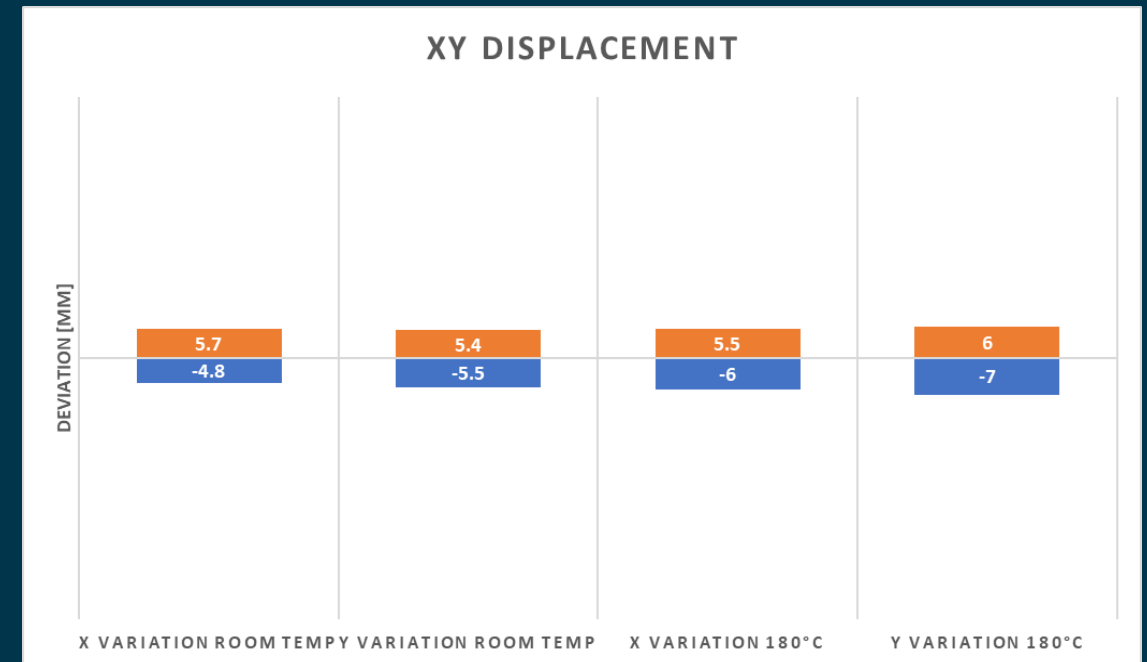
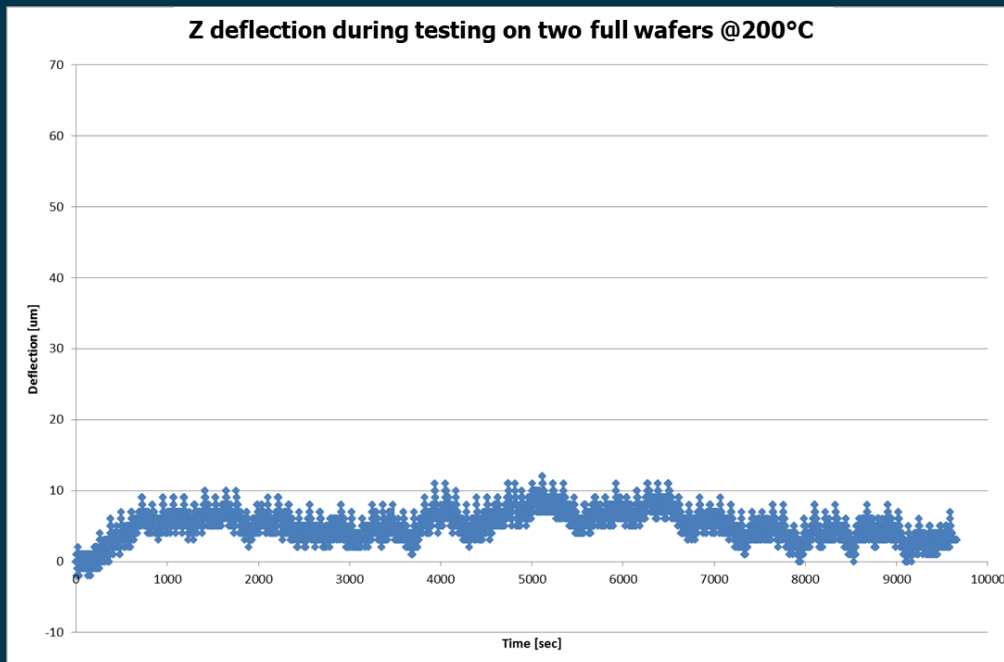
- Characterization tests up to +200° C
- Mechanical testing setup
  - Card fixed on the prober
  - Tests performed without pogo pins pressure
  - Laser sensor measures the vertical movement during a full wafer test
  - No sensors in contact with the card
  - Thermal sensors to detect card temperatures
  - Standard card and enhanced HW card both tested on Al blank wafer as well as customer wafer (Al pad)



# Z Deflection @ High Temperature: “Enhanced Mechanical Probe Card”

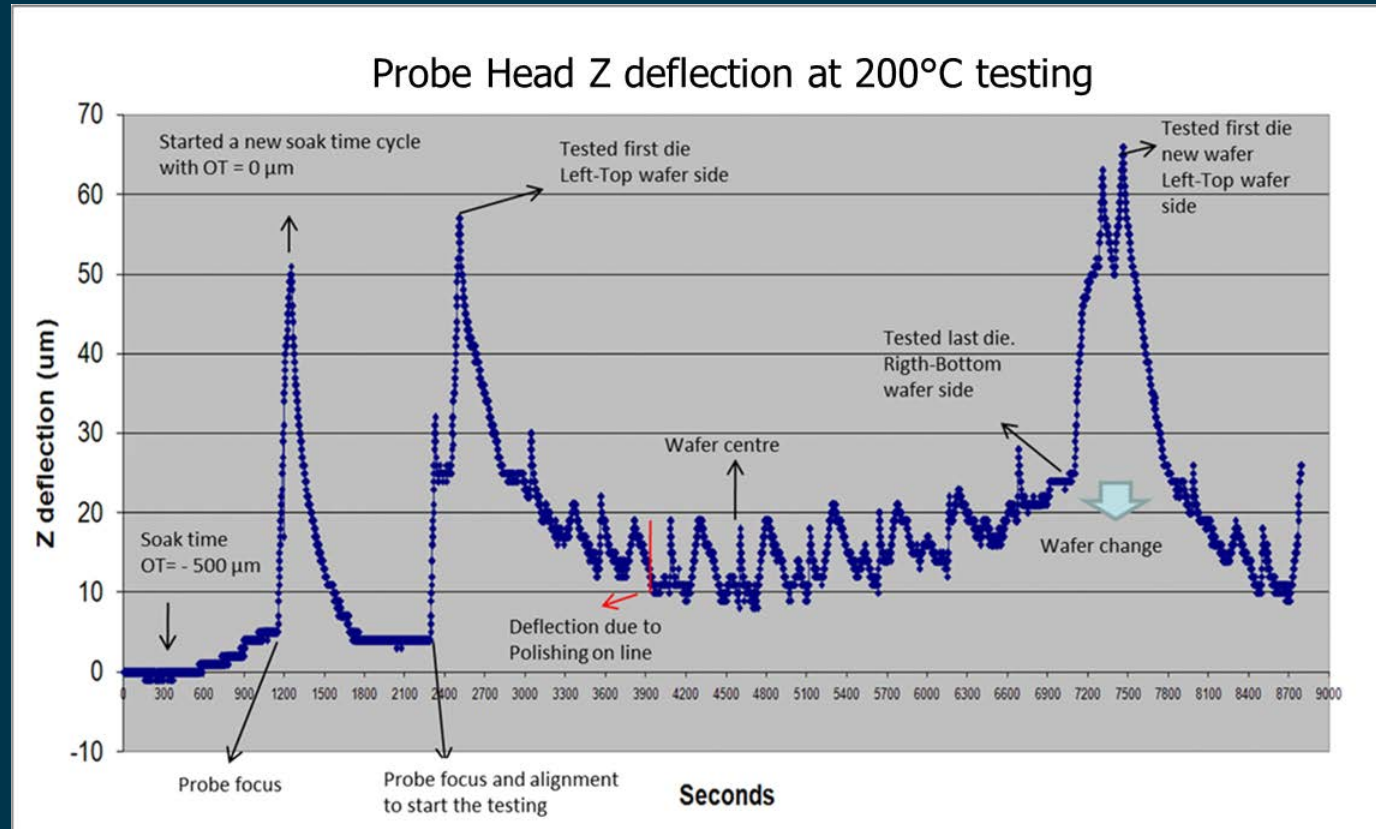
Characterization collected data on AL blank wafer at +200 ° C shows low XYZ variation vs. room temperature:

- Z deflection less than 20  $\mu\text{m}$
- XY displacement variation less than 10  $\mu\text{m}$



# Z Deflection @ High Temperature: “Standard Probe Card”

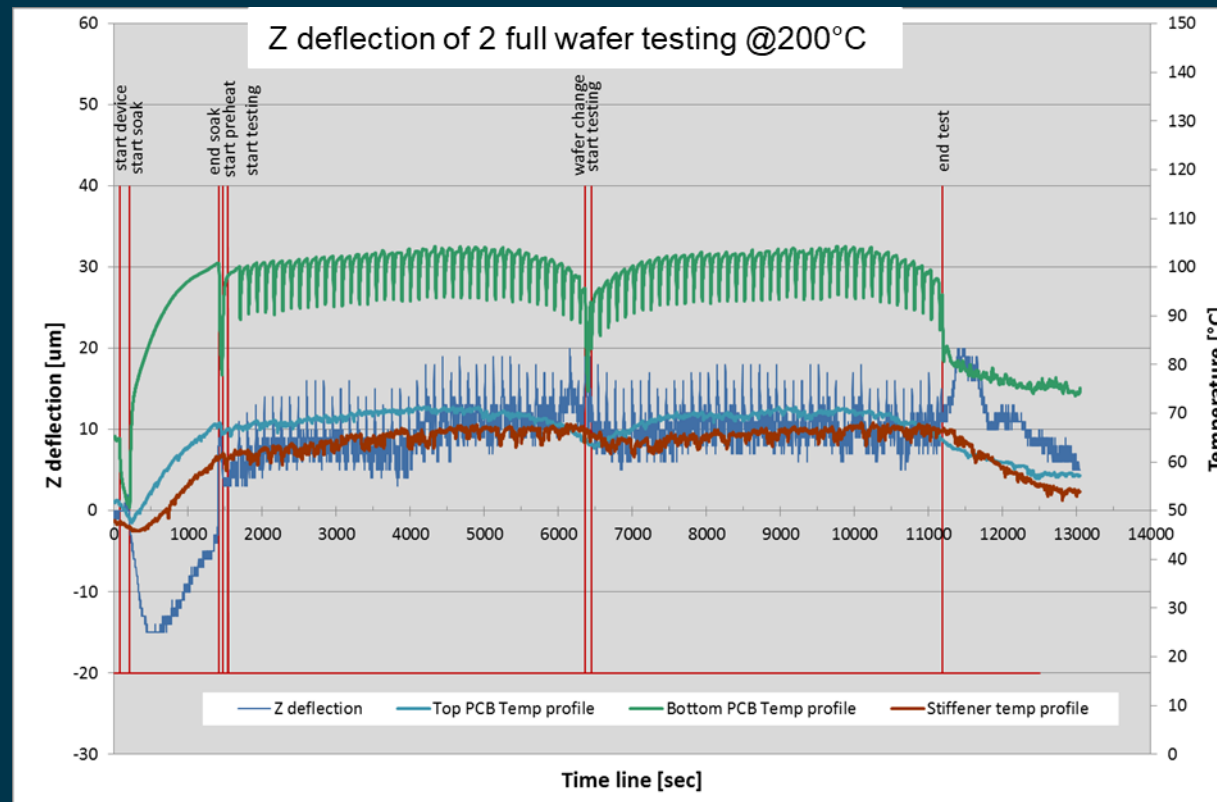
Characterization data on Customer wafer @200° C : Without enhanced high temperature hardware the characterization results showed large Z deflection



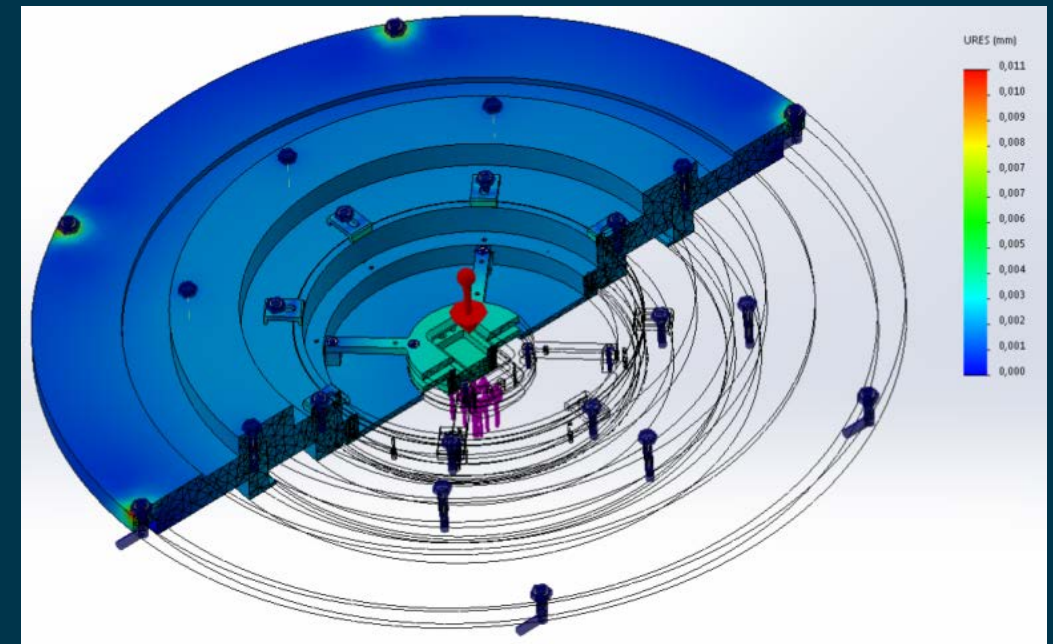
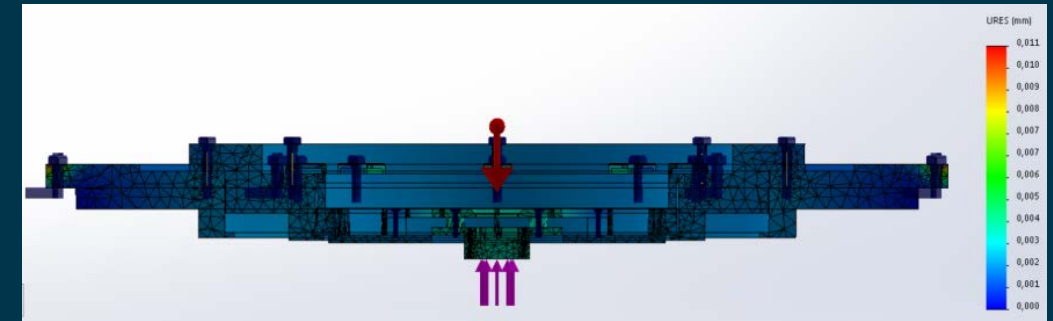
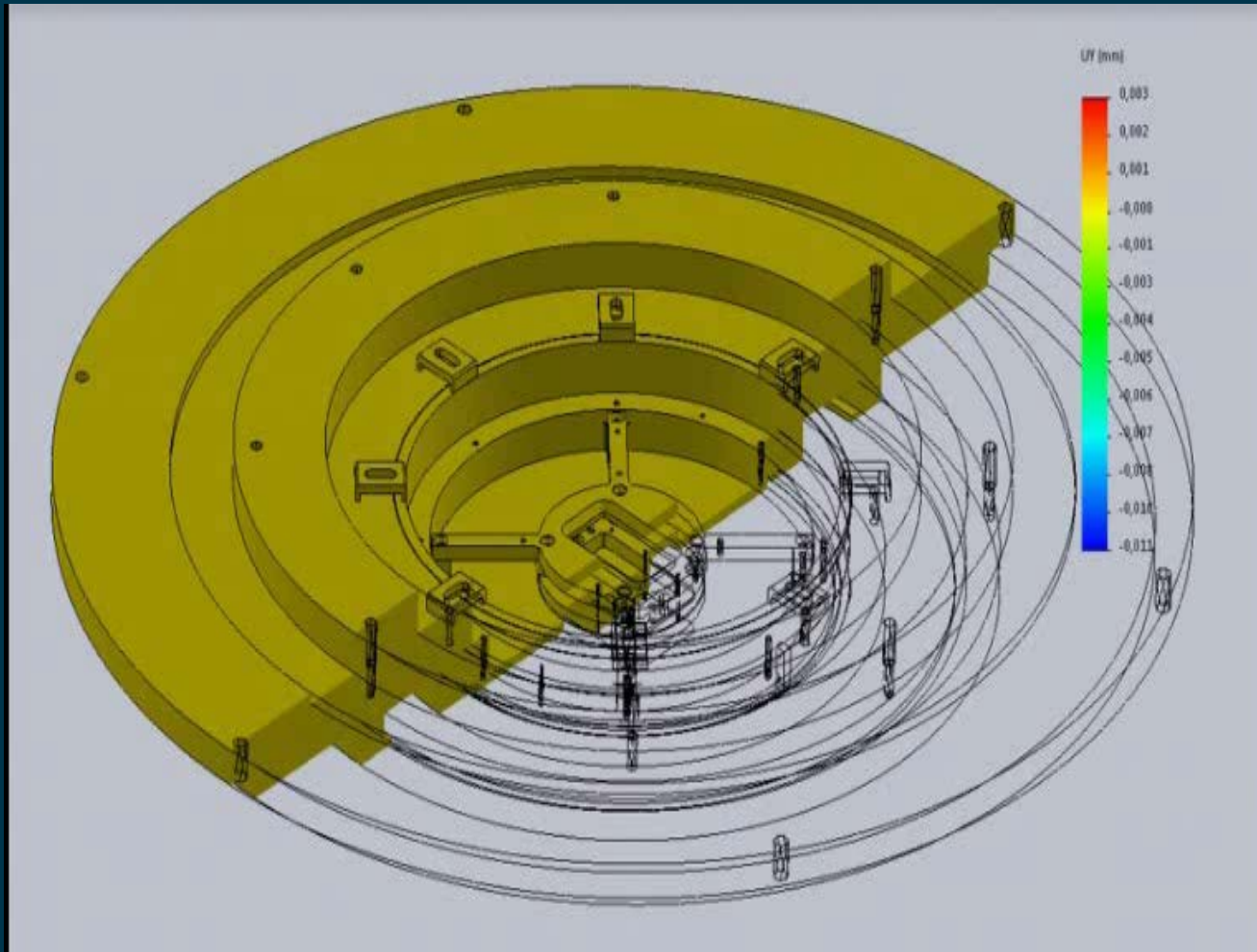


# Z Deflection @ High Temperature: “Enhanced Mechanical Probe Card”

Characterization data on Customer wafer @200° C: Enhanced mechanical structure for high temperature testing provides the required Z stability as probe head Z deflection follows stiffener (mechanical structure)



# WL $\mu$ BI System Simulation



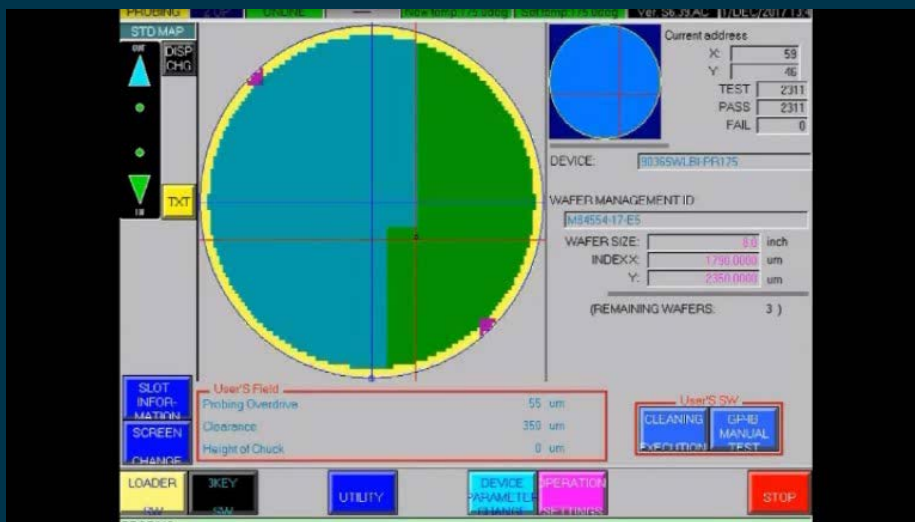
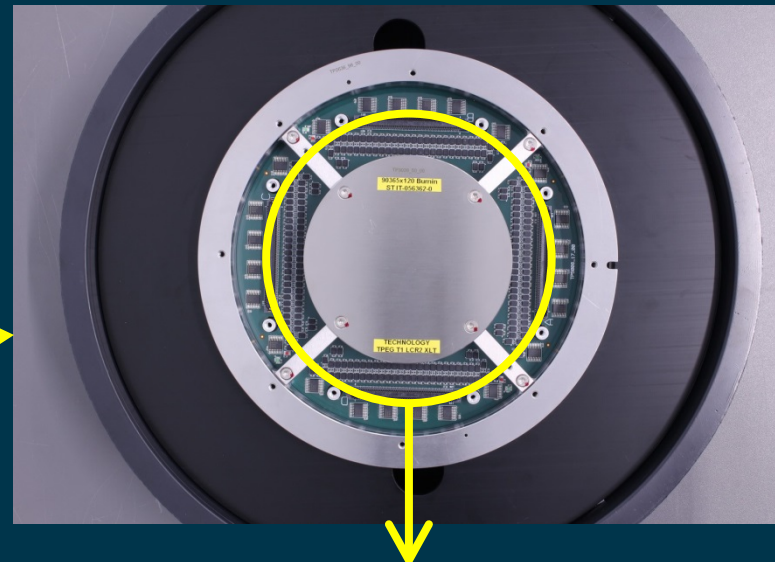


# WL $\mu$ BI System Setup

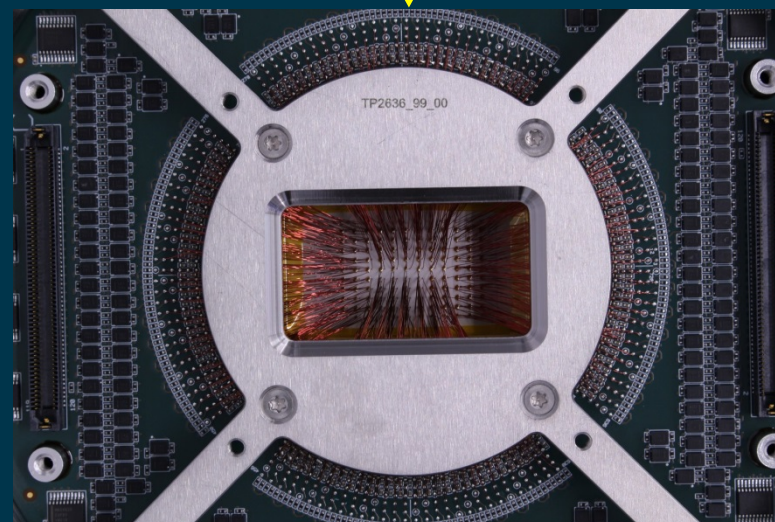
TSK UF2000 – ATT high temp. chuck



Technoprobe MEMS T1



Probing action

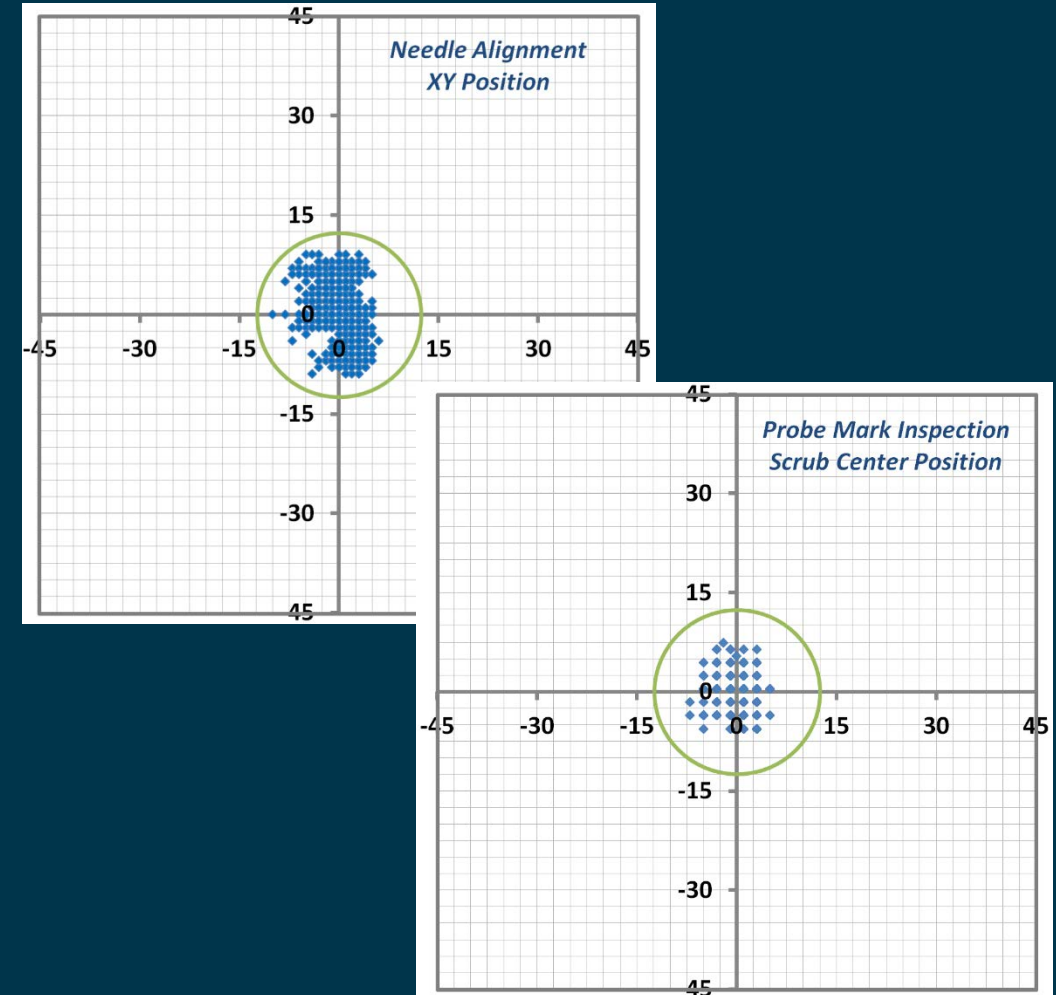
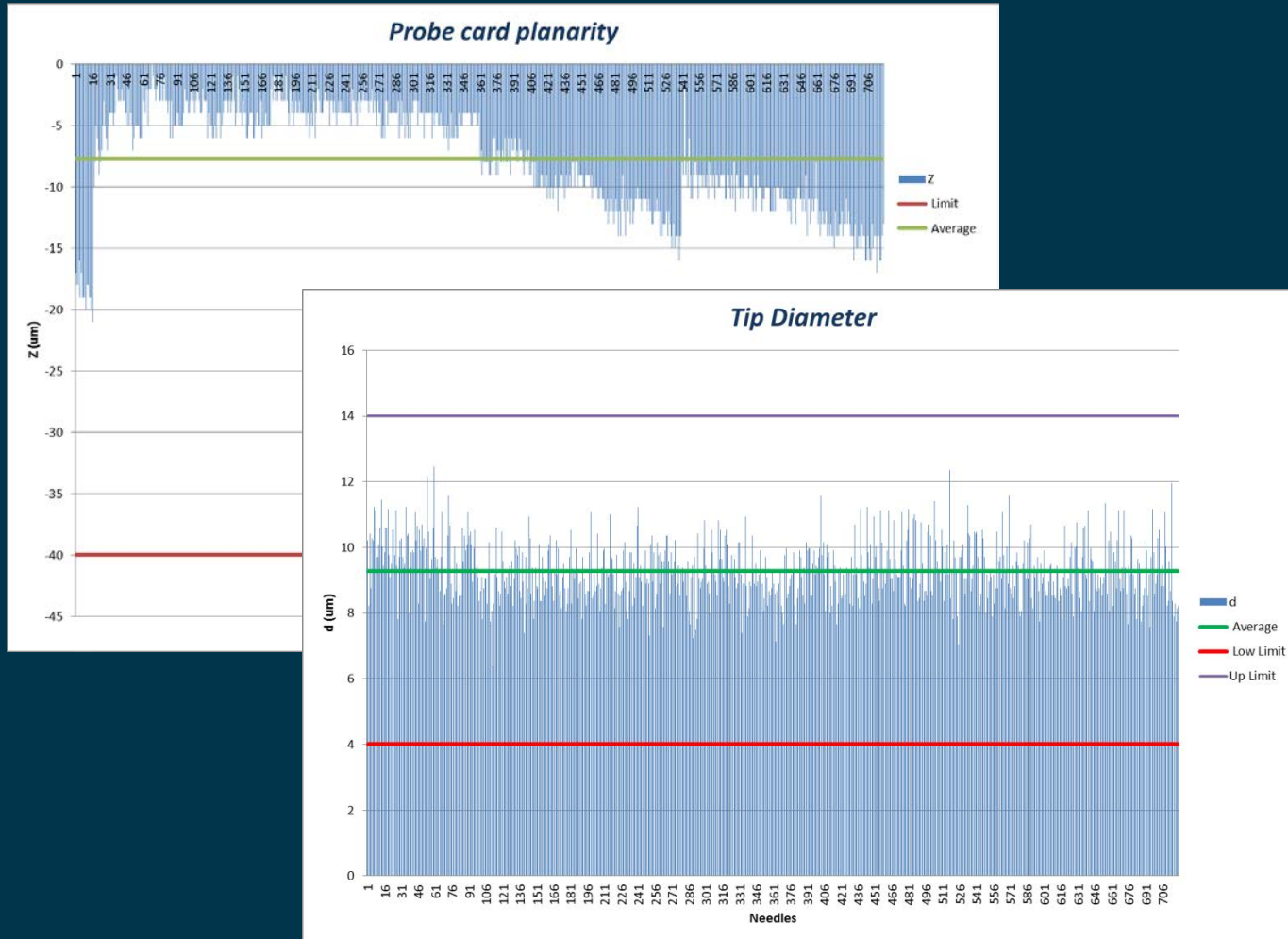


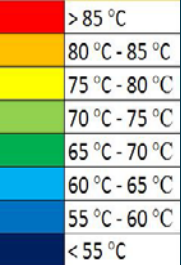
Tester side – space transformer

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# WL $\mu$ BI Validation Results





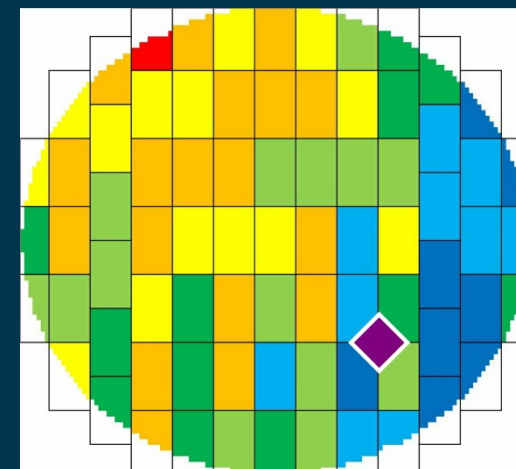
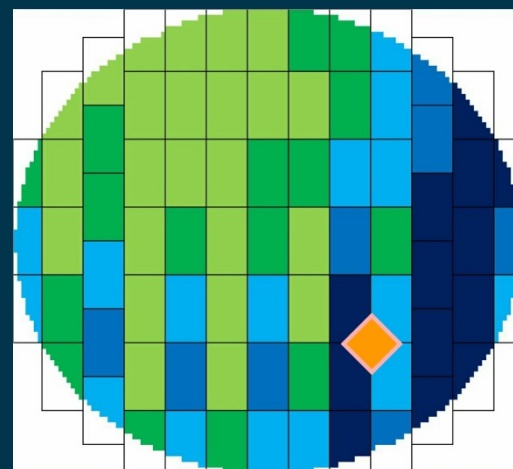
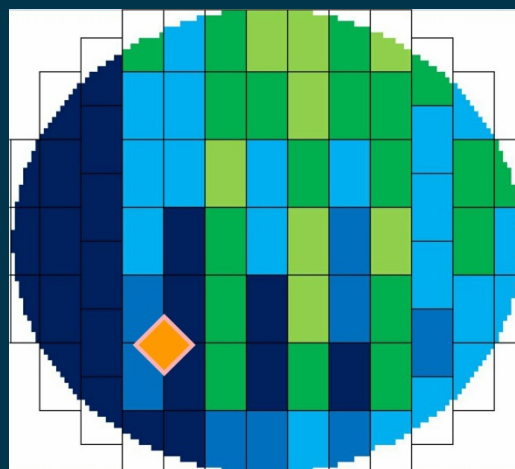
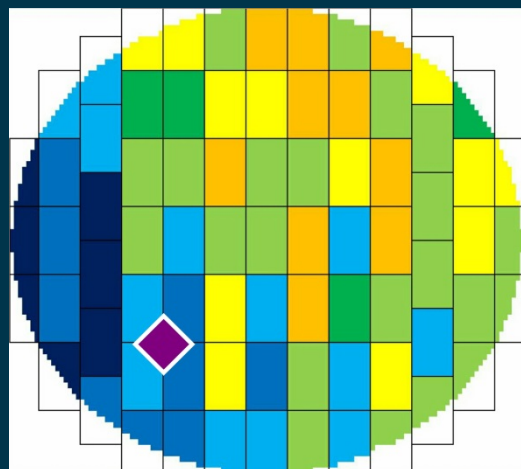
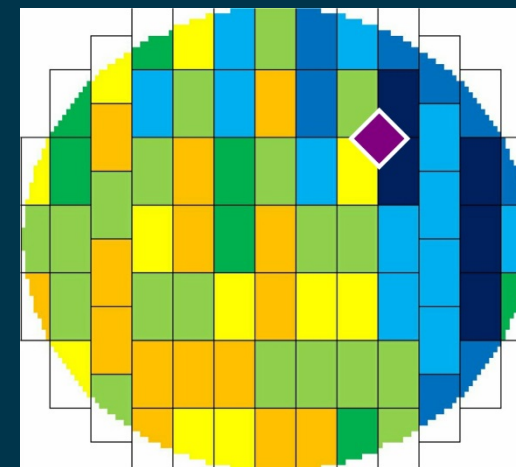
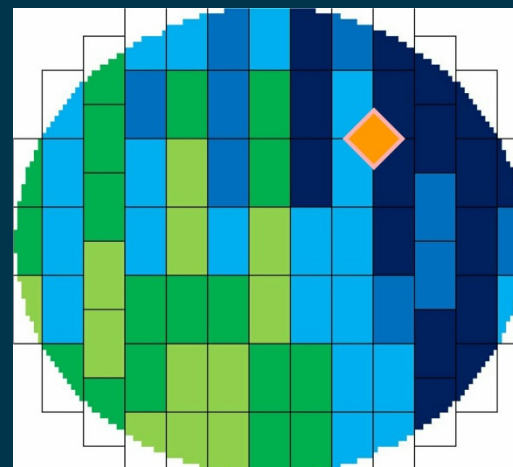
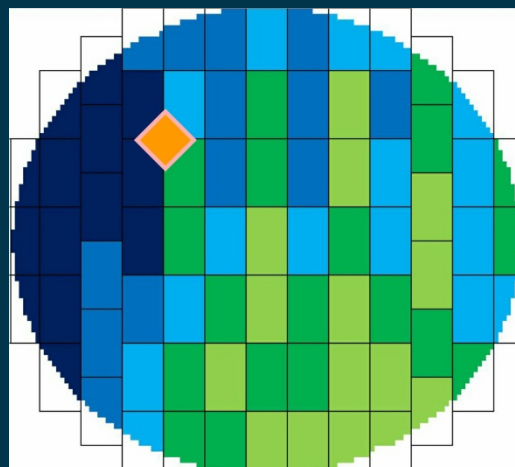
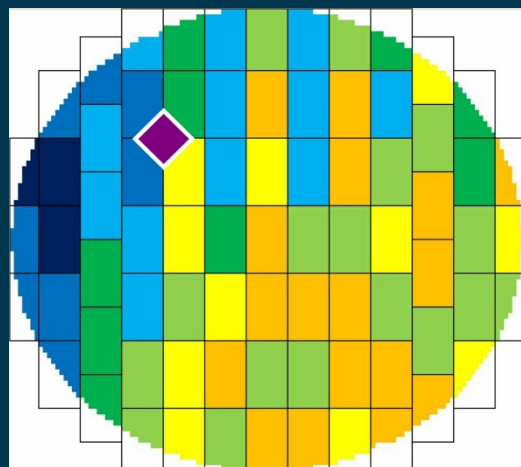
# WL $\mu$ BI Validation Results

Wafer side

Tester side

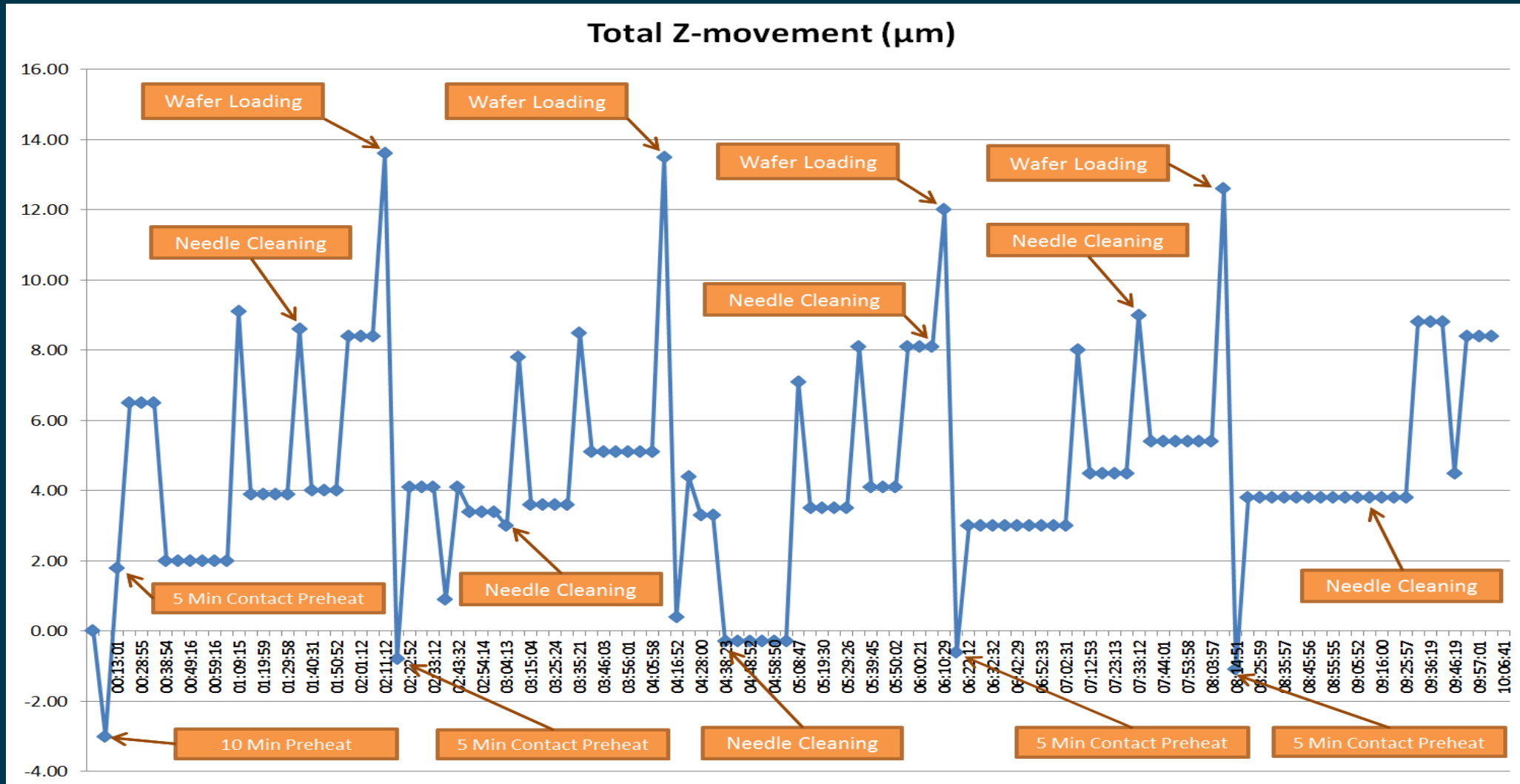
Tester side

Wafer side

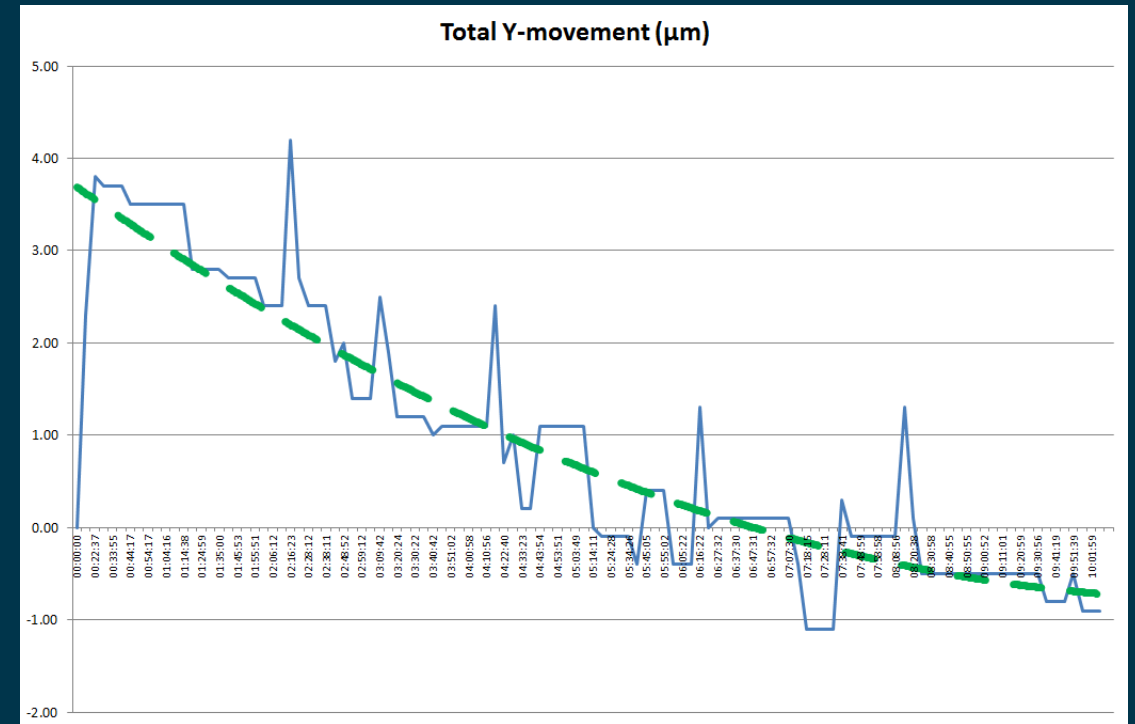
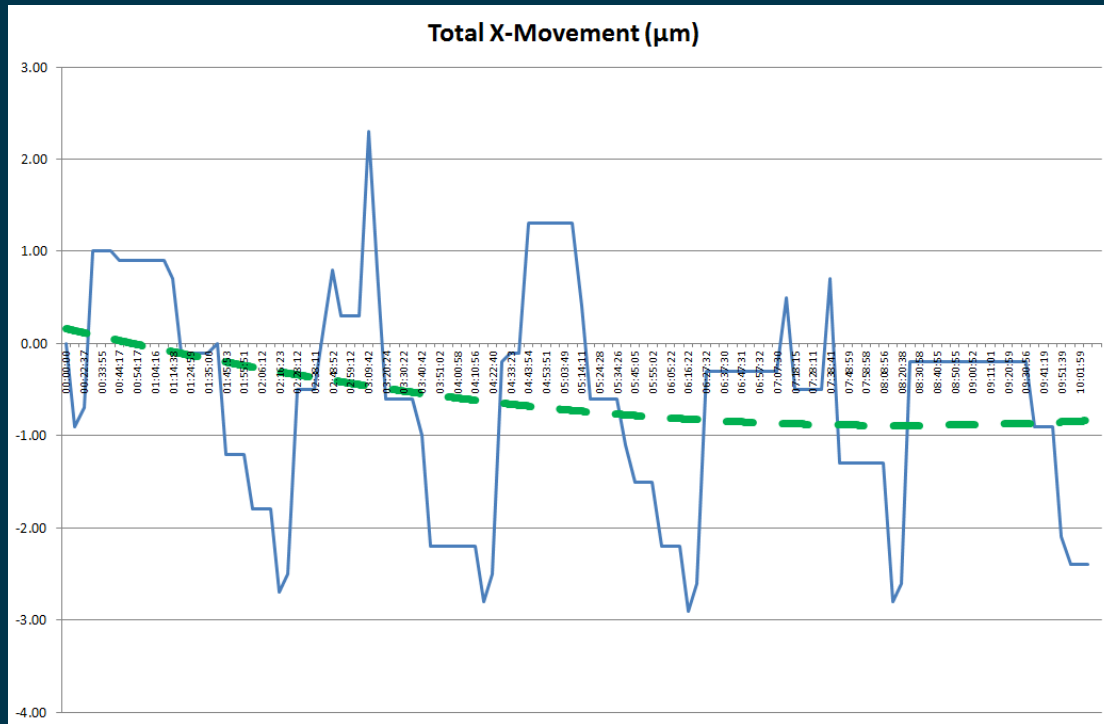




# WL $\mu$ BI Validation Results



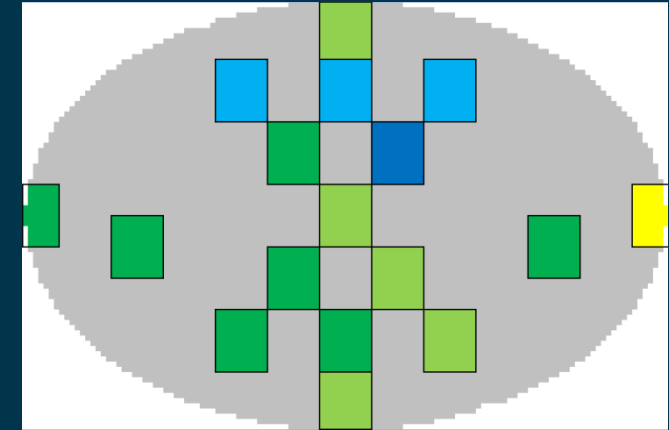
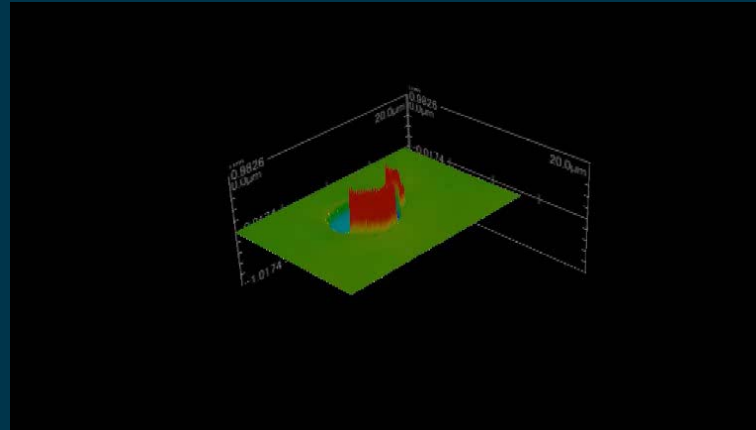
# WL $\mu$ BI Validation Results



# Scrub Profile & 3D @ 175 °C (55 μm OD)

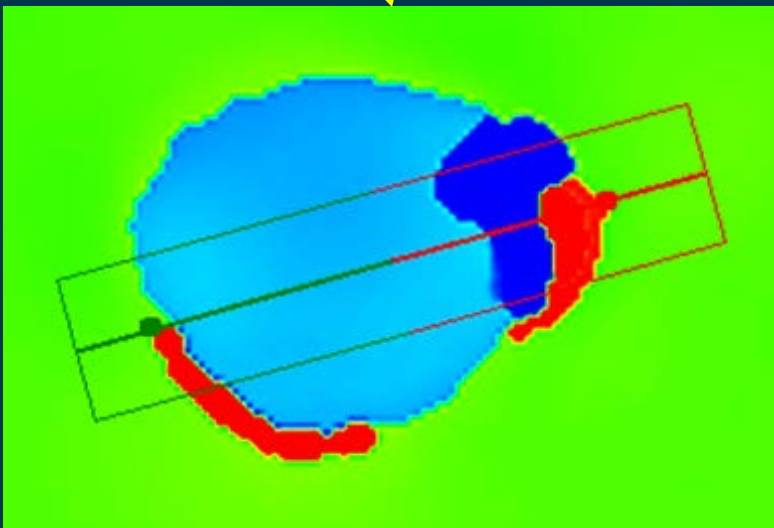
MEMS T1

Cantilever

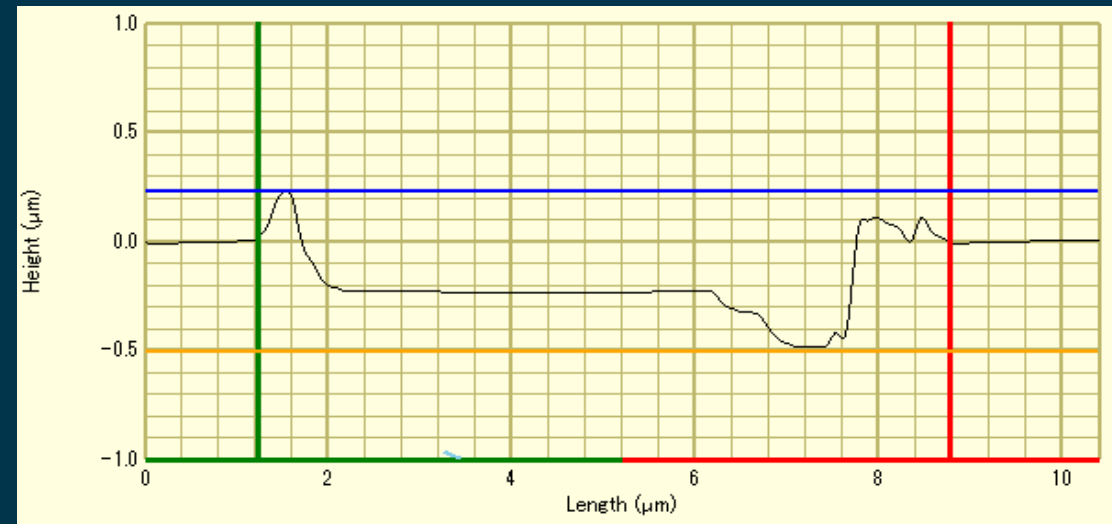


Scrub depth variation

> 400	Red
375 - 400	Orange
350 - 375	Yellow
325 - 350	Light Green
300 - 325	Green
275 - 300	Blue
250 - 275	Dark Blue
225 - 250	Black

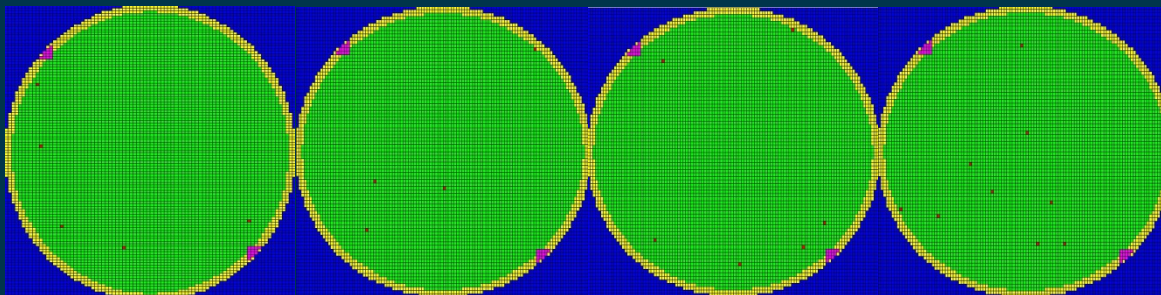
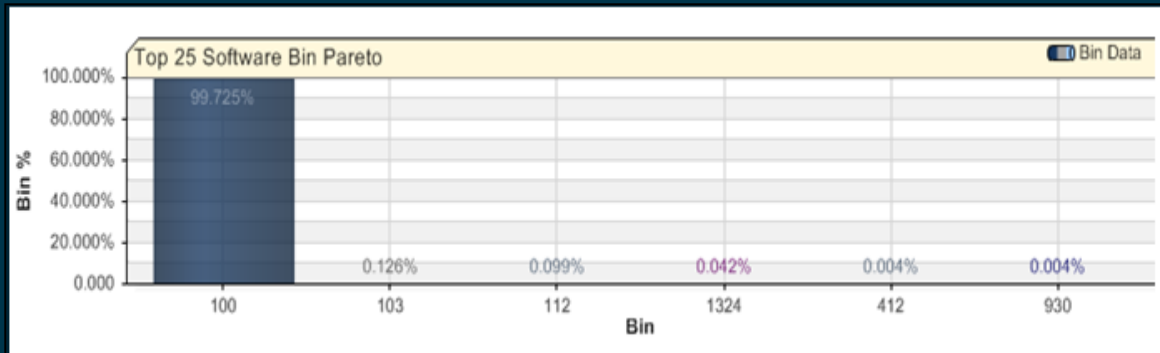
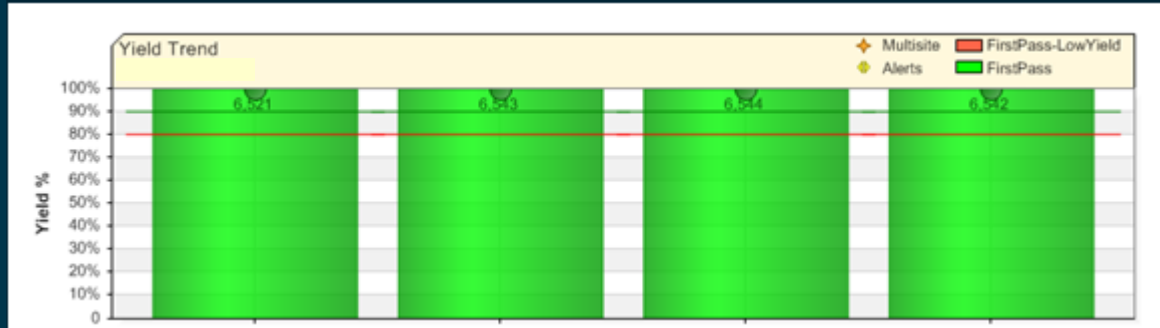


Scrub profiling

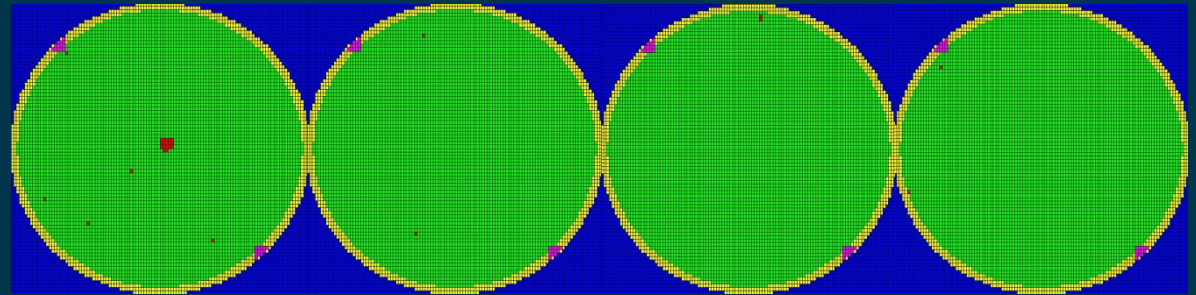
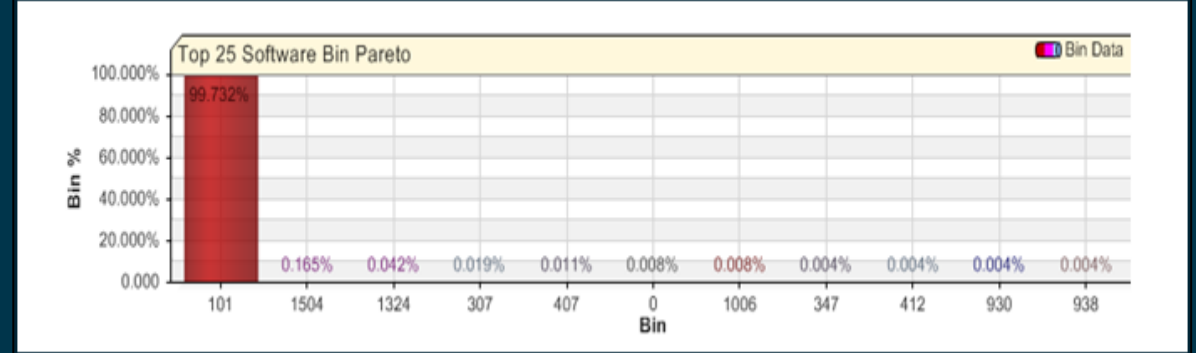
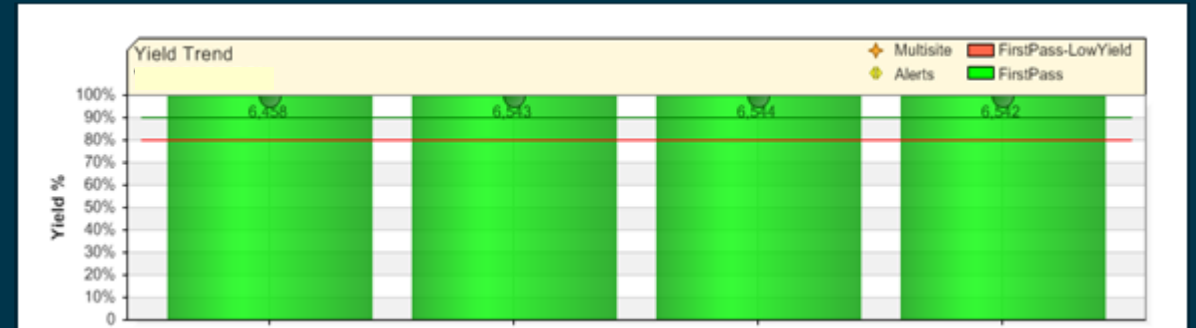


# Initial Functional Test Results

WITHOUT WL $\mu$ BI



WITH WL $\mu$ BI



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# Conclusions

- **WL $\mu$ BI system-level approach at 175 °C shows good performance in terms of yield with limited effect on supply chain lead time**
- **Wafers processed with WL $\mu$ BI have normal results in next probing step**
- **Parametric analysis highlighted no impact from WL $\mu$ BI**
- **Concept qualified for future products**



# Future Work


- **Observe the effect of probe card aging (in progress)**
- **Increase the temperature to reduce the test time**
- **Stepping optimization**
- **Probe card temperature control**

# Acknowledgements

**We would like to thank the following people for their support and input:**

- |                       |                 |                        |             |
|-----------------------|-----------------|------------------------|-------------|
| • Torsten Winkler     | Accretech       | • Jurgen Deketelaere   | Melexis     |
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| • Anneleen Claesen    | Melexis         | • Lindsey Ameele       | Melexis     |
| • Arnaud Devos        | Melexis         | • Marc Biron           | Melexis     |
| • Benoit Degroise     | Melexis         | • Morgan Obeissart     | Melexis     |
| • Davy Fieu           | Melexis         | • Peter Schops         | Melexis     |
| • Filip Beyens        | Melexis         | • Alessandro Antonioli | TechnoProbe |
| • Frederic Plancke    | Melexis         | • Haris Mesinovic      | TechnoProbe |
| • Gilles Cruchot      | Melexis         | • Matteo Meroni        | TechnoProbe |
| • Julien Throckmorton | Melexis         | • Raffaele Vallauri    | TechnoProbe |

# Thank You



***Wafer Level  $\mu$  Burn In is not the Holy Grail.  
It is a solution to extend test coverage when no  
other solution can be implemented.***