SW Test Workshop
Semiconductor Wafer Test Workshop

KGD – Known Good >POWER< Die
Diced Wafer Test at 7 kV and 1000 A

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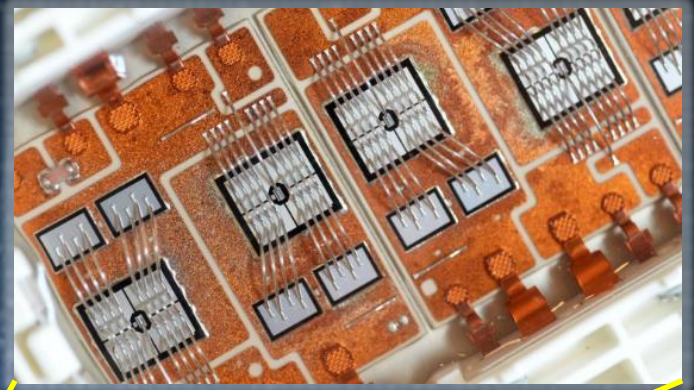
Overview

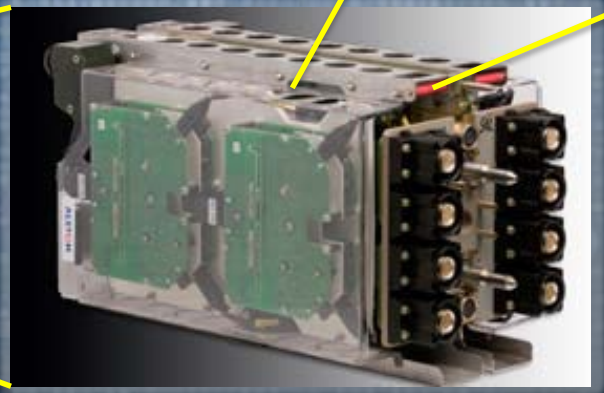
- IGBT Power Modules
- Classical chip test versus "KGD"?
- Challenges: Electric - Physics –Thermal
- Electrical Power Tests
- Chip Handling
- KGD Contactor
- Integration into a System and Challenges
- KGD "Turnkey" Test Cell
- Summary

IGBT Power Modules

High Speed Train (here: Alstom AGV)

IGBT and Diode chips mounted into a single power module (typically up to 32 chips)

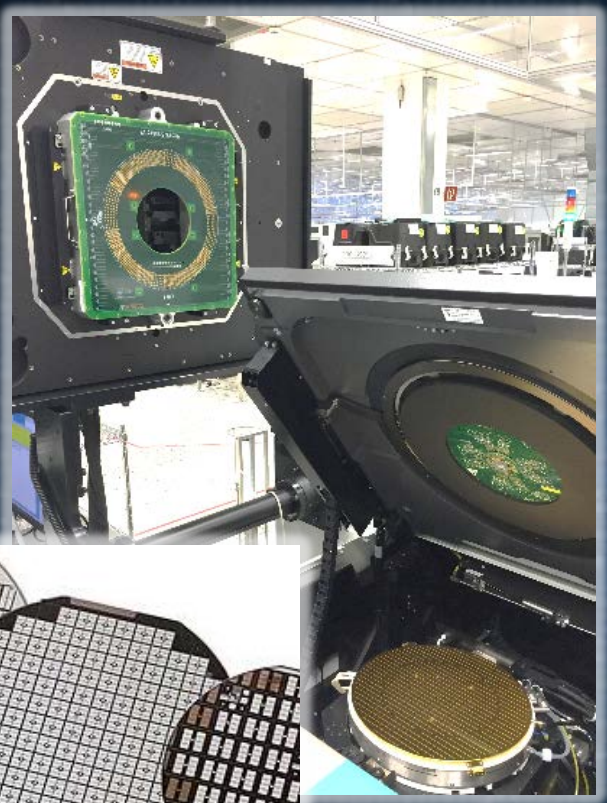


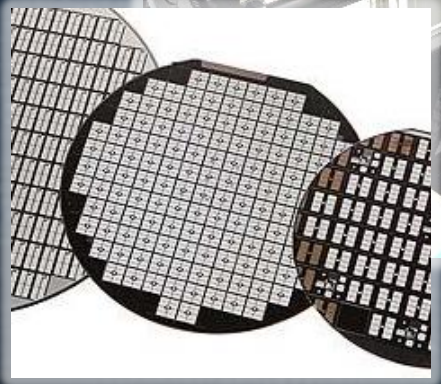


IGBT Power Module, 6.5 kV – 1500 A

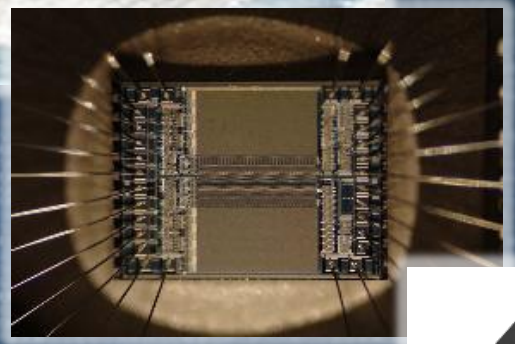
photo courtesy: Alstom

"Classical" Semiconductor Assembly and Test Process



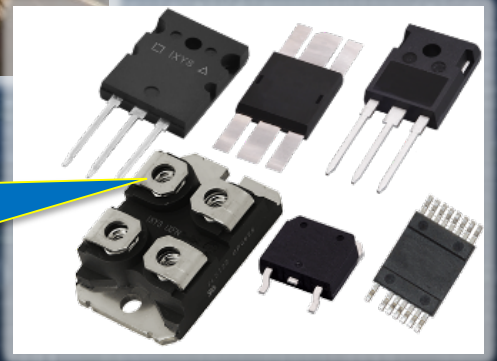


dicing...



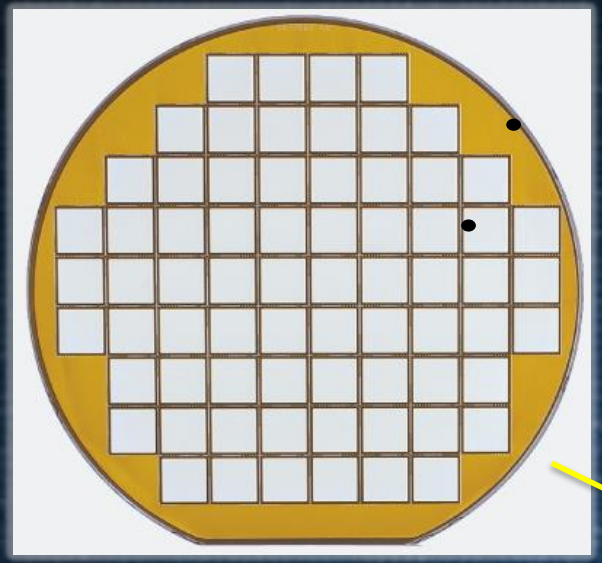
...assembly

typically
single die
or 2 dies

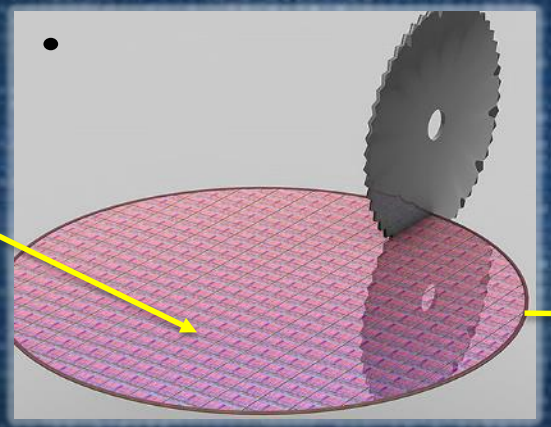


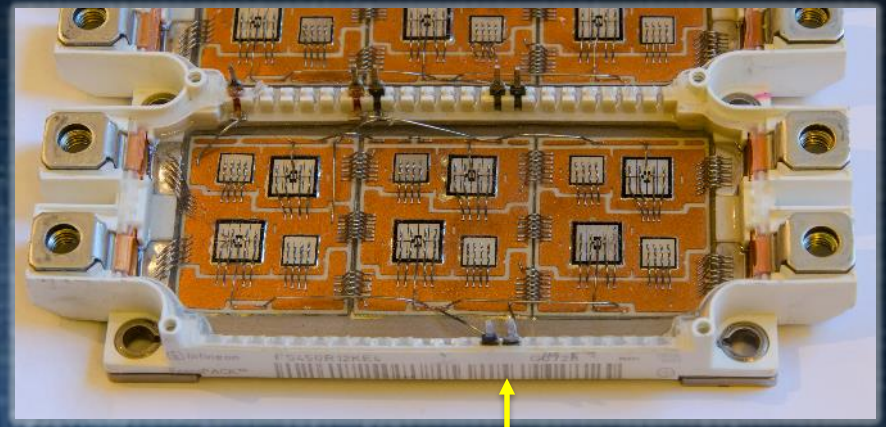
Wafer Sort on Prober... **....Dicing, Assembly....** **...Packaged Device Test**

Modules Yield...it's all about Statistics



Wafer tested



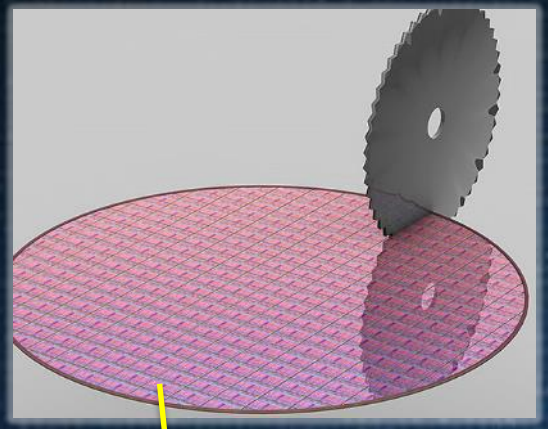


?

Cutting damage,
Dicing yield

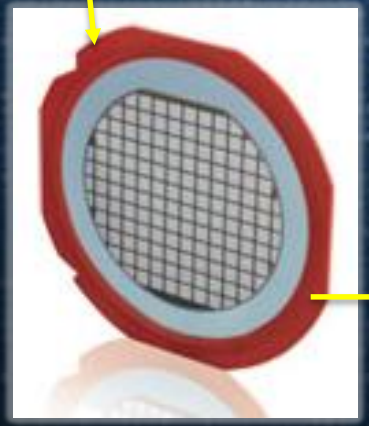
dicing process yield	single package yield	12x module combined yield	32x module combined yield
99%	99%	89%	72%
98%	98%	78%	52%
90%	90%	28%	3%

"Known Good Die" - Concept

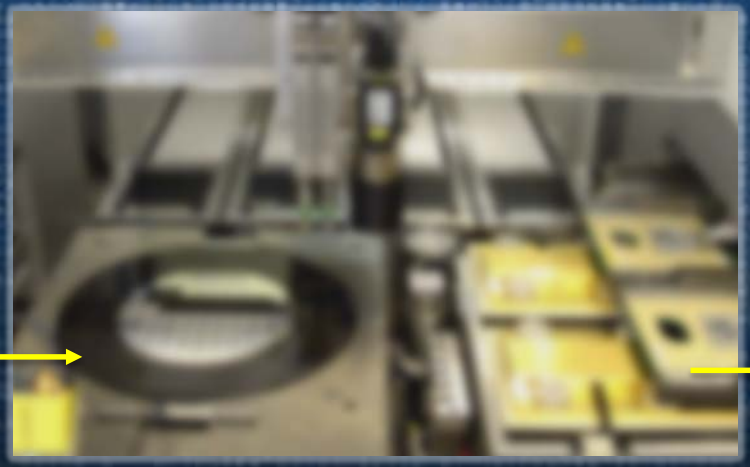


Dicing

?

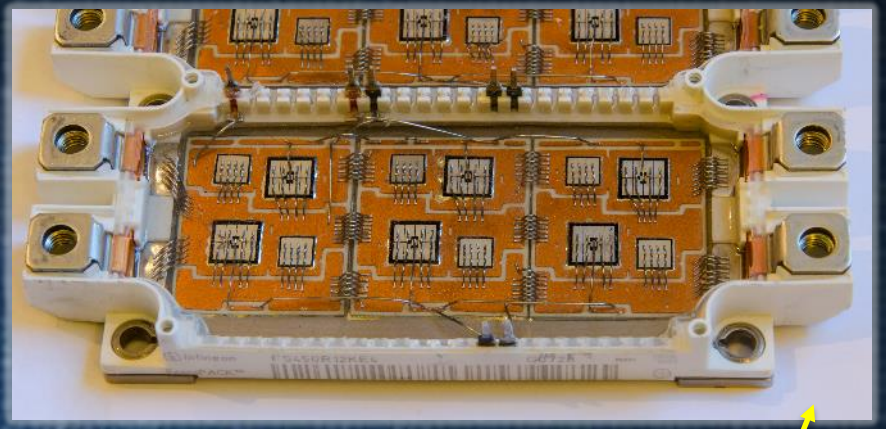


Diced Wafer
on Film Frame



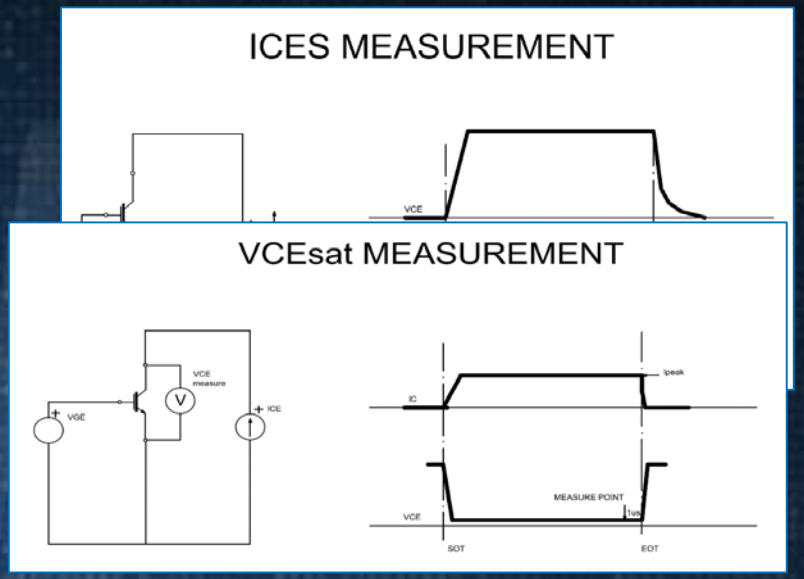
KGD Test - Singulated Chips

Module Assembly – with
Known Good Dies !



"Power" Die – Electrical Tests

2 main test regimes: Static and Dynamic Tests



– **<u>Static Tests (DC)</u> :** device steady state parameters verification (no large power dissipation in D.U.T.)

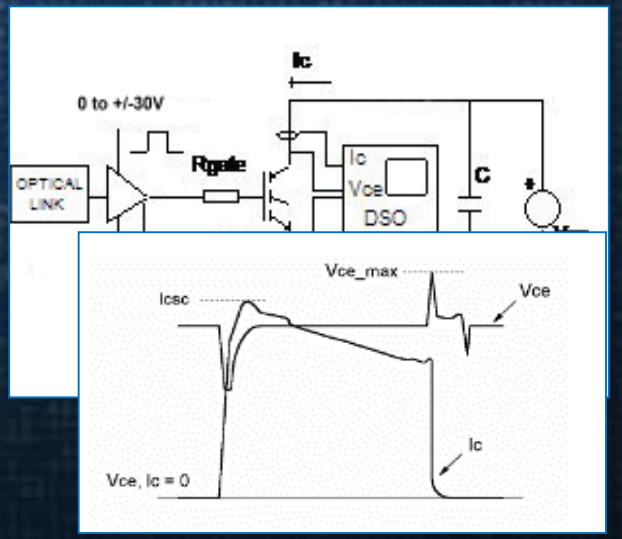
examples:

- High voltage leakage test ...up to **10 kV – but just a few mA**
- Vcesat, Rdson (high current test) ...**up to 200 A – but just a few V**
- Vgeth (gate threshold test)

– **<u>Dynamic Tests (AC)</u>**: device switching parameters verification large power dissipation in D.U.T, both high voltage and high current are **present at the same time)**

examples:

- double pulse test: switching losses of IGBT, diode recovery
- avalanche test: dissipation of breakthrough energy into DUT
- short circuit withstanding test: highest current – **1000+ A**!



Dynamic Test - Example

Unclamped Inductive Switching - **UIS** or **Avalanche** Test

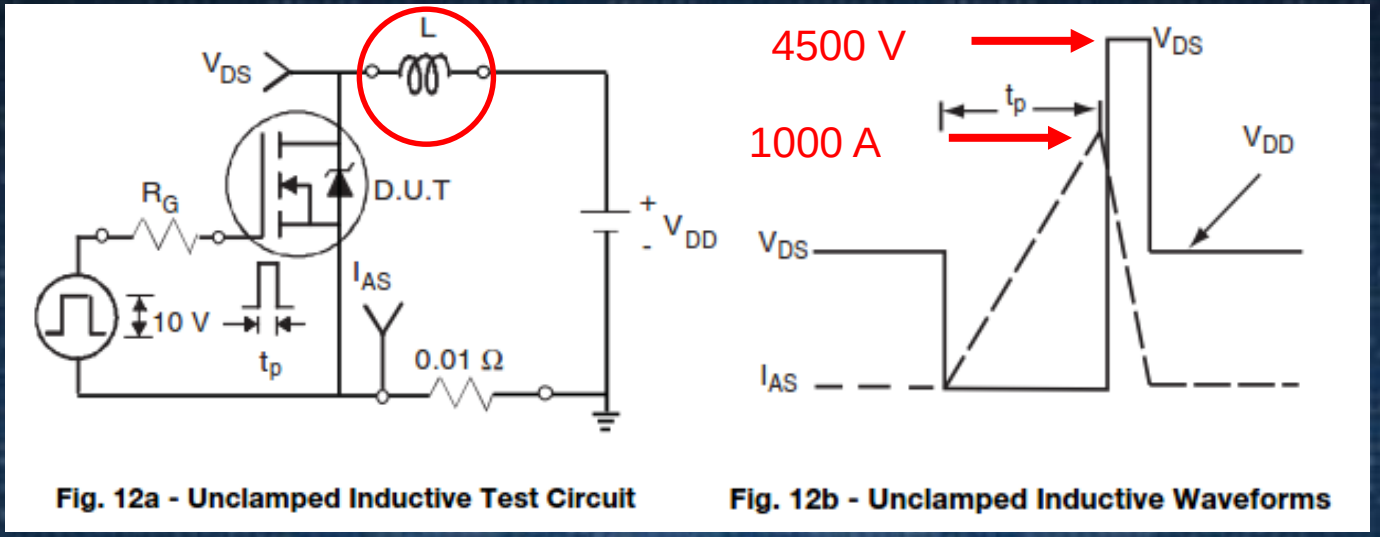


Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

from Vishay data sheet

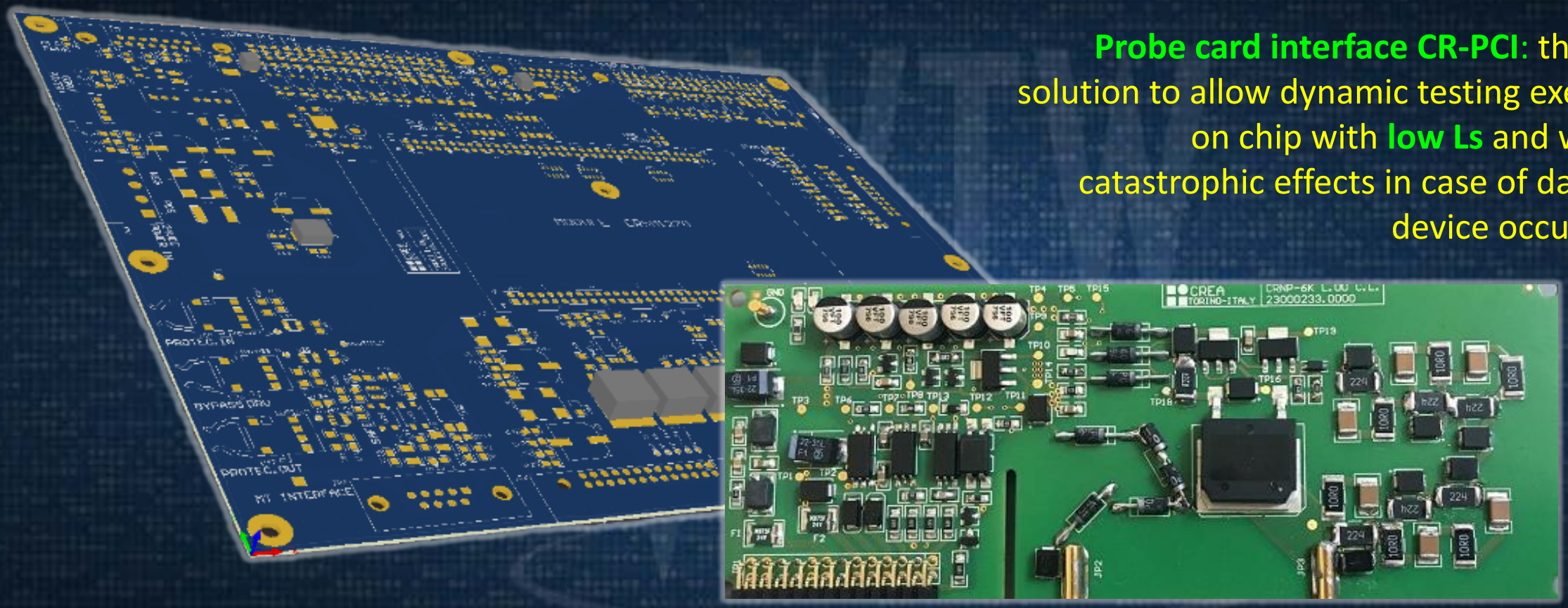
- **Energy** stored in inductor **is dissipated inside D.U.T.** at switch off.....

.... if everithing goes right.

- If things go wrong (DUT shorted): energy **is dissipated elsewhere**, and it IS dissipated (in probes, backside contact...)

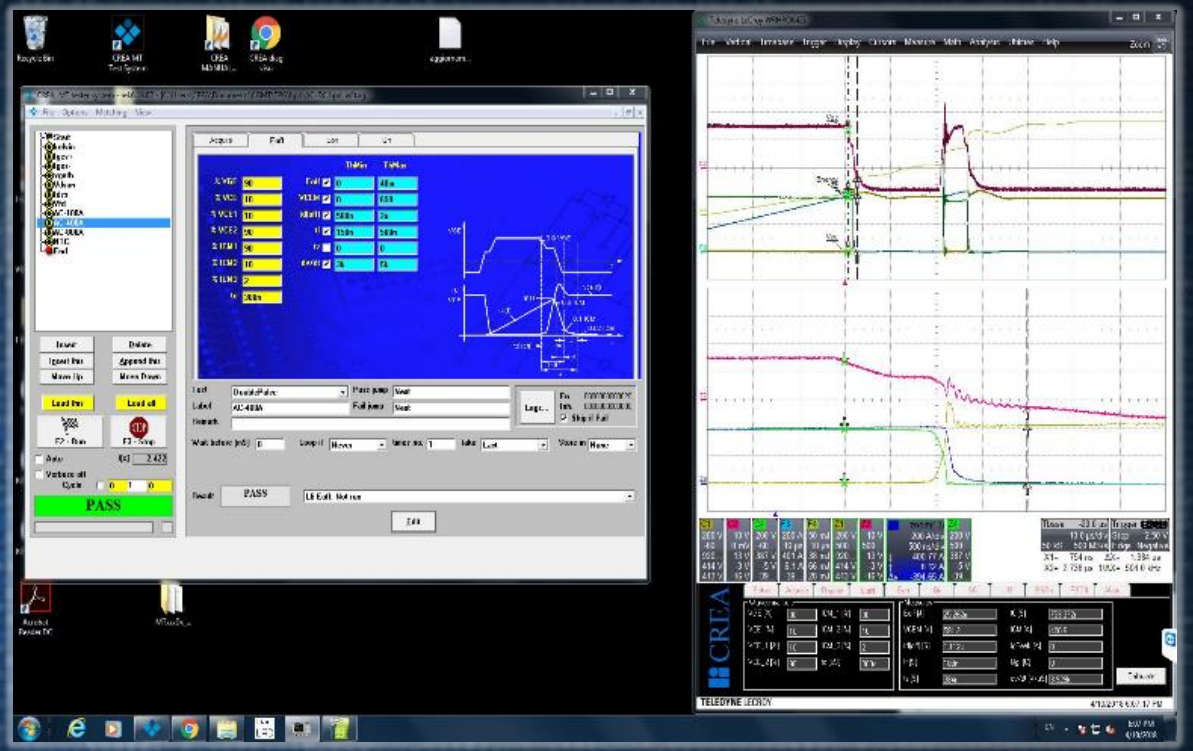
- It's similar to speeding downhill without brakes on:

LOW STRAY INDUCTANCE Technology



Probe card interface CR-PCI: the CREA solution to allow dynamic testing execution on chip with **low Ls** and without catastrophic effects in case of damaged device occurrence.

ATE Cabinet & Test Software



Power DYN generator **4500V/1000A**, max pulse time **1ms**

Floating gate drivers (up to **7KV**): **±30V**

Low output stray inductance design **(<50nH** at the sys bus bar)

Overcurrent protection fast circuitry to prevent system and accessories damage

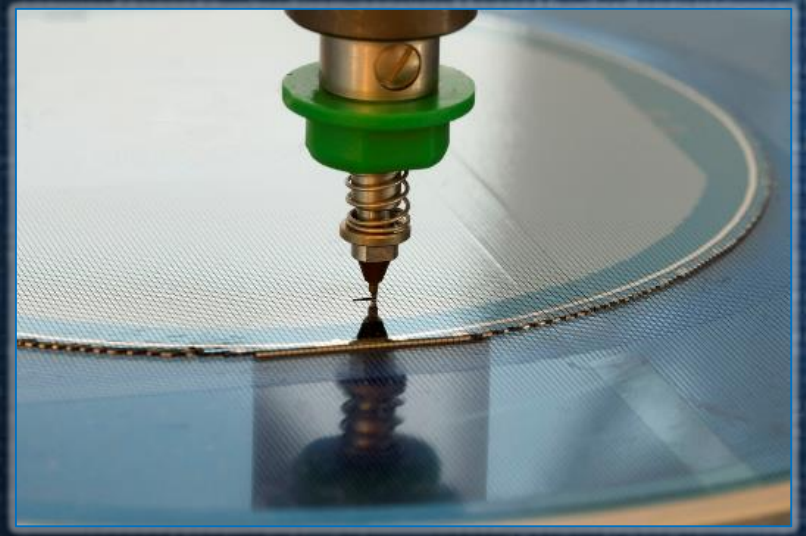
Handler interface: TTL, TCP/IP or GPIB

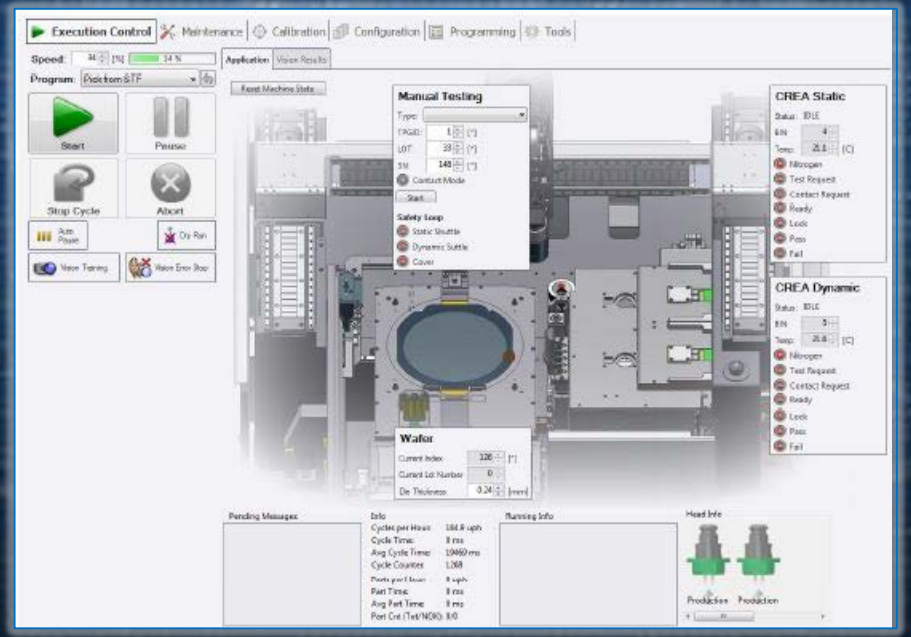
System Screen for AC Turn off measurement, 650V/400 A device

Handling the Chip...

- "Classical" KGD test: handling of diced wafer with **frame prober** - but this doesn't work here...
- High Current flow goes through backside of chip, this can't be supported by a film frame.

-> **dedicated chip handler** with contactor required here!



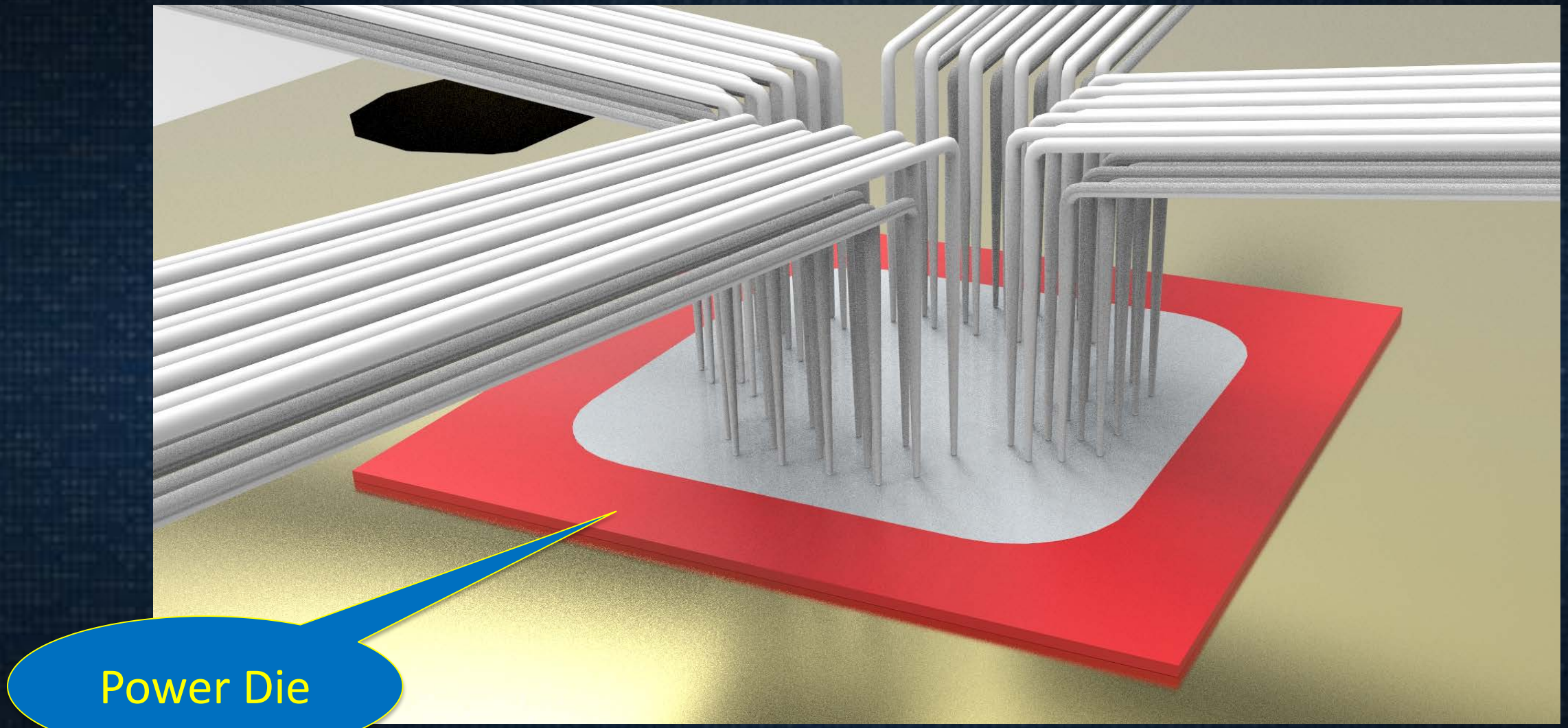


"The Missing Link": Making Contact !

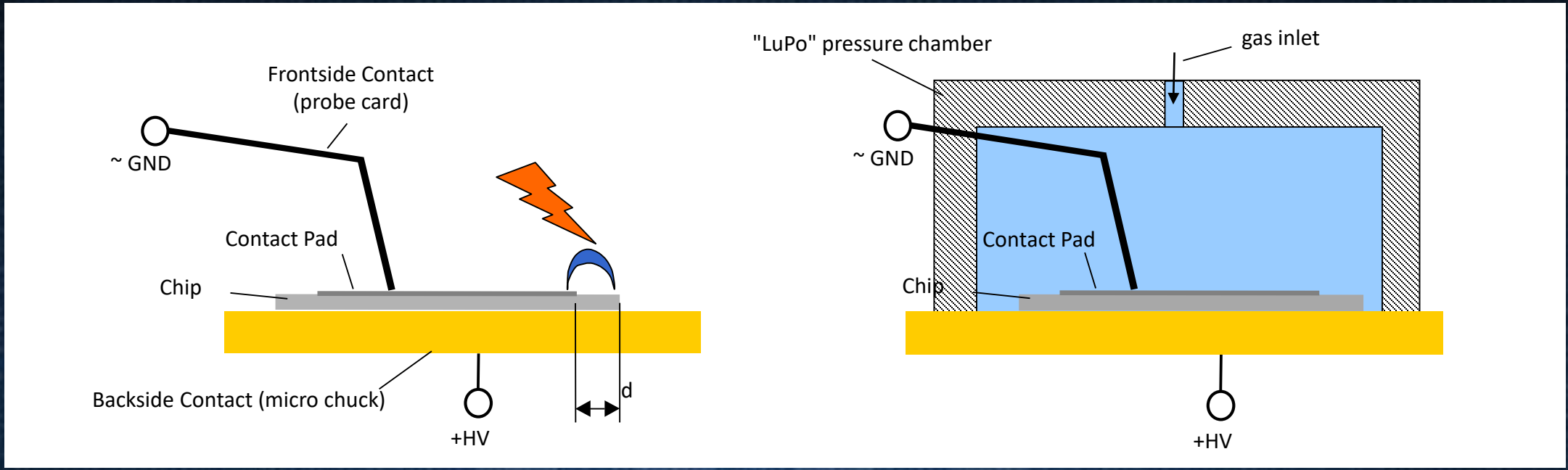
- Requirements for the KGD contactor:
  - High Voltage: up to **10 kV**
  - High Current: up to **1000 A**
  - High Temperature: up to **150 °C** test temperature
  - **Low Inductance solution** for dynamic test

Hmmmm...

Making Contact...



Contacting the Chip: High Voltage !

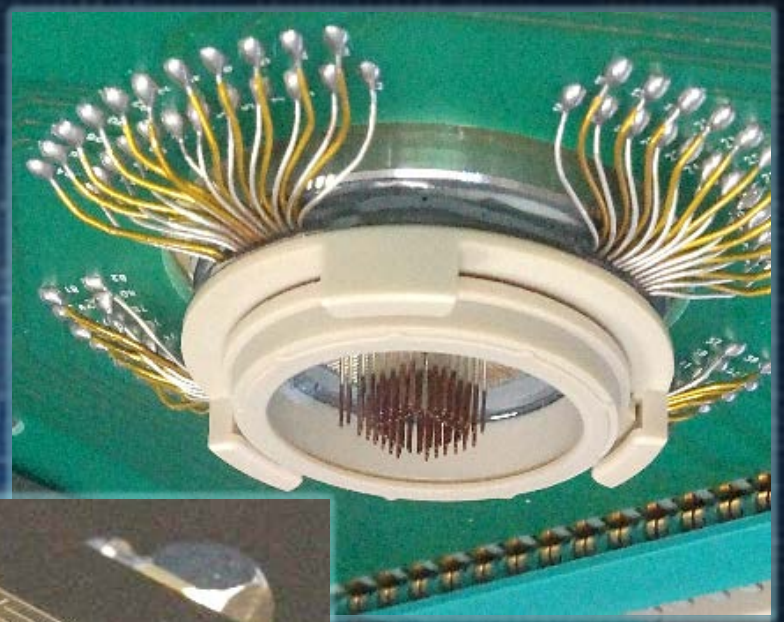


- **Bare chip:** electrical field strength across the "termination area" exceeds breakthrough field strength...
- ...and if tested at ambient atmosphere: **Arcing !**
- **"LuPo" pressure chamber** employed to create compressed air atmosphere making use of "Paschen Law" from gas discharge physics – **arcing suppressed!**

Contacting the Chip: High Current !

-> (Pulsed) Currents up to 1000+ A have to be transferred safely into and out of the chip

-> High Precision required for precise electrical test results (Kelvin force/sense contacts)



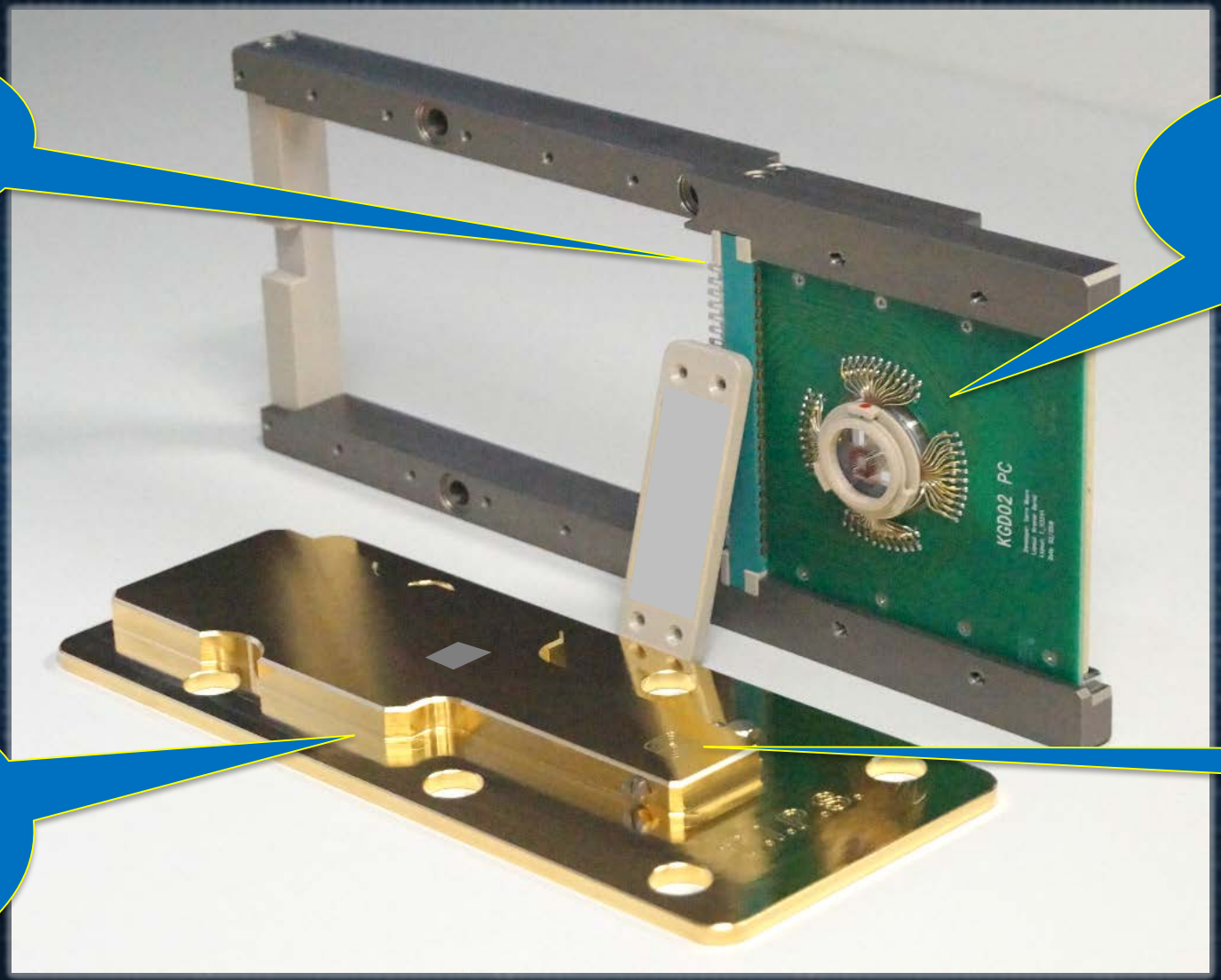
- Frontside Contact
  - Pogos? A nightmare on chip bond pads...
  - Test sockets: ?? handling fragile bare chips...

  -> **Probe Card**!
  - Well established performance for chip front side proven in wafer test.

- Backside Contact
  - fast chip transfer capability
  - very high current capability

  -> **Micro Chuck**!
  - vacuum chip handling
  - backside Kelvin sensing
  - high temperature capable

KGD Chip Contactor



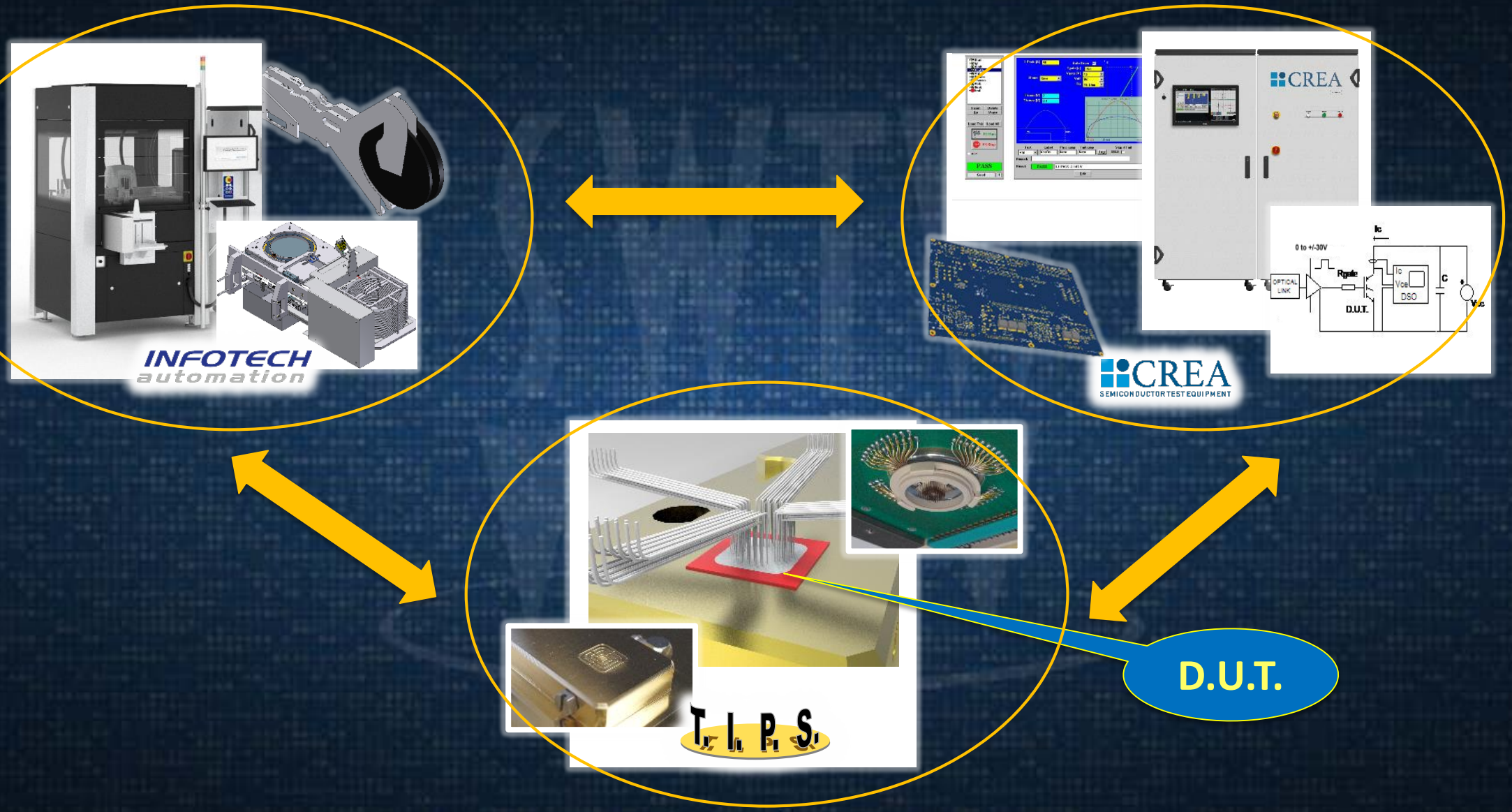
Probe Card holder, edge connector

"LuPo" Probe Card, low inductance design

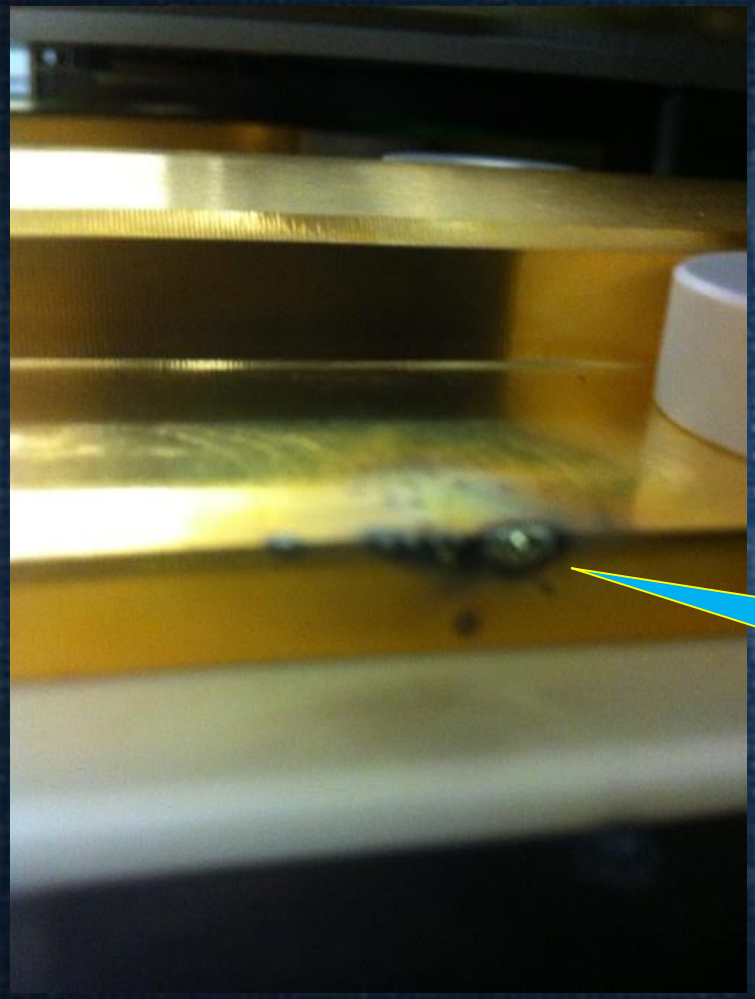
Micro Chuck, up to 10 kV, to be mounted on heater – 150 °C

Chip test location

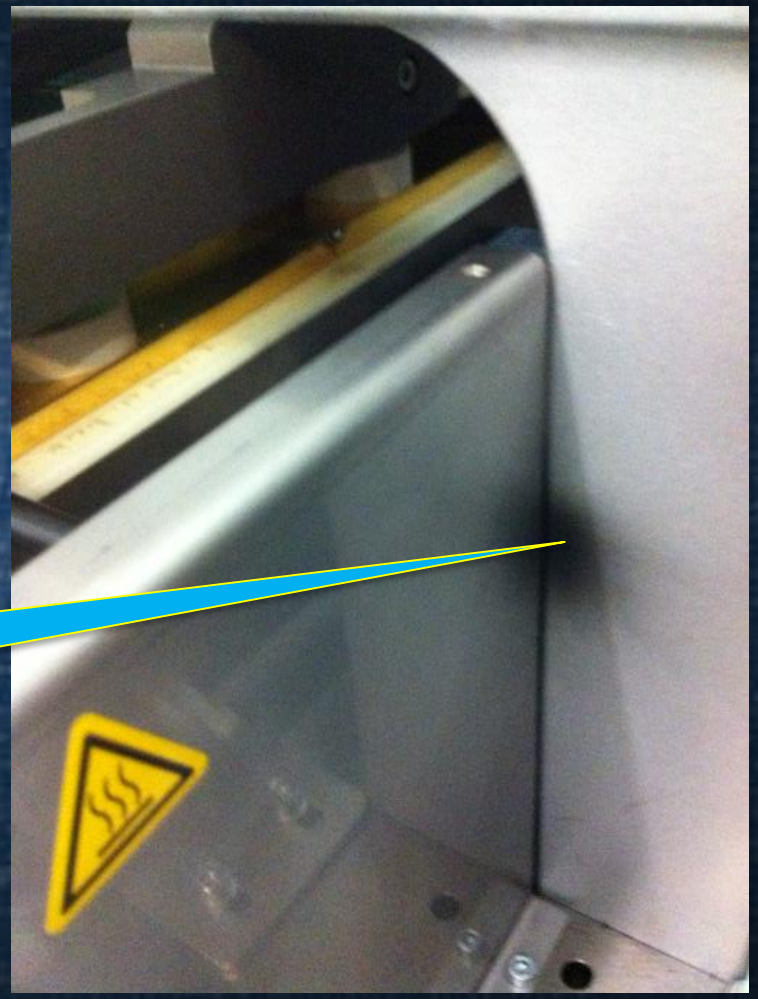
Integration into a System



Integration went smooth...

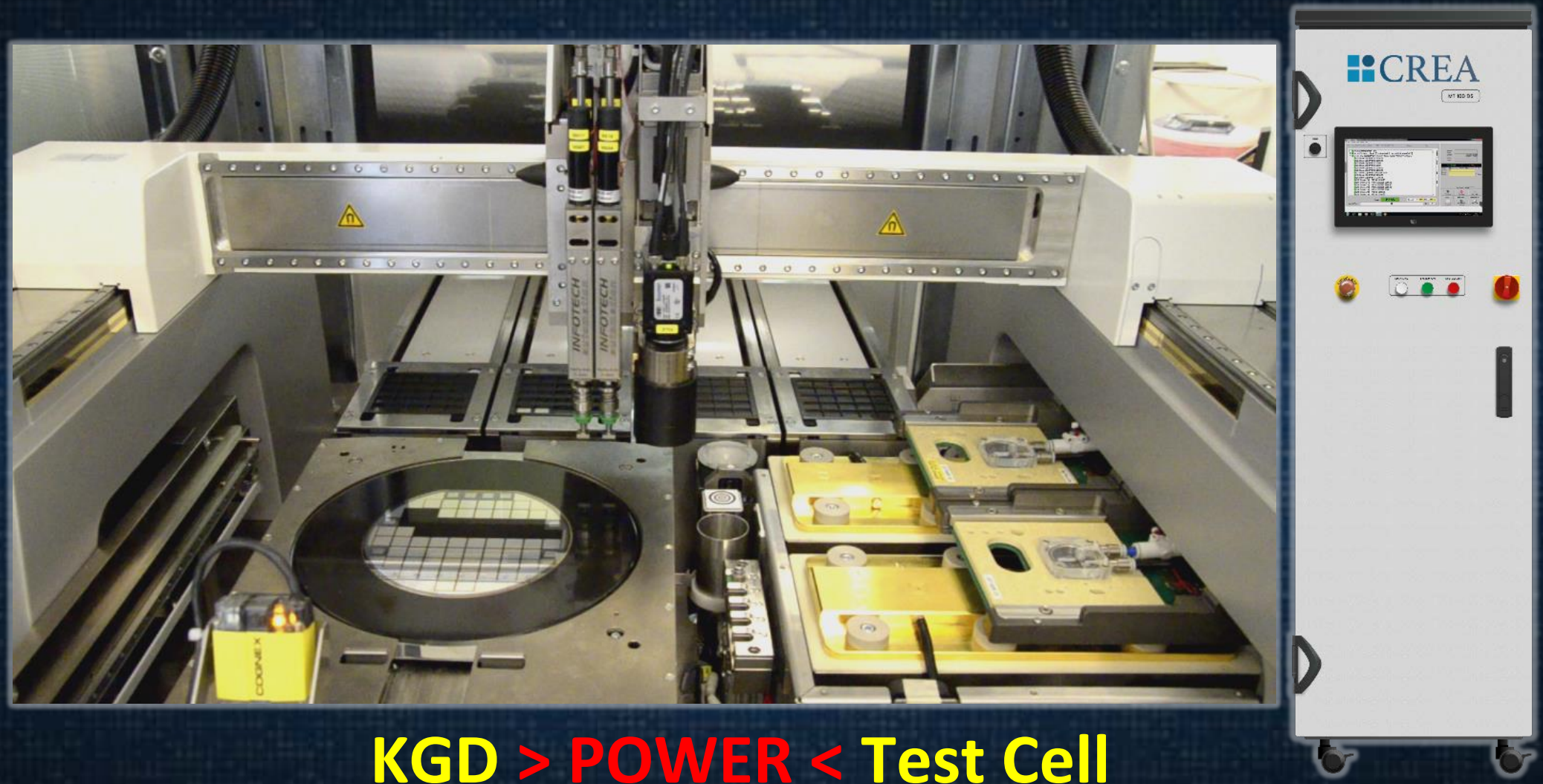


Arcing Burn Marks from insulation failure!



...mostly...

At the End: What does matter is the Result!



KGD > POWER < Test Cell

Summary

- KGD "Power" test shows its specific challenges from electrical, mechanical and physics point of view
- 3 individual companies - each deeply specialized in their field - have successfully created a turnkey solution
- end customer has been relieved of headaches for integration, finding the right sub-suppliers...
- State-of-the-Art "KGD Power Test Cell"
- "Limits of Test" – pushed a bit more forward...

Acknowledgements

- our staff at CREA, Infotech and T.I.P.S. Messtechnik
- a customer with confidence in a turnkey solution

THANK YOU!