SW Test Workshop

Semiconductor Wafer Test Workshop

Sub-milliOhm impedances on a thick probe card? No problem!

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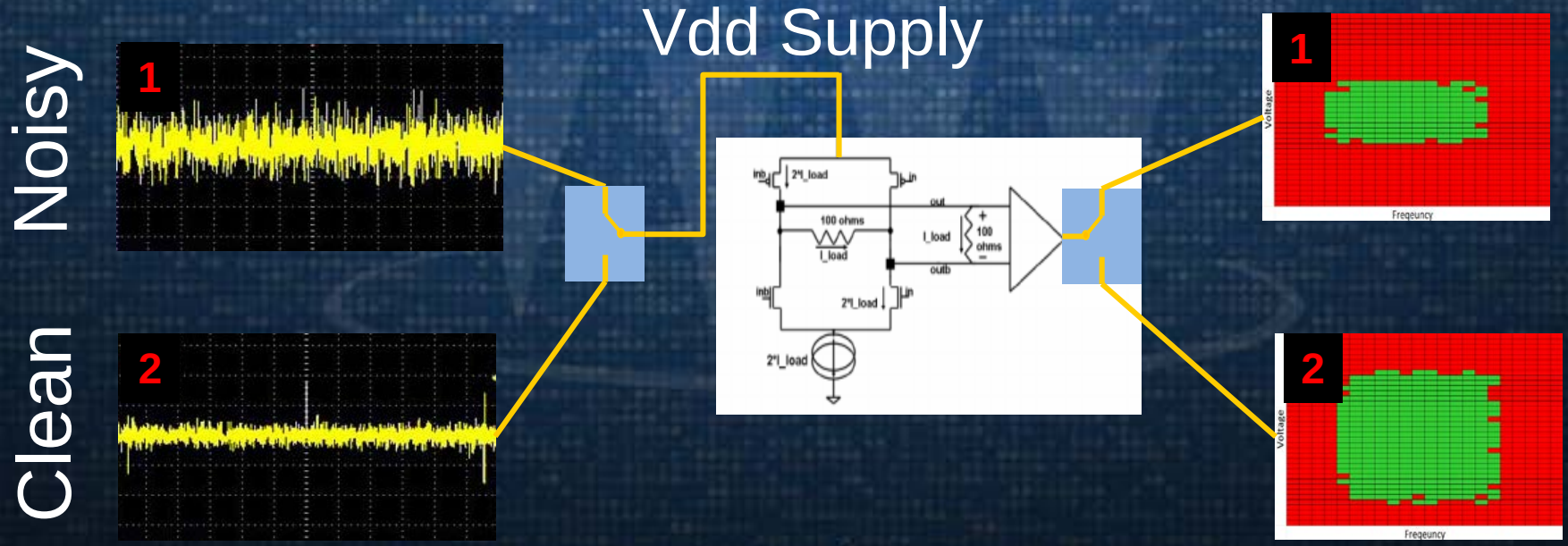
Overview

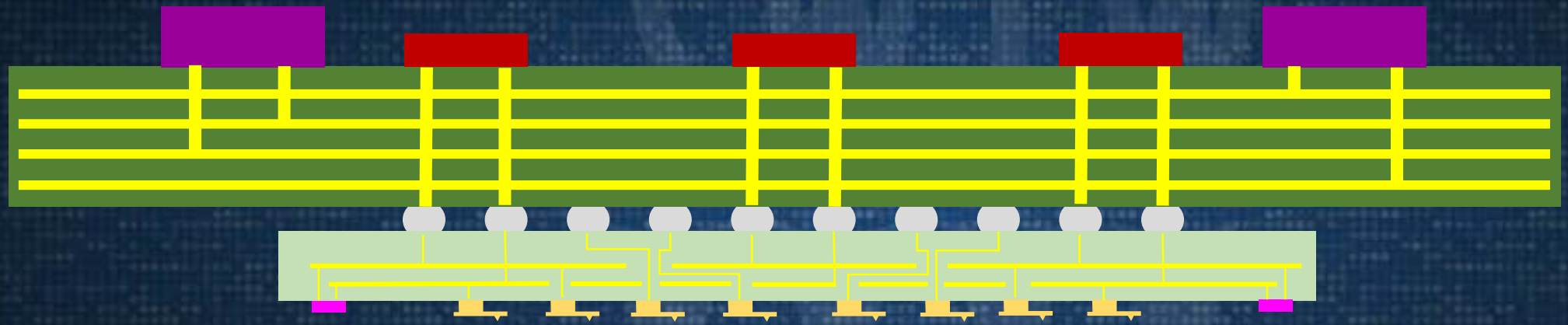
- Power integrity definitions
- Power integrity challenges for probe test
- How to successfully design the PDN
- Summary

Why do we care about Power Integrity?

- PI relates to how the power supply ripples under load. (Both PWR and GND!). PWR+GND = Power Distribution Network (PDN)
- Ripple on the PDN will lead to a yield hit and you may not even be aware of it!

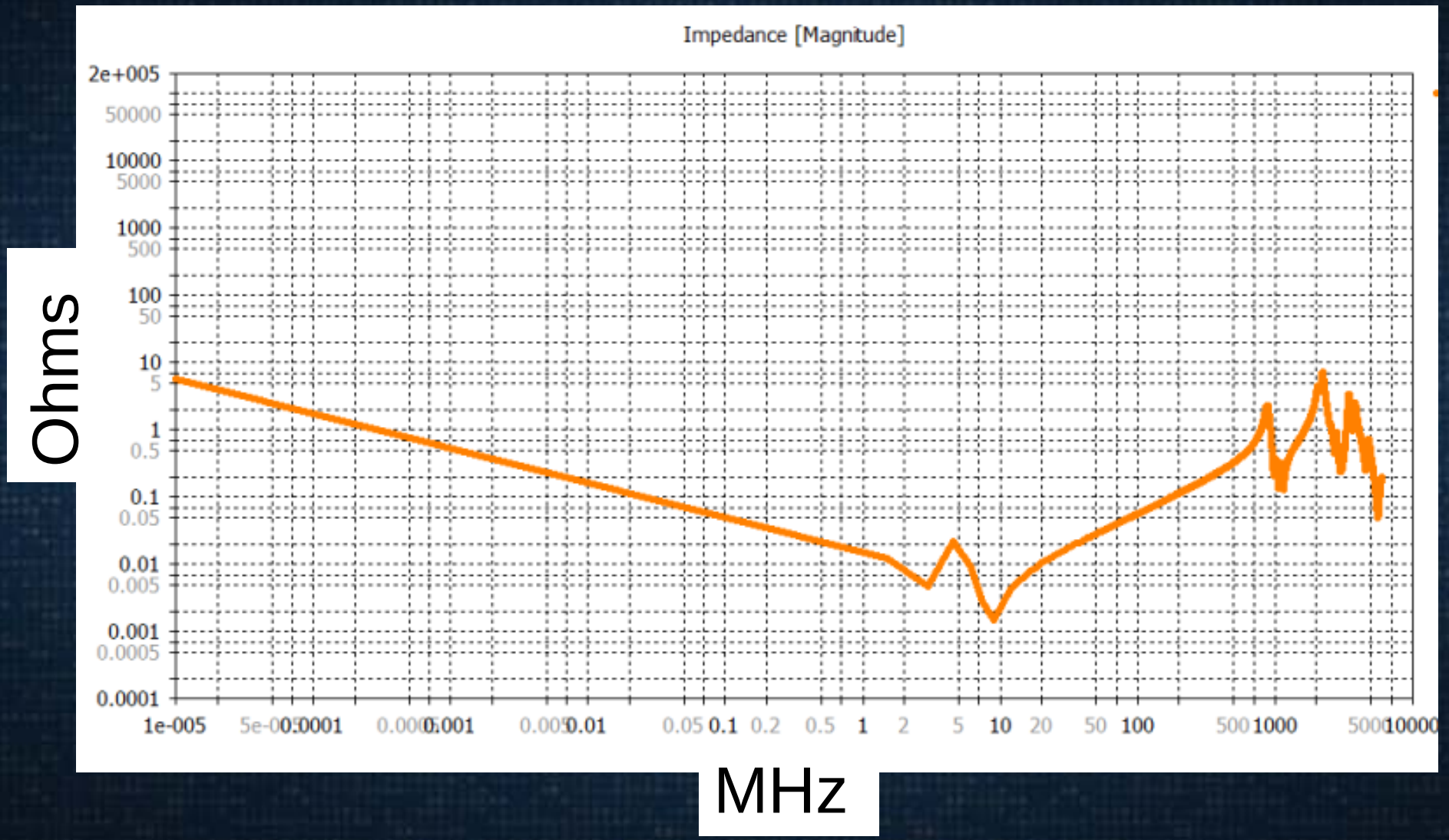


Translating PDN ripple to Design Spec for Probe

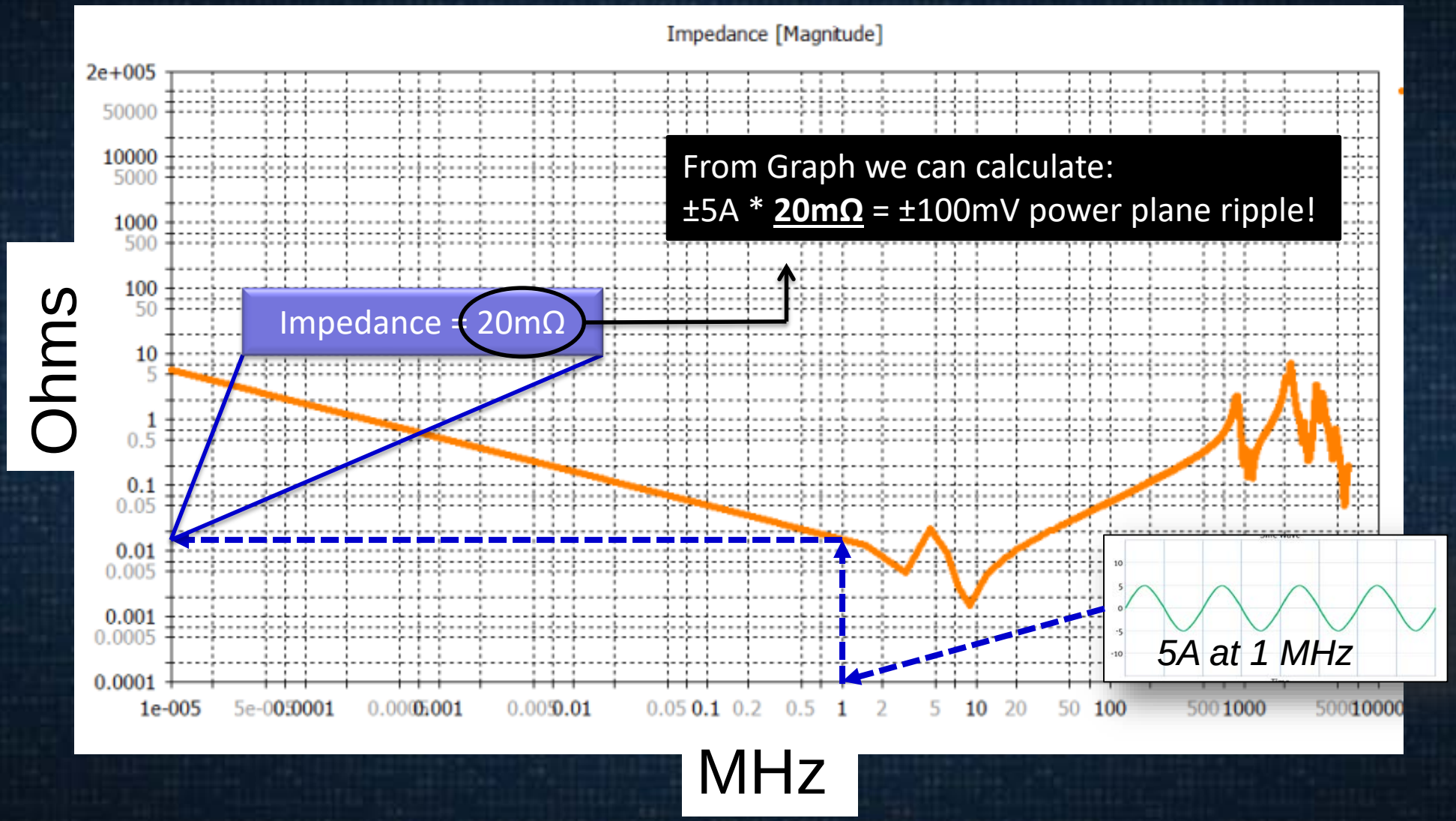


IC Designers / Past experience / Eval board / Simulation used to determine acceptable PDN spec. at probe needles

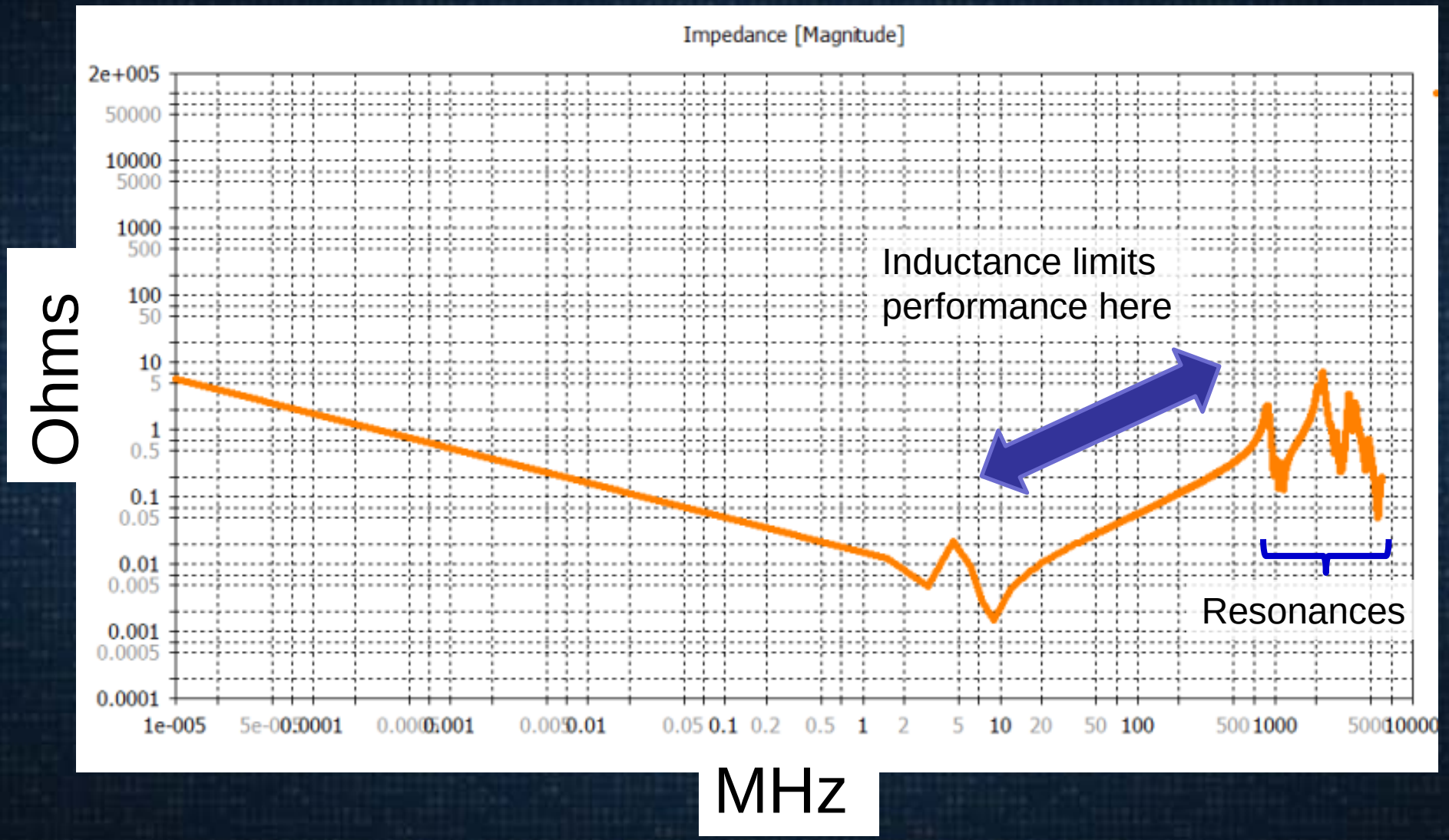
What does the PDN performance look like?



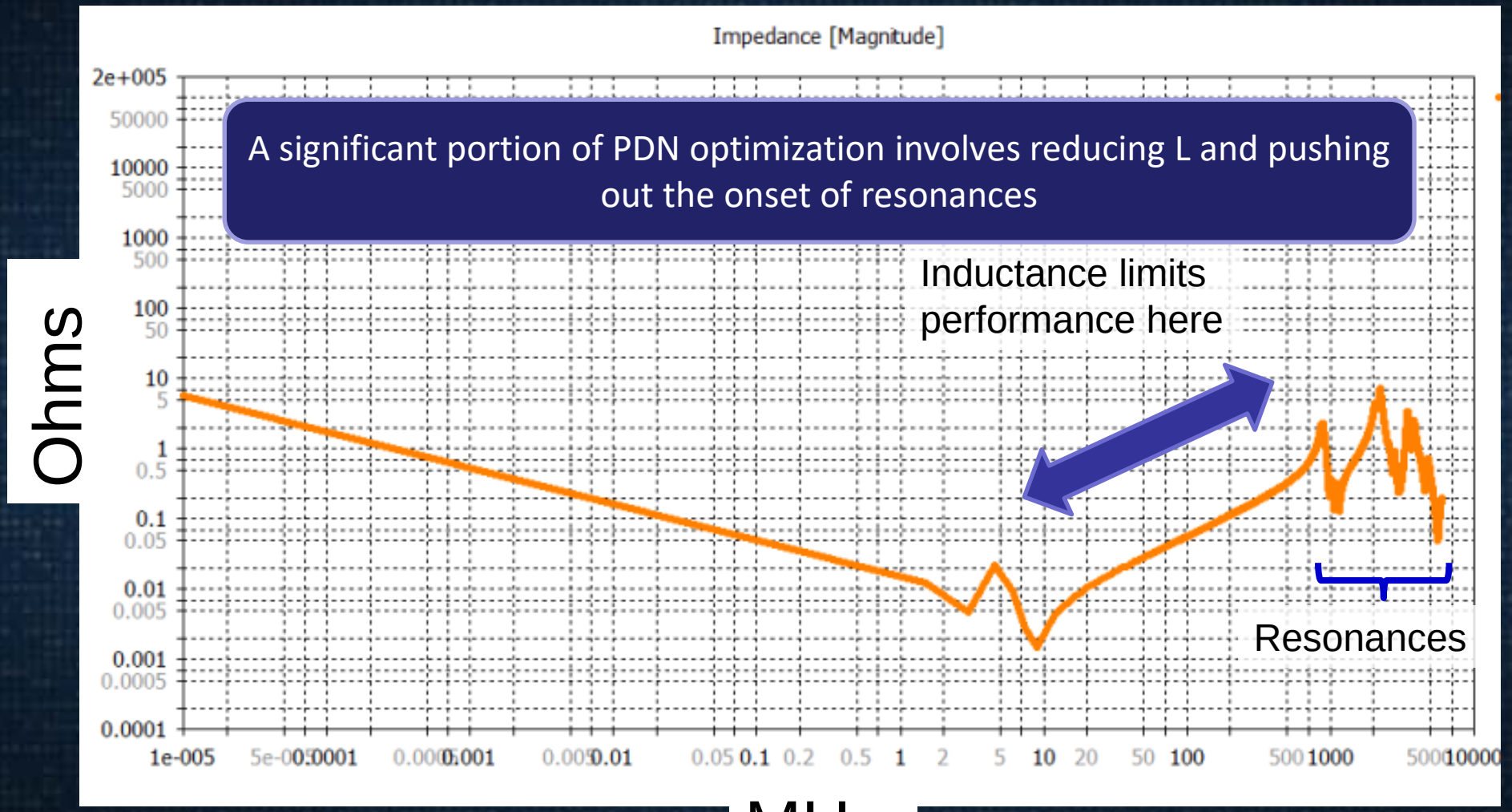
What does this graph mean?



What limits PDN performance?



What limits PDN performance?



Historical Method of meeting PI Spec

To Start:

- Capacitor scheme comes from device app notes for a soldered down device on a thin board

Apply Rules:

- Big caps can be placed anywhere on the board, but should be closer to DUT
- Small capacitors must be placed on back side of DUT
- Power and ground planes should be close together
- Shorter is better

And if it fails:

- Add more capacitors!
- Hold meetings and come up with wild guesses at what may be causing the problem!

Historical Method of meeting PI Spec

To Start:

- Capacitor scheme comes from device app notes for a soldered … thin board

Apply Rules:

- Big caps can be placed anywhere …
- Small capacitors must be …
- Power and grou…
- Shorter …

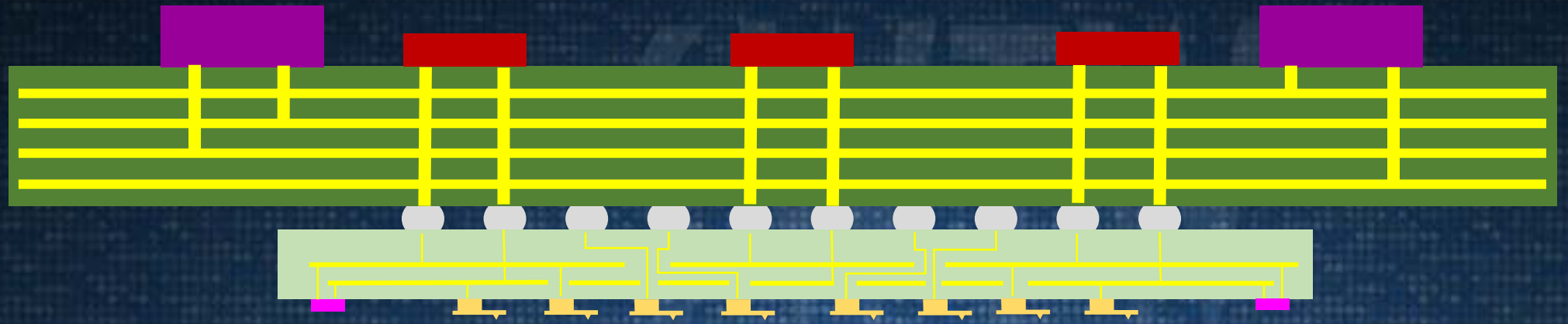
And if it fa…

- Add mor… …rs!
- Hold meetings and come up with wild guesses at what may be causing the problem!

DOESN'T WORK ANYMORE!

Probe Card PI Challenges

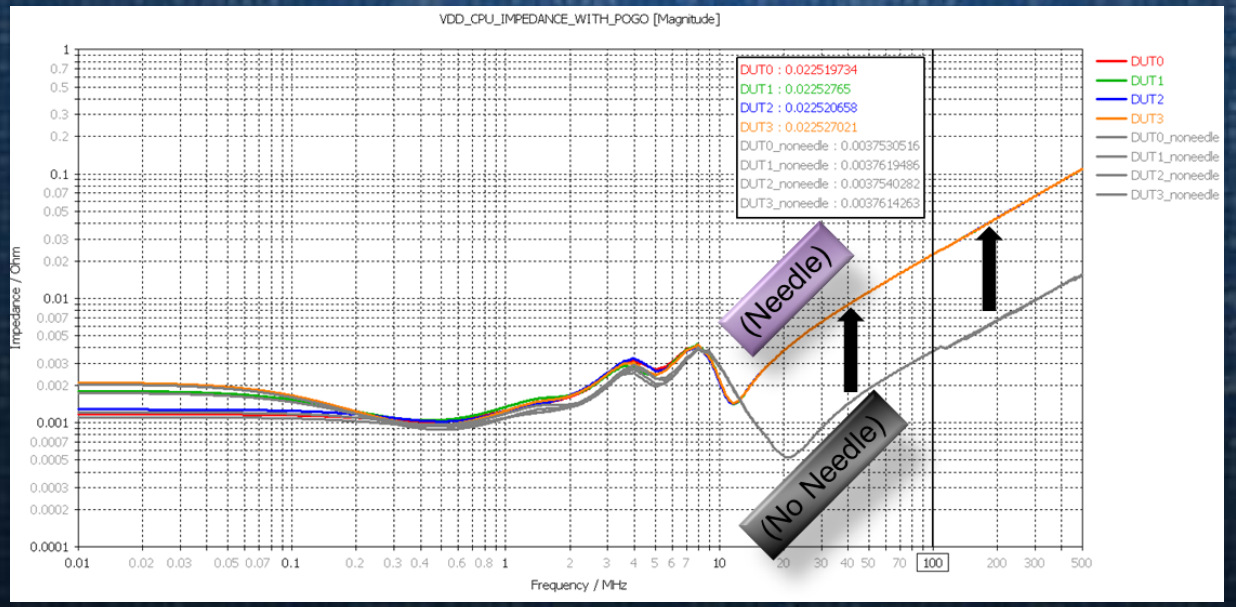
Probe Card PI Challenges: Probe Performance



Probe card

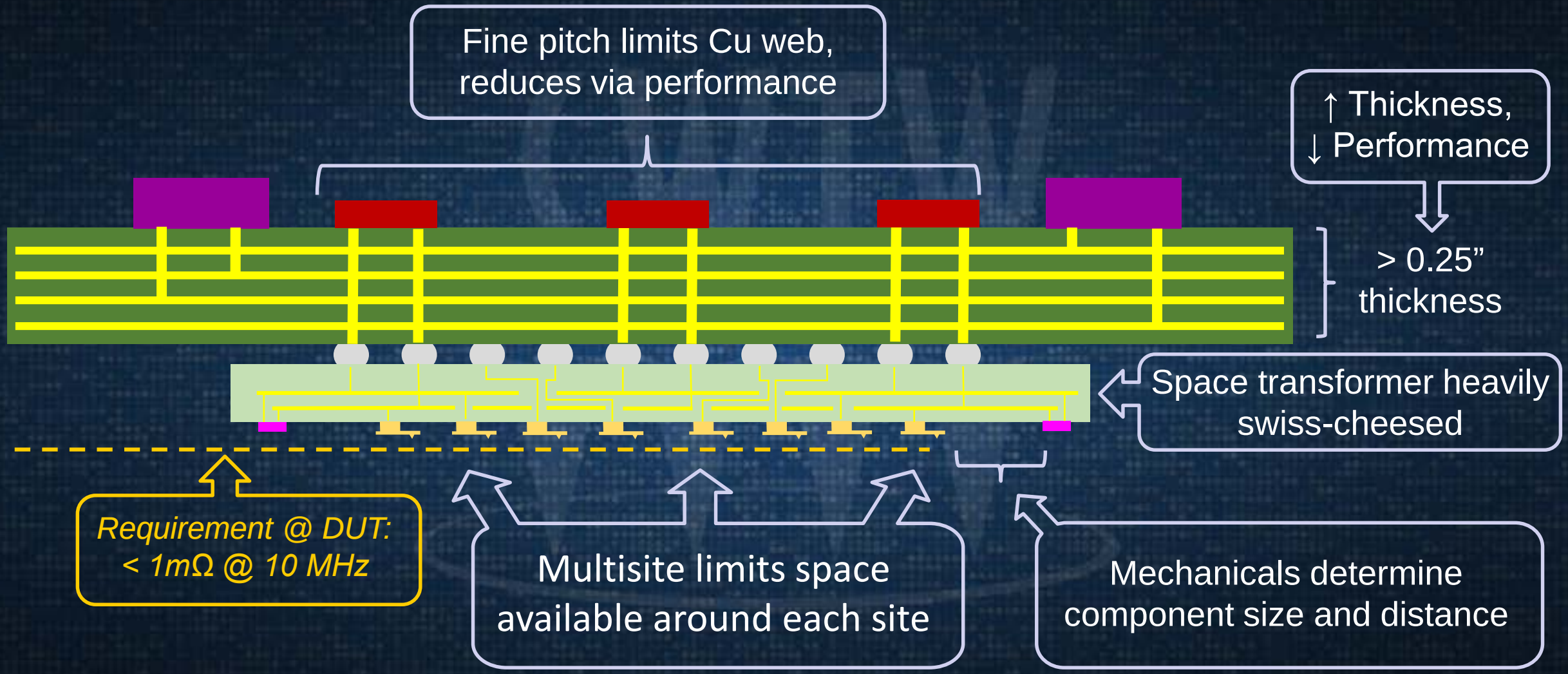
Space translator
MLC/MLO

Probes

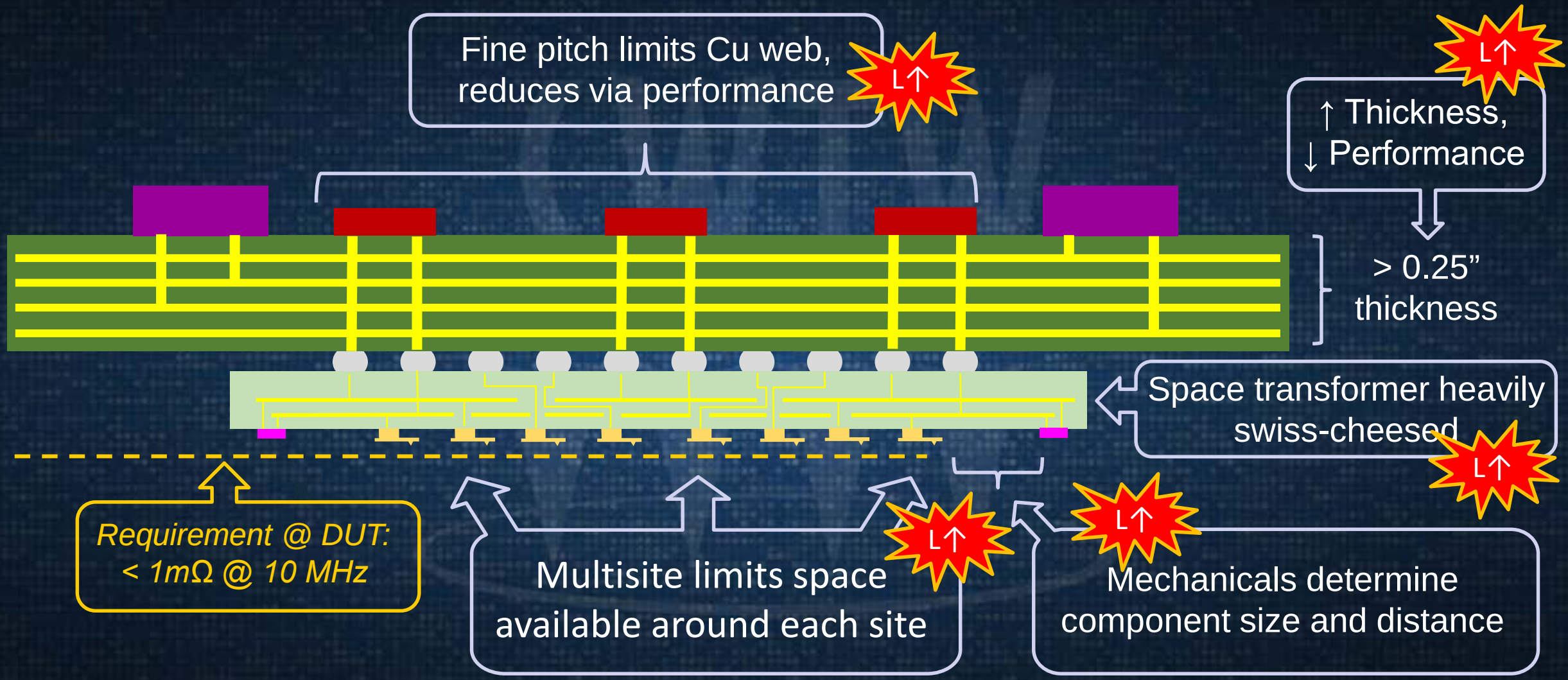


~ 1 order of magnitude increase in Z

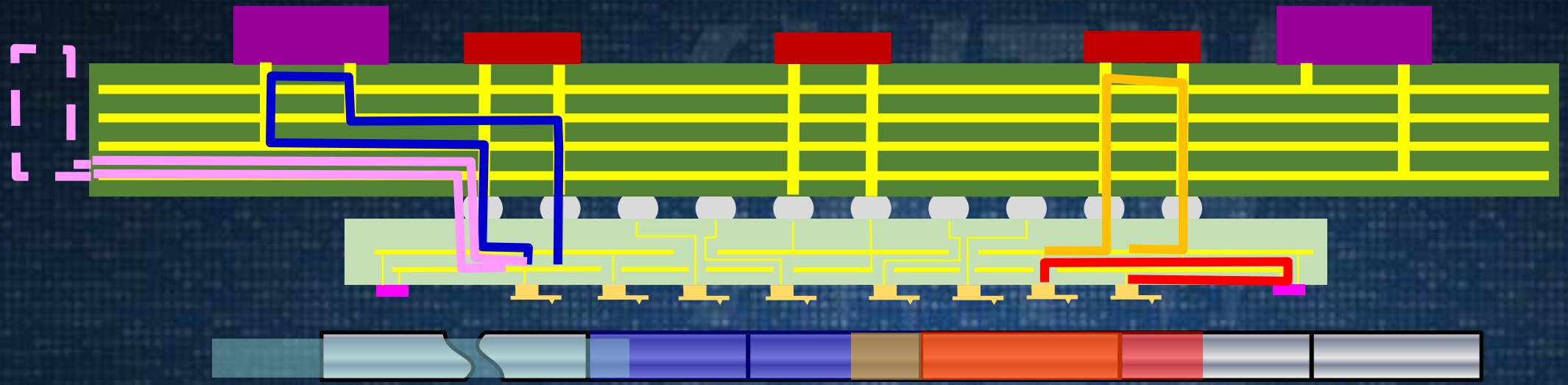
Probe Card PI Challenges: More than probe needle



Probe Card PI Challenges: More than probe needle



Probe Card PI Challenges: Cap Performance



Probe card

Space translator
MLC/MLO

Probes

DC 10kHz 100kHz 1MHz 10MHz 100MHz

Power Supply

Bulk Caps (10 kHz – 1 MHz)

Mid Tier (500 kHz – 10 MHz)

HF Caps (1 MHz – 25 MHz)

Bandwidth limited
due to vias and web

Designing a PDN to meet the PI Challenge of Probe Test

Successful PDN Design

Design Side

Good design practices
Quality simulation tools
Optimized simulation strategies
Measurement correlation

Fabrication Side

Fab design rules
Fab technologies
Manufacturing robustness

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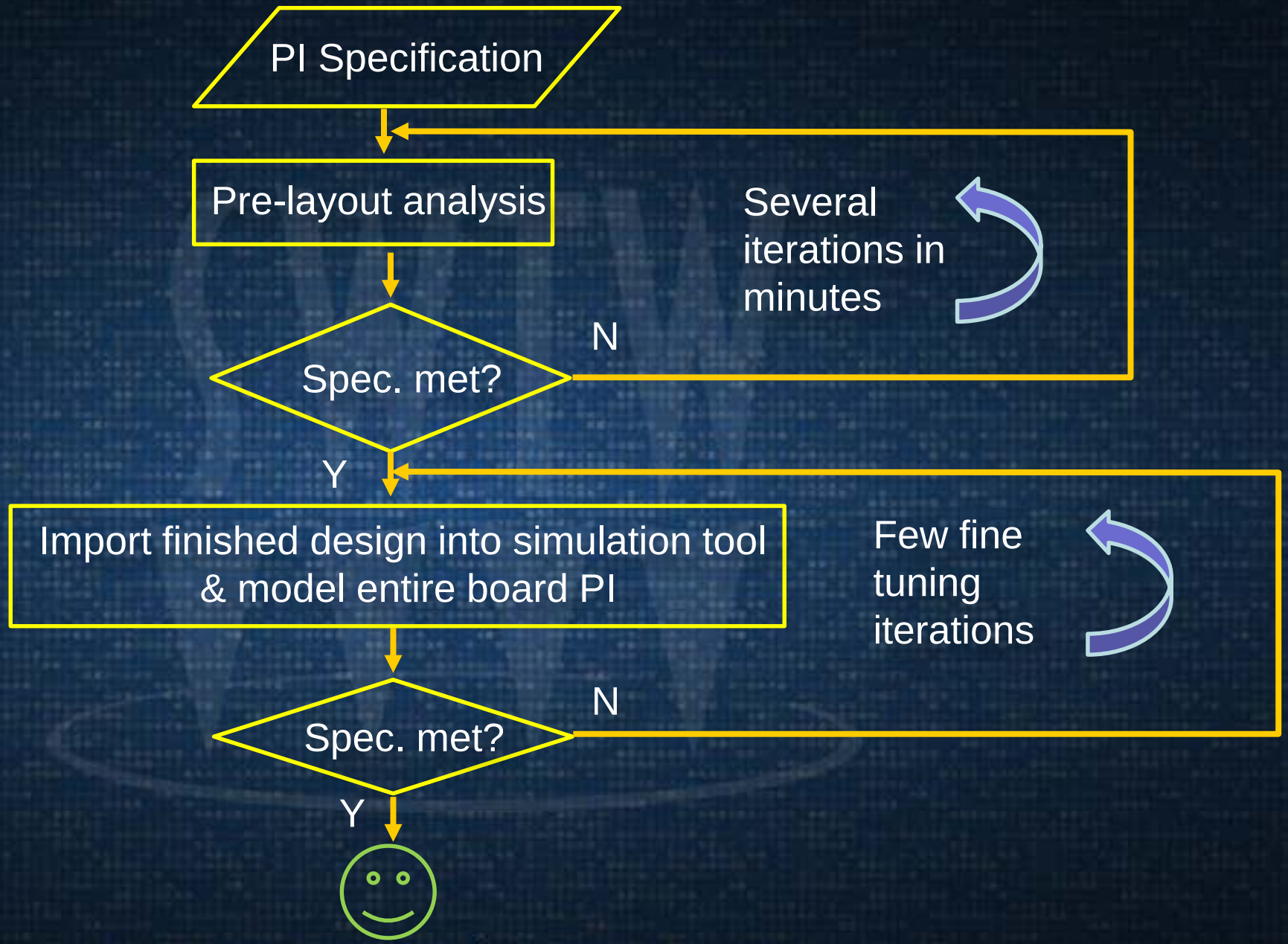
Design Side Flow



PDN Design: Design Side, step 1

- Questions that need to be answered:
  - How much of the budget is eaten up by the probe needle?
  - Have sufficient number of planes/plane regions been allocated to each supply?
  - Have enough quantity and types of caps been allocated?
  - Are there enough via connections to limit inductance?

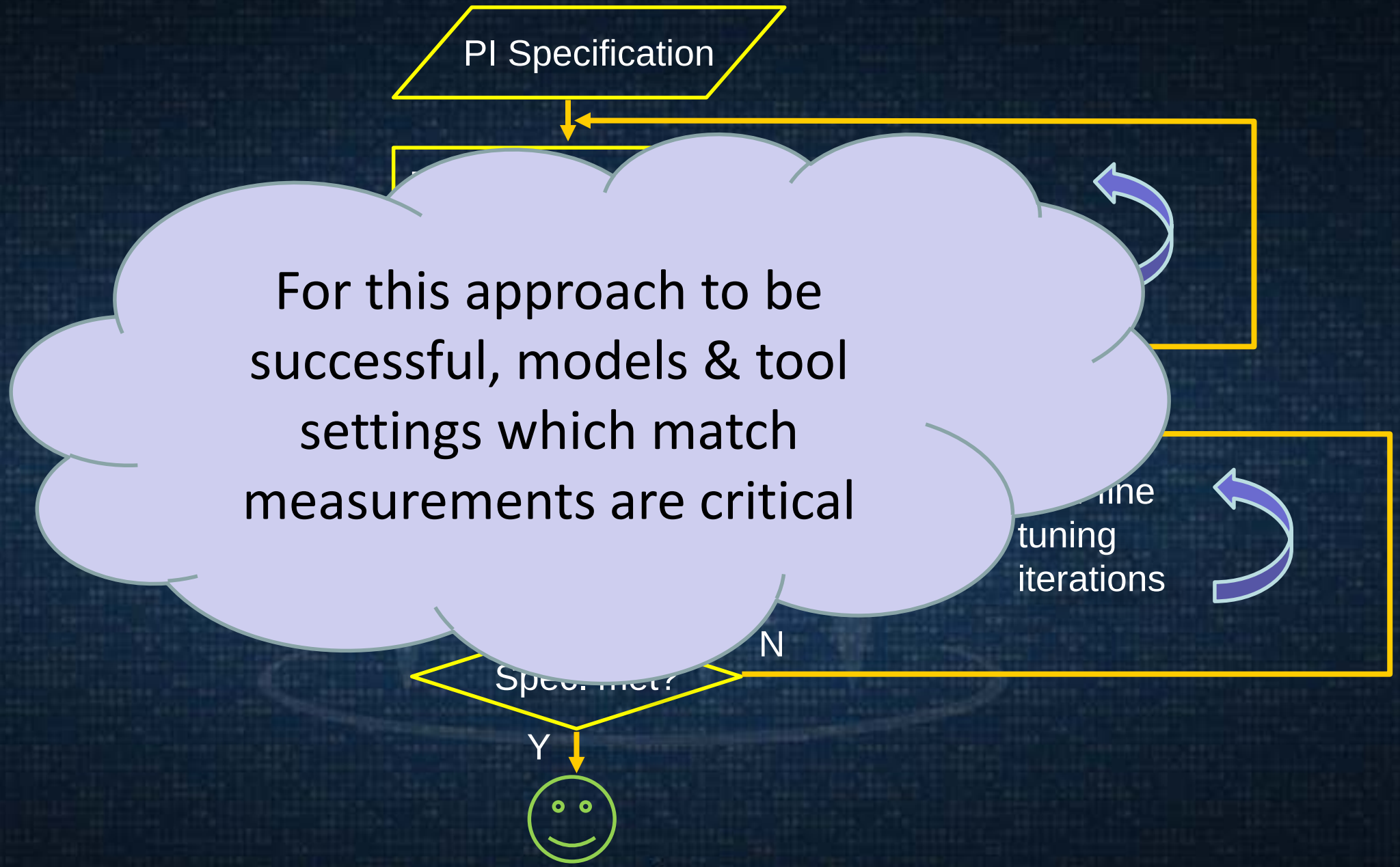
- Challenging designs require multiple iterations with different options to arrive at the optimal solution.

- Pre-Layout Analysis strategy is key. Fast (minutes) but accurate enough to be close to the final answer.

PDN Design: Design Side, step 2

- Design identified by Pre-Layout Analysis is implemented
- Complete design is loaded into 2.5D simulators. This takes several hours to simulate
- If Pre-Layout Analysis is done properly, final answer should be close
  - Critical planes will need fine tuning

Design Side Flow



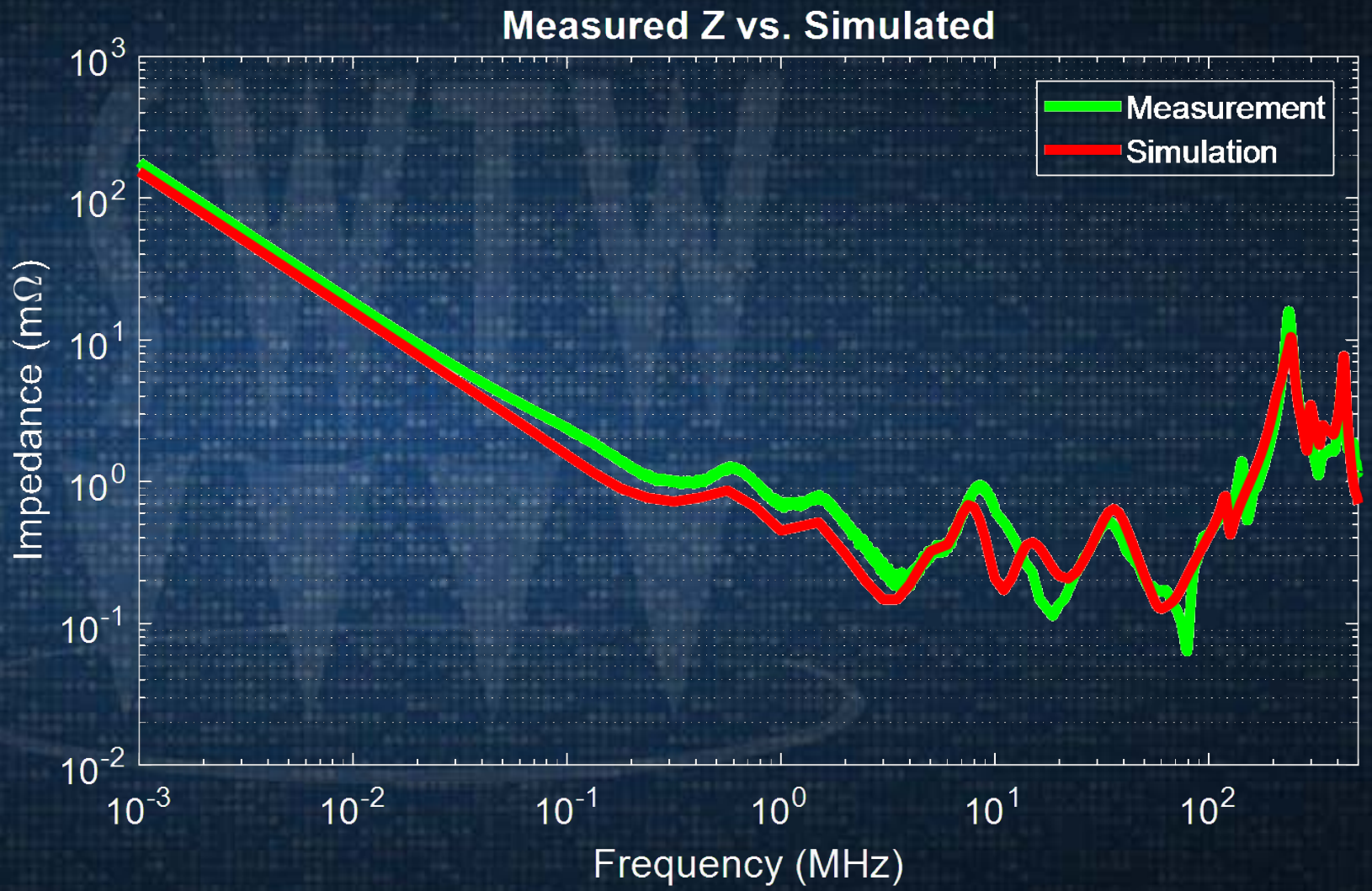
Simulation to Measurement Correlation

Simulation:

- PowerSI results
- 150 capacitors on supply
- 8 distributed DUT pins

Measured Results:

- 1 kHz to 500 MHz
- Socket included



Successful PDN Design

Design Side

Good design practices
Quality simulation tools
Optimized simulation strategies
Measurement correlation

Fabrication Side

Fab design rules
Fab technologies
Manufacturing robustness

Fab Toolbox

- Using thin cores between PWR & GND
- Unbalanced stackups
- Via sizing and count
- Capacitor placement strategies to reduce inductance

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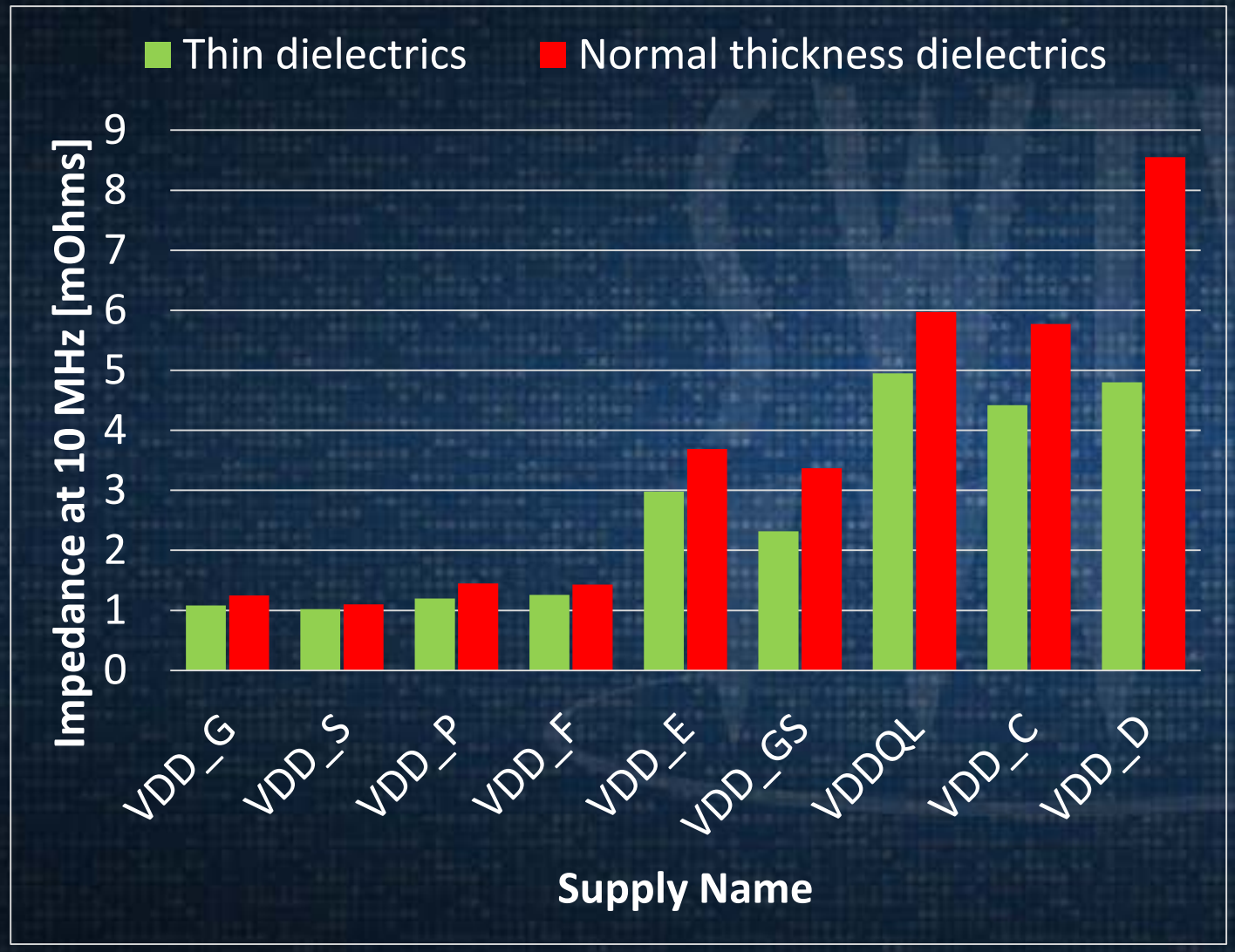
Toolbox: Thin cores

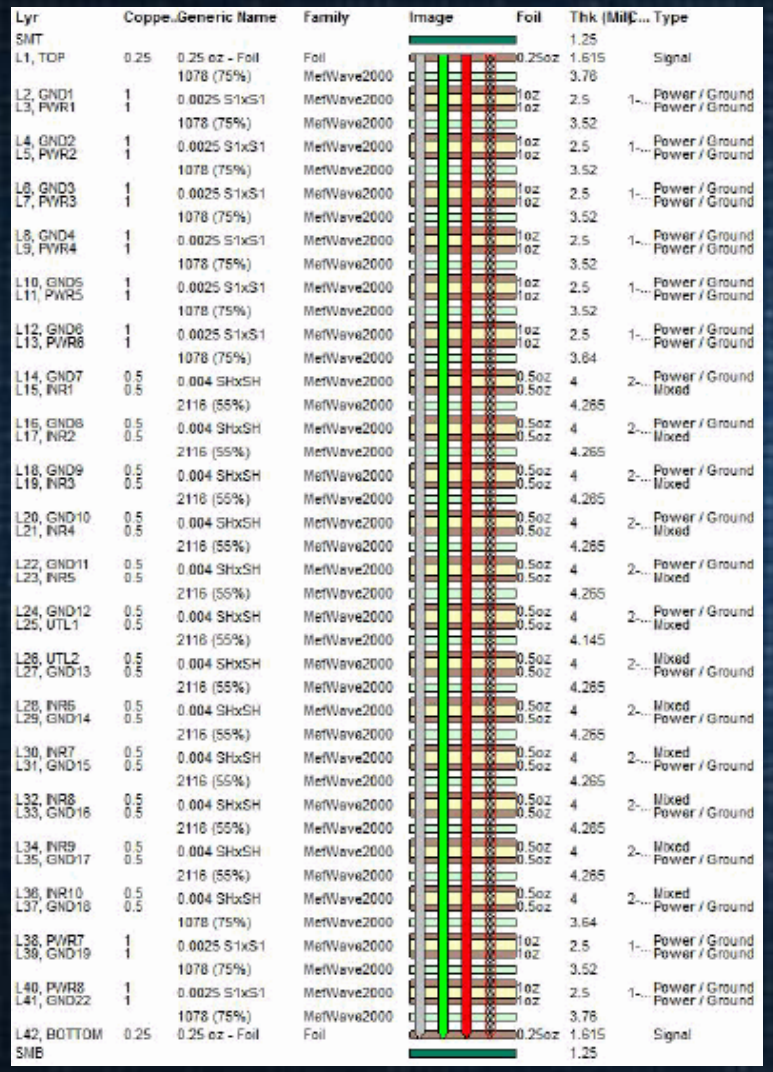


10 – 45 % improvement with thin dielectrics

Fab Toolbox

- Using thin cores between PWR & GND
- Unbalanced stackups
- Via sizing and count
- Capacitor placement strategies to reduce inductance

Toolbox: Unbalanced Stackups

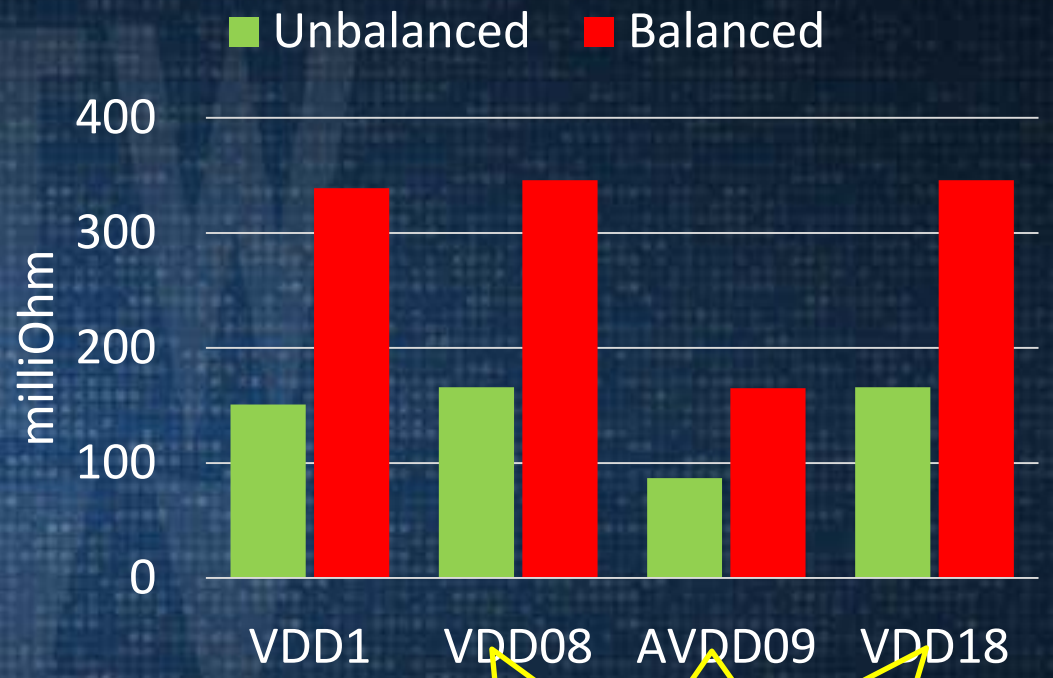


Lyr	Coppe..	Generic Name	Family	Image	Foil	Thk (Mil)	C...	Type
SMT						1.25		
L1, TOP	0.25	0.25 oz - Foil	Foil		0.25oz	1.615		Signal
		1078 (75%)	MetWave2000			3.78		
L2, GND1 L3, PWR1	1 1	0.0025 S1xS1	MetWave2000		1oz 1oz	2.5	1-...	Power / Ground Power / Ground
		1078 (75%)	MetWave2000			3.52		
L4, GND2 L5, PWR2	1 1	0.0025 S1xS1	MetWave2000		1oz 1oz	2.5	1-...	Power / Ground Power / Ground
		1078 (75%)	MetWave2000			3.52		
L6, GND3 L7, PWR3	1 1	0.0025 S1xS1	MetWave2000		1oz 1oz	2.5	1-...	Power / Ground Power / Ground
		1078 (75%)	MetWave2000			3.52		
L8, GND4 L9, PWR4	1 1	0.0025 S1xS1	MetWave2000		1oz 1oz	2.5	1-...	Power / Ground Power / Ground
		1078 (75%)	MetWave2000			3.52		
L10, GND5 L11, PWR5	1 1	0.0025 S1xS1	MetWave2000		1oz 1oz	2.5	1-...	Power / Ground Power / Ground
		1078 (75%)	MetWave2000			3.52		
L12, GND6 L13, PWR6	1 1	0.0025 S1xS1	MetWave2000		1oz 1oz	2.5	1-...	Power / Ground Power / Ground
		1078 (75%)	MetWave2000			3.64		
L14, GND7 L15, INR1	0.5 0.5	0.004 SHxSH	MetWave2000		0.5oz 0.5oz	4	2-...	Power / Ground Mixed
		2116 (55%)	MetWave2000			4.265		
L16, GND8 L17, INR2	0.5 0.5	0.004 SHxSH	MetWave2000		0.5oz 0.5oz	4	2-...	Power / Ground Mixed
		2116 (55%)	MetWave2000			4.265		
L18, GND9 L19, INR3	0.5 0.5	0.004 SHxSH	MetWave2000		0.5oz 0.5oz	4	2-...	Power / Ground Mixed
		2116 (55%)	MetWave2000			4.265		
L20, GND10 L21, INR4	0.5 0.5	0.004 SHxSH	MetWave2000		0.5oz 0.5oz	4	2-...	Power / Ground Mixed
		2116 (55%)	MetWave2000			4.265		
L22, GND11 L23, INR5	0.5 0.5	0.004 SHxSH	MetWave2000		0.5oz 0.5oz	4	2-...	Power / Ground Mixed
		2116 (55%)	MetWave2000			4.265		
L24, GND12 L25, UTL1	0.5 0.5	0.004 SHxSH	MetWave2000		0.5oz 0.5oz	4	2-...	Power / Ground Mixed
		2116 (55%)	MetWave2000			4.145		
L26, UTL2 L27, GND13	0.5 0.5	0.004 SHxSH	MetWave2000		0.5oz 0.5oz	4	2-...	Mixed Power / Ground
		2116 (55%)	MetWave2000			4.265		
L28, INR6 L29, GND14	0.5 0.5	0.004 SHxSH	MetWave2000		0.5oz 0.5oz	4	2-...	Mixed Power / Ground
		2116 (55%)	MetWave2000			4.265		
L30, INR7 L31, GND15	0.5 0.5	0.004 SHxSH	MetWave2000		0.5oz 0.5oz	4	2-...	Mixed Power / Ground
		2116 (55%)	MetWave2000			4.265		
L32, INR8 L33, GND16	0.5 0.5	0.004 SHxSH	MetWave2000		0.5oz 0.5oz	4	2-...	Mixed Power / Ground
		2116 (55%)	MetWave2000			4.265		
L34, INR9 L35, GND17	0.5 0.5	0.004 SHxSH	MetWave2000		0.5oz 0.5oz	4	2-...	Mixed Power / Ground
		2116 (55%)	MetWave2000			4.265		
L36, INR10 L37, GND18	0.5 0.5	0.004 SHxSH	MetWave2000		0.5oz 0.5oz	4	2-...	Mixed Power / Ground
		1078 (75%)	MetWave2000			3.64		
L38, PWR7 L39, GND19	1 1	0.0025 S1xS1	MetWave2000		1oz 1oz	2.5	1-...	Power / Ground Power / Ground
		1078 (75%)	MetWave2000			3.52		
L40, PWR8 L41, GND22	1 1	0.0025 S1xS1	MetWave2000		1oz 1oz	2.5	1-...	Power / Ground Power / Ground
		1078 (75%)	MetWave2000			3.78		
L42, BOTTOM	0.25	0.25 oz - Foil	Foil		0.25oz	1.615		Signal
SMB						1.25		

6 PWRs

0.19”

2 PWRs



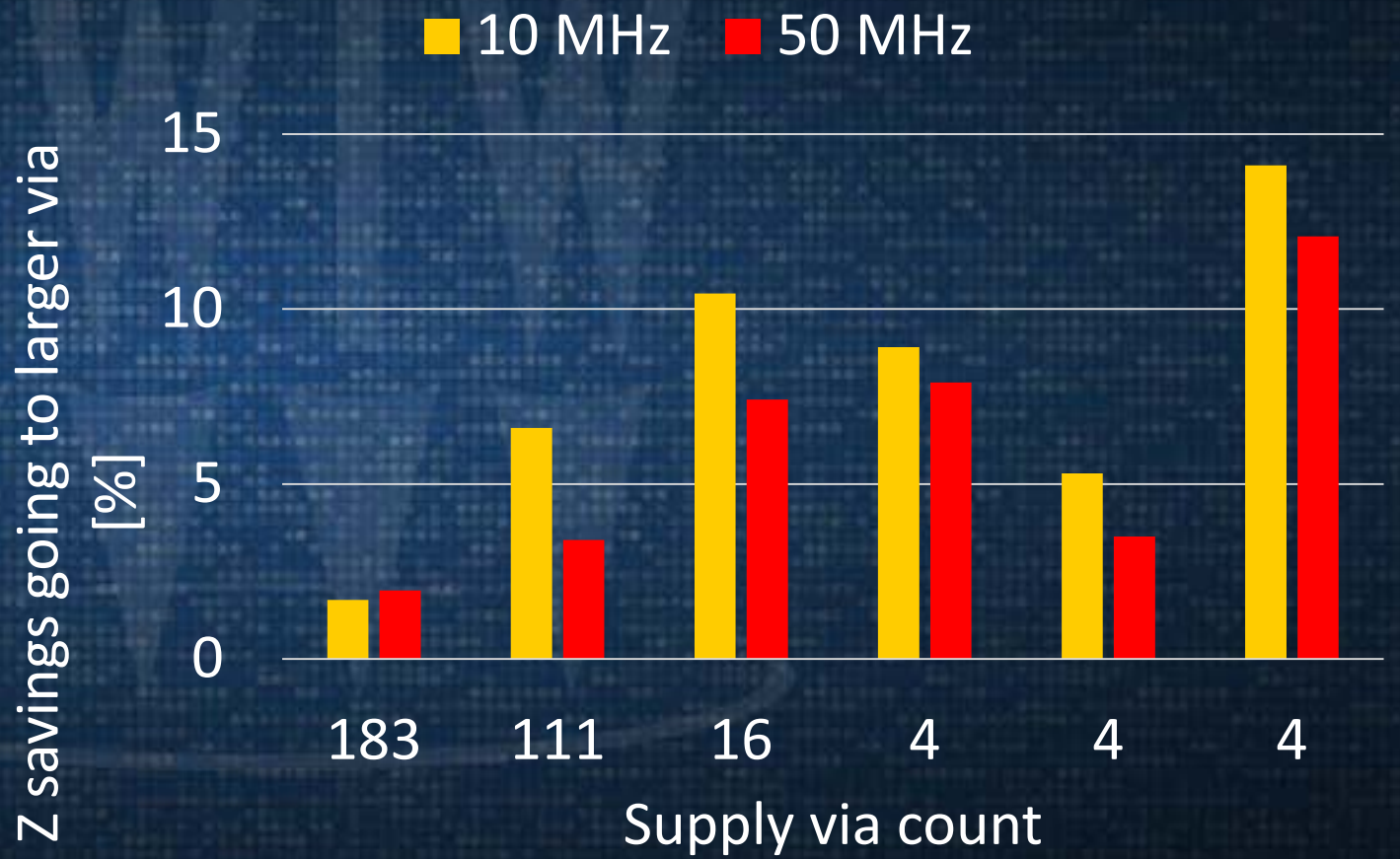
50 % improvement going unbalanced

Fab Toolbox

- Using thin cores between PWR & GND
- Unbalanced stackups
- Via sizing and count
- Capacitor placement strategies to reduce inductance

Toolbox: Via Sizing and Count

- 20 mil [0.5 mm] pitch
- Can use 7.9 mil or 5.9 mil via
- Need to balance Cu web size vs. via inductance
- Lower via count shows more variation in savings
- In this example, larger via always produced lower Z



Fab Toolbox

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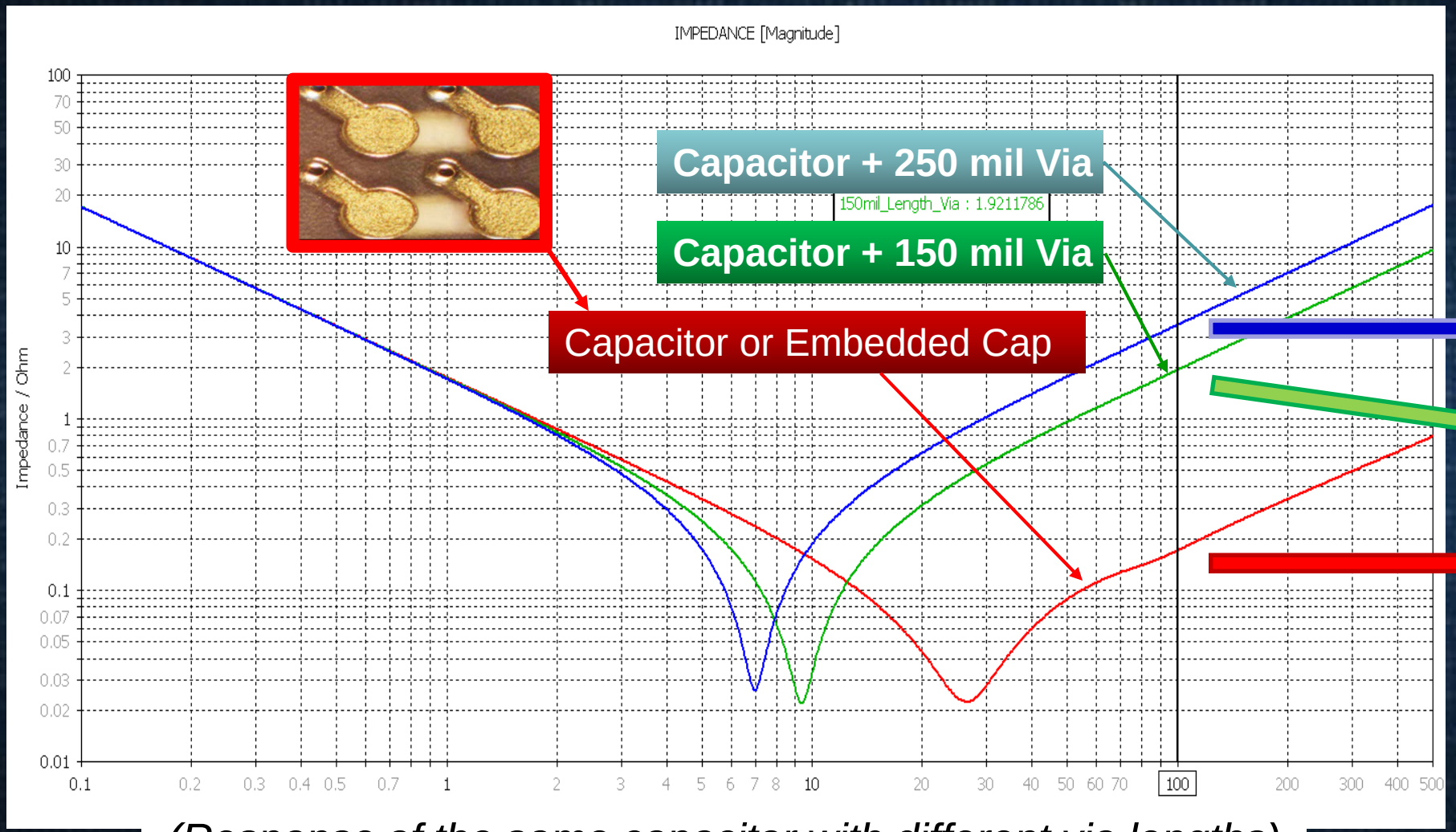
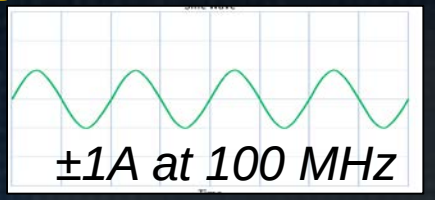
Toolbox: Capacitors – Via length





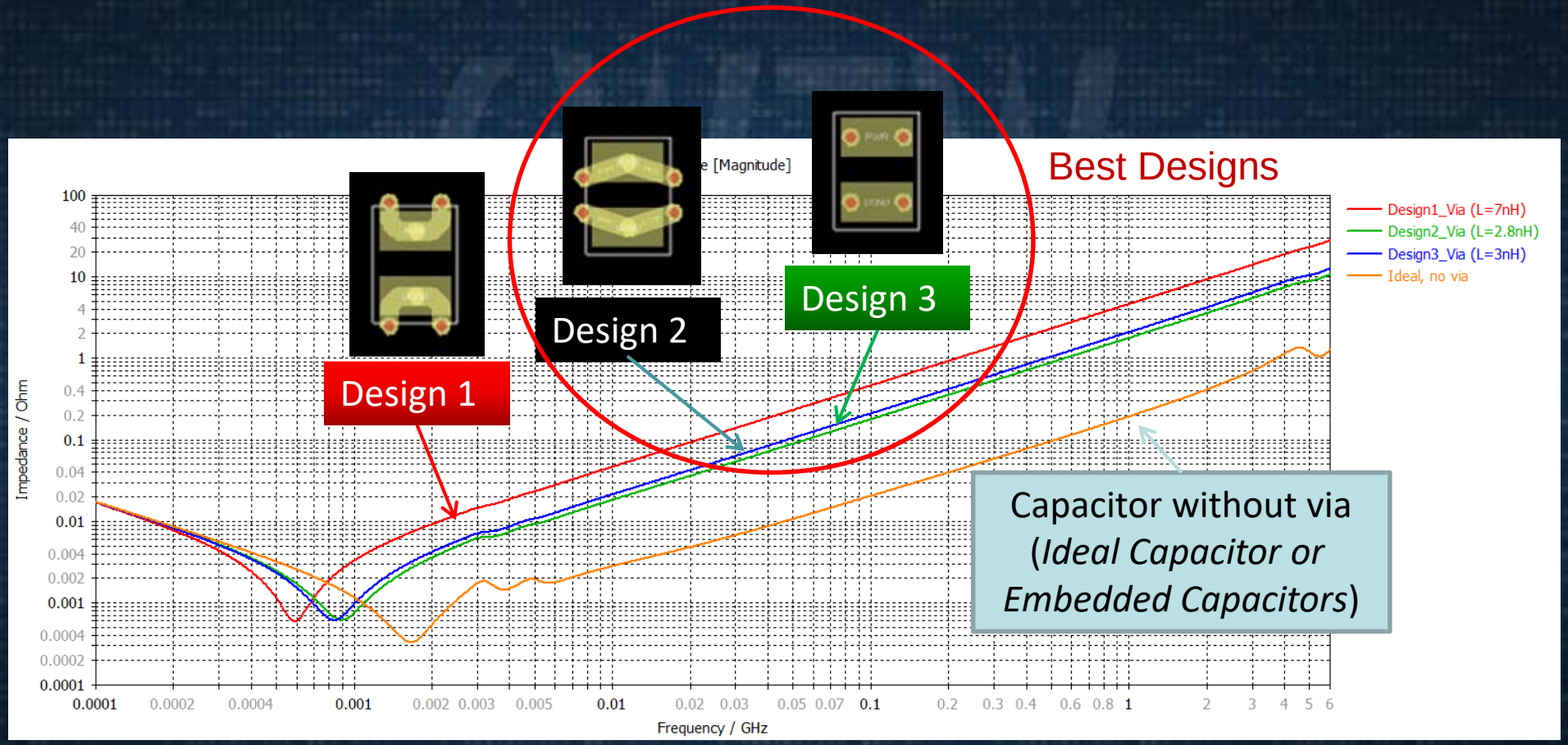
± 3.6V

± 2.0V

± 0.18V

(Response of the same capacitor with different via lengths)

Toolbox: Capacitors – Via placement



Summary

- Multi-site probe cards + space transformers are very challenging and require a sophisticated full path design and simulation methodology
- WLCSP is driving higher & higher test performance requirements
- Understanding the fundamental limiters to the PDN performance helps with a smarter, faster optimization
- Good models of probe pins that are verified with measurements to higher frequencies are difficult to come by
- The strategies outlined here along with measurement based models have been used to implement multiple successful designs