



SW Test Workshop
Semiconductor Wafer Test Workshop

An introduction for novel multi-layer thin film substrates applied in space transformers

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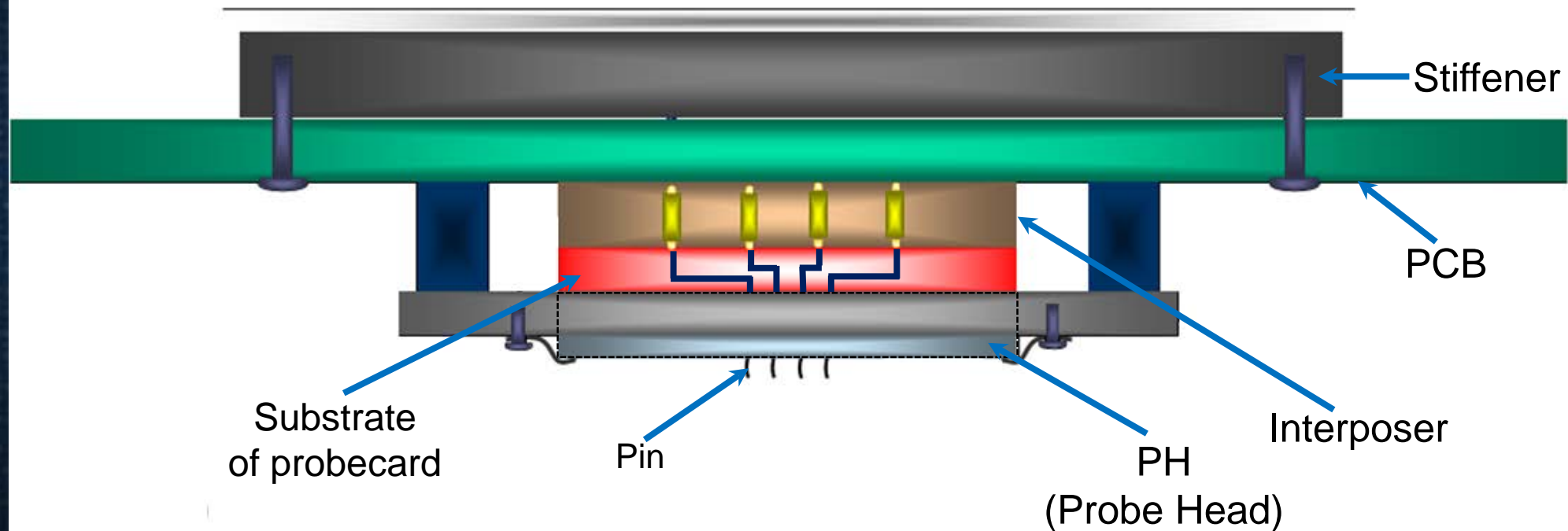
June 3-6, 2018

Agenda

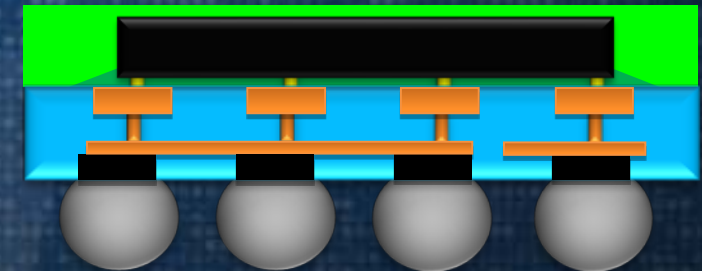
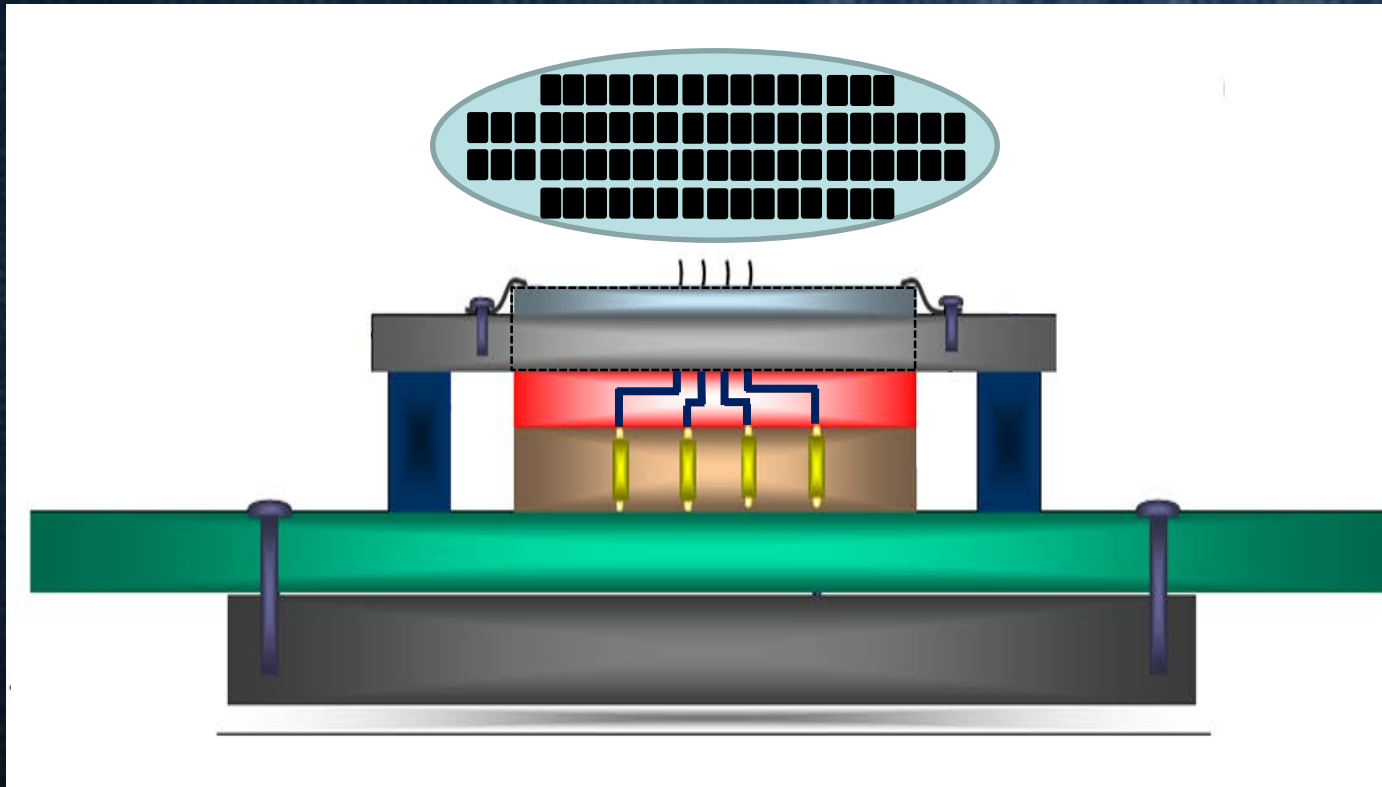
- New challenge coming from density
- Reviewing on different type substrates
- Extracting new ideas to realize multi-layer thin film substrates
- Conclusions

•Probe Card Structure

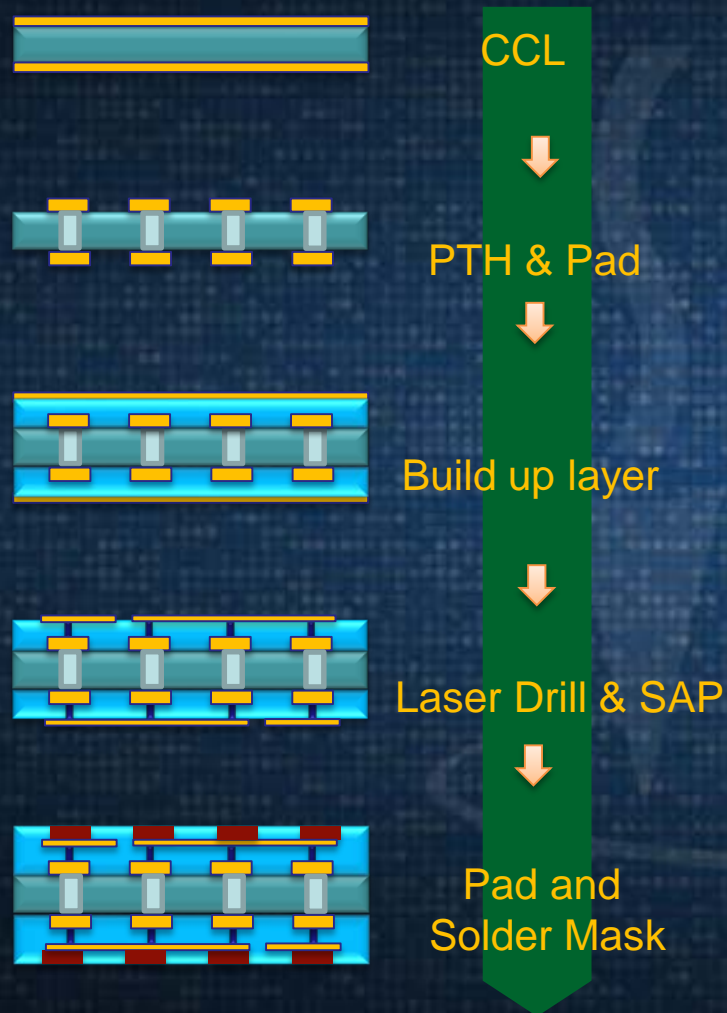
Typical Vertical Probe Card Structure - With Interposer



- **Probe card** is the leading tech. on semiconductor testing and packaging

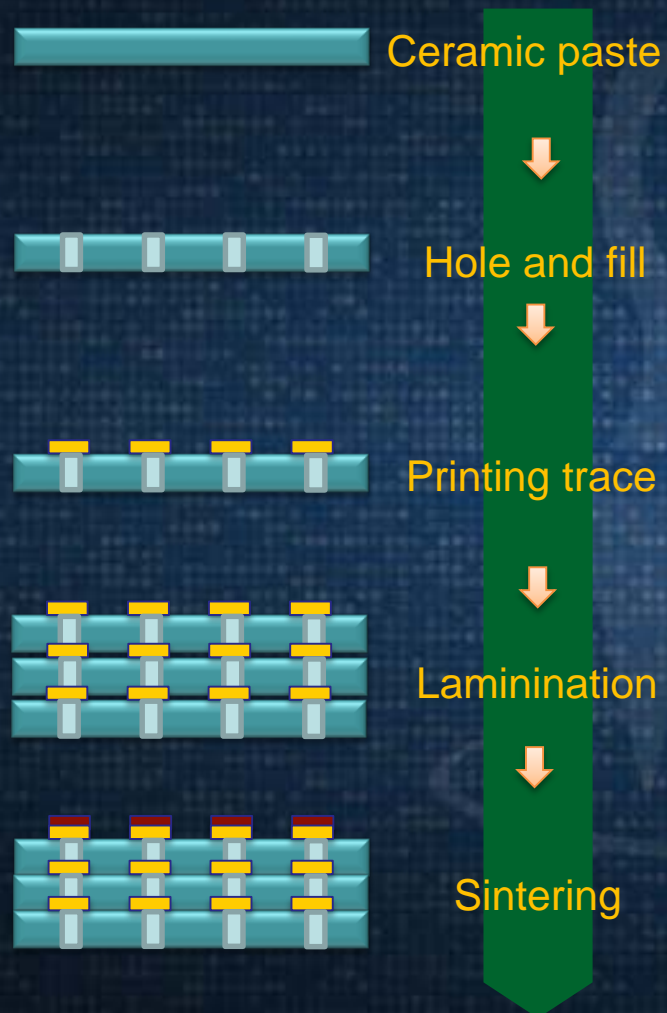


Process of HDI(MLO)



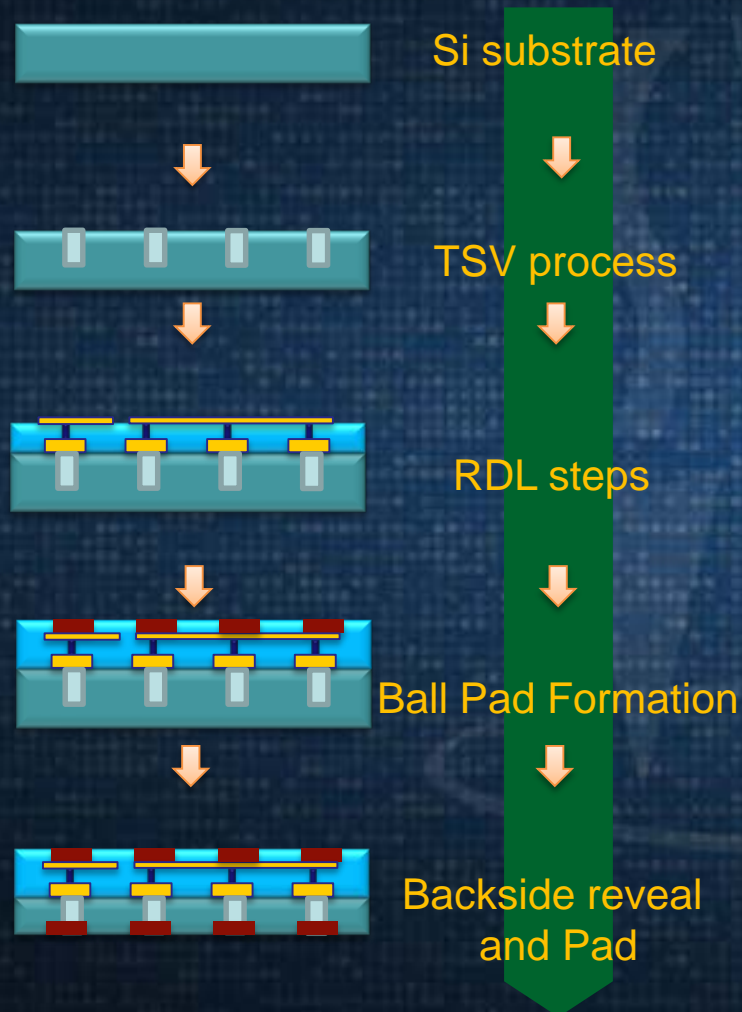
- CCL(copper clad lamination) as a core, dimension stability depends on material
- Routing capability related with PTH and SAP process (Plating through hole and Semi-additive process)
- Very high layer counts

Process of MLC



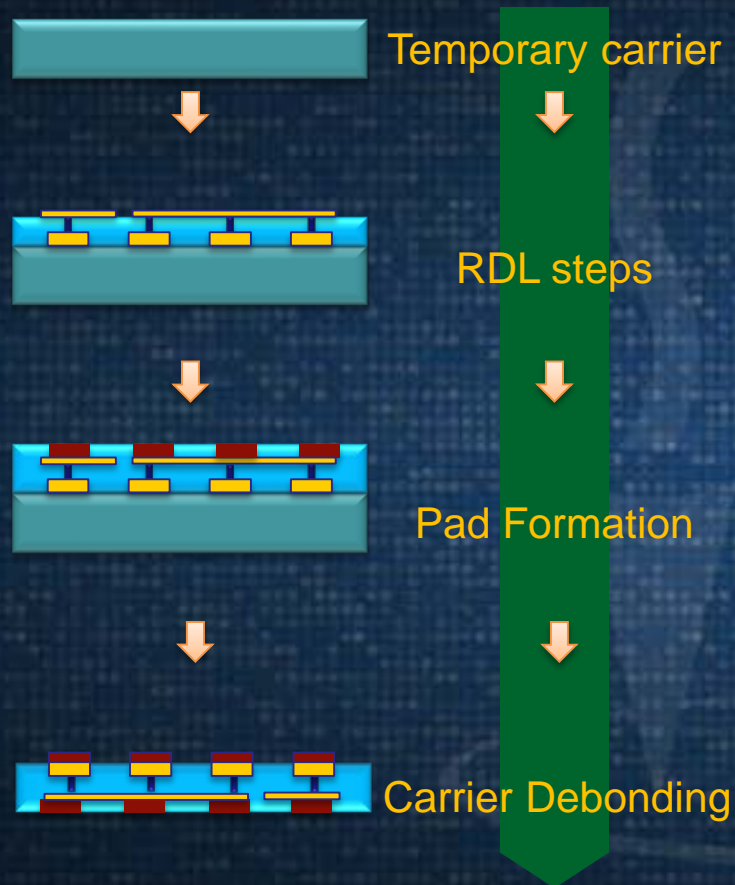
- Ceramic pastes as core substrate, Dimension stability limited
- Routing capability related with Hole punching and printing process
- Very high layer counts

Process of Si interposer



- Si substrate as a Core, (Very stable dimension in Process)
- TSV as through holes
- RDL process as Bump RDL or Dual-Damascus process, Can be micron-m or sub-micron level
- Usually limited on layer counts

Process of ML-Thin film



- **Si wafer or Glass for Temporary carrier. (Very stable dimension in process)**
- **RDL process as Bump RDL or Dual-Damascus process, Can be micron-m or sub-micron level**
- **Need to attach on other substrate**

- **Major comparison/Pros & Cons**

- Fan-out related topic
- Impedance control related topic

Comparison in fan-out related dimension

	Process type	Min. Line width	Min. Via Dia.	Max. Layer count
MLO	Lamination/ Semi-additive	○	○	◎
MLC	Co-fired/ Printing	△	△	◎
Si interposer	RDL/TSV	◎	◎	△
ML-Thin film	RDL Process/ Carrier debonding	◎	◎	◎

Cases study: comparison in routing

Level	L/S	Via	Via Pad	Pitch of 2 Pad	Pitch of 2 Pad with 1 line in between
1	50/50 (Etching)	100 (Mech. Drill)	150	200	350
2	30/30 (SAP)	25 (CO2 Laser)	50	80	140
3	20/20 (SAP)	15 (UV laser)	30	50	90
4	5/5 (RDL)	10 (Litho.)	20	25	35

- **Trace patterning & Via process will be the key for density going further.**
- **RDL and Dual-Damascus will be candidates for Traces formation.**
- **Lithography via and UV Laser drill will be candidates for Via formation.**

Comparison in impedance related prometers

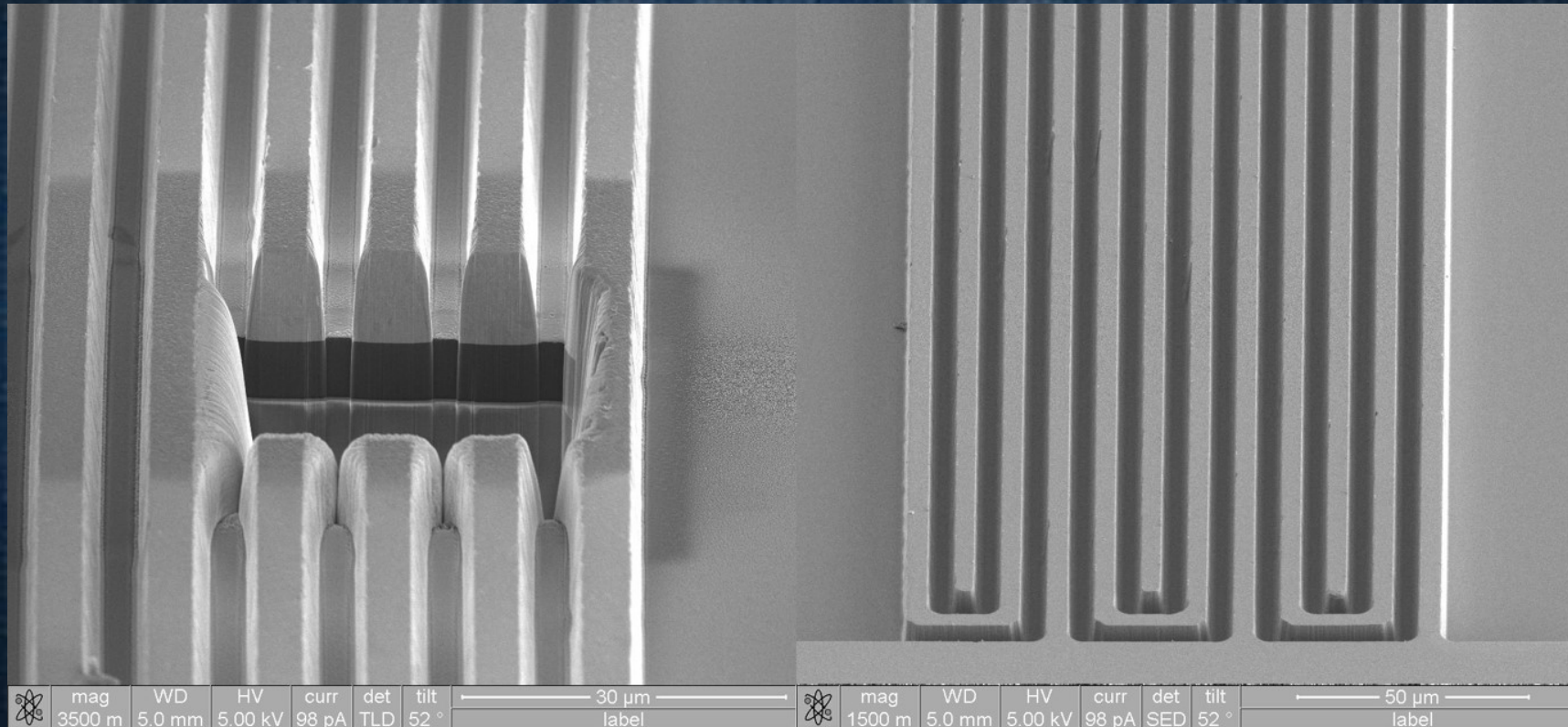
	Dk	Capability of PWR/GND layer	Max. Layer count	Capability of impedance control
MLO	Medium	◎	60~70	○
MLC	High	◎	50~60	○
Si interposer	Low	△	4	△
ML-Thin film	Low	◎	30+	◎

Cases study: width on impedance control

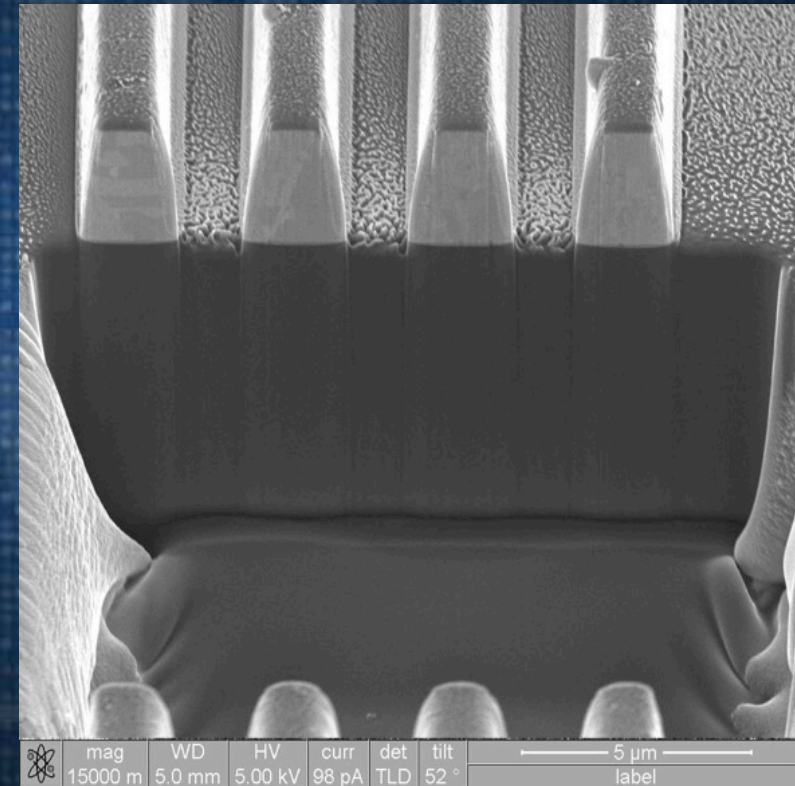
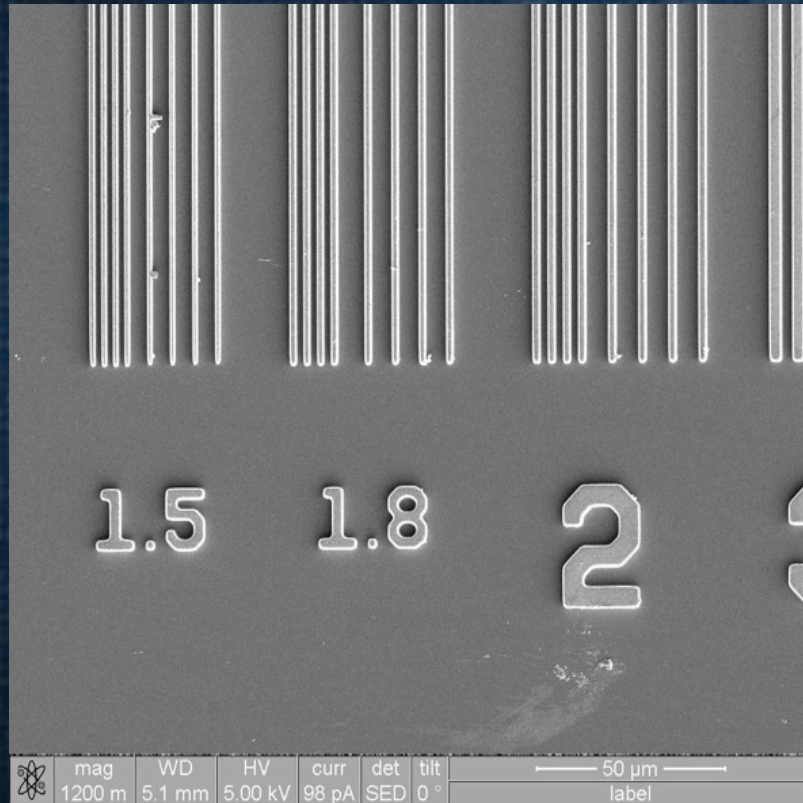
<div>Dielectric Th /Metal.</div> <div>Th. Dk</div>	10 μm /2.5 μm	25 μm / 5 μm	50 μm / 10 μm
3(LK M.)	9.5 μm	25 μm	49 μm
4(Epoxy)	7 μm	18 μm	37 μm
6(Ceramic)	3.8 μm	11 μm	22 μm

- **Thinner dielectric layer is necessary for Higher routing density**
- **Dielectric material related with process choose**
- **Lk material for TF and Si interposer**
- **Epoxy for MLO**
- **Ceramic for MLC**

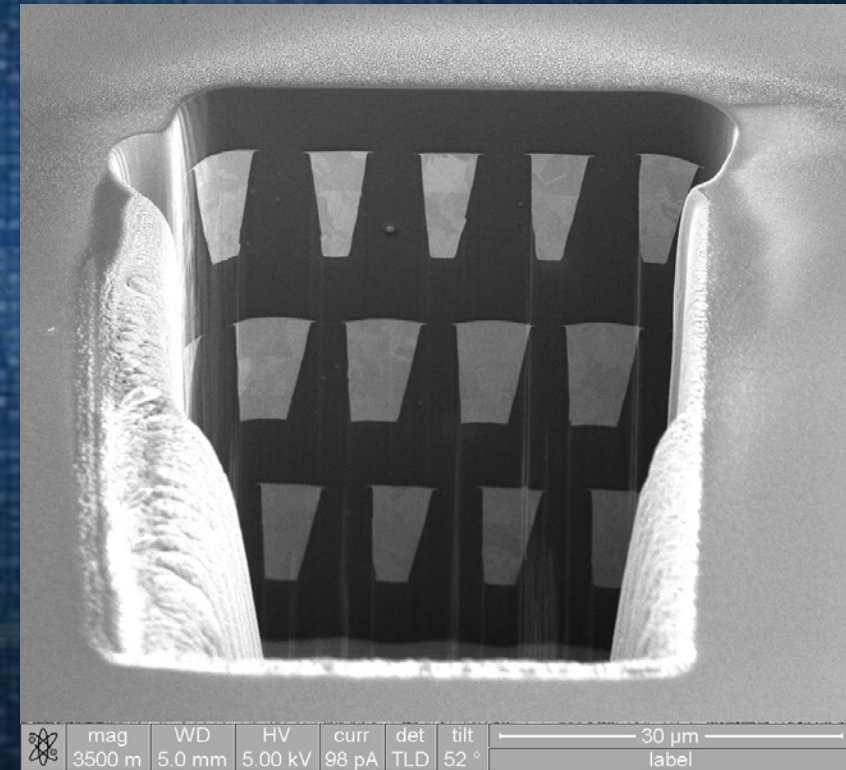
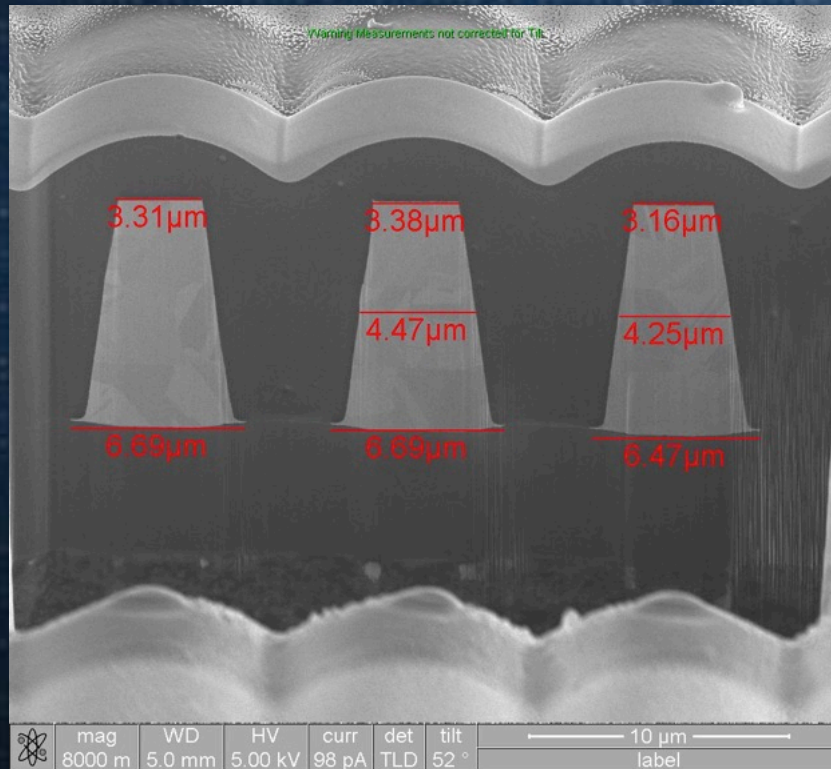
- Line width/space width=5 μ m/5 μ m
- 365nm UV, Aligner



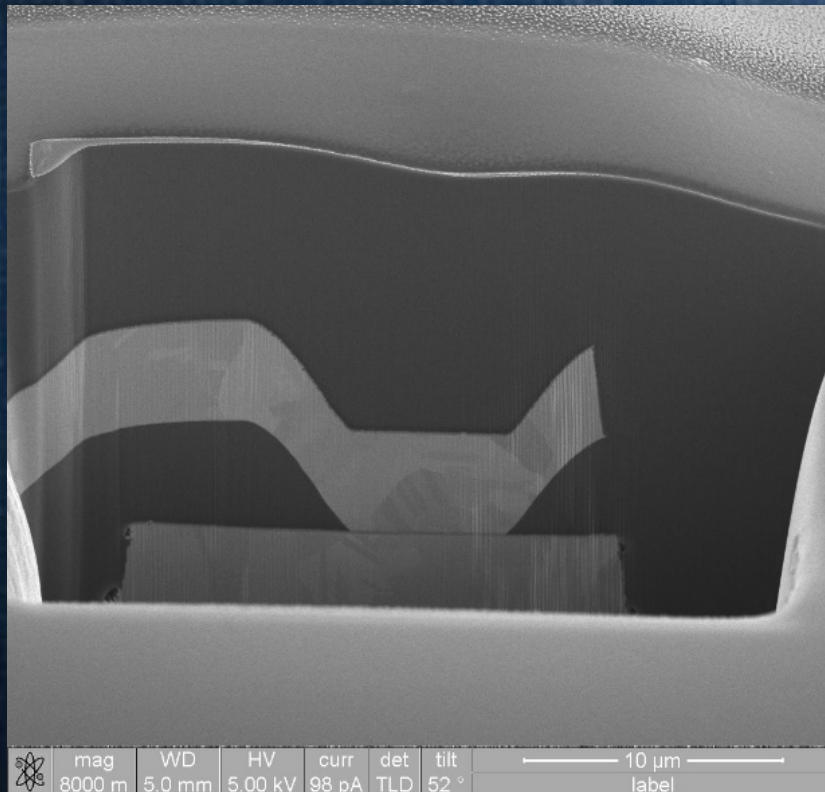
- Line width/space: 1.8 μ m/1.8 μ m
- 365nm UV stepper



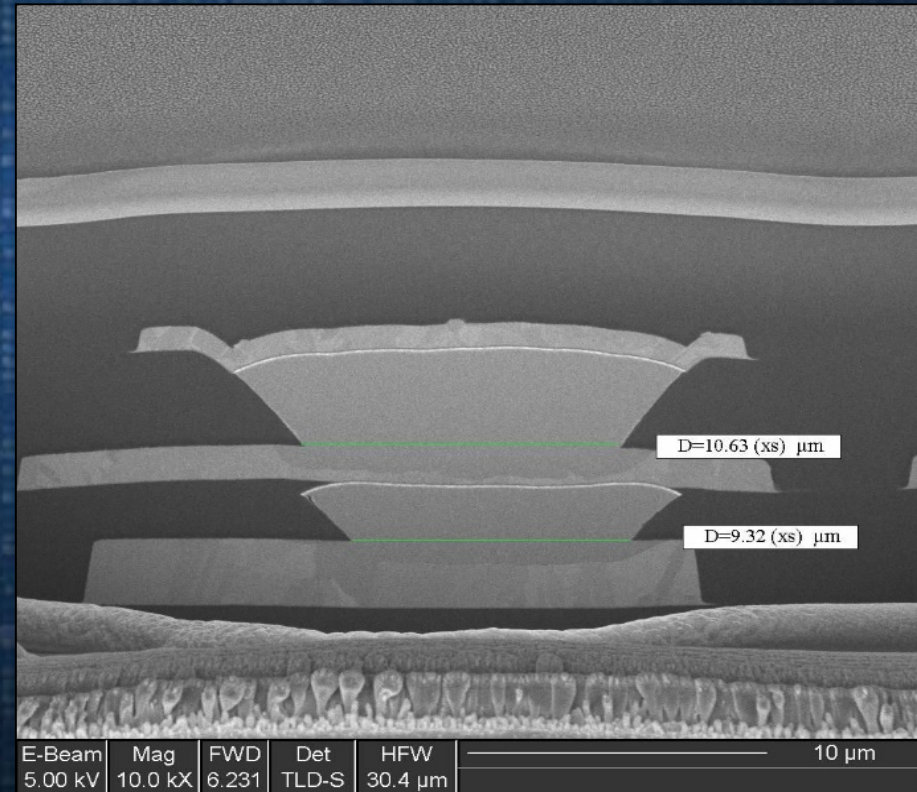
- Line width/space: 5 μ m/5 μ m
- Polyimide vanish coating for dielectric layer
- With planarization process



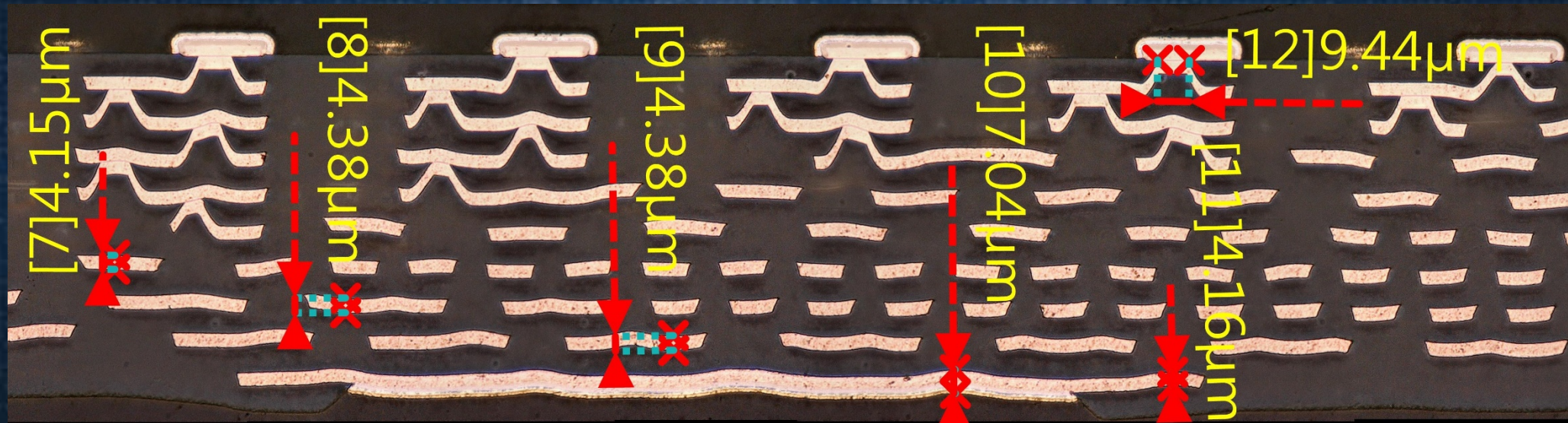
- 10 um Via
- Lithography process



- Filled via for stacking



Cross section of 10-layer TF



Conclusion

- Next generation probecard substrate need novel ideas for their processes
- Thinking “out-of-the-box”, but not thinking “out-of-the-blue”
- Bumping process and semiconductor backend process provide good hints
- Based on modified backend process, ML-thin film is a good candidate for next Gen. probecard substrate



Thank you for your attention!

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