2023

Semiconductor Wafer Test Conference

SWTEST

PROBE TODAY, FOR TOMORROW

PROGRAM SCHEDULE

Monday, June 5

7:00 AM - 12:30 PM	REGISTRATION / EXHIBITOR CHECK IN
7:00 - 8:00 AM	CONTINENTAL BREAKFAST
8:00 - 9:30 AM	SWTest 2023 Visionary Keynote – Luca Fasoli, PhD (WD)
9:30 - 10:00 AM	Coffee Break and POSTER SESSION
10:00 – 10:30	Welcome to SWTest 2023
10:30 - Noon	Session 1 – RF Applications
Noon – 1:30PM	Lunch
1:30 - 3:00 PM	Session 2 – Probecard Optimizations
3:00 - 3:30 PM	Coffee Break and POSTER SESSION
3:30 - 5:00 PM	Session 3 – Fine Pitch and High Parallelism
5:00 – 8:00 PM	SWTest 2023 Exhibition
	8:00 – 10:00 PM Sponsor Hospitality Suites

Tuesday, June 6

7:00 AM - Noon	REGISTRATION
7:00 - 8:00 AM	CONTINENTAL BREAKFAST
8:00 - 8:30 AM	SWT Crew and Mentoring Initiative Update
8:30 - 9:30 AM	Session 4 – RF Design Considerations
9:30 - 10:00 AM	Coffee Break and POSTER SESSION
10:00 – Noon	Session 5 – High Power Testing Challenges
Noon – 1:30PM	Lunch
1:30 - 3:00 PM	Session 6 – Probe Card Mechanical Characteristics
3:00 – 5:00 PM	SWTest 2023 Exhibition
4:30 - 5:30 PM	SWT Crew Mixer
6:00 - 9:00 PM	Cocktails, Dinner, and SWTest Social Event
9:00 - 10:00 PM	Sponsor Hospitality Suites

Wednesday, June 7

7:00 - 8:00 AM	CONTINENTAL BREAKFAST
8:00 - 9:30 AM	Session 7 – Probe Potpourri
9:30 - 10:00 AM	Coffee Break
10:00 – 11:30 AM	Session 8 – Probe Card Design Considerations
11:30 to 11:45 PM	AWARDS
Noon	Final ADJOURNMENT … see you in 2024!

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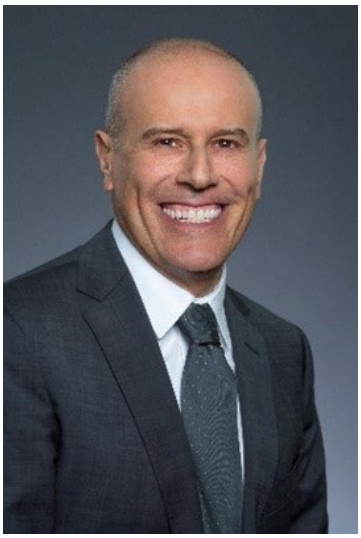
June 5, 2023 (Monday)

7:00 – 8:00 CONTINENTAL BREAKFAST
7:00 – Noon REGISTRATION/EXHIBITOR CHECK IN

8:00 – 9:30	Welcome and Visionary Keynote Speaker
8:00 – 8:15	**Opening Remarks for SWTest 2023** Jerry Broz, PhD, SWTest General Chair, Advanced Probing Systems
8:15 – 9:30	**VISIONARY KEYNOTE** **Test in the 3D NAND Zettabyte Era:** **How to achieve quality and minimize cost**  **Luca FASOLI, PhD** *Dr. Luca Fasoli* *Senior Vice President, Silicon Technology & Manufacturing* ***Western Digital, Inc.*** **Abstract:** The 3D NAND Flash industry is now approaching the Zettabyte era – an era in which the Flash industry will ship more than a trillion gigabytes every year. Technology innovations in silicon processing, device concepts, circuit design, and system architecture have consistently enabled us to achieve increased performance and reliability over multiple NAND generations. With every new 3D NAND generation, bit production has increased exponentially while cost per bit has correspondently been decreasing. This trend has disrupted industries and created new markets. From mobile devices and connected vehicles to gaming and data centers, Flash is at the core. Always hidden from view, 3D NAND testing has been evolving to keep up with this on-going revolution. Armies of engineers have been working in parallel to perfect test architectures, test equipment, and test flows to make sure that test cost per bit scales similarly while not affecting product quality. Transition to the Zettabyte era poses a new set of challenges to the test industry and demands close cooperation between NAND vendors and equipment manufacturers to ensure quality without affecting overall cost per bit. In this keynote, we will cover how Western Digital has been approaching the 3D NAND technology evolution and its testing challenges and relative opportunities. **Biography:** Dr. Luca Fasoli is responsible for the strategy and the development of Western Digital solid-state memory technologies. A 25-year industry veteran and IEEE Senior Member, Dr. Fasoli has held engineering management positions at Waferscale Integration, STMicroelectronics, Matrix Semi and SanDisk. Dr. Fasoli has worked on non-volatile memory technologies and solid-state storage products, leading product development teams from concept definition to HVM. Dr. Fasoli has numerous technical papers and holds more than 90 U.S. patents. He earned a PhD and MS in Electronic Engineering from the Polytechnic University of Milan, and completed Engineering Leadership Professional Program at UC Berkeley.

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June 5, 2023 (Monday)	
9:30 to 10:00 – **Coffee Break**	**POSTER SESSION** Session Chair: John CALDWELL (MJC Electronics Corporation - USA)
10:00 – 10:30	**Welcome to SWTest 2023** Jerry BROZ, PhD (SWTest Conference Chair - Longmont, USA)
10:30 AM – Noon	**SESSION 1: RF Applications** **Session Chair: Mark OJEDA (Infineon Semiconductor - USA)**
10:30 – 11:00	**On Membrane Attenuators for 60 GHz Loopback Transceiver Testing** Herve POZIN-ROUX, Nicolas FALCOT, Philippe TRIBOLO, and Benoit GUBERT (ST Microelectronics - France) and Andrew NELSON (FormFactor -USA)
11:00 – 11:30	**30GHz & 70µm pitch Phantom Technology. Advanced probe solution for RF test up to 30 GHz and fine pitch up to 70 µm** Giulia ROTTOLI (Technoprobe Spa - Italy) and Dale VENTURA (Marvell Technology-USA)
11:30 – Noon	**Enabling high speed loopback tests for Serdes, PCIE Gen5/6 on Probe using embedded Capacitors on the MLO** Quaid Joher FURNITUREWALA (Advantest America Inc. - San Jose, USA)
Noon - 13:30 – Enjoy Lunch and Networking with Colleagues and Attendees!	
13:30 – 15:00	**SESSION 2: Probecard Optimizations** **Session Chair: Michael HUEBNER, PhD (FormFactor - USA)**
13:30 – 14:00	**Overcoming New Challenges in Advanced Vertical Probe Card Guide Plate Drilling** Chris STOKES, Alan FERGUSON, PhD, and Dimitris KARNAKIS (Oxford Lasers Ltd - UK)
14:00 – 14:30	**Fully Automated Integrated Silicon Photonic Wafer Test** Golam BAPPI (Ayar Labs - USA) and Dan RISHAVY (FormFactor – USA)
14:30 – 15:00	**PTSL MEMs RF Wafer Probes** Don THOMPSON (PTSL - USA)
15:00 – 15:30 – Coffee Break	**POSTER SESSION** Session Chair : John CALDWELL (MJC Electronics Corporation - USA)

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June 5, 2023 (Monday)

15:30 – 17:00	**SESSION 3: Fine Pitch & High Parallelism** **Session Chair: Raffaele VALLAURI (Technoprobe Spa - Italy)**
15:30 – 16:00	**Advance Technology WAT probecard challenges** Jeffrey LAM, (National University of Singapore - Singapore), TEE WHAY LIM, JEE FONG JONG ((GLOBALFOUNDRIES - Singapore), Eric Sik Kiang LAU, Tai Lin GOH, Yu-Ming CHIEN, Albert NINALGA (STAr Tech – Singapore)
16:00 – 16:30	**Staying Ahead of the Probe Card Complexity Curve** Eric SHOEMAKER and Steve LEDFORD (Teradyne, Inc - USA)
16:30 – 17:00	**Challenges and Innovations in Developing High-Density, Low-Power DPS Solutions for 5nm and Smaller Process Geometries in ATE** Tim BAKKEN (Elevate Semiconductor - USA)
17:00	**Technical Sessions Adjourn and EXPO Opens at 17:00**

	SWTest EXPO - 2023
17:00 – 20:00	**SWTest 2023 – Supplier and Sponsor EXPO with new Speakers' Corner!** **Communicate, Collaborate and Celebrate!**
20:00	**Sponsor Hospitality Suites and Events**

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PROGRAM SCHEDULE

Poster Session Overview

09:30 – 10:00 **15:00 – 15:30**	**POSTER SESSION** **John CALDWELL (MJC Electronics Corporation - USA)**
	Reducing to thermal soak time of probe card with tunable power of heater in space transformer Kwangjae OH, KYOUNGTAE MOON, Yong Ho CHO (PROTEC MEMS Technology. - South Korea) **Micro-Textured Film Offers Promise in Universal Handling of Microelectronics** Raj VARMA (Delphon - USA) **Burn-in test system controlled in real temperature** Junas NA (SEMICS - South Korea) **Pushing Temperature Limits of High Voltage Wafer Test** Georg FRANZ (T.I.P.S. Messtechnik GmbH - Austria) **High speed probe card using flexible multilayer polyimide fabricated by 3D MEMS Process** TAE KYUN KIM, Yong Ho CHO, Jong Gwan and, YOOKTAE KYUN KIM (MICROFRIEND – South Korea) **Importance of ceramic substrates with low thermal expansion coefficient in semiconductor wafer testing** Chiseung IN, Dae Hyeong LEE, Dooyun CHUNG, JUNGHWAN CHO, Huntae KIM, Yujin CHOI and Chiseung IN (SEMCNS – South Korea)
	Simplifying the Process of Probe Card Design Through Software Automation Adam SCHULTZ (Cohu - USA) **Designing High Bandwidth Vertical Probes (Download files)** Don THOMPSON (PTSL - USA) **Full Wafer MSP Contact and the Challenges of Material Deflection (Download** Gordon COWAN (Probe Test Solutions Ltd - UK) **Optimizing a Contactor Design Using a J-Tuned™ Process on Spring Probe Technology** Valts TREIBERGS and James HATTIS (Johnstech - USA)

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June 6, 2023 (Tuesday)	
7:00 – 8:00 CONTINENTAL BREAKFAST **7:00 – Noon REGISTRATION**	
8:00 – 8:30	**Update SWT-Crew Initiative and Mentoring Program** Karen Armendariz (Celadon Systems) and Amy Leong (FormFactor)
8:30 – 9:30 AM	**SESSION 4: RF Design Considerations** **Session Chair: Karen ARMENDARIZ (Celadon Systems - USA)**
8:30 – 9:00	**Pyramid Probe: RF Calibration and Probe Aging Considerations in HVM High Speed IO Devices** Daniel BOCK, PhD (FormFactor - USA) and Walter CONTRATA (Marvell - USA)
9:00 – 9:30	**High Speed Probe Card architecture for High End Devices** Xin-Reng FOO and Chee Hoe LIN (AMD - Singapore)
9:30 – 10:00 - Coffee Break	**POSTER SESSION** Session Chair : John CALDWELL (MJC Electronics Corporation - USA)
10:00 AM - Noon	**SESSION 5: High Power Testing Challenges** **Session Chair: Amy LEONG (FormFactor Inc. - USA)**
10:00 – 10:30	**Maximizing CCC in a Probe Card and the March to an Unburnable Probe** David RASCHKO and Najar HA**DI (**FormFactor - USA)
10:30 – 11:00	**High Heat Dissipation: Facing New Challenges with High-Power Testing at the Wafer Level** Lane HUSTON (Micron Technology, Inc. - USA)
11:00 – 11:30	**Dynamic high wattage wafer test, a novel approach to keep DUT temperature constant** Klemens REITINGER (ERS electronic GmbH - Germany)
11:30 – Noon	**High Voltage Probing goes Multi-Site** Rainer GAGGL (T.I.P.S. Messtechnik GmbH - Austria)
Noon - 13:30 – Enjoy Lunch and Networking with Colleagues and Attendees!	

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June 6, 2023 (Tuesday)

13:30 - 15:00	SESSION 6: Probecard Mechanical Characteristics Session Chair: Connie Smith (Texas Instruments)
13:30 – 14:00	**Considerations for Vertical High Probe Count Testing** Keith MARTIN (FormFactor - USA)
14:00 – 14:30	**Optimization of thermomechanical characteristics of a probe card** ChoongSik KIM, Dong Il KIM, In Buhm CHUNG, and Daejyeong LEE, Dooyun CHUNG (AMST - South Korea)
14:30 – 15:00	**Challenges and Improvement Actions for HPC Wafer Testing** Kenny TANG and Oscar LEE (TSMC - Taiwan)
15:00	**Technical Sessions Adjourn and EXPO Opens**

	SWTest EXPO - 2023
15:00 – 17:00	**SWTest 2023 – Supplier and Sponsor EXPO with new Speakers' Corner!** **Communicate, Collaborate and Celebrate!**

	SWTest Social Event
18:00 – 21:00	**SWTest 2023 – SOCIAL EVENT**
21:00PM	**Sponsor Hospitality Suites and Events**

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June 7, 2023 (Wednesday)	
7:00 - 8:00 CONTINENTAL BREAKFAST	
8:00 – 9:30	**SESSION 7: Probe Potpourri** **Session Chair: Jerry BROZ, PhD (SWTest Conference Chair- Longmont, USA)**
8:00 – 8:30	**Flying Probe Card Design for Medical and Other Challenging Applications** Luca FANELLI (SPEA S.p.A. - Italy)
8:30 – 9:00	**Automotive as a key driver for Test Demand** Panchami PHADKE (TechInsights Inc. - USA)
9:00 – 9:30	**SIlicon Photonics Wafer Testing with Edge Coupling capability in High Volume Production** Jeffrey LAM (National University of Singapore - Singapore), Soon Leng TAN (CompoundTek Pte Ltd - Singapore) and Wei Liang SIO, and Song Kim LAM, Albert NINALGA (STAr Tech – Singapore)
9:30 – 10:00	**Coffee Break**
10:00 – 11:30	**SESSION 8: Probecard Design Optimization** **Session Chair: Patrick Mui (JEM America)**
10:00 – 10:30	**MEMS probe card implementation in high volume production** Jeffrey LAM (National University of Singapore - Singapore) and Travis YAW, Song Kim LAM, Albert NINALGA (STAr Tech – Singapore)
10:30 – 11:00	**Bump test seminar and future ubump demand research** Zach HSIEH (MPI Corporation - Taiwan)
11:00 – 11:30	**Thermal challenges in fine pitch testing solutions** Pang-Chi HUANG, Paul TAI, and Kyle DALY (CHPT. Co., Ltd. - USA)
11:30 – 11:45	**SWTest 2023 Awards and Adjournment** **See you in 2024 … Travel Safe and Keep Healthy!**