Extending burn-in test at full wafer level to reduce overall cost of test at HVM

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Agenda

- **Introduction**
  - Automotive safety requirements and Burn-In
  - Wafer Level Burn-In
- **Full Wafer Level Burn-In customer requirements**
- **Technoprobe V-Mantis**
- **Full Wafer Level Burn-In probe card for SiC**
- **Qualification test and results**
- **Summary**
- **Follow up work**

Automotive safety requirements

Automotive semiconductor devices require a high level of reliability

- **Prevent early life failure at customer side**
- **Focus on digital failures**
- **Low impact on supply chain lead-time**

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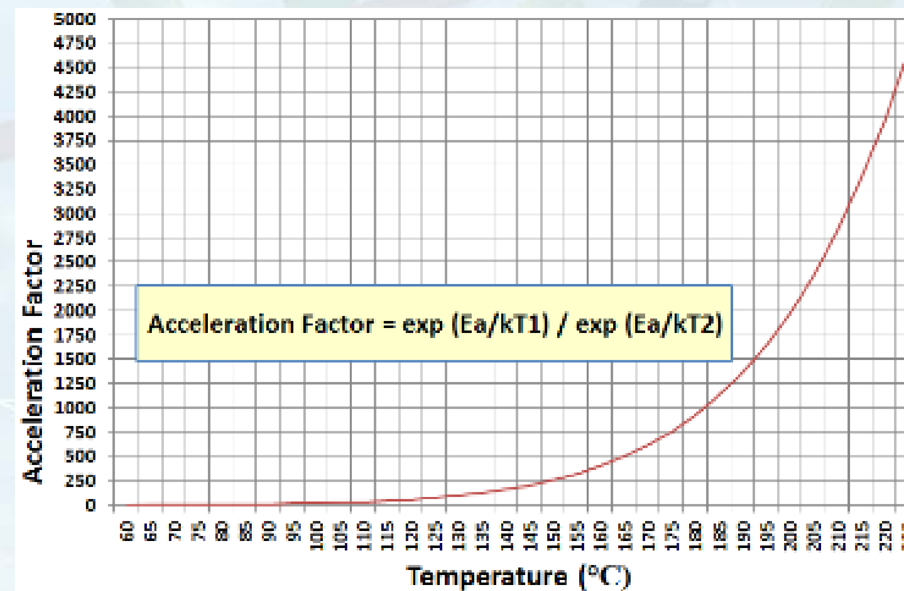
Burn-In test concept

- **Burn-In test consists of electrical stimuli on semiconductor devices at high temperature over a period of time**
  - The product failure rate is represented by the bathtub curve: the automotive industry goal is to reduce the early failures also known as "**infant mortality**" to part per billion (ppb)
  - Wafer Level Burn-In test captures such defective devices before they are packaged by the manufacturer
  - In order to capture the early failures, an acceleration factor must be applied during Burn-In test compared to normal usage of the device

Burn-In test concept

- **The accelerating factor is a function of the temperature during Burn-In test.**
- **The accelerating factor increases exponentially with temperature:**
  - Higher temperature means lower Burn-In time to capture early failures.



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Wafer Level Burn-In

- **Traditional Burn-In is performed on packaged devices with several bottlenecks:**
  - Expensive Burn-In systems
  - Temperature limit set by the package
  - Not applicable to known-good-die or bare die
  - Low throughput

- **Wafer Level Burn-In (WLBI) has several advantages vs traditional Burn-In:**
  - High parallelism
  - Use the same wafer sort equipment for functional test and to perform Burn-In
  - Very high temperatures to increase activation energy and reduce Burn-In time
  - Lower cost
  - Burn-In on known-good-die and bare die

Wafer Level Burn-In

- **Micro Burn-in**
  - Very high temperature for a short time (minutes)
  - Presented at SWTW 2018: “Micro burn-in techniques at wafer-level test to implement cost effective solutions”

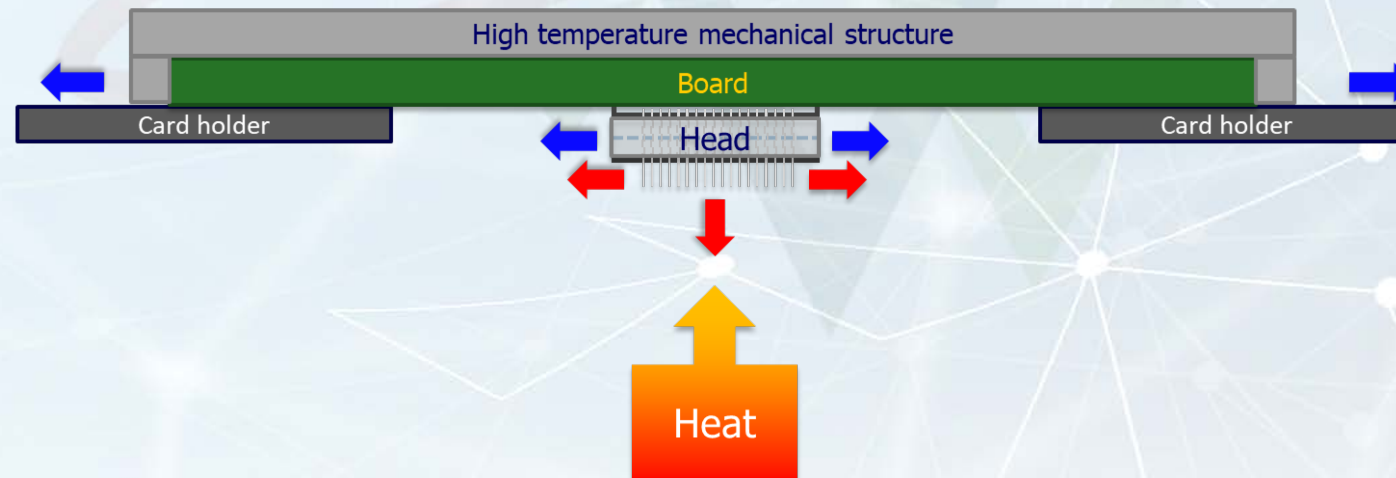
- **Full Wafer Burn-in (FWBI)**
  - Contact all devices on wafer
  - Long time typically up to 6h
  - High Temperature up to +150°C

Full Wafer Level Burn-In customer requirements

- **STM requirement for Silicon Carbide (SiC), IGBTs and MOSFETs widely used in automotive market (car electrification)**
  - Very high voltage
  - High Power
  - Manufactured in 6" wafer as of today
  - Known Good Dies and Bare dies business
  - The highest reliability level to screen infant mortality
- **Burn-In needs to be done a wafer level**
  - Full wafer contact Burn-In to support mass production
  - Conditions: 150°C, 6h, 1KV
  - Production environment

Probe card requirements for WLBI

- **Technoprobe has several years of experience in probe card design for Wafer Level Burn-In applications**
  - High temperature mechanical structure to achieve the required mechanical stability during Burn-In test
  - Dedicated wafer probing technologies to address stable contact over time



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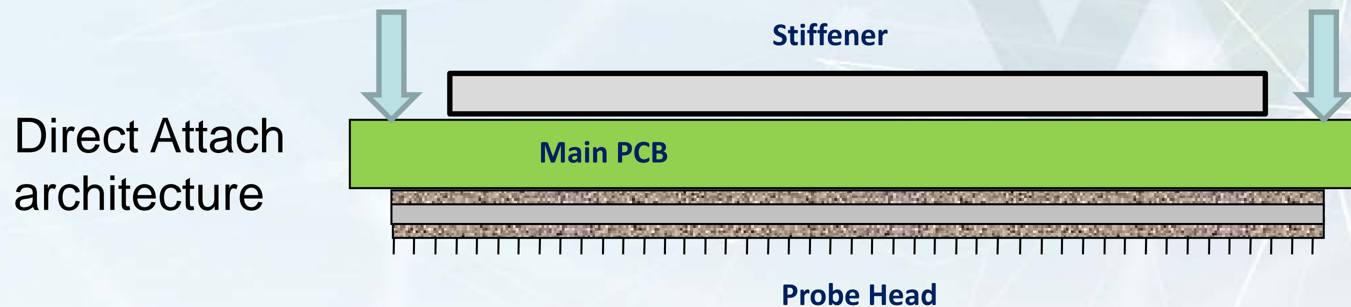
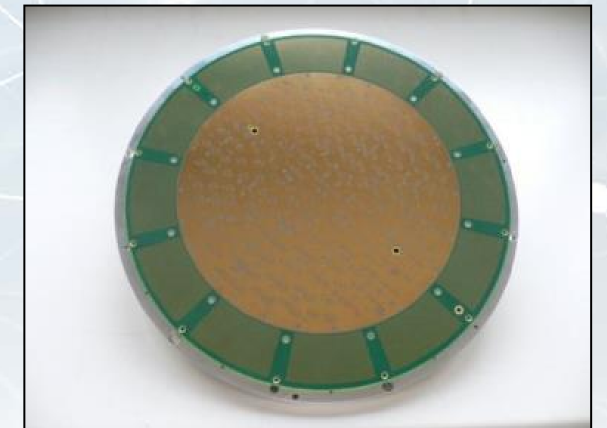
Technoprobe V-Mantis

- **V-Mantis vertical probe technology was selected as space transformation is realized thru V-Mantis probes themselves**
- **Key Advantages**
  - Shorter **Lead time** versus architectures using MLC space transformers
  - **Lower Cost solution** based on **Direct Attach**
  - **Low pad damage** due to reduced scrub motion and controlled force
  - **Cres** – Stable and Uniform across the entire lifetime of the PC (tip section)
  - **Reparability** – needle replaceable as a std vertical PC

Direct Attach architecture

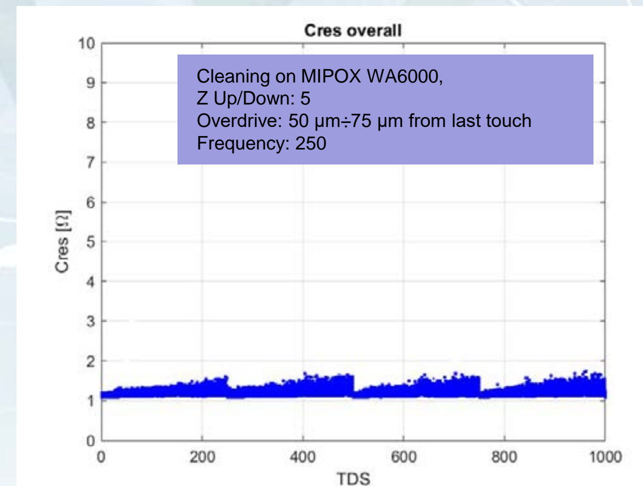


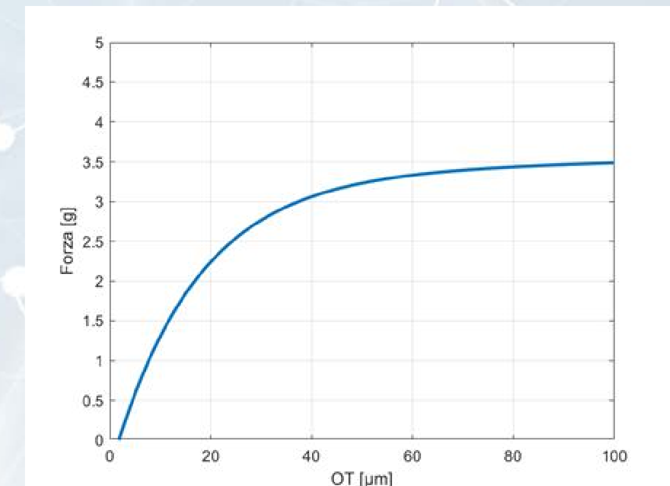


TPEG™ MEMS T7 Vertical Mantis probe technology

- **TPEG™ MEMS T7 main characteristics:**
  - Low force & low pad damage
  - Stable contact over time and temperature

PARAMETER at RT	TPEG™ MEMS T7
Alloy	LCR2
Max pin count	> 30.000 pins
Tip shape	Pointed
Tip Diameter (Typical)	9±3
X, Y alignment accuracy and Z planarity (Typical)	X,Y: ± 8 µm; Z plan: Δ 20 µm
Min pitch and configuration	70 µm Linear
Pin Current (CCC)	450 mA
Nominal Force (at 3 mils OT)	3.3g
Temperature Range	-45°C / +200°C

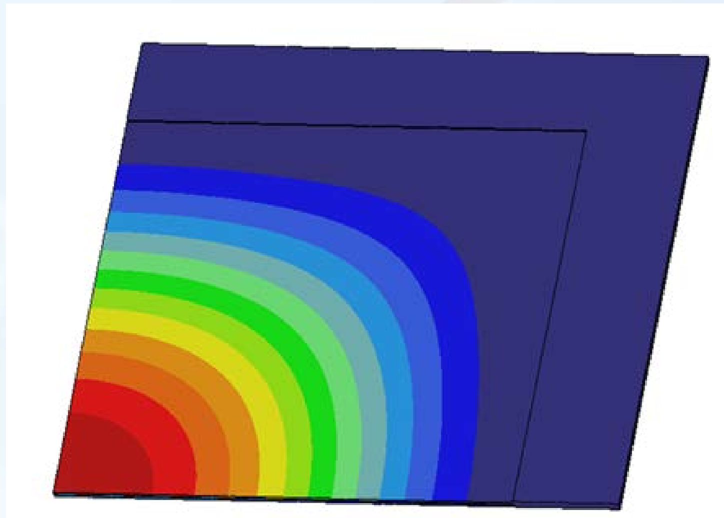


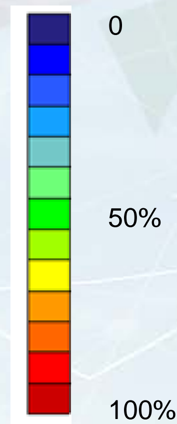


Mechanical stability

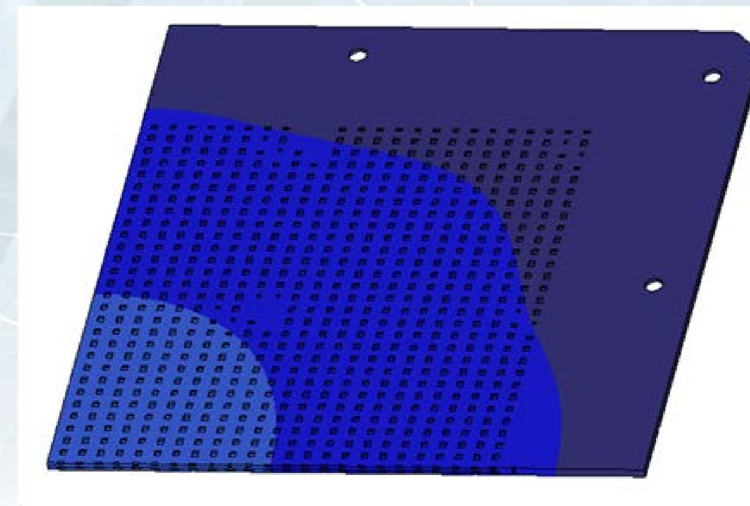
- **Large Probe head array might suffer of mechanical deformation due to large area and temperature variations**
- **Study was carried out to enhanced probe head mechanics**
  - Innovative approach based on TPEG™ MEMS T7 improved probe head mechanical stability of

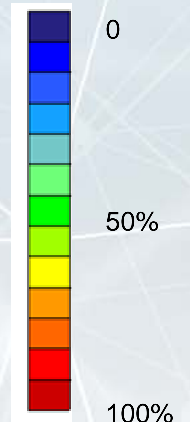
Traditional probe head approach





Innovative probe head approach with V-Mantis





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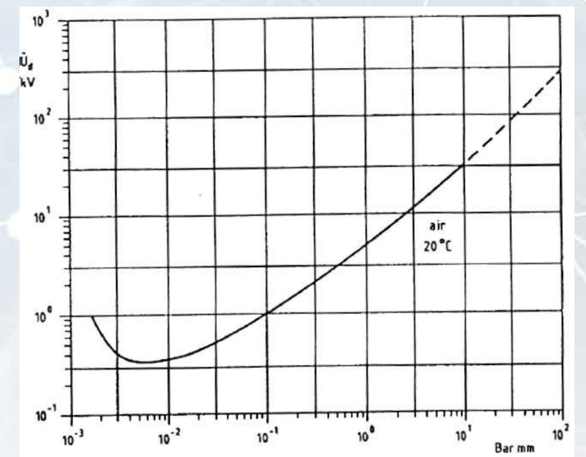
High Voltage design considerations

- **Goal to support up to 2KV**
- **PCB rules for high voltage**
  - Routing done by the internal layers and no routing done on top/bottom layer of the Probe card
  - Trace distance conditions for high voltage isolation between DUTs:
    - x,y >= 1.0mm
    - z >= 0.9mm
  - Laminate with high electric strength >50 KV/mm
- **Avoid arc effects**
  - Paschen low: discharge happens around 3KV / mm at 20°C in air at 1 ATM.



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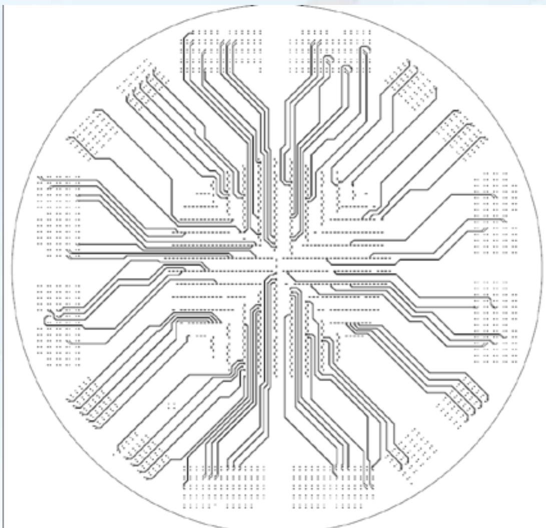
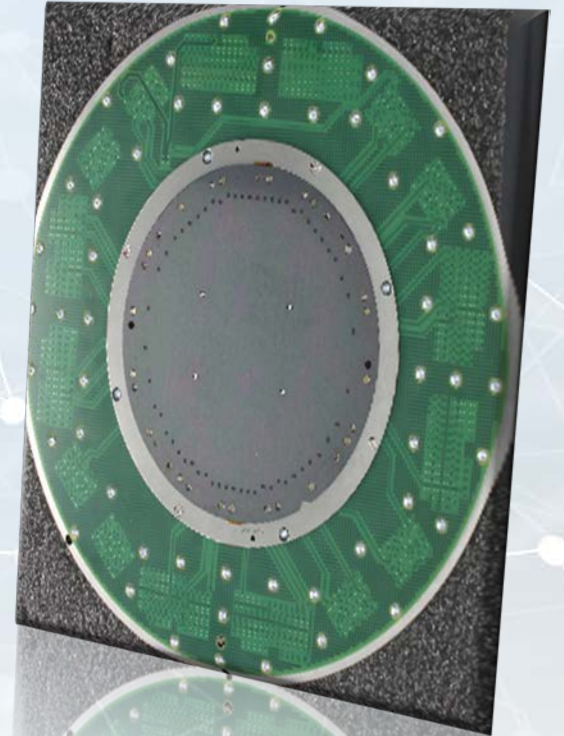
Full Wafer Level Burn-In (FWLBI) probe card for STMicroelectronic SiC product

- 6" array probe head with enhanced mechanics
- V-Mantis TPEG™ MEMS T7 probing technology
- Direct Attach space transformer
- PCB design and routing for high voltage applications





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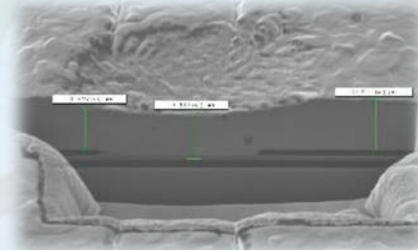
Electrical and Mechanical Qualification at STMicroelectronics

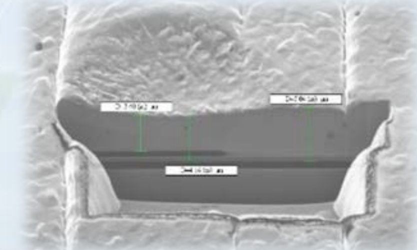
- **Qualification performed on SiC product @ 960V**
  - Mechanical characterization worst case condition
    - 6 Touch
    - 105um overdrive
    - Temperature Test 85 °C

    Cp and Cpk full inside specification

    Scrub Area < 1% of bonding area



Pad FIB Std case



Pad FIB Worst case

  - Electrical Characterization
    - HTGB @30V
    - HTRB @ 960V
    - Qualification test time: 6h x Wafer

    Electrical results inline with the expectation

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Summary

- **Automotive industry applies Burn-In technique to reduce infant mortality**
- **Full Wafer Burn-In is required for SiC, IGBT and Power MOSFET devices (Know-Good-Die / Bare Die)**
- **Technoprobe V-Mantis technology has been proved by STM as effective solution for 6inch SiC Full Wafer Burn-In**

Follow up work

- Higher voltage, more than 1KV
- Implement 6inch FWLBI in mass production / HVM
- Support 8inch wafer evolution of SiC, IGBT and Power MOSFET manufacturing

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