



# SWTEST

PROBE TODAY, FOR TOMORROW






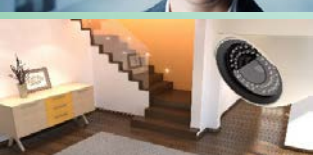
**2022 CONFERENCE**

## Probe Card Total Cost of Ownership Consumable economics in the Era of Complexity

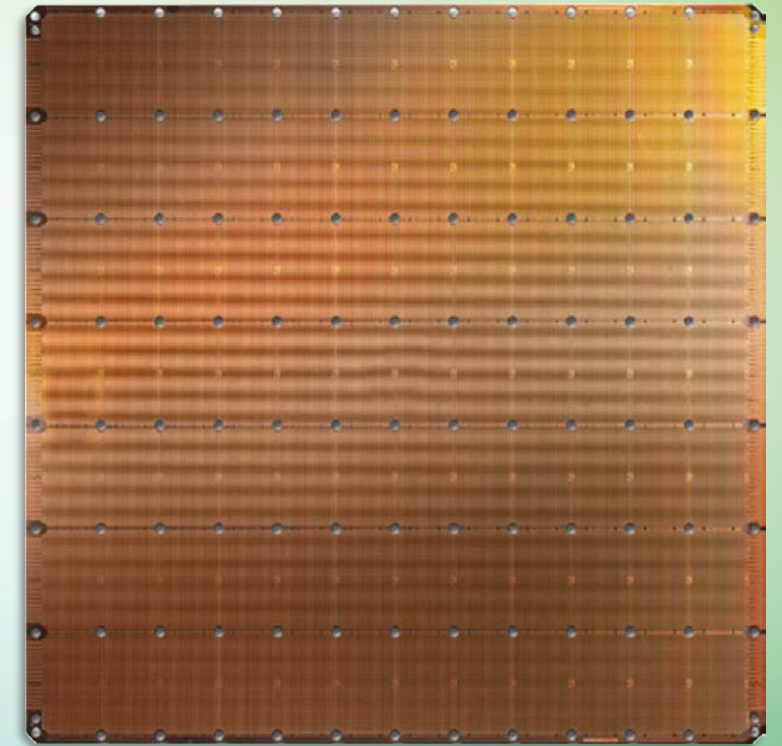
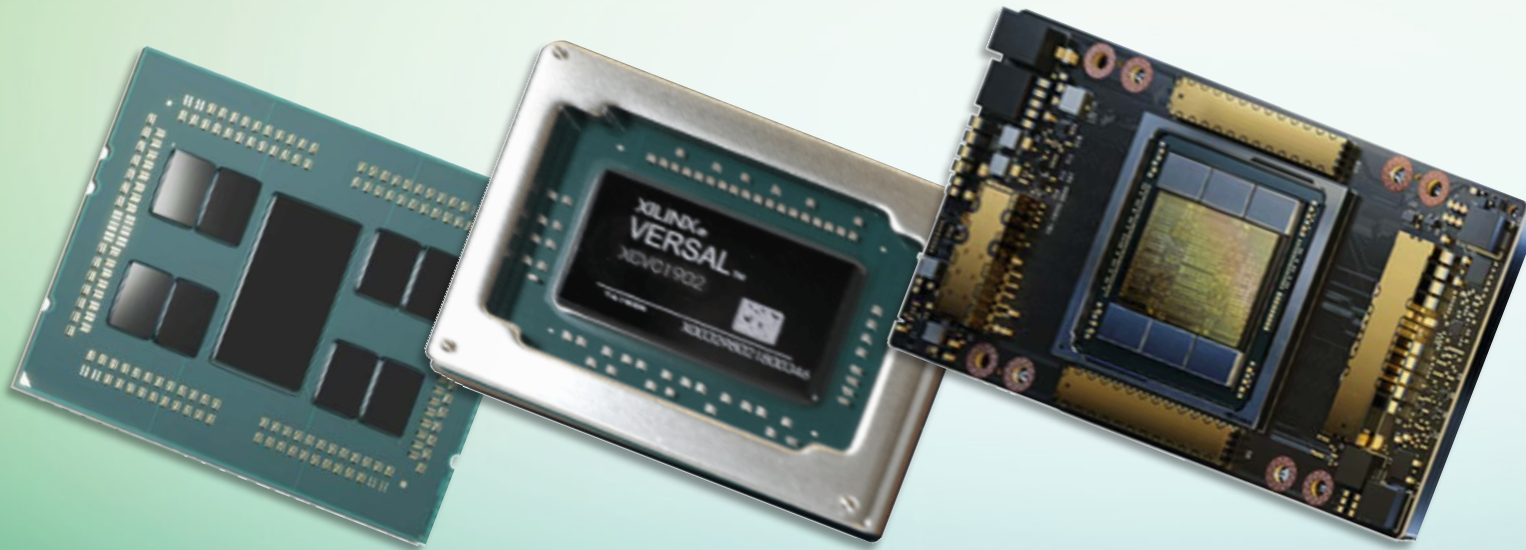
# TERADYNE

Steve Ledford  
Eric Shoemaker

# What's Driving the Semiconductor Industry Now?

	Natural Language Processing	<b>Common Requirements</b>  Enormous Processing Power  Huge Mobile Network Capacity  Gigantic Storage	<b>Key Device Trends</b>  <b>Processors</b> <ul style="list-style-type: none"><li>• Rapid adoption of new process</li><li>• Neural Coprocessing</li><li>• Aggressive AQLs</li></ul> <b>Mobile Network</b> <ul style="list-style-type: none"><li>• 5G Infrastructure</li><li>• mmWave</li><li>• Expanding Backhaul</li></ul> <b>Storage</b> <ul style="list-style-type: none"><li>• Flash: More layers</li><li>• DRAM: faster speed</li><li>• HDD: Still a thing</li></ul>
	Autonomous Vehicles		
	Augmented Reality		
	Personal Medicine		
	Facial and Image Recognition		
	Video - Security		

# High Performance Computing Enabled by N7 and N5 Complexity



## AMD Epyc

39B Transistors  
64 cores

## Xilinx Versal

37B Transistors  
3.3M logic cells

## nVidia Ampere

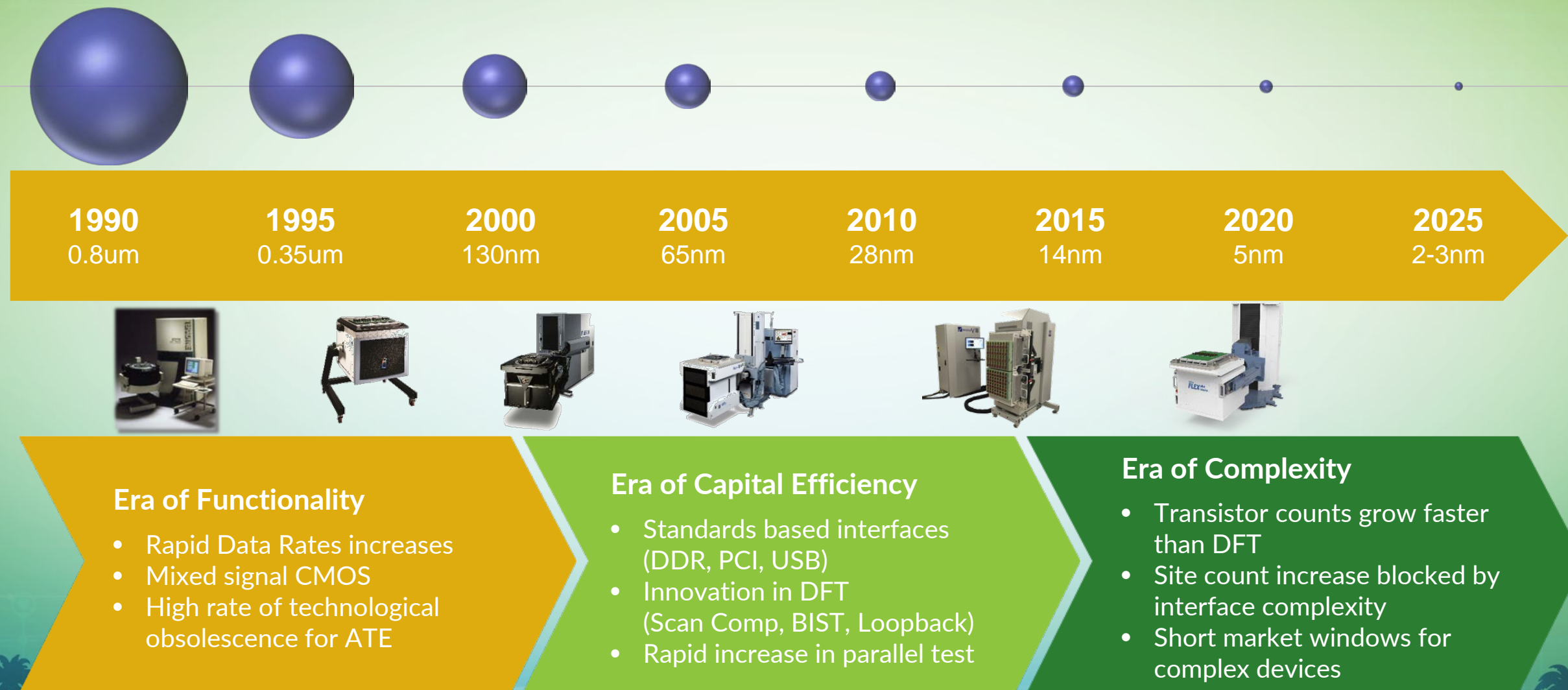
54B Transistors  
6912 CUDA cores

## Cerebras WSE2

2600B Transistors  
Wafer Scale Engine

Sources: Wikipedia, Company Websites


# Semiconductor Test: A New Era of Complexity



# Interface Technical Complexity Check-in

**“2 x 4 Scaling” = 2x pins, 2x performance,  
every 4 years**

Complexity trends are on pace to be at 2022  
targets (1 cycle) or in some cases beyond



**SW Test Workshop**  
Semiconductor Wafer Test Workshop

**Device Interface Challenges of the  
Next Decade**

**TERADYNE**

Steve Ledford  
Teradyne

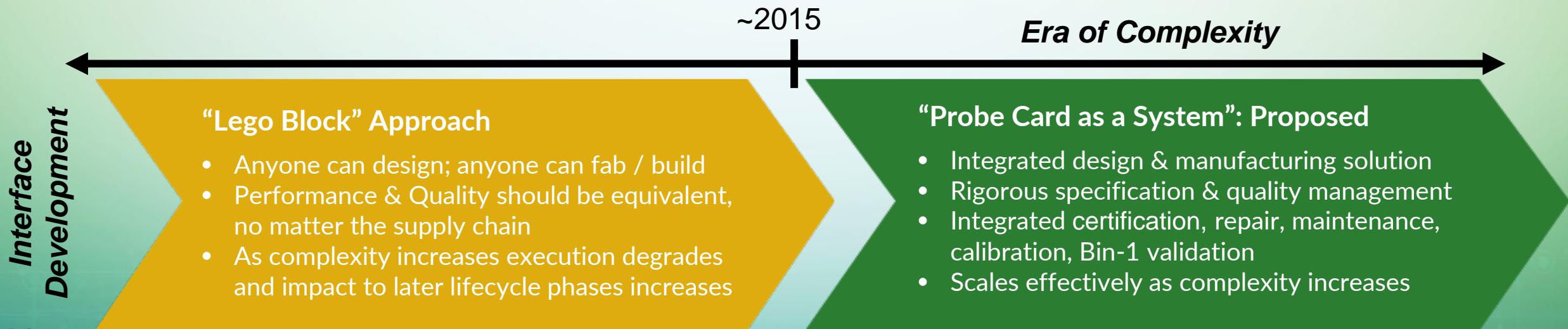
June 3-6, 2018

		2018 Level 4	2022 Level 5	2026 Level 6
Pin Density	Pin pitch	90um	70um ✓	50um
	Total Contact Force	80 Kg	150 Kg ✓	250 Kg
I/O Speed	Digital	32 Gbps	64 Gbps ✓	128 Gbps
	RF / mmWave	< 12 GHz	29 GHz ✓	+60 GHz
Device Power	Main power	900 mV	750 mV ✓	625 mV
	Single Rail	35A	50A ✓	100A
	Impedance	2.2 mOhm	1.4 mOhm ✓	0.8 mOhm
Thermal	Self Heating	75 W	150 W ✓	300 W
	Operating Range	0 to +80C	0 to +105C ✓	-20 to +125C
Most Expensive Probe Card		\$400K *	> \$500K	> \$700K

\* Source: VLSI Research

# Complexity Drives Cost Management and Development Paradigms

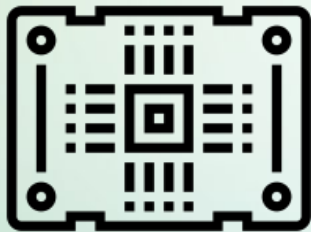
- The last major look at cost management was the ISMI Probe Card Cost of Ownership model (2007)
  - In 2007: DRAM single-contact probe cards were just ramping; no SoC in production; Cobra was dominant vertical tech
- The Semiconductor industry has changed significantly impacting probe card complexity:
  - 12x probe card interface complexity (14 years of “2x4 scaling”): PCB and MLO layers, electro-mechanical performance
  - Wide adoption of new probe technologies such as MEMs probe needles
  - Combined has exposed major “cracks” in interface development principles and strategies used widely in the industry



# Complexity Impact on Time and Yield

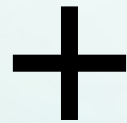
The Total Cost of Ownership (TCO) model builds on previous models to include the impact to time and entitled yield, key life cycle metrics

Better Performance + Quality + OTD = Lower cost of ownership



## Interface Eng

- Interface Cost
- Design Errors
- **On-Time** Delivery (OTD)



## Test Eng

- Test **Time**
- Test Quality (zero escapes)



## Ramp Eng

- NPI Bring-up **time** (TTM)
- Test Stability / Repeatability



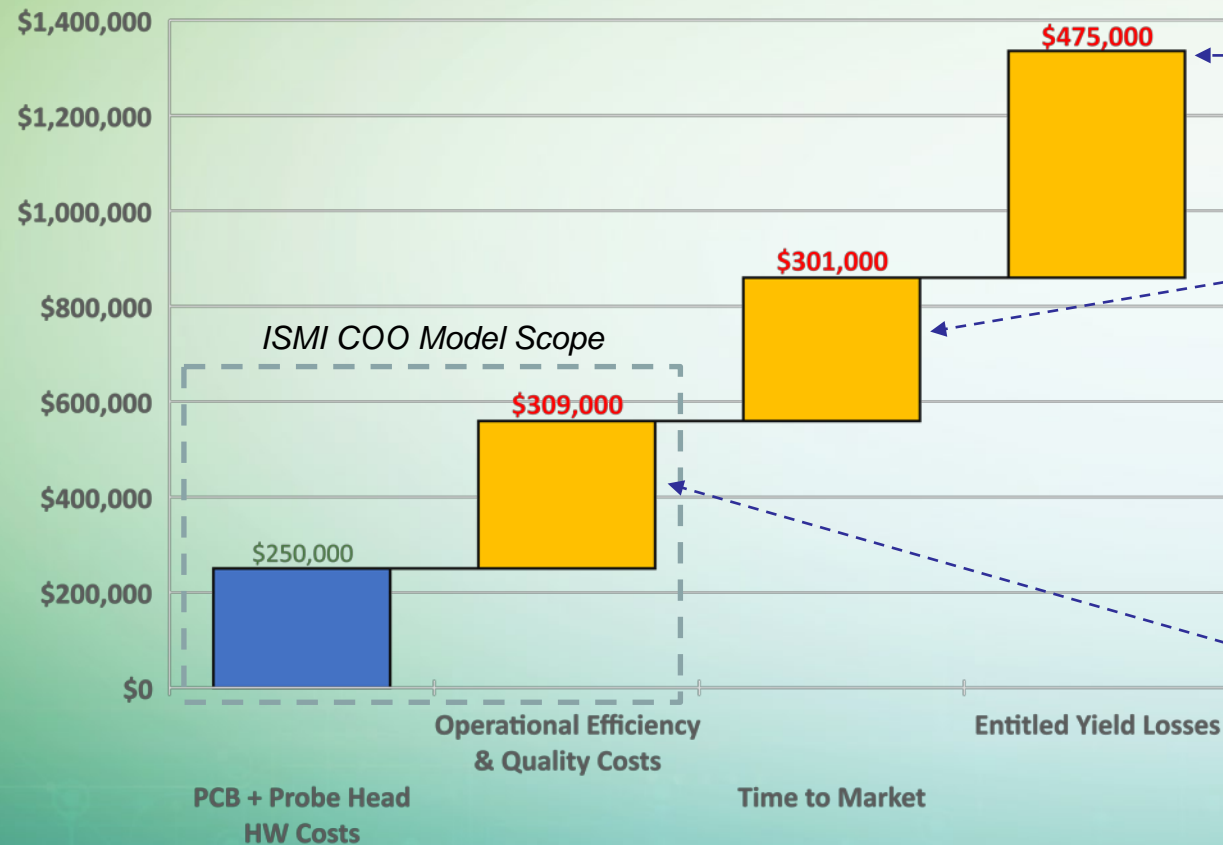
## Production Eng

- Ramp-up **time** (TTV)
- Throughput
- **Entitled Yield**

## KPIs

# Case Study: Time and Yield dominate TCO

## Probe Card Total Cost of Ownership Case Study: Legacy “***Lego Block***” Approach



“Lego Block” approach of lowest cost pieces can lead to significant cost increases across the device life cycle:

### Entitled Yield Losses: 1.5 – 2x probe card cost!

- Interface performance limits device measurement accuracy, resolution, and repeatability

### Time to Market Impacts: 1 – 1.5x probe card cost!

- Opportunity cost of lost sales in a project’s market lifecycle (mobile in particular)
- Engineering time on test cell / HW / program debug during bring-up; and repeated Bin-1 attempts before & after repairs

### Previous ISMI cost model addressed OEE & Quality:

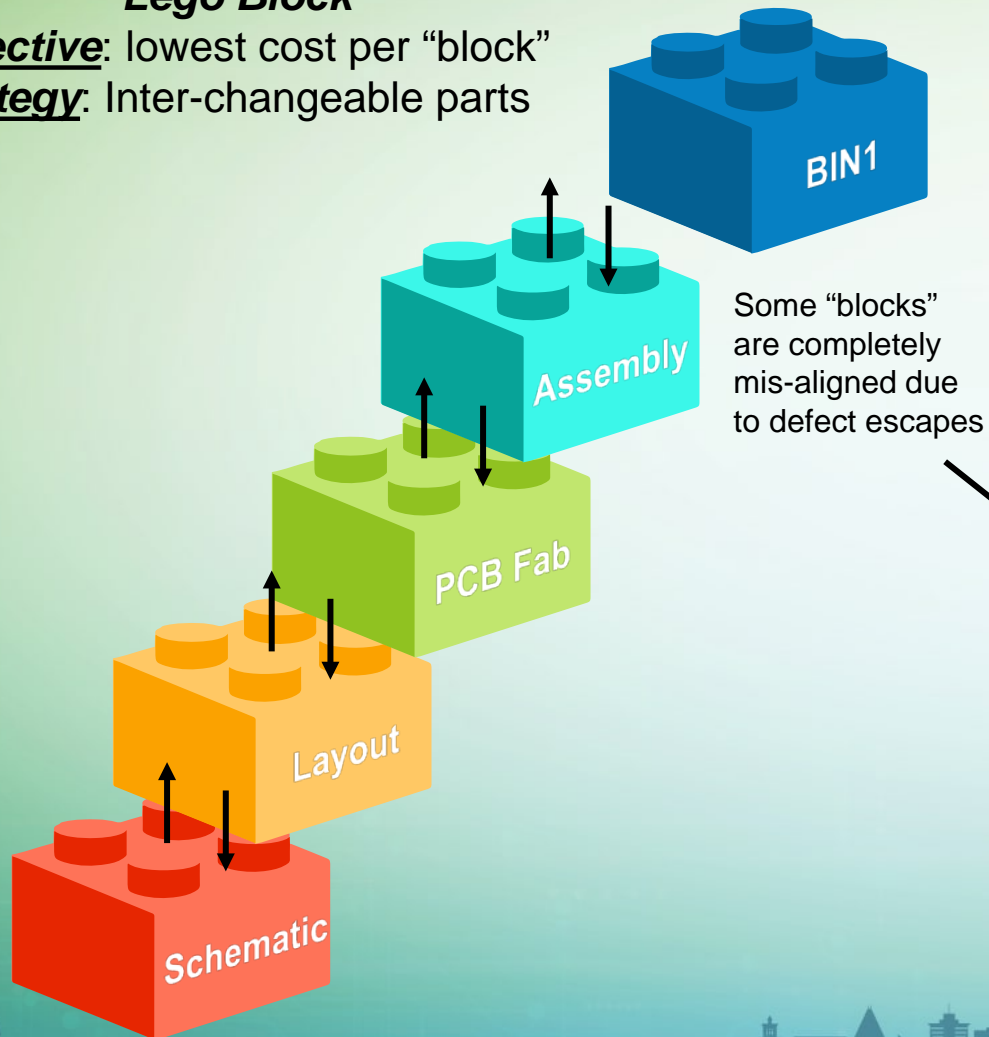
- Same principles but due to technical complexity the strategy and means to execute need to be updated
- Includes: Site shutdown, retest, spares, needle life, etc

# TCO Killer: Unmanaged & Undetected Defects

## “Lego Block”

**Objective:** lowest cost per “block”

**Strategy:** Inter-changeable parts

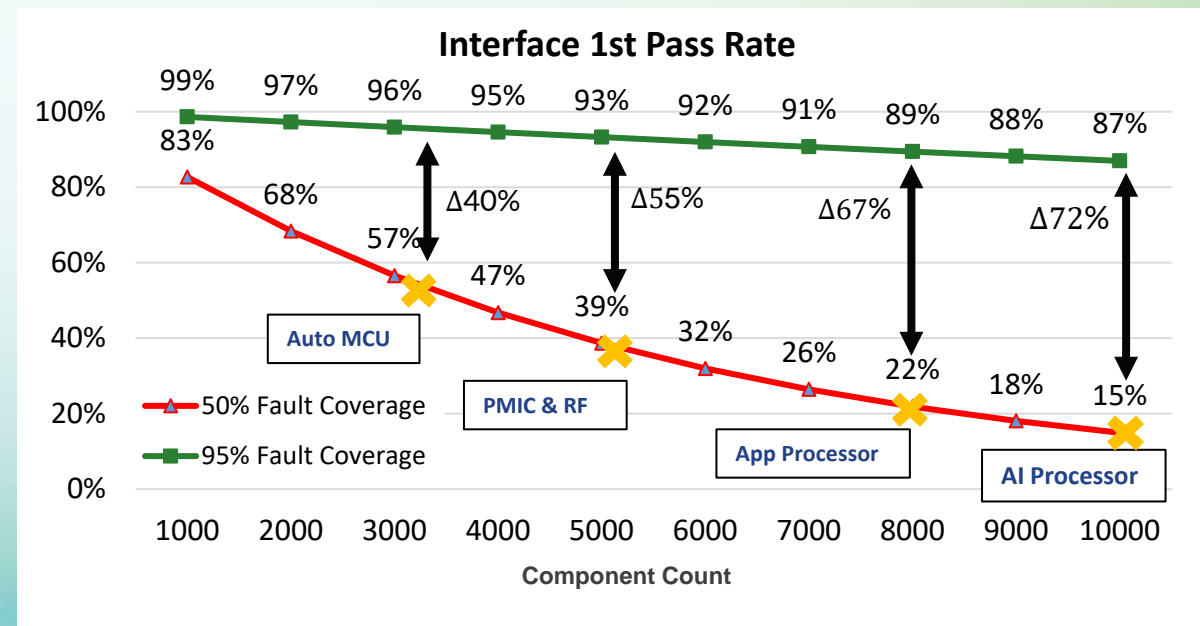


Defects passed on to later processes significantly impact TCoO

## Process Capability Case Study: Interface Test Fault Coverage

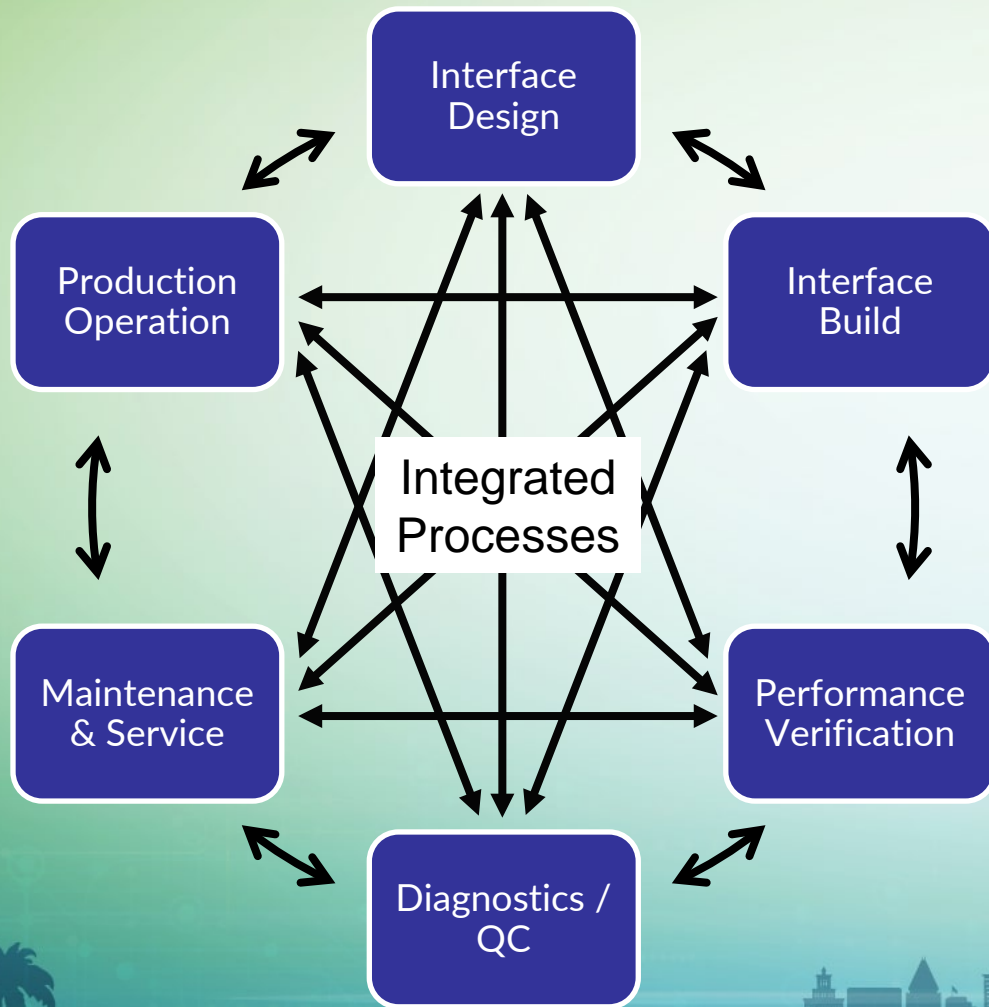
- Flying Probe Test (FPT) and Probe Card Analyzer capability limits (measurement capability, accuracy, access points, etc) result in **less than 50% fault coverage!**
  - Lack of rigorous Interface Fault Model
  - Poor test capability and methodology to implement fault coverage
- Smaller feature sizes introduce new defect mechanisms combined with rapidly increasing opportunities for failure

**Low Fault Coverage Test = Very low 1<sup>st</sup> Pass Rate = Delayed Bring-up (TTM)**



# “Probe Card as a System” Principles

## "Probe Card as a System"



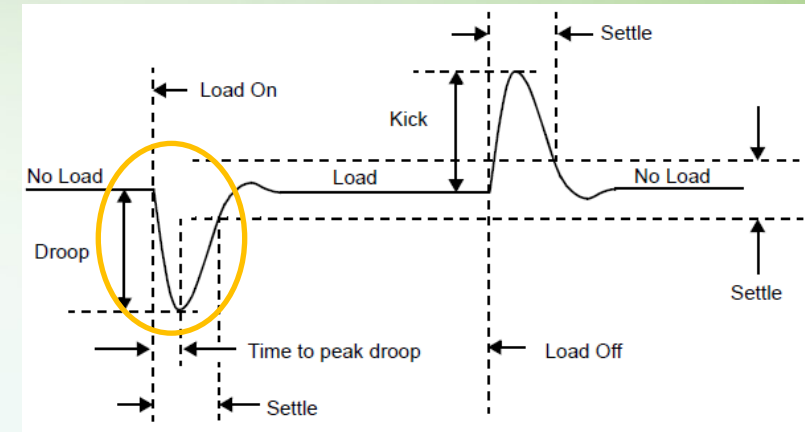
**Key Principle:** Each major phase of the Interface lifecycle is dependent on and impacts the robustness of the others

## Master the technical “white space” across the life cycle

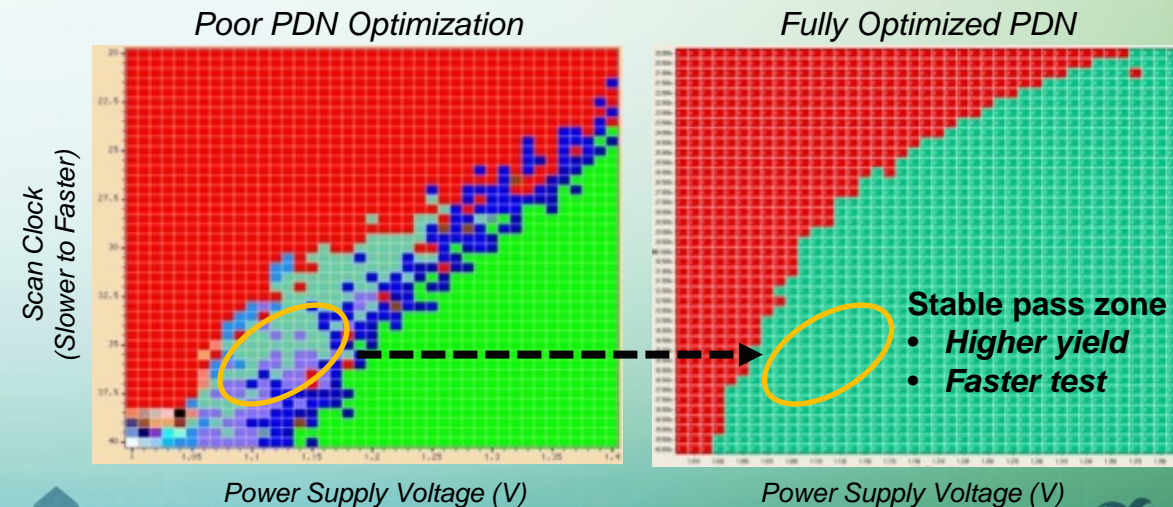
- **Example: Integrated Interface Design enables**
  - Repeatable manufacturing yields for on-time delivery & ability to ramp volume
  - PI/SI performance for maximum entitled yields in Production
  - Performance Verification can validate the interface truly performs to the simulated results and trust in the test results
- **Example: Integrated Diagnostics & QC enables**
  - Higher probe card validation test coverage and faster bring-up & repairs for Engineers
  - Higher reliability and calibrated/characterized signal paths
- **Example: Integrated Maintenance and Service enables**
  - Longer operating life of Probe Cards & needles, and real-time monitoring for maintenance
  - Extend interface operating life
- **All supported by a “Systems Engineering Capability” roadmap that qualifies new technologies off the project critical path**

# Case Study: Poor Performance impacts Entitled Yield

- **Problem: Over-kill of good die in high-performance application**
  - Lost revenue, higher cost of goods sold, longer test times
- **Root Cause: Insufficient test margin due to poor power integrity**
  - Poor Power Integrity response (droop and kick) in high-current operation (ex: high-speed scan)
  - Wide site-to-site variation and poor test result stability
- **“Probe Card as a System”: Integrated Design, Manufacturing, Performance Verification, and QC**
  - IC yield increase of +1%
  - Excellent parallel test stability enabled by site-to-site matching of +/- 2%.
  - Full Performance Verification to validate and refine simulation models and fabrication process for future designs
  - Yield improvement generated more cost savings than price of the Probe Cards

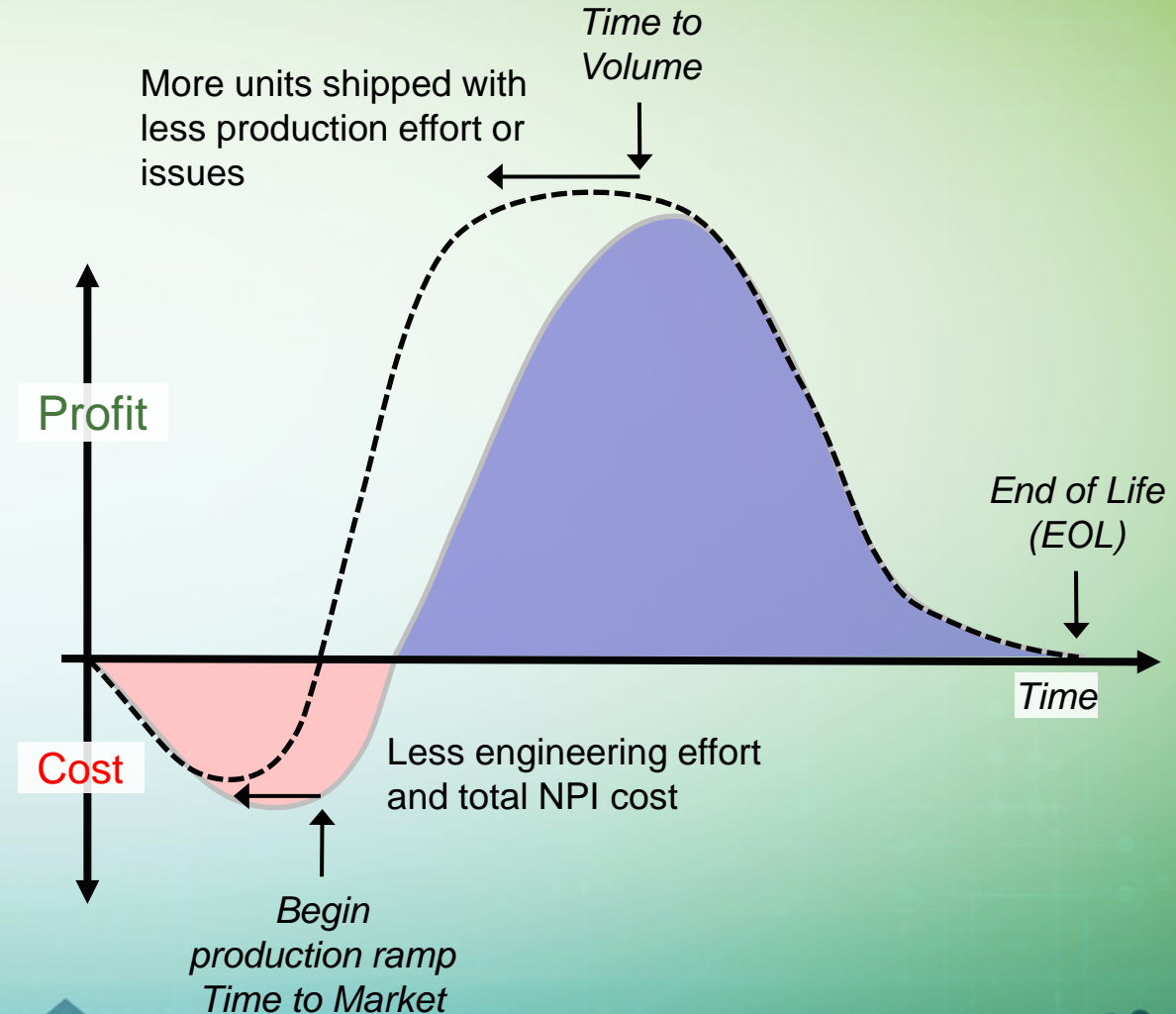


Time domain response of the Power Supply to transistor switching  
Large droop → Yield below targets and/or lower device specs



# Case Study: Undetected defects impact Time to Market & Volume

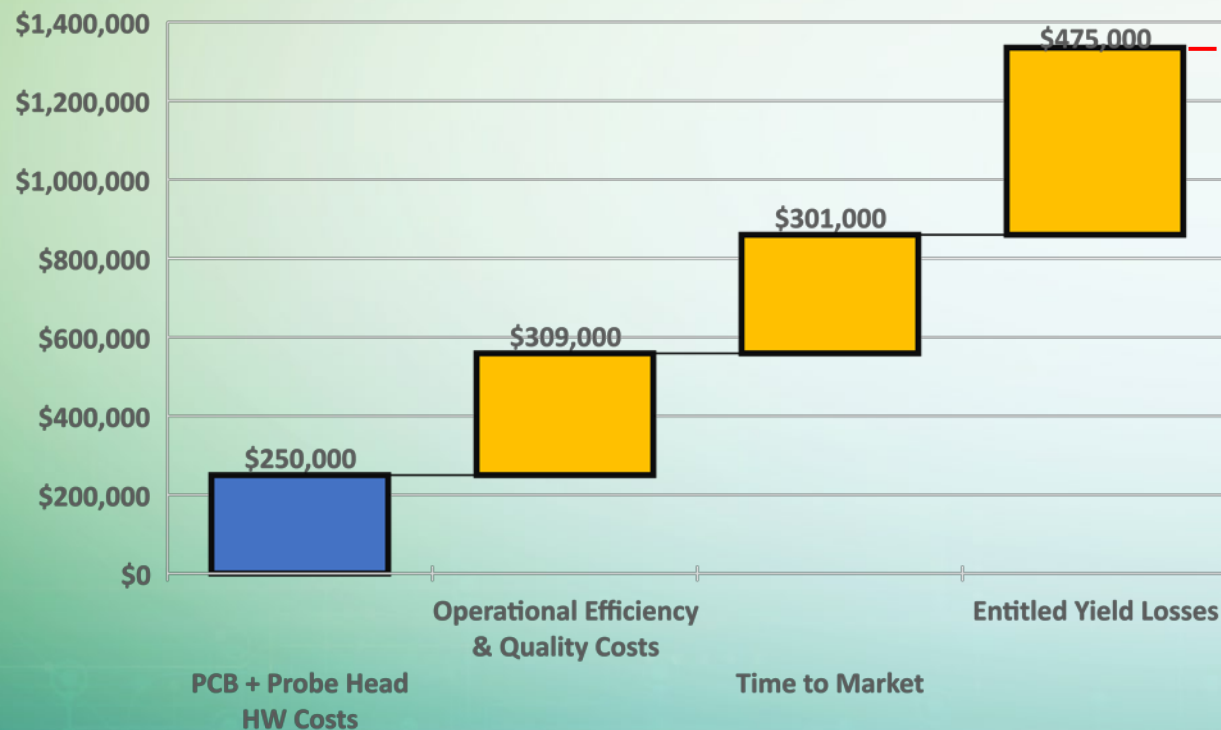
- **Problem: Defective probe cards lead to wasted Engineering time “chasing ghosts” in silicon and test program, resulting in NPI bring-up delays**
  - Engineers dealing with untested silicon, new test program, and new HW all at the same time
  - Any probe card issues introduce random, unpredictable defects into a complex debug process during a time-sensitive period trying to get silicon into production
- **Root Cause: Unknown defects create unpredictable test results**
  - Low fault coverage and measurement capability for Flying Probe test (FPT) and Probe Card Analyzer
  - No “golden units” available to “Bin-1 certify” the probe card and eliminate the probe card from the fault tree
- **“Probe Card as a System”: Integrated Diagnostics into Design, QC, Service, and Production**
  - NPI bring-up from “days to hours” and ramp from “weeks to days”
  - Significant savings in NPI Engineering and higher total Revenue



# Case Study: Your Probe Card Can Pay For Itself!

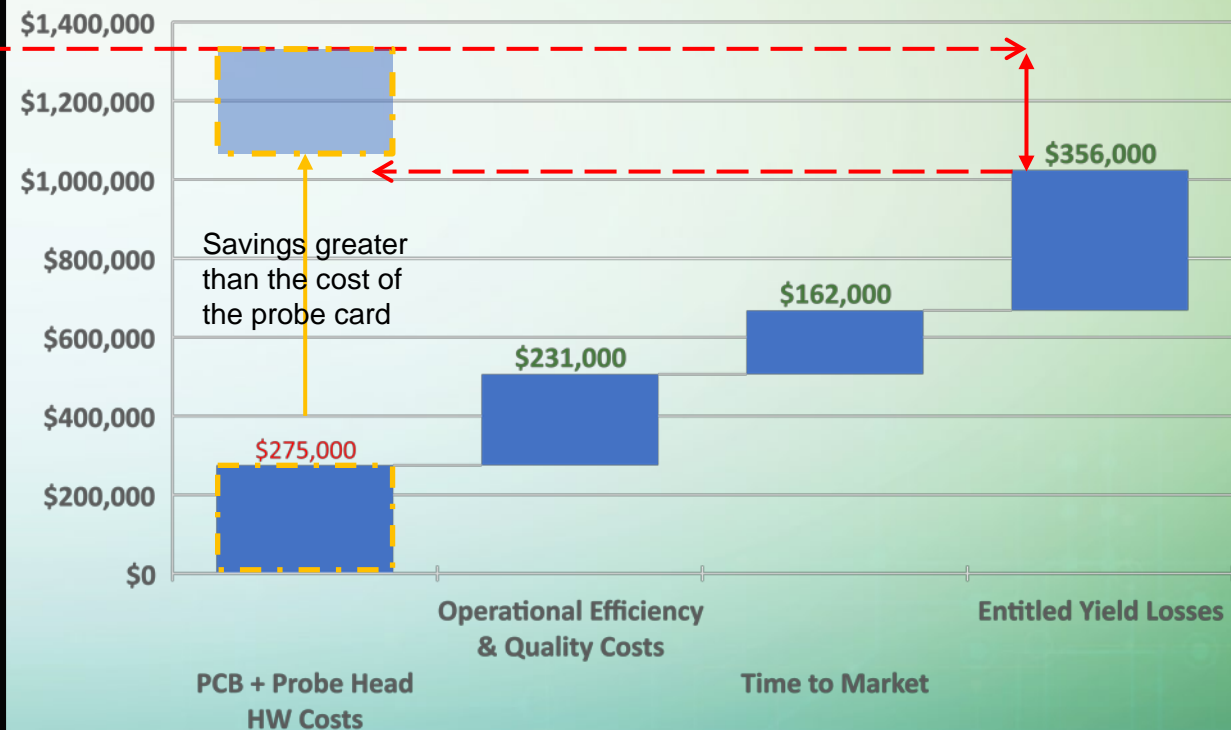
*TCO quantifies hidden costs and inefficiencies that can be 2-3x the cost of the probe card*

Probe Card Total Cost of Ownership  
Case Study: Legacy "Lego Block" Approach



*A probe card that is on-time, defect free, with full performance can drive savings greater than its cost!*

Probe Card Total Cost of Ownership  
Case Study: "Probe Card as a System"



# Case Study: Model Inputs & Results

Model Assumptions	“Lego Block”	“Probe Card as a System”	Impact
Expected Product Lifetime Revenue	\$750M	\$750M	
Production lifetime (years)	1.5	1.5	
Product Net Profit Margin target	40%	40%	
Expected Total Test Cells in Production	15	15	
Total Probe Card Cost	\$250,000	\$275,000	Increase 10%
Engineering Labor Rate (hourly)	\$125	\$125	
Test Cell Hourly Rate (hourly)	\$150	\$150	
HW Bring-up Engineering Effort (days)	45	33.75	Reduced 25%
Production Test Cell OEE Expected target	85%	85%	
Production Release Timing Delay (days)	7	3.5	Reduced 50%
Average Site Shutdown (1 out of X sites)	16	21.28	Improved 33%
Typical HW Spares Need (1 out of X sets)	10	15	Improved 50%
Probe test time per wafer (hours)	3	3	
Probe Test Time per Touchdown (minutes)	1.5	1.5	
Needle Touchdown Lifetime (cycles)	500,000	665,000	Improved 33%
Wafer Cost	\$7,500	\$7,500	
Modeled probe test yield expectations	85%	85%	
Entitled yield loss (% below model)	3.0%	2.3%	Reduced 25%

# TCO Key Success Criteria & Impact

## Examples of Key Success Criteria

- ✓ On-time delivery metrics & execution planning tools including risk mitigation
- ✓ Fault-model-driven diagnostic tools, including signal path and component diagnostic test traceability
- ✓ Visual defect detection coverage & resolution
- ✓ Site-to-site simulation measurement results (target <5% variation)
- ✓ Full-board signal-path simulations at speed
- ✓ Interface board level RF calibration and program integration
- ✓ Needle/Socket performance verification and QC

- **Stop “chasing ghosts” during new IC bring-ups in order to stay on schedule**
  - Is the problem in silicon, software, tester, or probe card?
  - Eliminate “Probe Card” from the fault tree and speed up debug, validation, and production release!
- **Get the entitled yields your design should generate and maximize your test cell throughput**
  - Don’t let the probe cards be the bottleneck in your test measurement capability
  - Require full-board simulations and bench validations/characterizations to match

# Conclusion

- Legacy “Lego Block” development strategy has significant scaling limitations as complexity increases
  - Delayed product launches (time) and lower performance device limits and specs (yield)
- By applying a “Probe Card as a System” approach the Probe Card can pay for itself, thereby greatly improving the Total Cost of Ownership (TCO)
  - Improvements to Time and Yield can return value of 2x to 3x the cost of the probe card
  - Each major phase of the Interface lifecycle is dependent on and impacts the robustness of the others
  - Master the technical “white space” across the life cycle utilizing a fully integrated development process

**Best Performance + Quality + OTD = Best Total Cost of Ownership**