SWTEST

PROBE TODAY, FOR TOMORROW

2022 CONFERENCE

Shifting Left = More Wafer Probe

Real-World Implications

ADVANTEST®

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Last-Year's News

https://www.youtube.com/watch?v=YObxvk5sqSQ&t=4s

https://www.youtube.com/watch?v=352Ds89PoBM&t=1401s

The industry is clearly changing. The role of wafer probe is expanding. Let's discuss what this means for all of us.

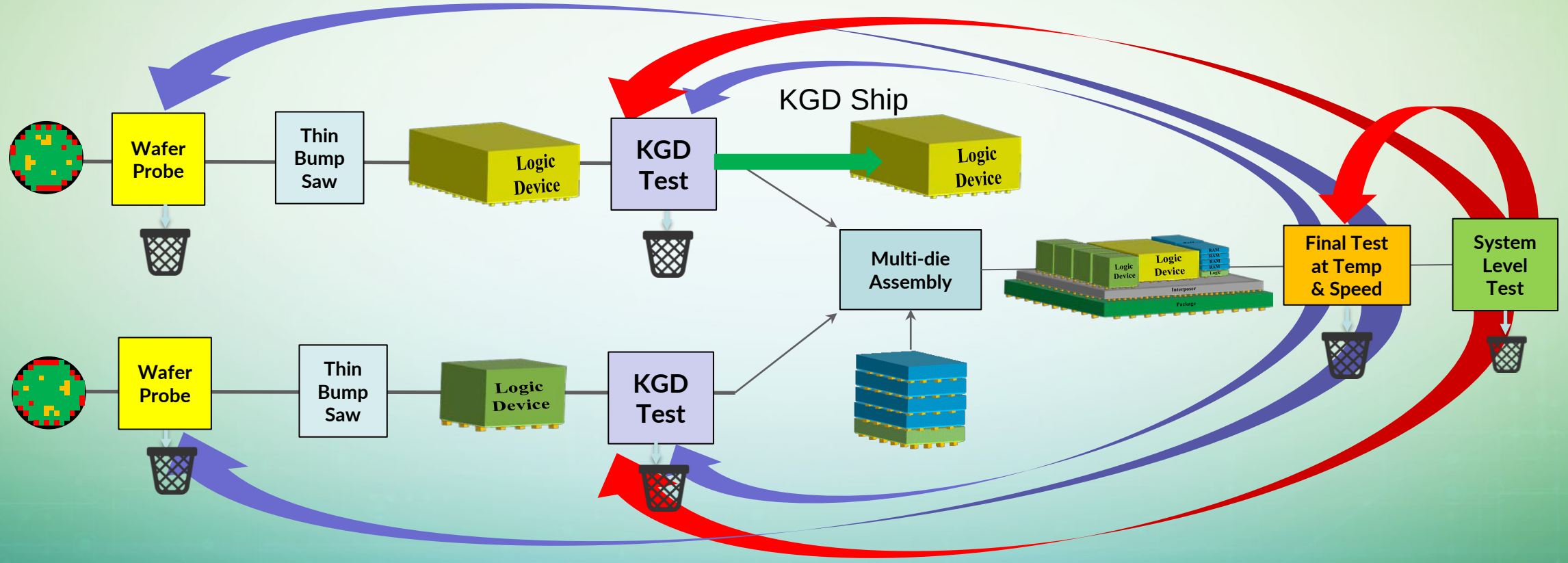
Outline

- Review what is Shifting Left and what it means for wafer probe.
- Discuss implications for probe.
- Explore best methods for power delivery at wafer probe.
- Mention leading edge adaptive techniques to avoid probe-burn.
- Summary – Implications for today, tomorrow, and all of us.

What is the Shift-Left Trend?

Two forces driving this:

1. More data sooner ➔ Reduces costs.
2. Known-Good-Die ➔ Better Chiplet Yields



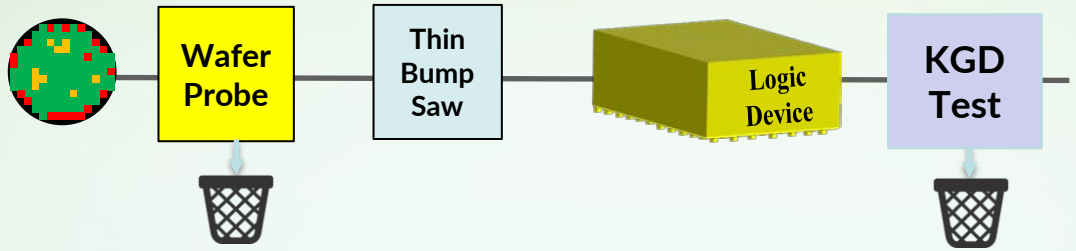
Why is this Happening?

- In the 1970's HP put forth the concept that:
  - "The cost of detecting a failure increases by an order of magnitude (10x) with each manufacturing step."

➔ More testing sooner has a direct impact on your bottom line!

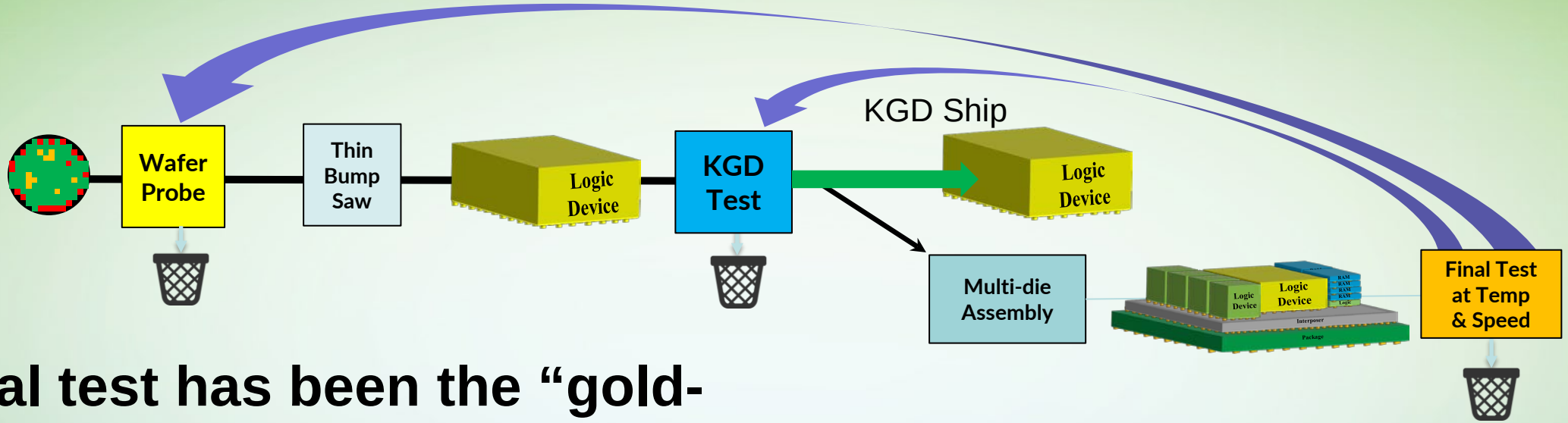
Two-Step Wafer Probe

- **All semiconductors are tested at multiple temperatures.**



- **Separating out the two test steps allows more failures to be captured sooner. This has many benefits including:**
  1. Faults induced by thin / bump / saw operation found.
  2. Final device thermal pathways in place (no extra cooling/heating from neighbor parts)
  3. Faster thermal response time due to reduce thermal mass.
  4. Full Active-Thermal-Control (like at final test) is possible
  5. Improves final test yields (and costs) and also reduces number of bad parts being packaged.

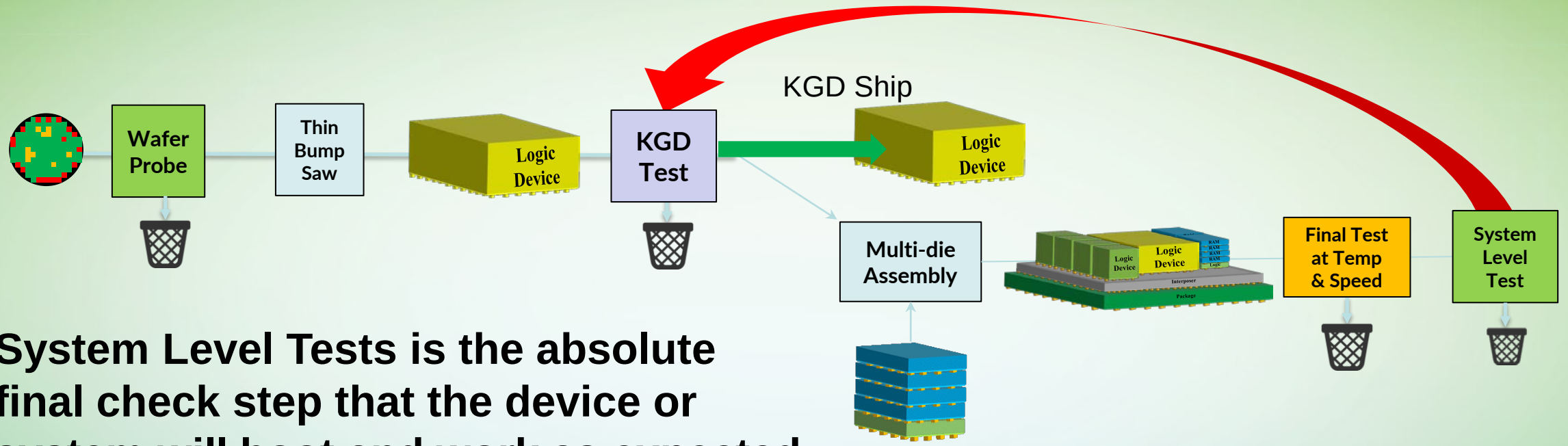
Final Test at Wafer Sort



Final test has been the "gold-standard" of the industry for years to confirm a device is ready to ship.

Doing final-test at Wafer Probe requires us to move High-Speed and High-Power tests to the Wafer Probe environment.

System Level Test at Wafer Sort



System Level Tests is the absolute final check step that the device or system will boot and work as expected.

Two challenges to doing this are 1) Creative ways to minimize SLT test times, and 2) ATE based instruments to support this bring up.

Doing SLT at Wafer Probe requires us to move High-Speed and High-Power tests to the Wafer Probe environment.

Pains and Gains

- **What do we need to shift-left all of this test content?**
  - Probe cards with 10's of thousands probes and 100's of high-speed probes (>25GHz BW and ↑)
  - Probe cards with HSIO and high-power (500~1500A) delivery designed in. (High CCC, probe-card cooling, more power planes)
  - Much more attention to Signal and Power Integrity when designing probe cards and probe heads.
  - ATE cards which support System Level Testing or at least System Like Testing.

- **What does this get us?**
  - Chiplets which are as good as fully-tested packaged parts have always been. (KGD?)
  - Reduced product costs by only packaging good parts. This is especially critical when integrating multiple devices together on one assembly. (see my original Shift-Left paper for a cost savings analysis of this value.)
  - Less labor and ATE costs. Work on the good ones and sideline the rest.
  - More data sooner. Outing failed parts sooner allows failure analysis to find the issues quicker.

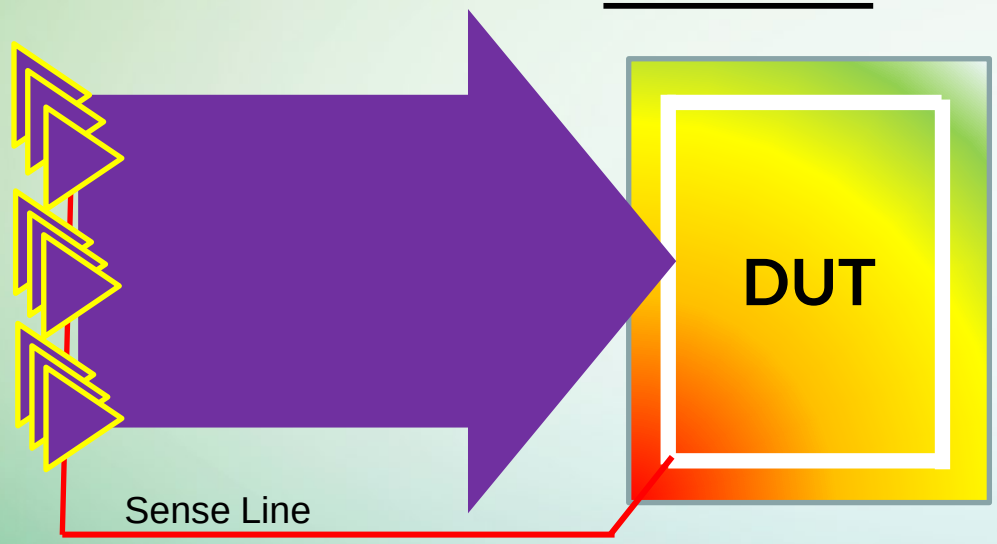
So, How Do We Deliver This Much Current?

(without burning probes)

- **With the introduction of the XPS256 Advantest has set a new standard in power delivery for the industry. What's different?**

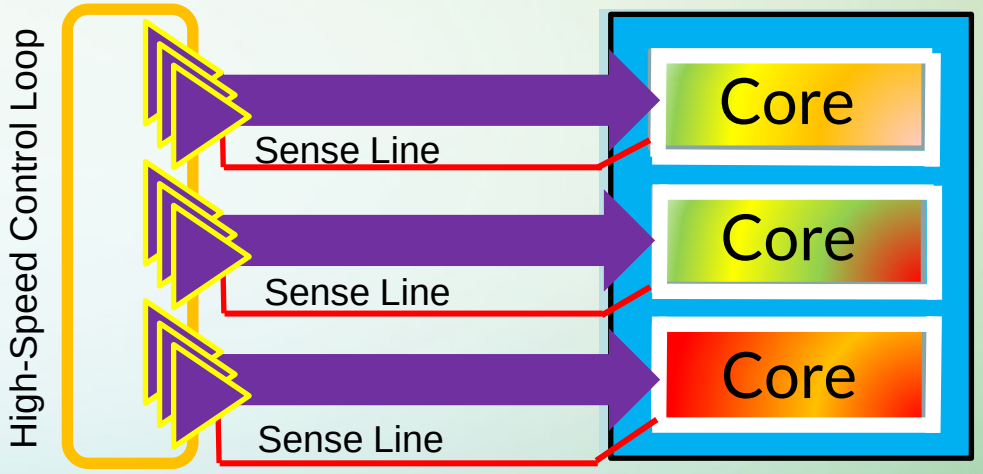
"Fine-Granularity Power Delivery"

In the Past



- Supply ganging made one big voltage source.
- Vcc defined at one-point on the device (at sense)
- Any delivery path issues resulted in 100's of amps funneling to the remaining interconnects.

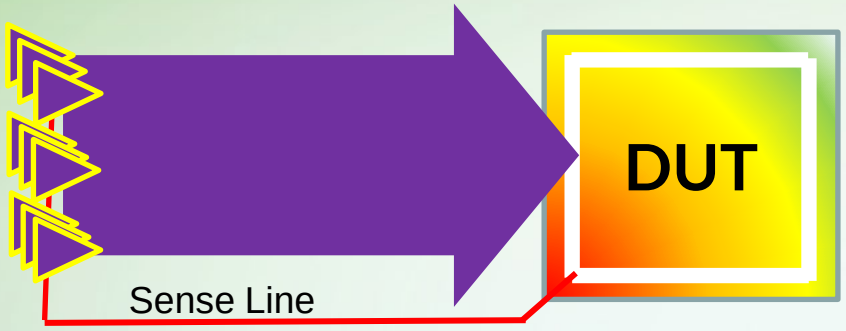
Now – XPS256



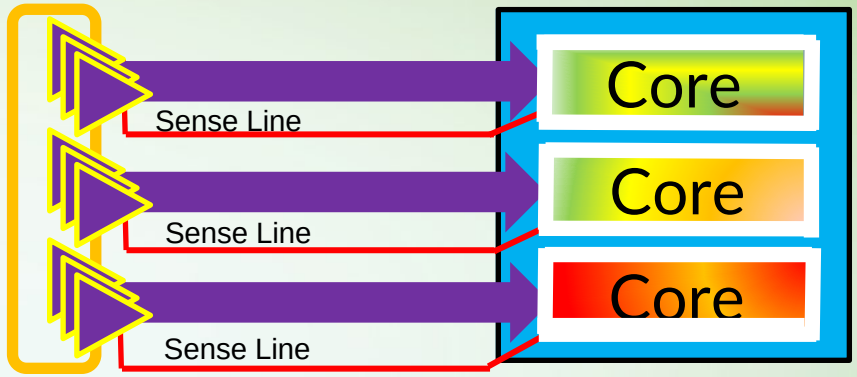
- ATE supply divided up into smaller planes.
- Vcc defined at multiple sense points around DUT.
- ATE resident control loops keep supplies balanced.
- Better-yet = power-island per core.

Only Four Options for Power Delivery

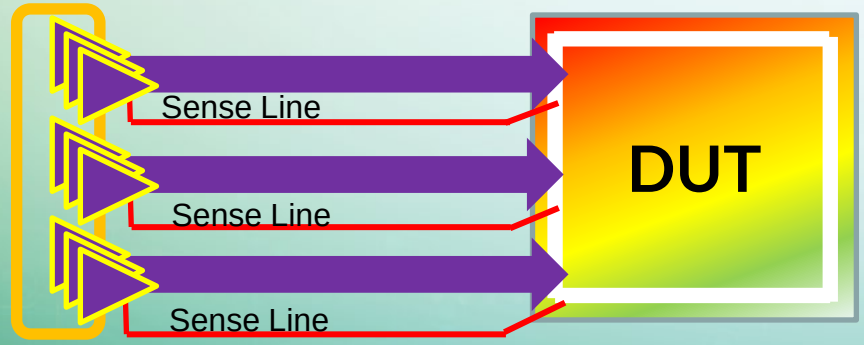
Full-current Power Plane



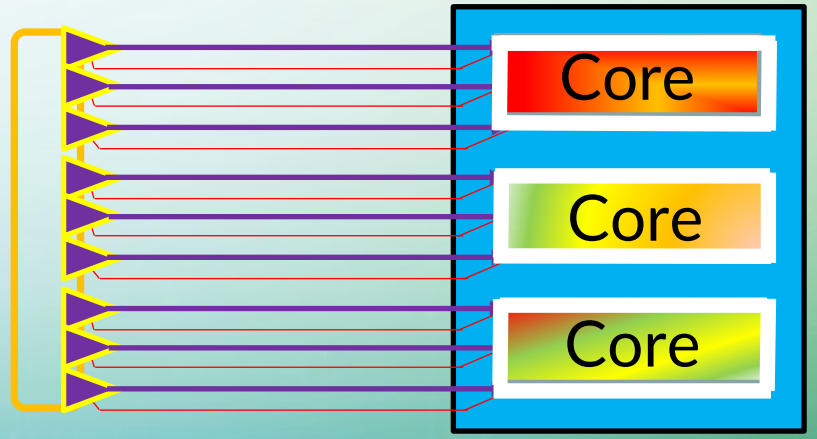
Per-Core Power Delivery



Subdivided Power Plane



Per-Pin Power Delivery



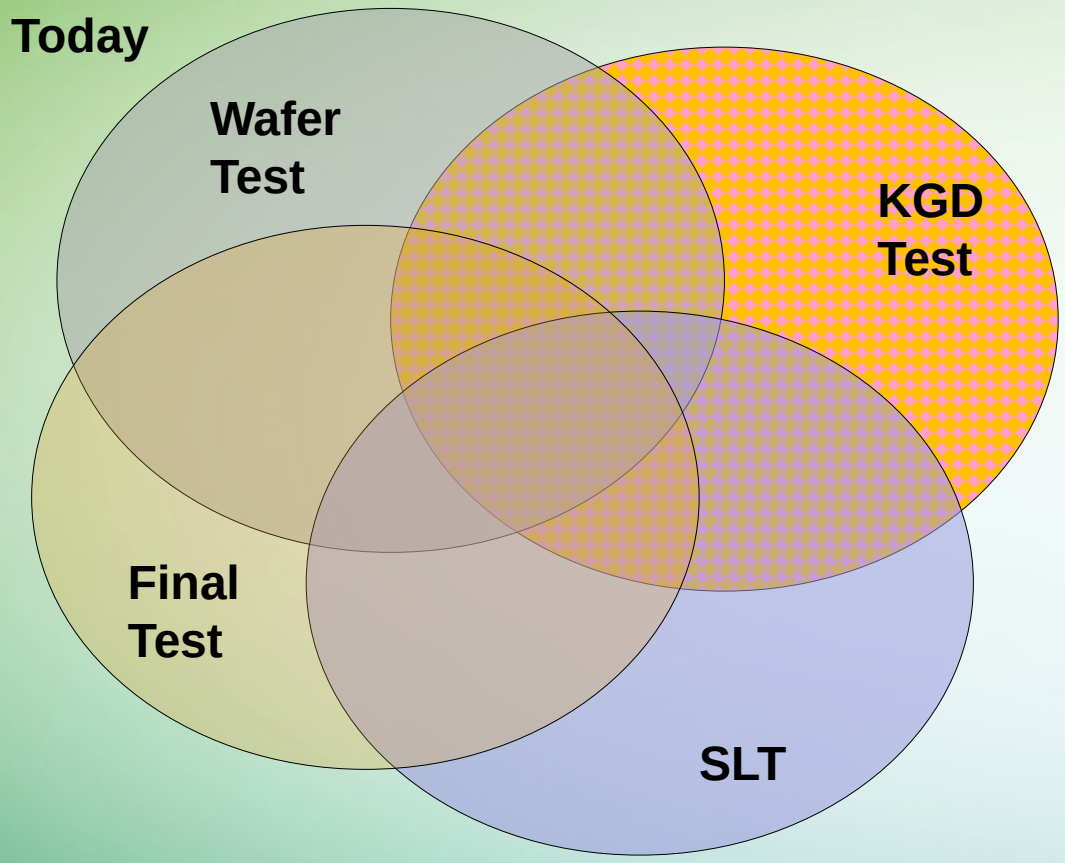
Power Delivery Tradeoffs

	Burnt Probe Risk	Damaged DUT Risk	Voltage Accuracy	Layout Complexity
Full-Current Power Plane				
Subdivided Power Plane				
Per-Core Power Delivery				
Per-Pin Power Delivery				

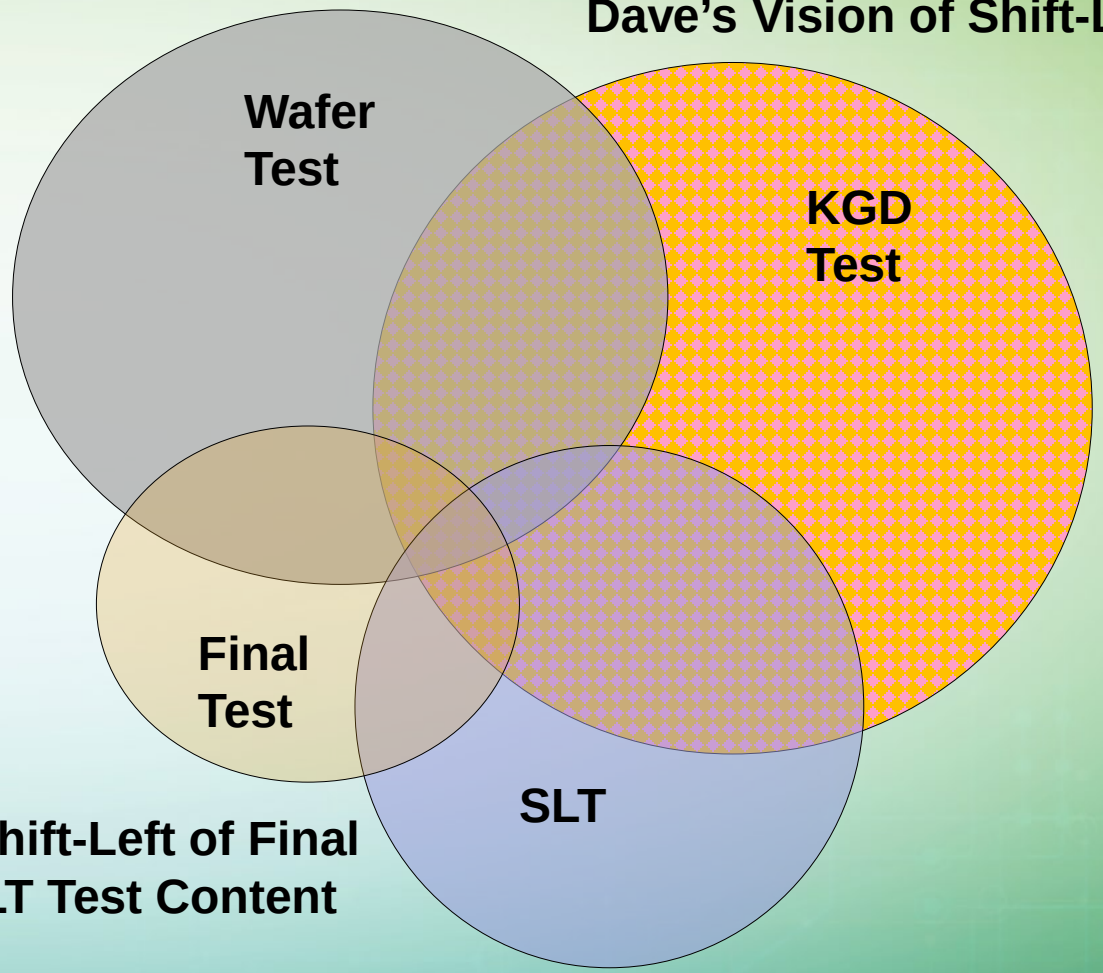
➔ If design will divide up the main supply on chip the per-core power delivery is the best choice.

➔ If design won't divide up the main supply on chip, the subdivided power plane provide better probe & DUT protection than the full-current power plane.

Impact of Shift-Left



Without Shift-Left



With Shift-Left of Final and SLT Test Content

Other Methods for Tackling Probe Burn

- For years, the industry has used Adaptive Test to enable and disable tests based on previous test results.
- Now Advantest has figured out how to do Adaptive Probe-card Cleaning (APC).
- By carefully monitoring the test results as a function of probe location and order one can both reduce the number of cleanings done and improve the reliability of your contact.
- Benefits include:
  - Fewer cleanings ➔ Better probing efficiencies.
  - Fewer cleanings ➔ Longer probe card life.
  - Better contact resistances ➔ Higher yield
  - Better contact resistances ➔ Less probe burn

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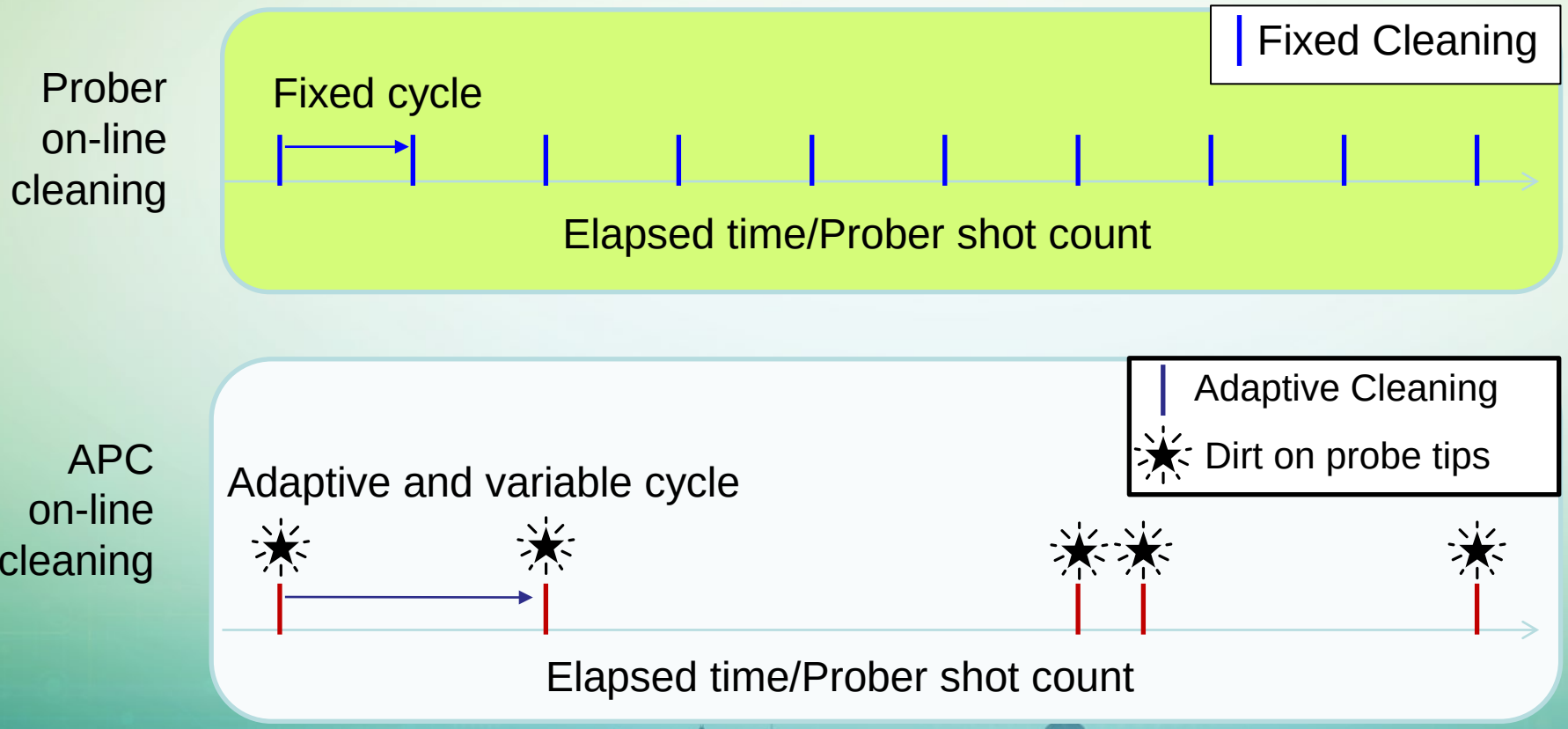
Adaptive Probe Cleaning (APC) Operation

Wafer prober performs fixed cyclic on-line cleaning. On other hand, Adaptative Probe Cleaning (APC) realizes a flexible on-line cleaning depending on the probe tip condition. APC can dramatically reduce the number of on-line cleanings, as APC can detect dirty tips using A.I.



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Real-World Experience with APC

The record of APC performance on a real mass production line of showed the following:

Product	Probe Needle Type	Reduction Ratio	Impact on Yield
A	Vertical probe needle	85%	No impact. Stable yield.
B	Cantilever probe needle	72%	No impact. Stable yield.
C	Cantilever probe needle	65%	Yield improved by 1.0%
D	Cantilever probe needle (sharp tip)	72%	No impact. Stable yield.
E	Vertical probe needle	77%	Yield slightly improved

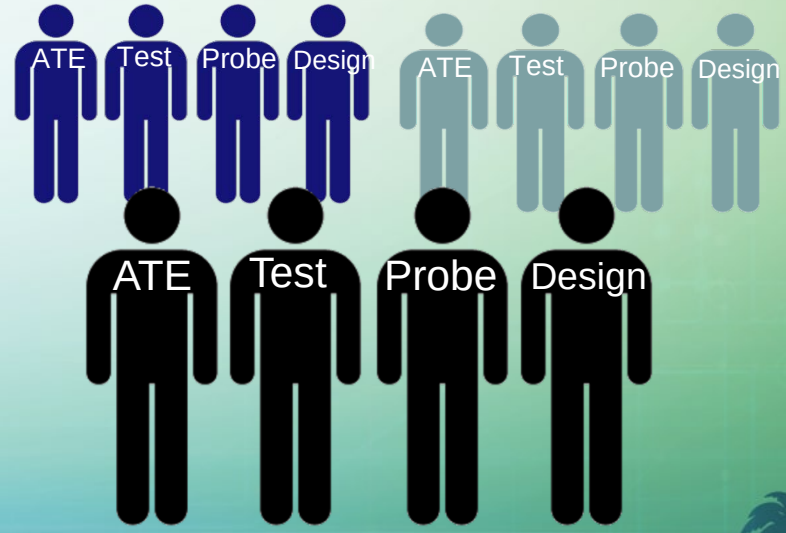
'Reduction ratio' is the ratio of decreasing times of on-line cleaning to times of fixed cycle cleaning which was performed by a prober.

Summary

The needs of the industry for more testing at wafer probe and more high-power probing are clear.

Solutions to meet this need without burning up a bunch of probes are available - - - but they require us to do things differently.

Working together, I'm certain that we can overcome the challenges that this means and allow us all to Shift-Left together.




thank you
danke
謝謝
ngiyabonga
teşekkür ederim
gracias
merci
obrigado
bedankt
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go raibh maith agat
mochchakkeram
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terima kasih
감사합니다
ありがとう
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