Technoprobe Corporate Introduction

TP Communication Team

TECHNOPROBE

Innovation begins with Us

A leading company in the field of semiconductors and microelectronics

Our numbers*

10	23	+600	4
Countries where we are present	Legal entities Worldwide	Proprietary patents	R&D Centers

3,355	1,724	44%
Employees Worldwide	Employees in Italy	Personnel under 30 in Italy

*as at 31/12/2024

What we do

Testing solutions

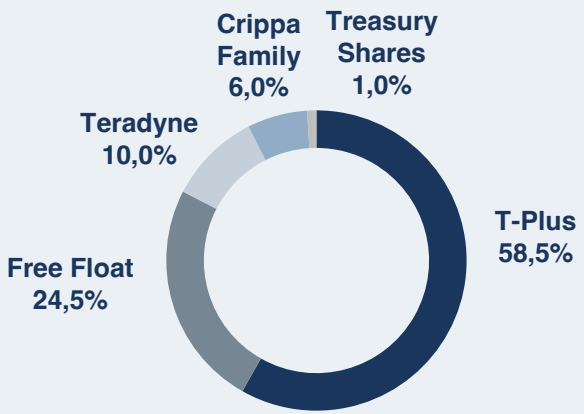
Technoprobe develops testing solutions for chips, the electronic hearts that bring to life the world of today and build that of tomorrow.

Company Overview

2024 Key financial metrics

Revenue	Ebitda	Net Income	Net Financial Position	Mkt Cap
€543.2m **+22%** CAGR 19-24	**€136.5m** **25%** EBITDA margin	**€62.8m** **12%** on revenues	**€656.3m** as at 31/12/2024	**~€3,4bln** as at 04/04/2025

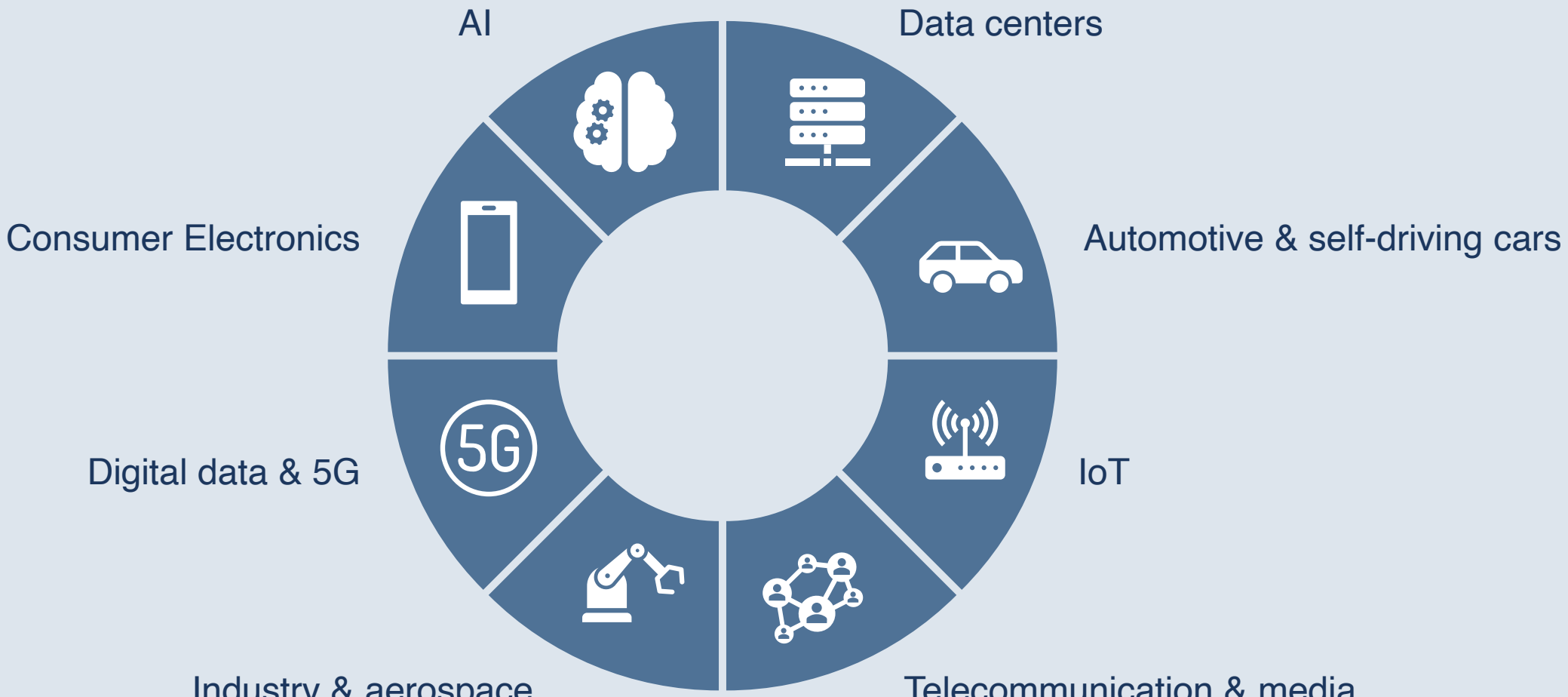
Shareholding Structure*



- Leading player in designing and manufacturing of **probe cards**
- Manufacturing process **vertical integrated**
- Strong focus on **innovation**
- Extensive **global presence** and widespread **local footprint**

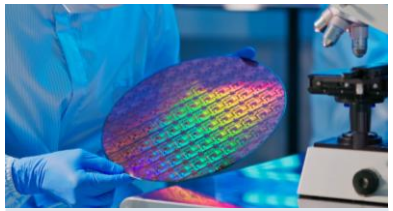
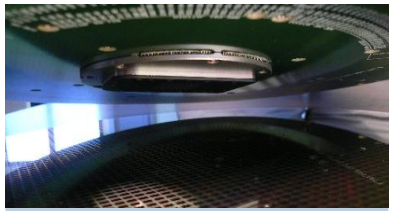
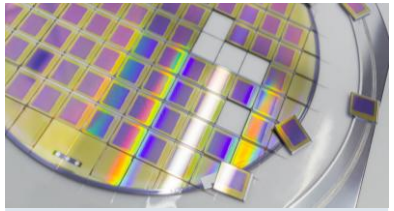
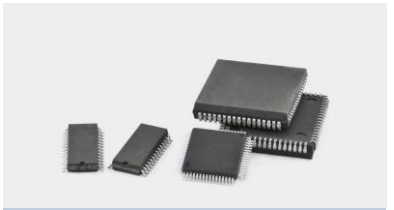
*Listed on Euronext Milan since May 2, 2023

The markets we serve



What we do

Technoprobe operates both in wafer-level testing and in final testing.

Wafer (multi-chip)	Electrical Wafer Sorting (EWS)	Chip is singulated	Chip is packaged	Final Testing	Integration into electronic devices
					
The silicon wafer contains hundreds of **unsingulated microchips**	The **probe card** electrically tests each chip on the wafer to **check functionality** and **identify any defects**	The wafer is sliced into individual chips, known as "**dies**"	Each chip is **encapsulated** in a package that enables electrical connections and protects it from damage	Packaged chips undergo **final tests** to ensure proper functionality	The packaged chip is **integrated into electronic devices** via printed circuit boards

Probe Card

Device Interface Board

Business model

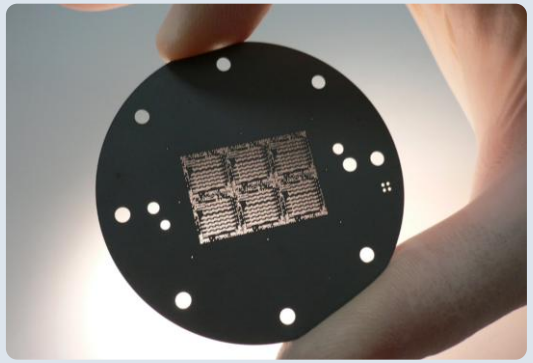
A successful and vertically integrated business model

		Design	Manufacturing	Assembly
Wafer Testing Level				
Mechanics		✓	✓	✓
PCB		✓	Manufacturing partners & other suppliers	✓
Interconnection		✓	✓	✓
Probe head Ceramic plates Contact probes		✓	✓	✓
Final Testing Level				
Device Interface Boards		✓	Manufacturing partners & other suppliers	✓

A wide range of highly innovative technologies

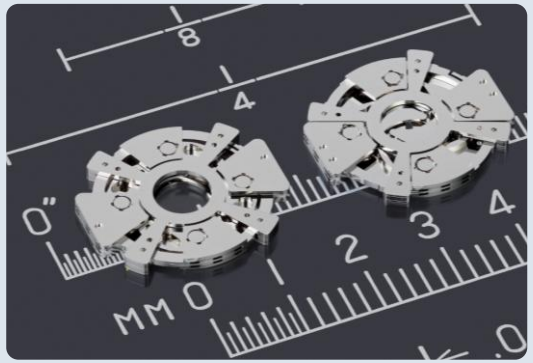
Advanced micromachining

Advanced laser cutting:
high accuracy and fast lead time



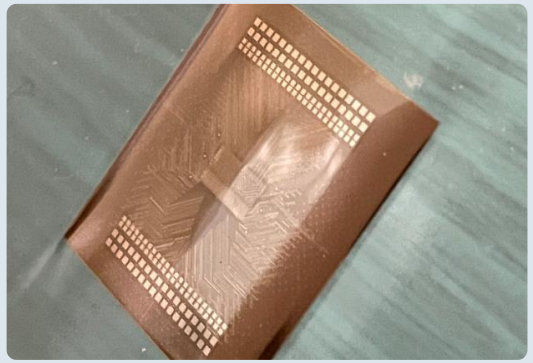
Thin film

Strong investment in advanced thin film technology to reduce lead time and improve quality and complexity



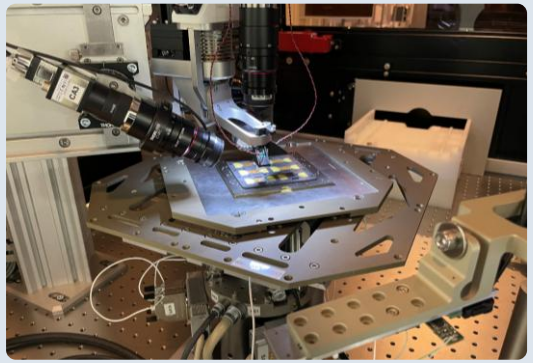
3D MEMS

Acquisition of MICROFABRICA in 2019; the sole company in the world specialized in 3D metallic MEMS manufacturing



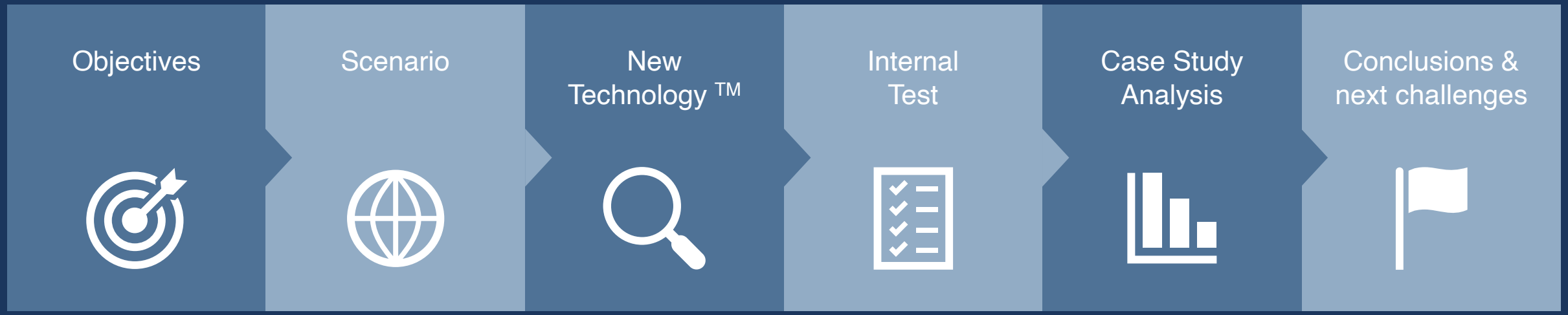
Advanced manufacturing

Advanced manufacturing for high volume and best quality assembly of micro components



New technologies development

+600 proprietary patents

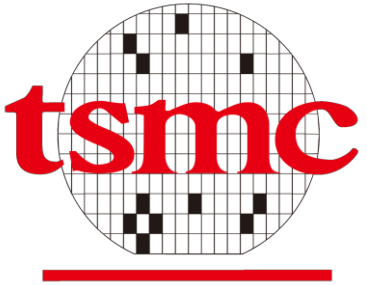


Who we work for

Our clients

Technoprobe is a strategic partner for the world's leading semiconductor companies.

Important players like…



Our reputation

For the seventh year in a row (2018-2024), we are the Highest-Rated Test Subsystems Supplier in the TechInsights Customer Satisfaction Survey.

Our reputation

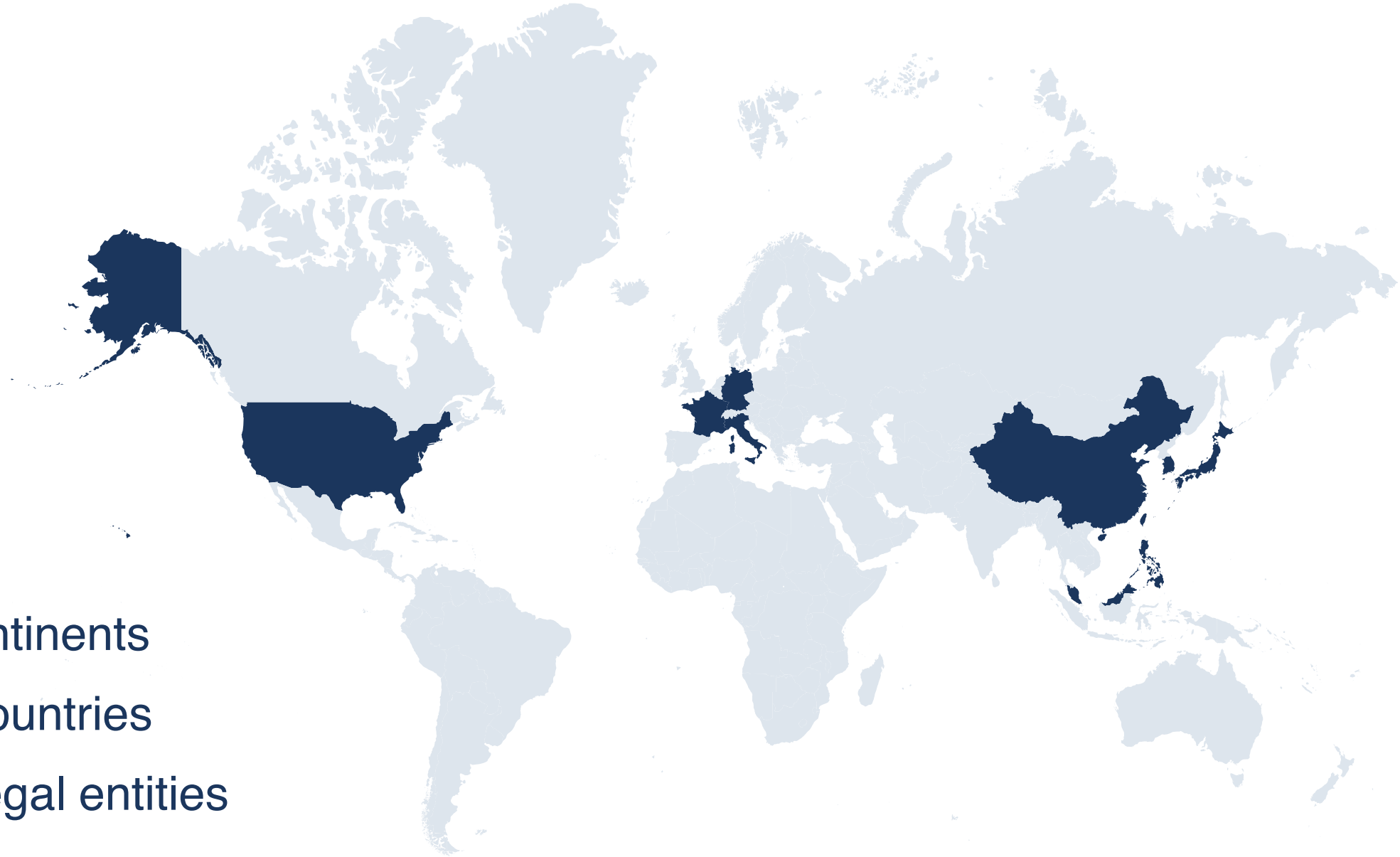
TSMC's Excellent
Performance Award 2024

From 2018 to 2024
Best Probe Card supplier worldwide*

From 2020 to 2025
Intel EPIC Supplier Award

*Customer survey conducted by TechInsights

Worldwide presence



3 Continents

10 Countries

23 Legal entities

Our evolution

1996-2024 Revenues evolution (€m)

Our evolution

Technoprobe worldwide - 2010-2024: headcount evolution*

*Data as of December 31st of each year.

Mastering Emerging Probing Challenges

The Power of Agile and Continuous Innovation

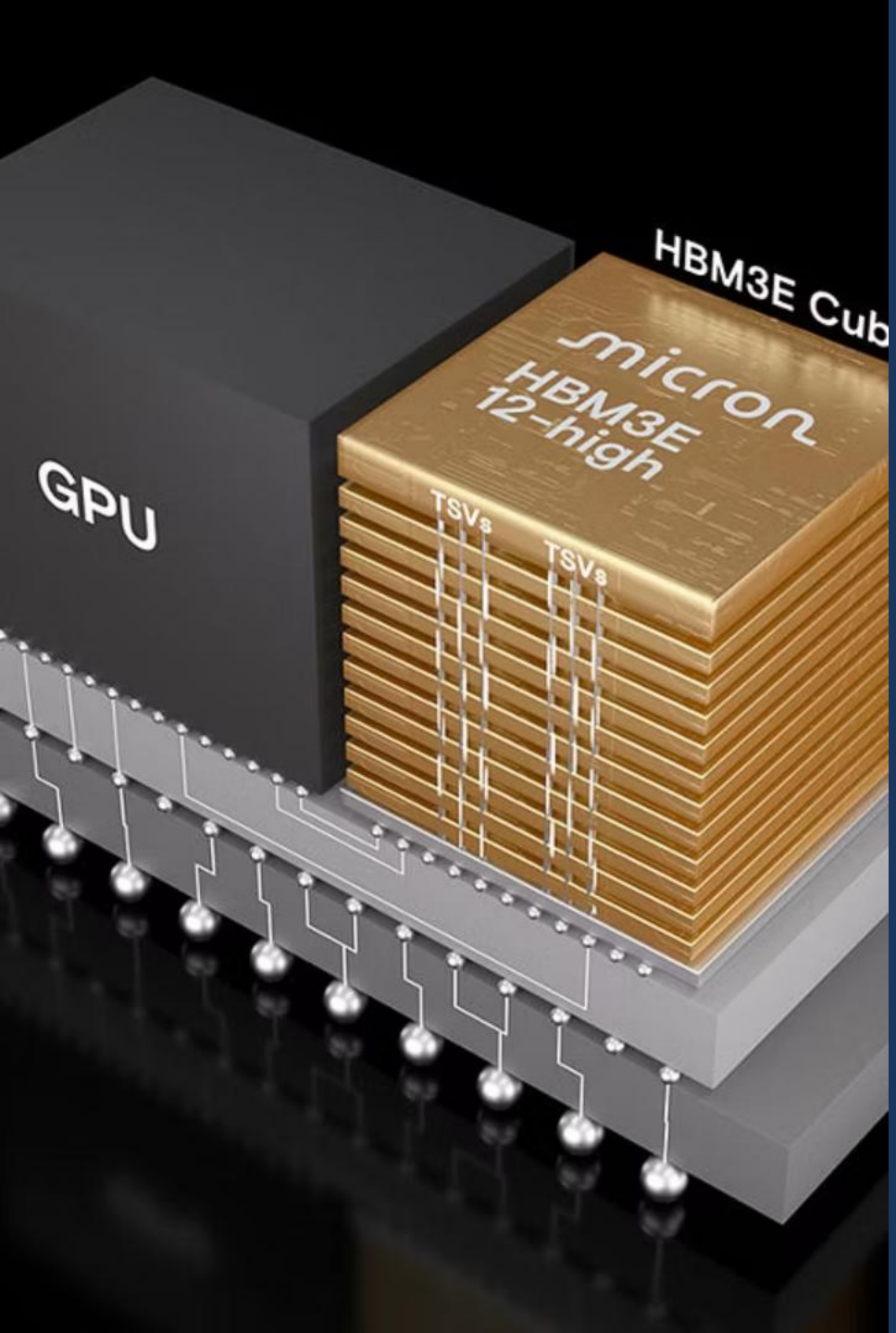
Raffaele Vallauri
VP Director @ Technoprobe

SWTW Conference 2025, San Diego

TECHNOPROBE

Agenda

- **The Inflection Point**
  Setting the stage for unprecedented semiconductor complexity
- **The Probing Challenge**
  Understanding the technical hurdles and development bottlenecks
- **The Agile Imperative**
  Shifting towards Lean, Agile, and Collaborative solutions
- **Accelerating Innovation**
  Leveraging Concurrent Engineering, Simulation, and MVP approaches
- **Insights from Parallel Worlds**
  Lessons in rapid adaptation (F1, Aerospace)
- **Impact & Path Forward**
  Achieving faster TTM, higher reliability, and a call to action



Semiconductor Industry at Inflection Point

AI, HPC, Automotive

drive exponential device complexity

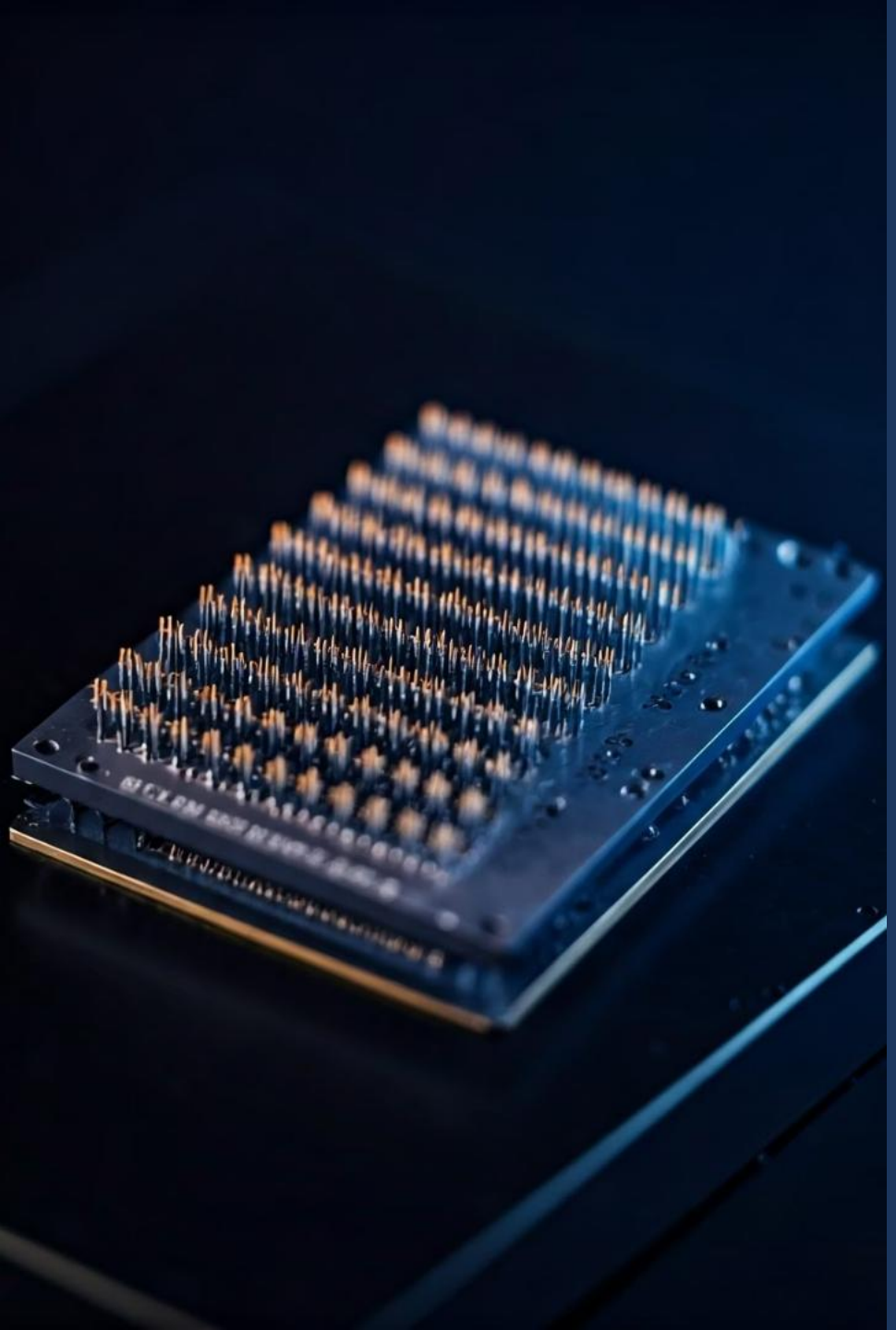
Zettabyte Era

demands higher wafer testing precision

Emerging Technologies

push innovation boundaries

Wafer test/probing are more and more critical path enablers.
We need to deliver Value faster than ever.



PROBLEM: Unprecedented Probing Challenges

Ultra-fine Pitch

Pitches below 30 μm down to 10 μm, micro-bumps, and hybrid bonding require extreme precision (ref. Tadayon/Parks)

High-Speed Interfaces and Power Delivery

Interfaces exceeding 100 Gbps/lane demand superior signal integrity, together with High current, low impedance and thermal hotspots (ref Miller/Stork/Parks)

3D Structures

New materials and complex 3D architectures create testing barriers (ref Slessor/Parks/Tadayon)

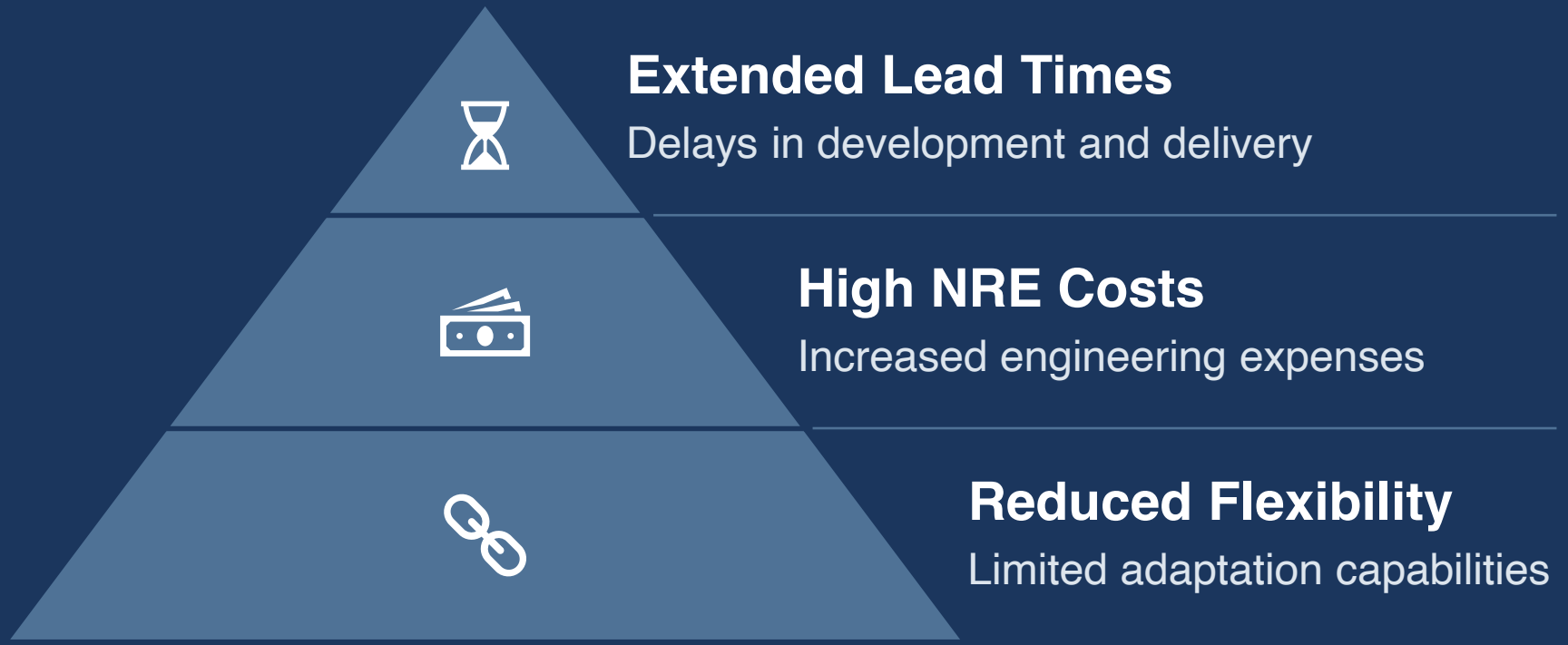
Development Timelines

Vendors face rapid innovation cycles with limited pre-deployment validation

PROBLEM: The Probe Card Vendor’s Dilemma

Challenges for probe card developers:

- IC innovation cadence outpacing traditional hardware development cycles.
- Shrinking windows for test/validation before customer high-volume manufacturing (HVM).
- Escalating demands: Performance (SI/PI), Reliability (lifetime, CRES), and Cost.



Extended Lead Times
Delays in development and delivery

High NRE Costs
Increased engineering expenses

Reduced Flexibility
Limited adaptation capabilities

Increasing requirements lead to development complexity with more probe types and tighter specifications. Traditional methods risk becoming bottlenecks.

The Bottleneck of Traditional Development

Traditional Approach

- Rigid sequential processes
- Limited collaboration
- Fixed specifications
- Reactive development

Limitations

- Late discovery of issues = High Cost of Change
- Limited flexibility to adapt. Siloed Teams
- Inherent waste “Muda”: Waiting, rework, overprocessing...
- Risk of becoming the critical bottleneck in overall semiconductor TTM

VISION - Shifting the Development Paradigm: Towards LPPD* & Agility

Traditional Approach

- Rigid sequential processes
- Limited collaboration
- Fixed specifications
- Reactive development

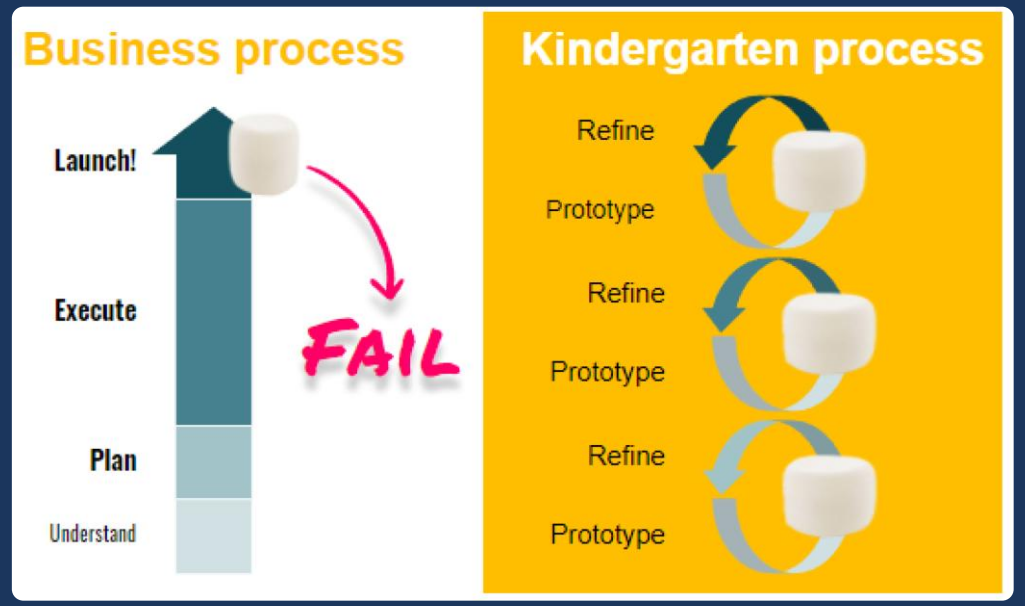
New Vision

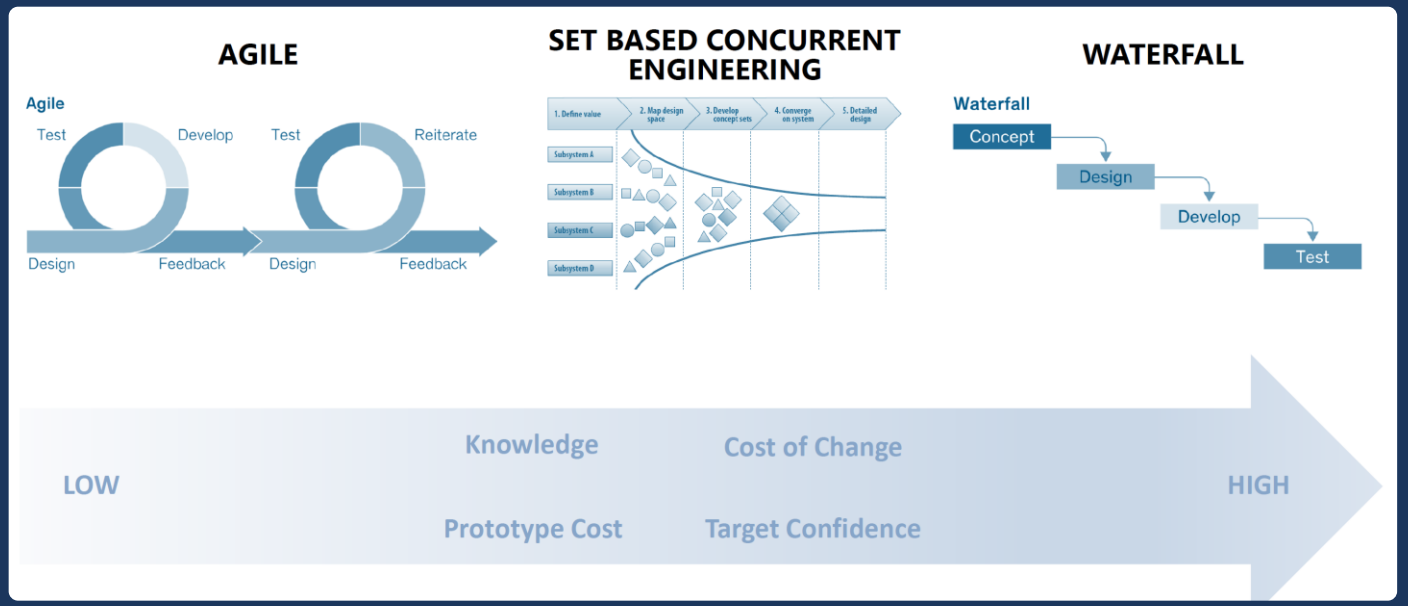
- Dynamic adaptive models
- Deep partnerships
- Evolving requirements
- Anticipatory innovation

From rigid, sequential processes to dynamic, adaptive, collaborative models rooted in LPPD* and Agile principles. Towards an ecosystem where probe innovation (driven by skilled people, aligned processes, adapted tools) keeps pace with semiconductor advancements.

* LPPD : Lean Process & Product Development

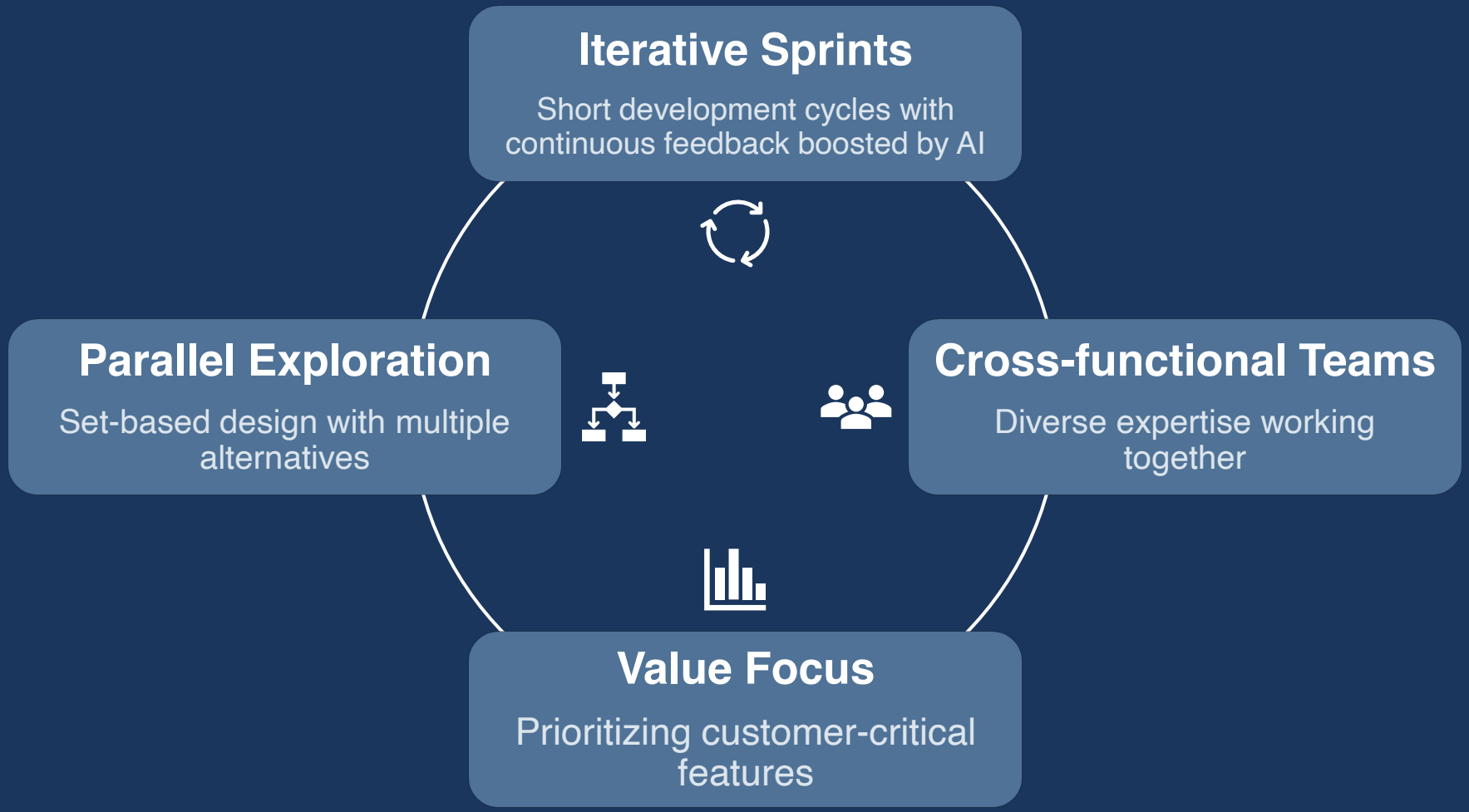
Adapting LPPD/Agile Core Principles to PC





- **Define Value**: Deeply understand customer needs & tradeoffs upfront (Nemawashi)
- **Iterative Cycles:** Rapid Design-Build-Test-Learn loops (like the "Kindergarten process" above)
- Focus on **“learning fast”**

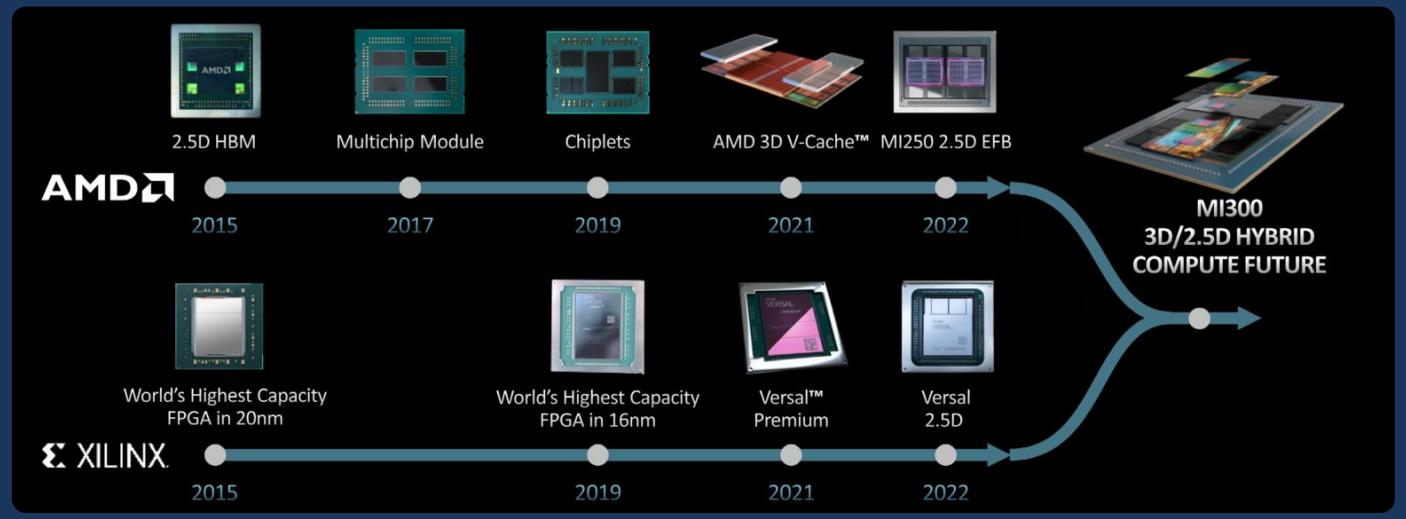
SOLUTION: Agile, Lean Principles & Concurrent Engineering

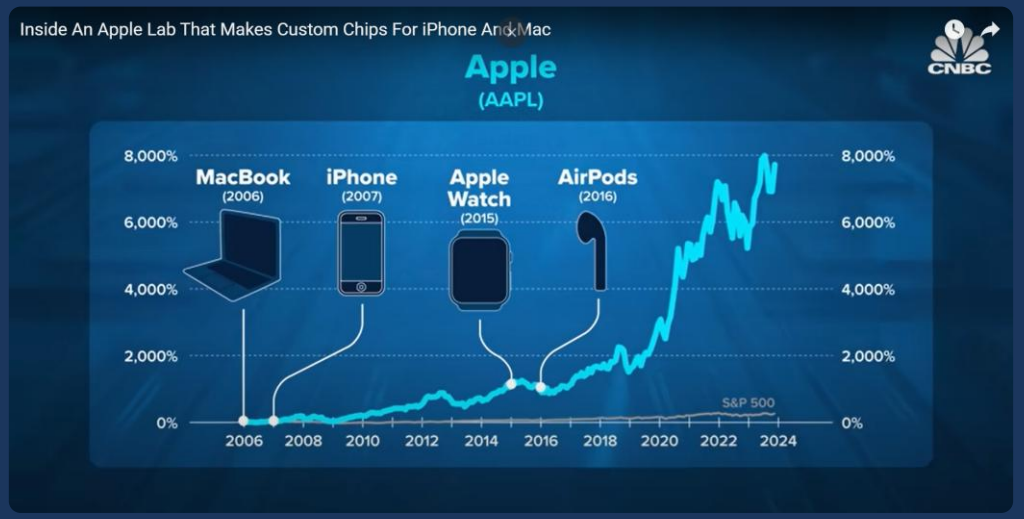


Agile/Lean in Semiconductor Giants: Industry Examples

How leading semi companies apply similar principles:

- **Platform Strategy**: Iterated core architectures (Ref : Intel, Nvidia)
- **Concurrent Engineering**: Intense co-design (Ref: Apple Silicon)
- **Rapid Cadence & Supplier Integration**: quick node deployment (Ref: TSMC)
- **Modular Design & Standard Interfaces**: Chiplet ecosystems (Ref: TSMC, AMD, Intel …)





https://youtu.be/UdhWvg5mycY

Video source: CNBC YouTube Channel

Early Collaboration & MVP Testing

IC Designers

Share roadmaps and requirements early

Probe Vendors

Develop MVP probe cards for testing

ATE Partners

Integrate and validate solutions

OSATs

Provide real-world testing environments

Deep partnerships enable Minimum Viable Product probe cards for rapid feedback before full-scale development.

Learning from Parallel Worlds: F1 racing

Rapid Iteration & Data-Driven Adaptation

- F1 teams design, simulate, build, and test car updates between races (weekly sprints).
- Massive reliance on telemetry data and simulation for performance tuning.
- Modular designs allow rapid component swaps/upgrades.
- Extreme cross-functional team collaboration
- High pressure, rapid learning cycles

Parallel to Probing

- Need for rapid design iterations based on wafer test data, modular probe head concepts, tight vendor-customer feedback for tuning, high performing cross-functional Teams

Learning from Parallel Worlds: Aerospace

Managing Complexity, Reliability & Long Lifecycles

- Aerospace uses digital twins for design, predictive maintenance, and upgrade planning over decades.
- Complex systems integration across vast supply chains using standardized interfaces and rigorous validation.
- Extreme reliability requirements drive simulation and fault tolerance.

Parallel to Probing

- Need for predictive probe lifetime/maintenance models, simulation for reliability under stress (thermal, mechanical).
- Managing complex system interactions

IMPACT: Accelerating TTM & Innovation

40%

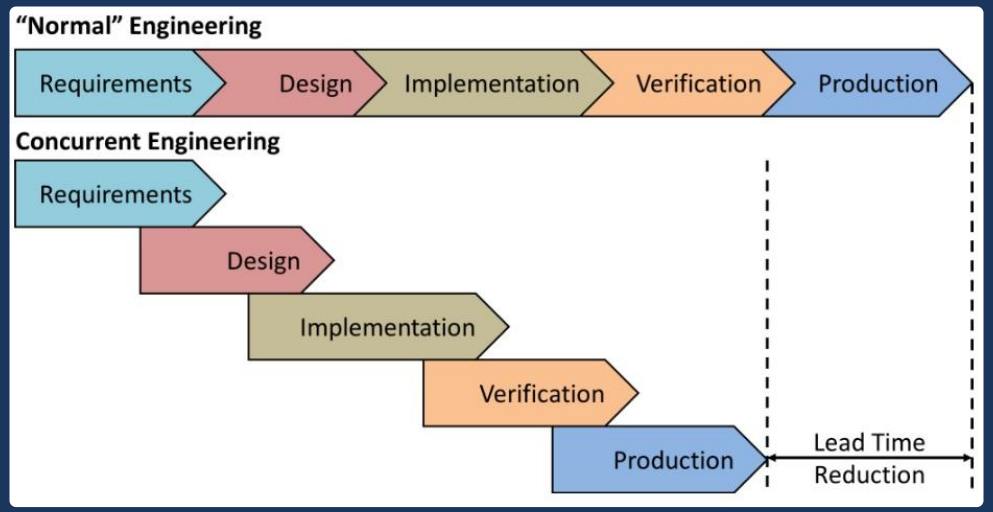
Development Cycle Reduction

Potential time savings with agile methodologies

2x

Response Speed

Faster adaptation to new IC designs



Unlocking faster innovation across the semiconductor ecosystem by removing test hardware bottlenecks.

Iterative refinement and early feedback lead to solutions meeting extreme specifications for speed, pitch, power, and lifetime.

IMPACT:
Enabling Performance, Reliability & Cost-Effectiveness

Delivering the right solution

Iterative refinement & SBCE ensure solutions meet extreme performance specs and customer Value

Enhanced reliability from early validation & robust convergence

Achieving this cost-effectively by eliminating waste, optimizing processes, and focusing development effort

Co-Creating the Future of Test

Reiterate the opportunity: Transform probing challenges into catalysts for collective innovation using LPPD/Agile principles

Probe Vendors

Embrace agility, LPPD, continuous learning

IC Designers/Foundries

Design for Testability, collaborate early (Nemawashi), share roadmaps

ATE/OSAT/Ecosystem partners

Drive integrated solutions, standards, support agile flows