



**SWTEST**

PROBE TODAY, FOR TOMORROW

2025 CONFERENCE

# Wafer-Level Testing of Photonic Devices

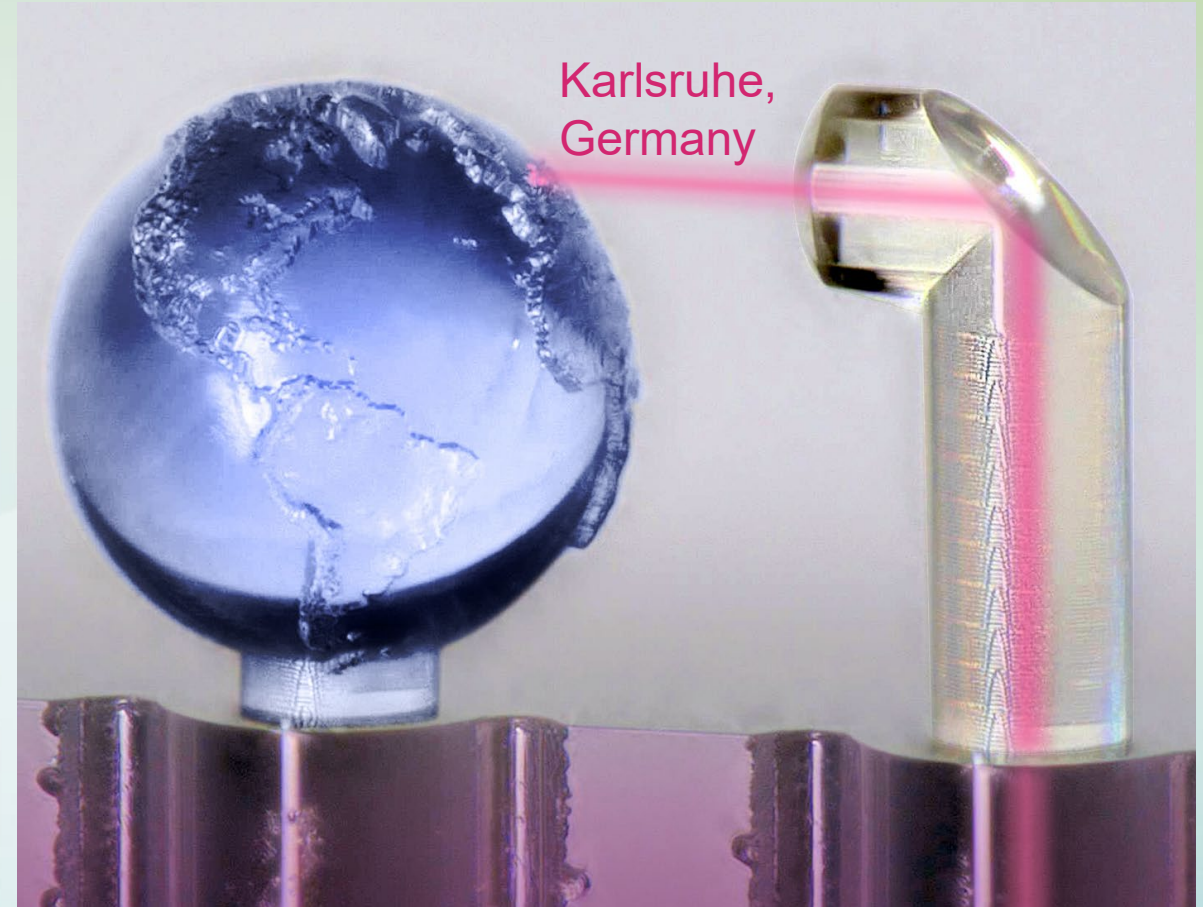
**Keystone**  
photonics

Philipp Dietrich  
Andrés Machado  
Florian Rupp  
Roman Zvahelskyi

Keystone Photonics

# Content

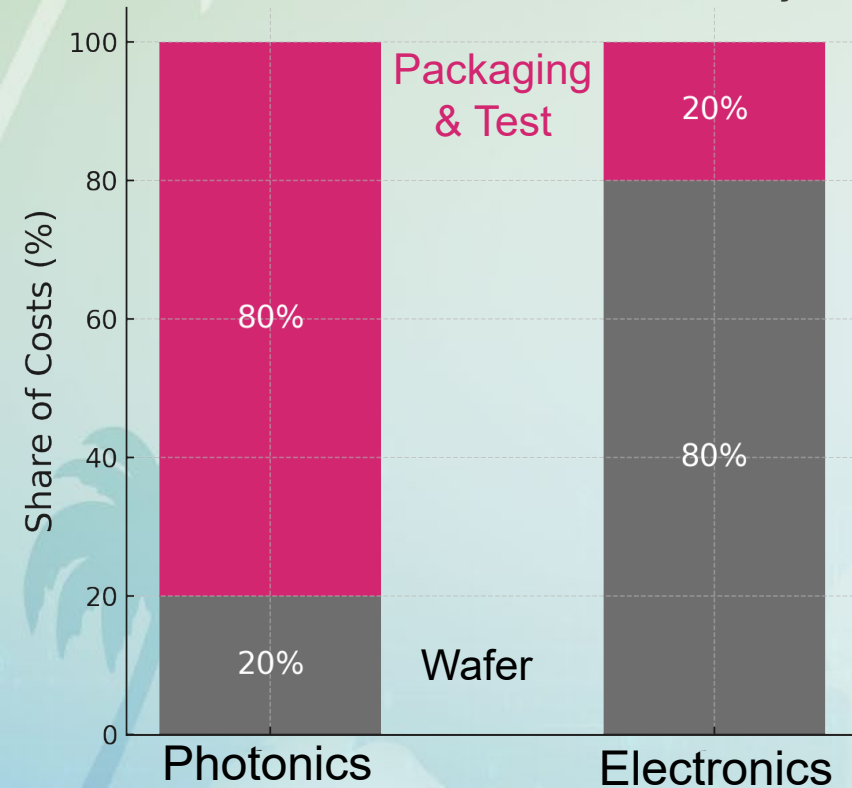
- Relevance and challenges of photonic wafer-level testing
- In-situ printed micro-optics
- Comparison to other testing approaches
- Reproducibility
- Production-readiness
- Challenges



# Test After Singulation is Too Late!

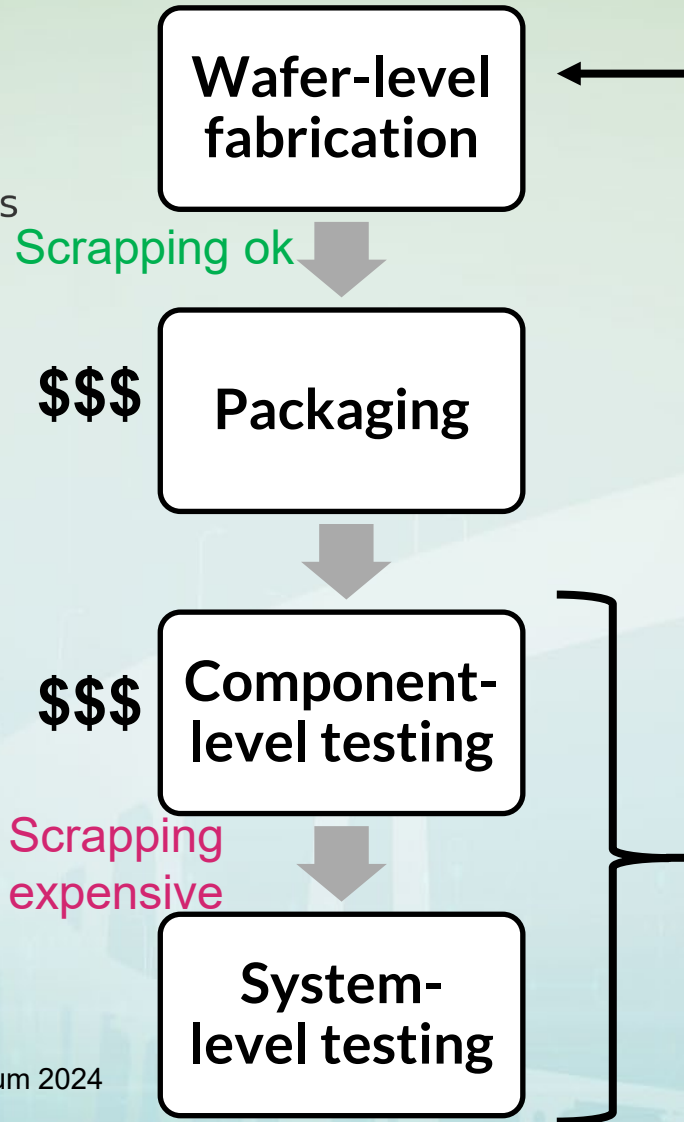
**Test (and packaging) is the largest cost-driver in integrated photonics**

Share of Fabrication versus Assembly Costs



Fuchs et al. 10.1109/JLT.2011.2159260;  
Gregg Barlett, Global Foundries at Global Photonic Economic Forum 2024  
[https://youtu.be/H0\\_H9M0i7Og?si=nPdJyWC5KYMoJ8TR](https://youtu.be/H0_H9M0i7Og?si=nPdJyWC5KYMoJ8TR)

Philipp Dietrich



**Key Takeaway:**

**Packaging in photonics is a major cost driver + testing can be automated at wafer-level => Test before packaging**

“Drum **prüfe**, wer sich ewig bindet, Ob sich das Herz zum Herzen findet!”

**"Test** who binds themselves for eternity, whether heart meets heart in unity."



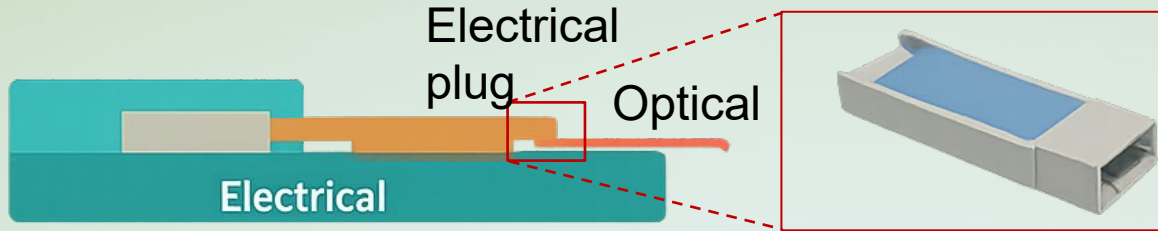
Friedrich Schiller, 1799



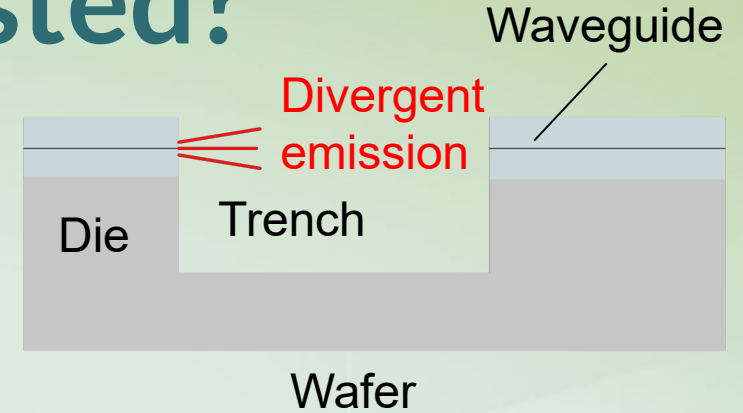
# What has to be tested?

Pluggable  
Will grow for  
5y; **Arista**  
claims still ok  
for 1600.

## Pluggable Transceiver

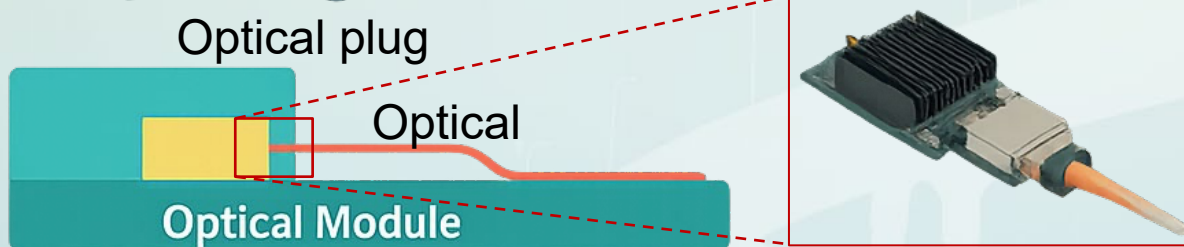


Laser +  
Fiber interface

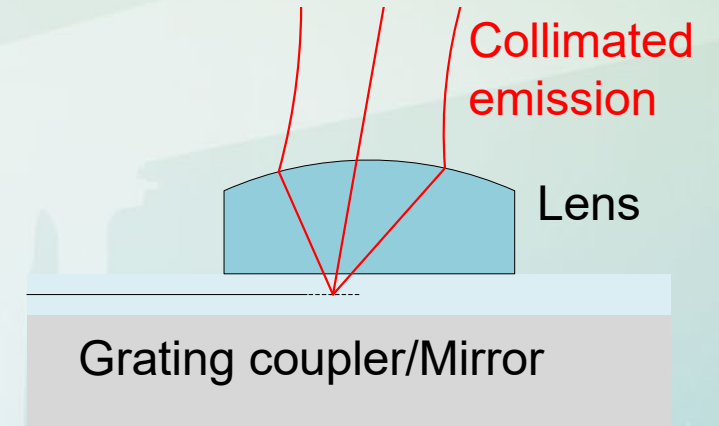


**CPO:**  
**Nvidia/TSMC**  
COUPE, will  
ramp soon!

## Co-packaged



Fiber only, laser  
is separate



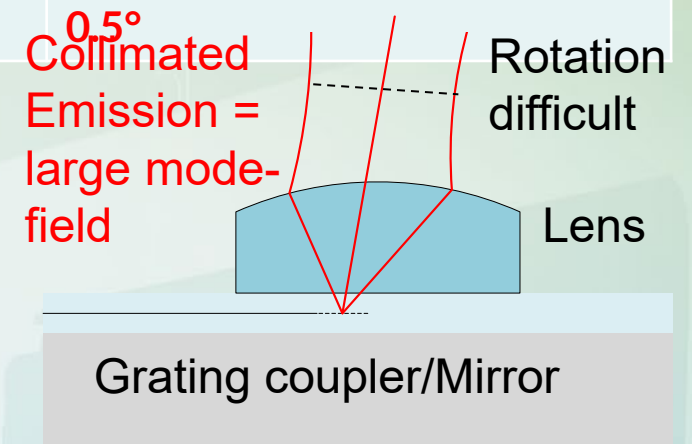
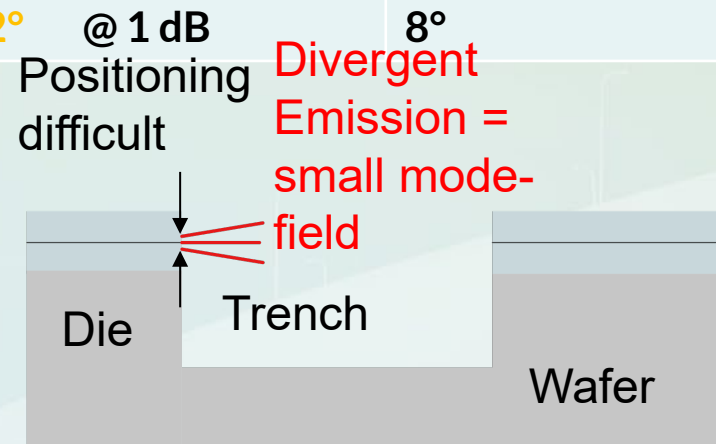
**Key Takeaway:** There are two competing architecture. Electrical pluggable with “more” electrical signal and mostly trench-coupling and CPO with “more” optical signal and mostly surface coupling.

# How is Optical Testing Different?

	Electrical	SMF interface	High RI interface	Optical plug
Size	50 $\mu\text{m}$	10 $\mu\text{m}$ @ $1/e^2$	2.5 $\mu\text{m}$	40 $\mu\text{m}$
Position	20 $\mu\text{m}$	2 $\mu\text{m}$ @ 1 dB	0.5 $\mu\text{m}$	8 $\mu\text{m}$
Angular	-	2° @ 1 dB	8°	0.5°

50  $\mu\text{m}$

Electrical pad



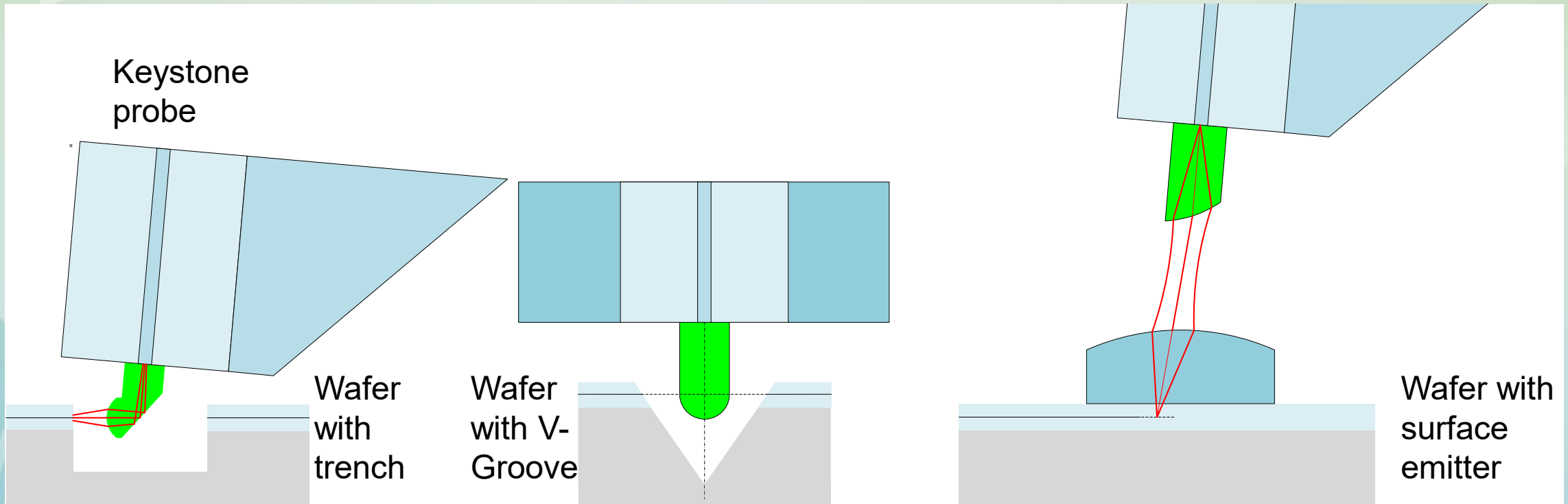
**Key Takeaway: Optical testing always has high alignment requirements – either translational or angular.**

# Micro-Optics for Coupling

Trench for „pluggable“

V-Groove for „pluggable“

Surface coupling for „CPO“



**Key Takeaway: Can adapt to all relevant coupling interfaces.**



# In-situ printed micro-optics

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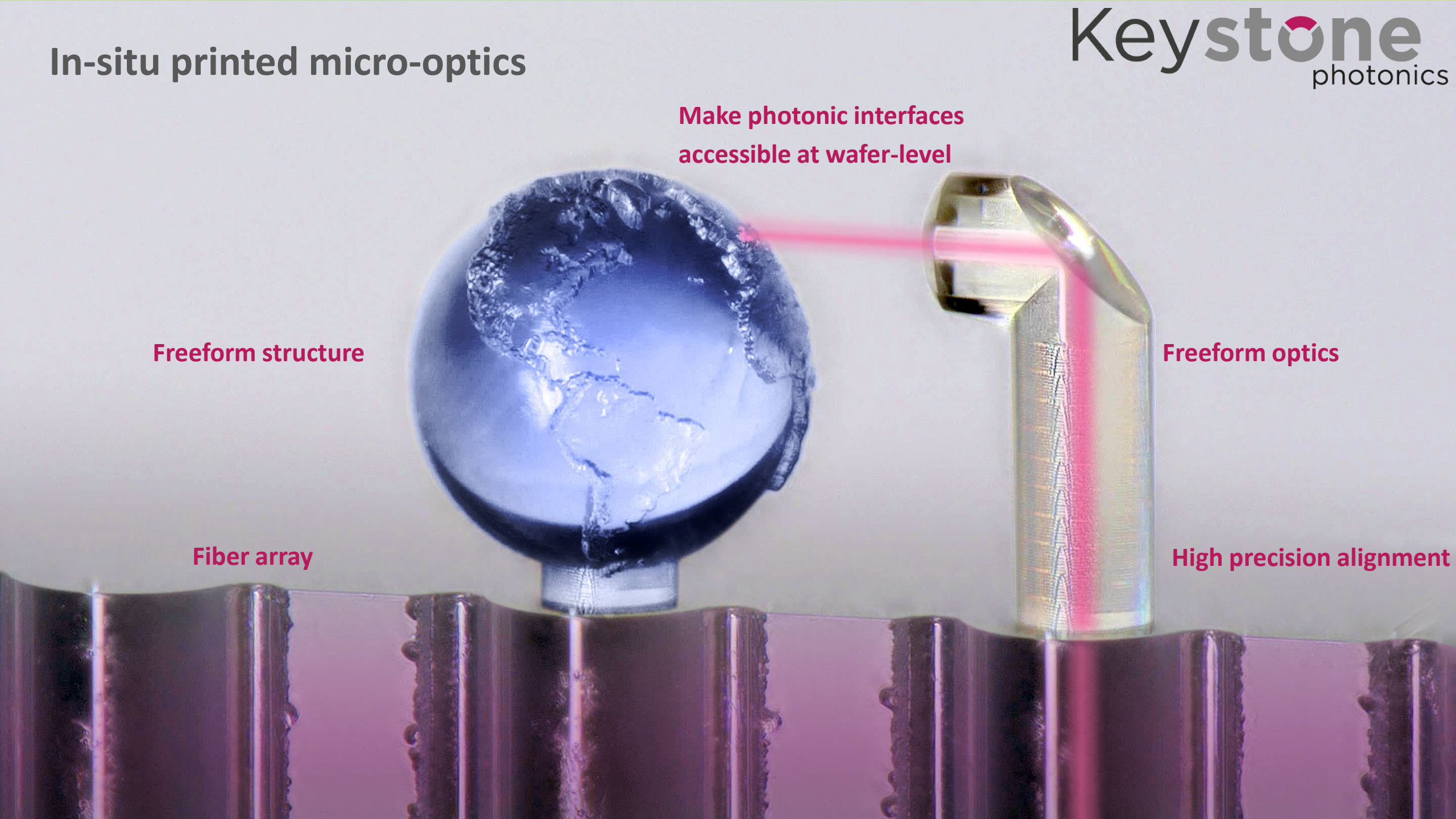
Make photonic interfaces  
accessible at wafer-level

Freeform structure

Fiber array

Freeform optics

High precision alignment



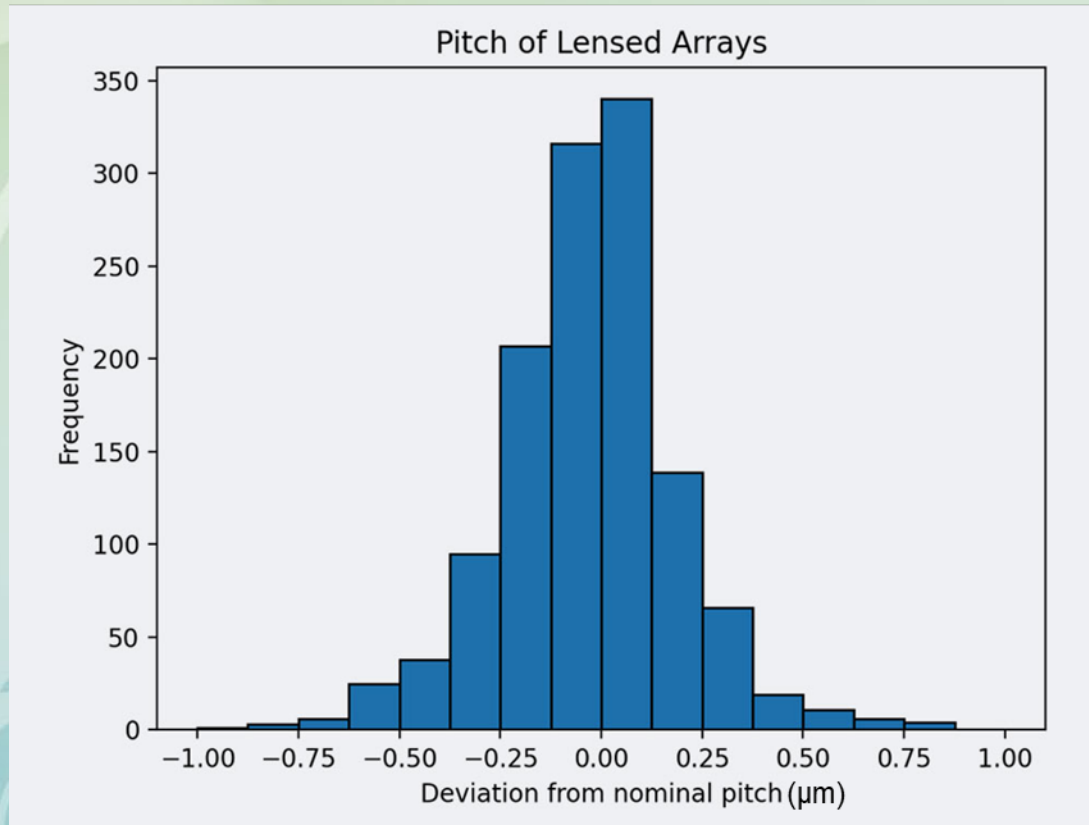


Real focus at  
Karlsruhe,  
Germany

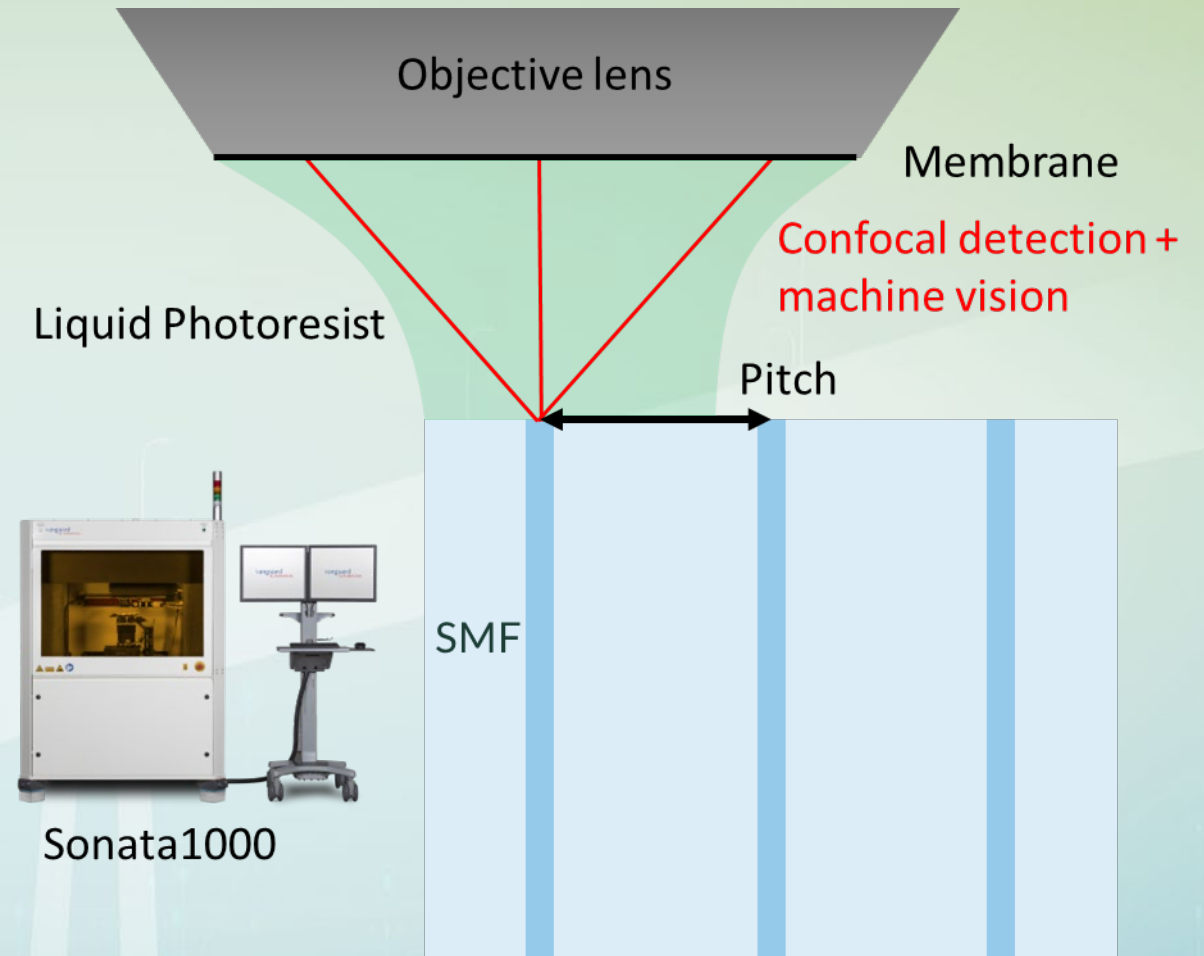




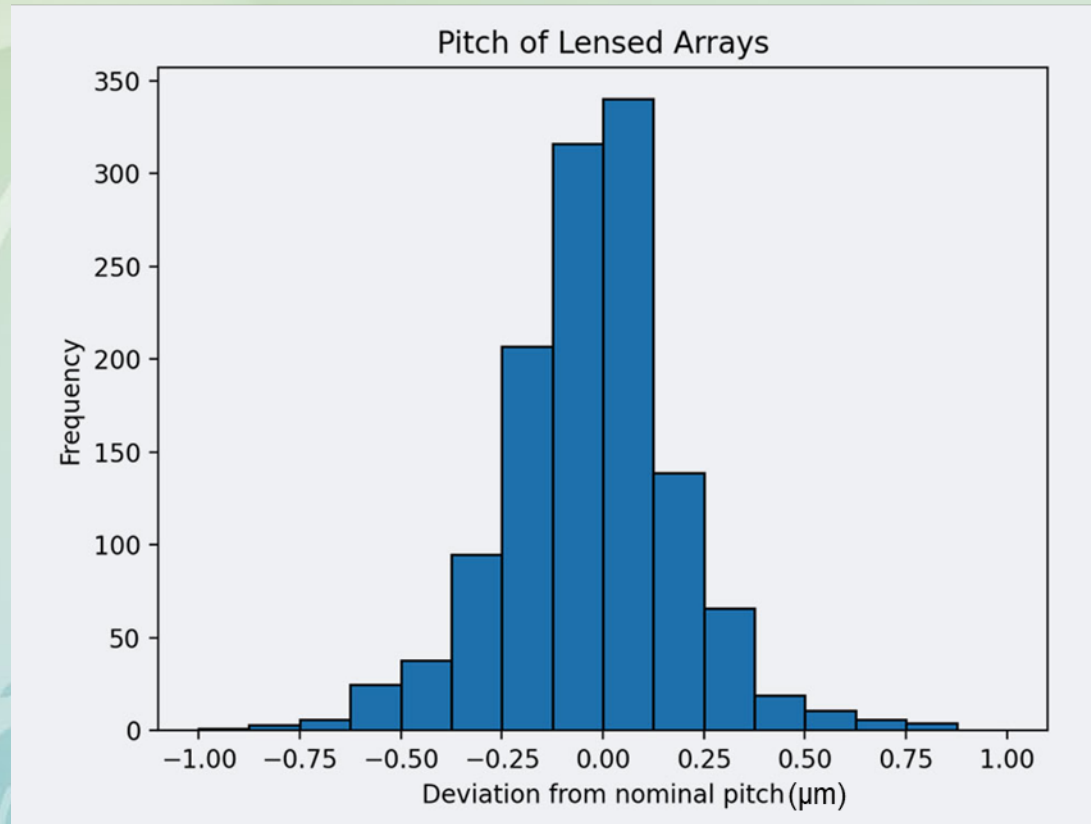
# Fabrication



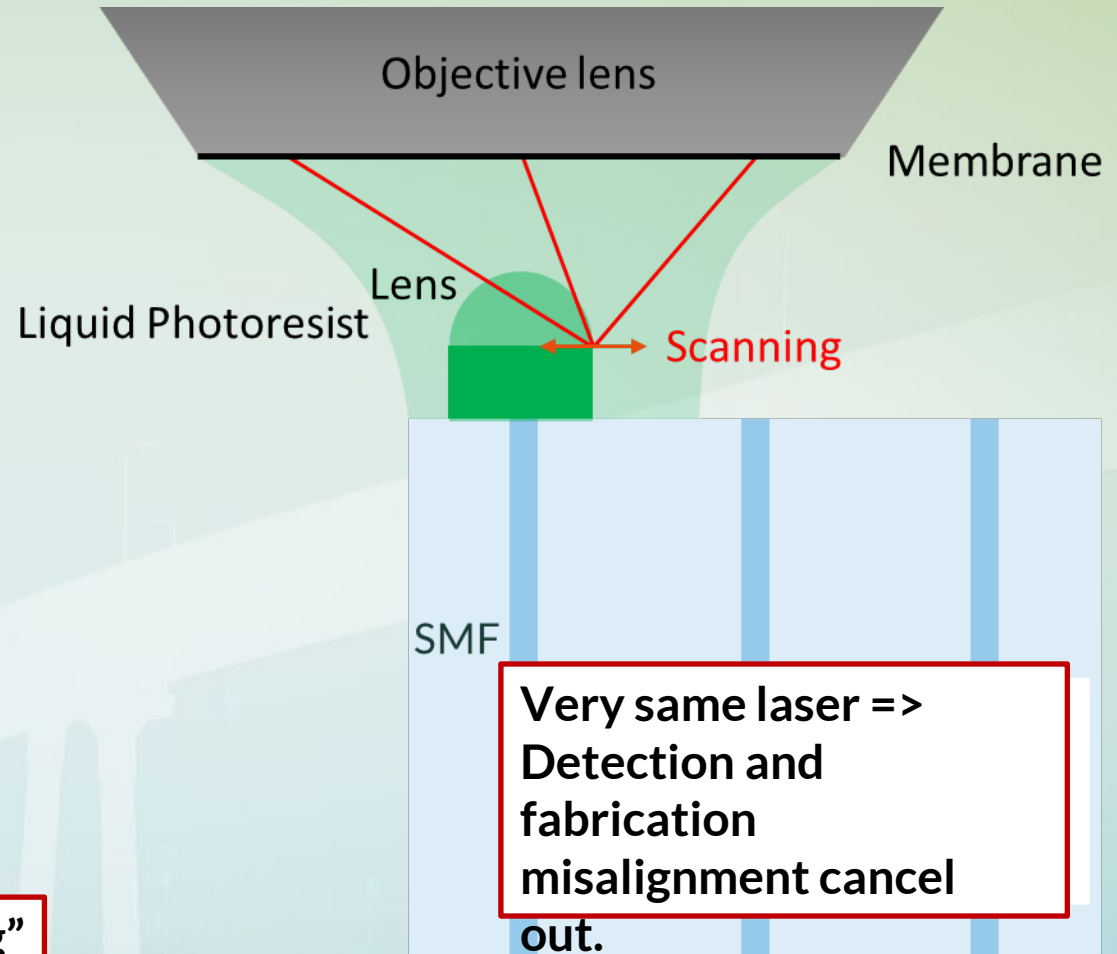
**Key Takeaway: Fabrication inherently does in-line inspection.**



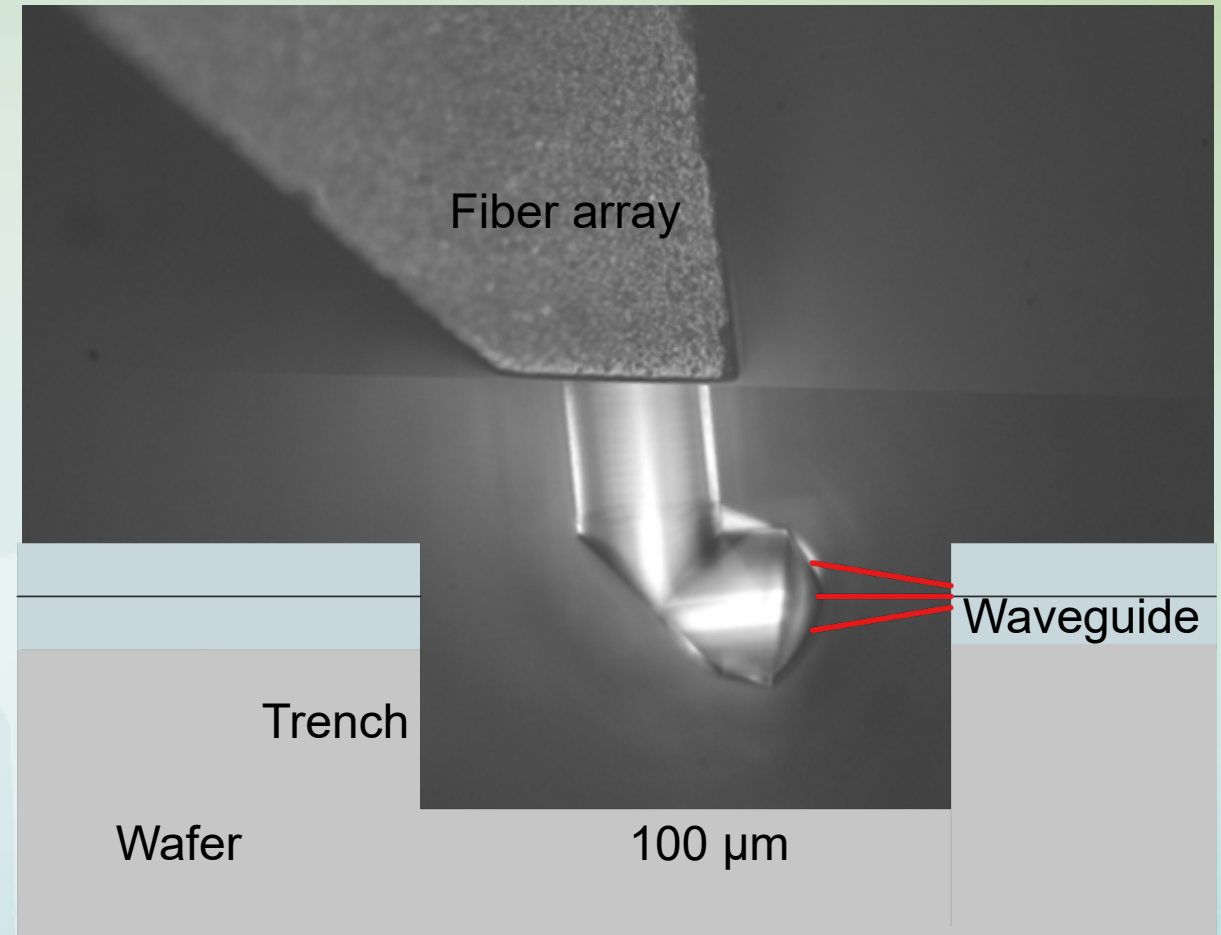
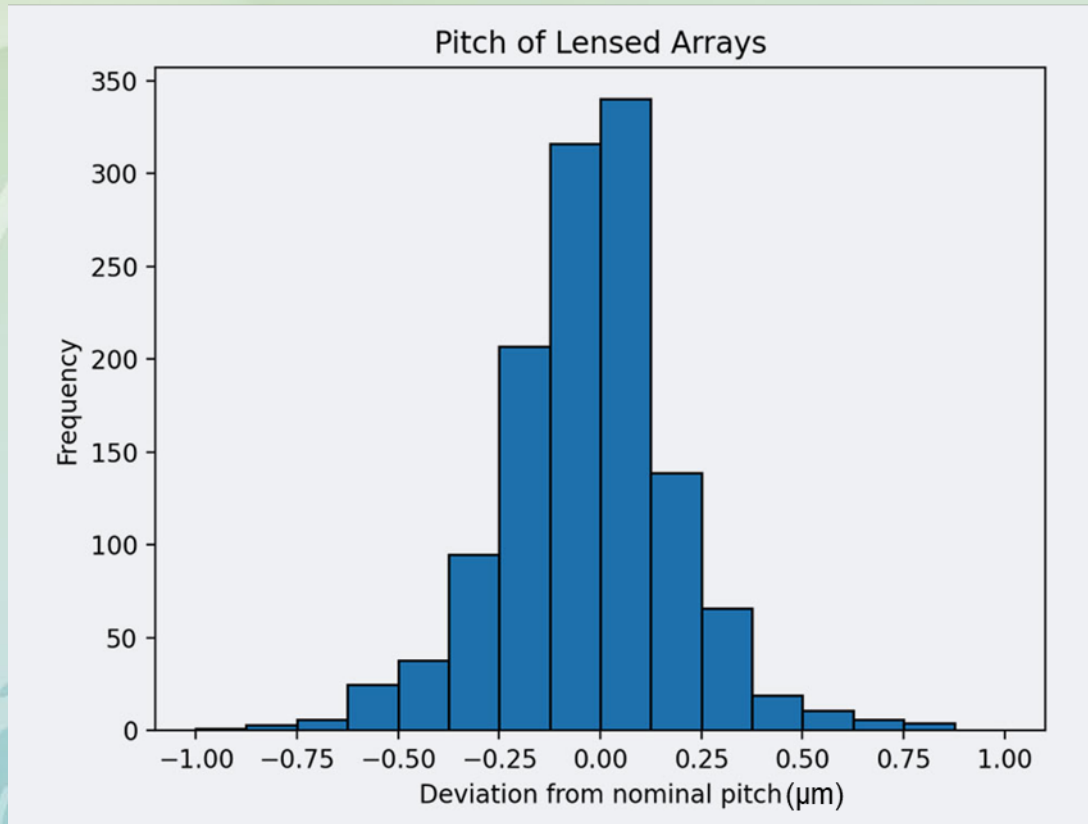
# Fabrication



**Key Takeaway: Fabrication can happen on “anything” including interposer, optical probe cards etc.**

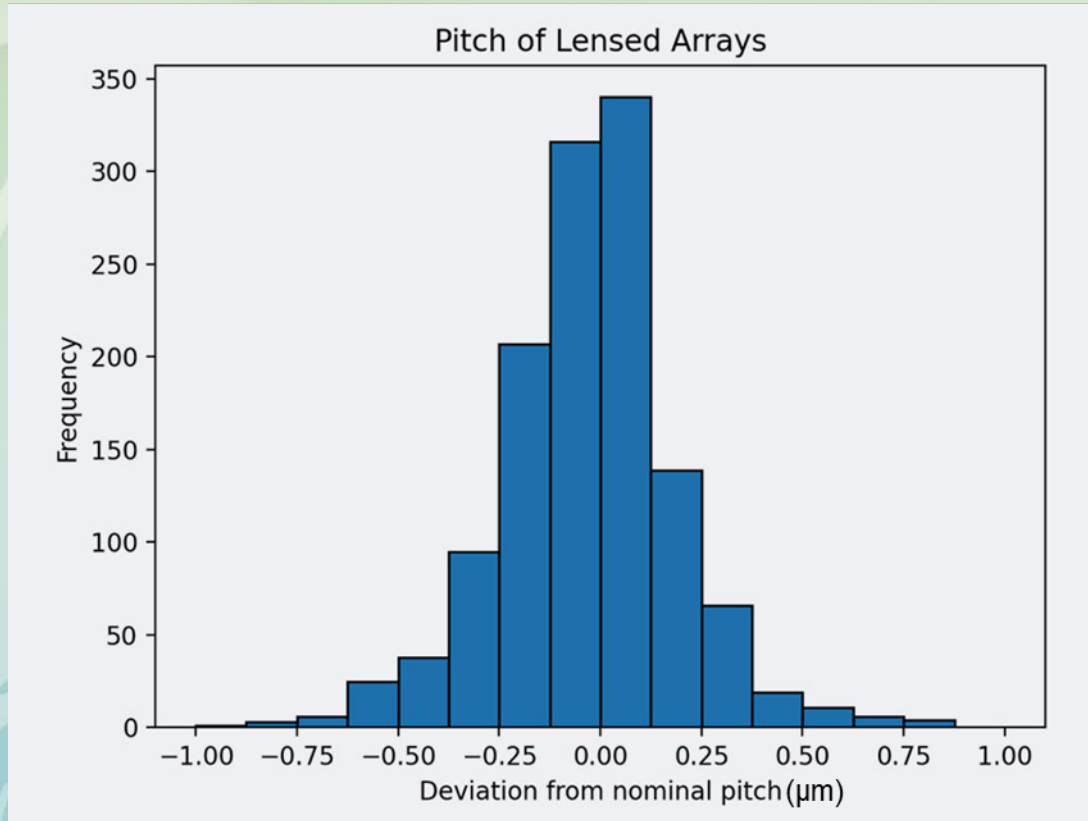


# Fabrication

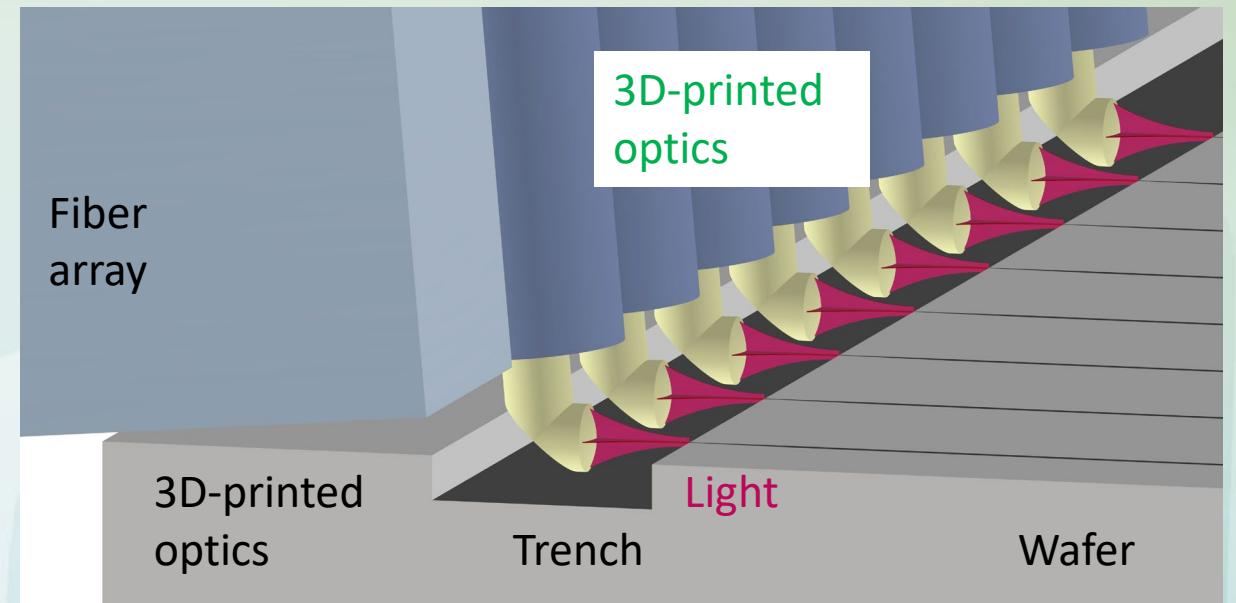




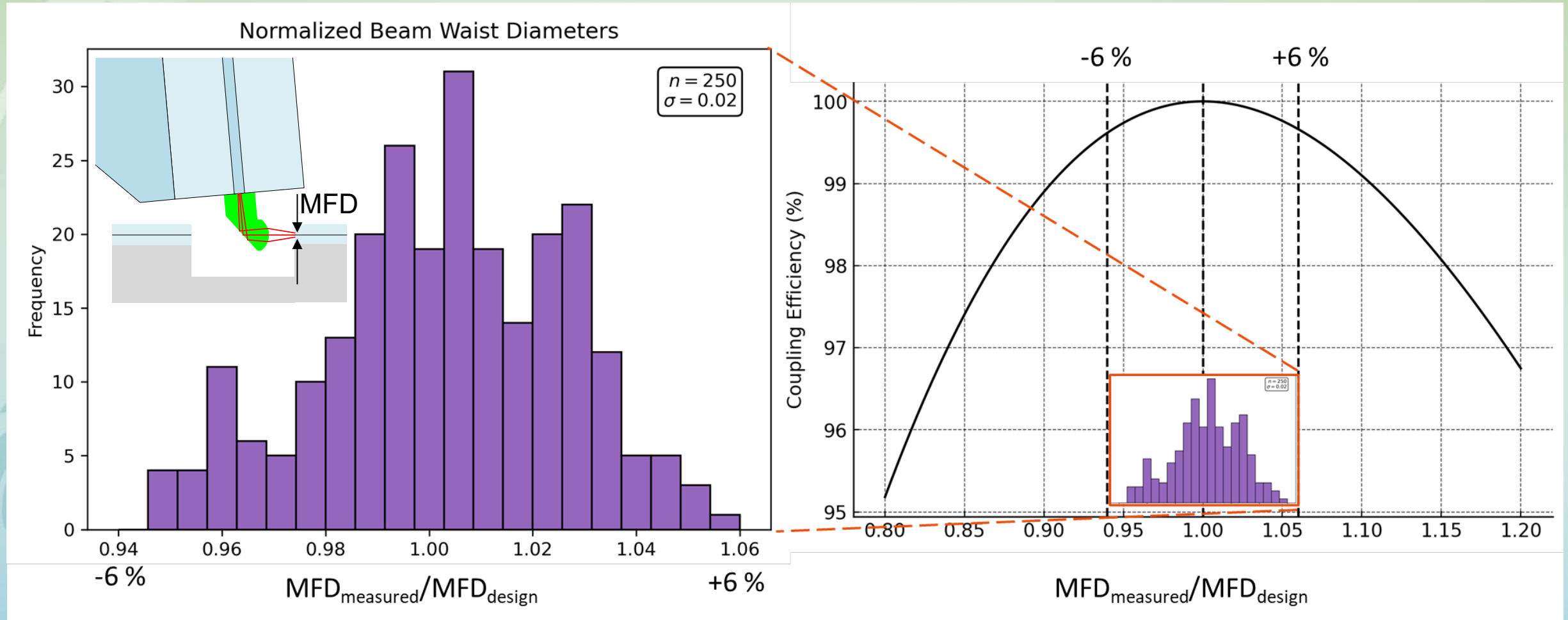
# Multi Channel



**Key Takeaway: Pitch accuracy is sufficient for arrays.**

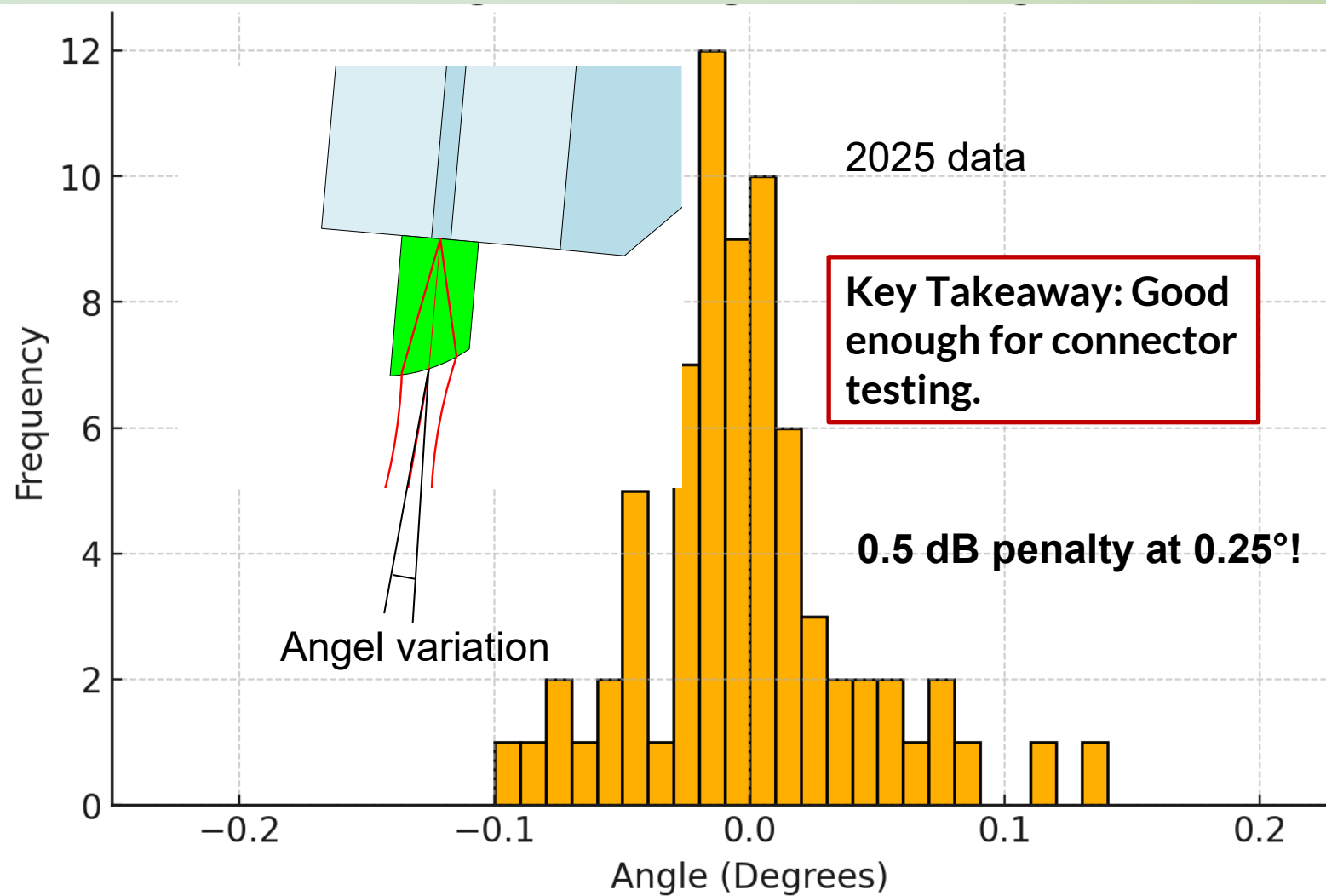
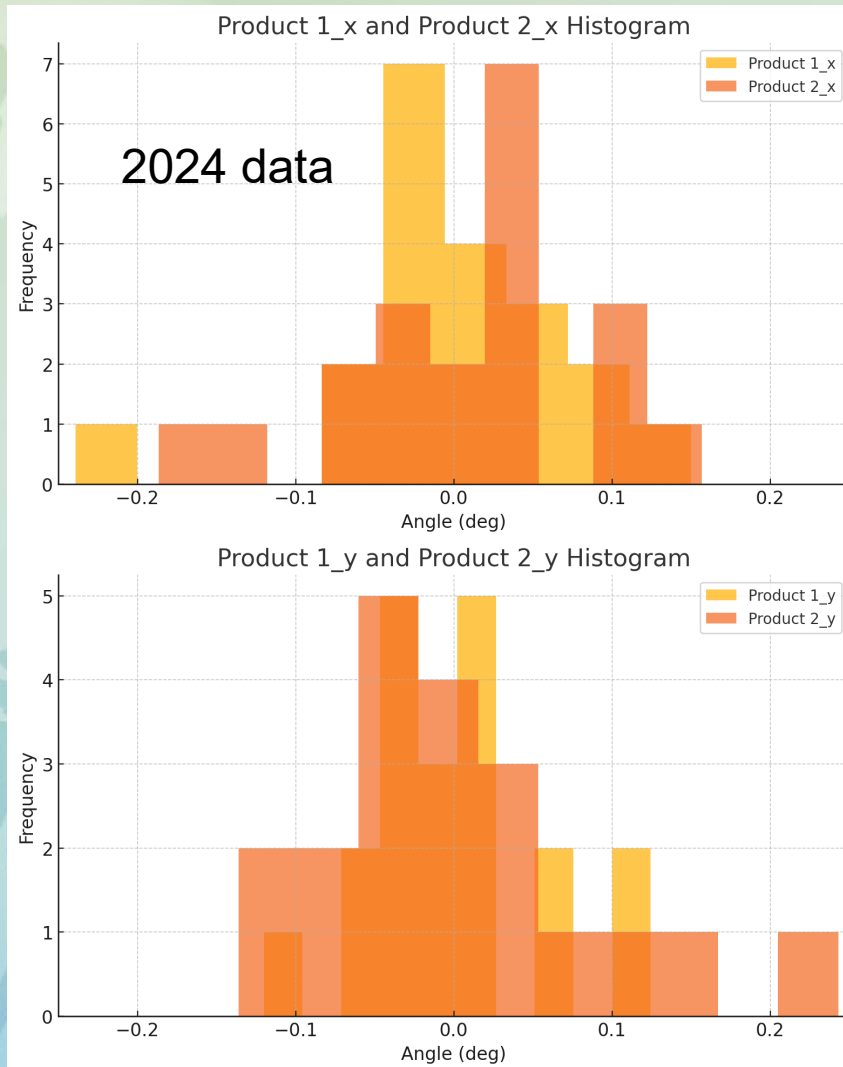


# Mode-Field Size Reproducibility



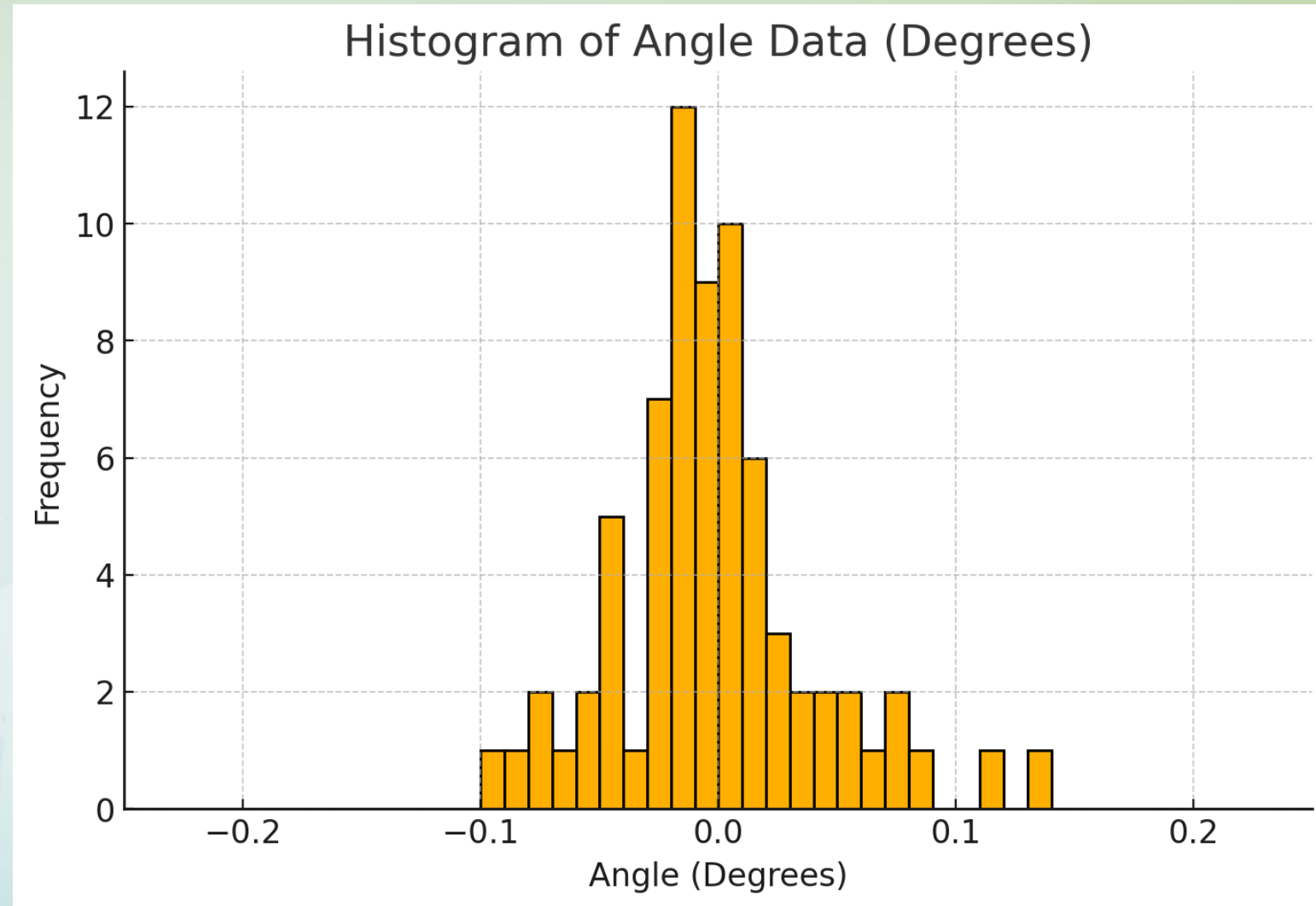
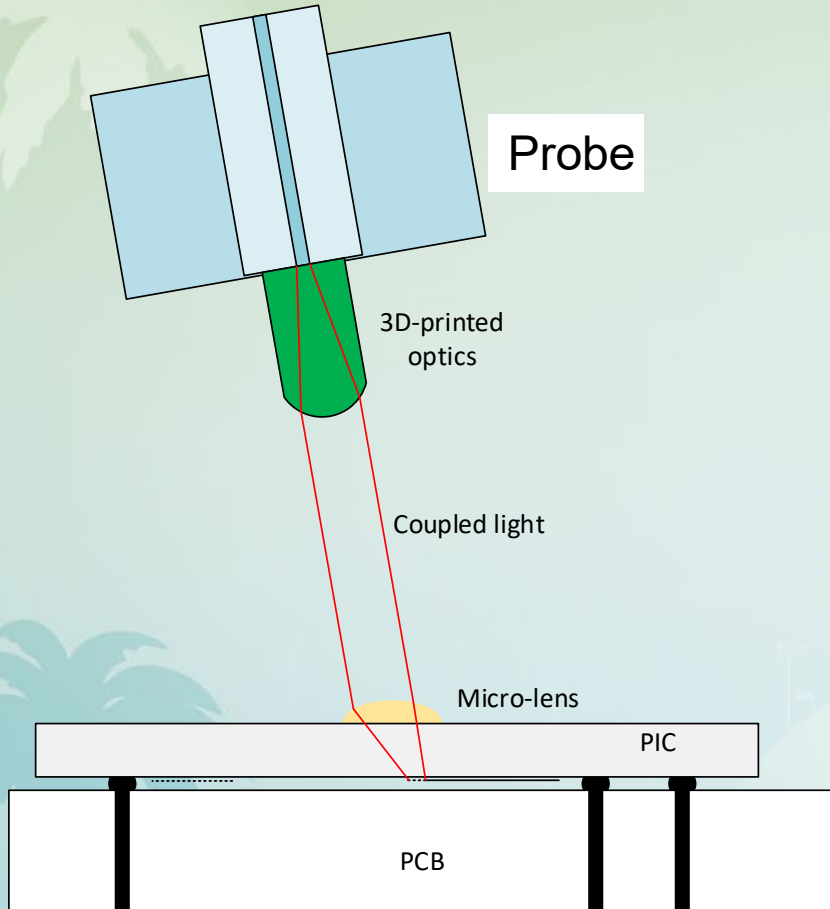
**Key Takeaway: There is “no” mode-field variation.**

# Angular Accuracy

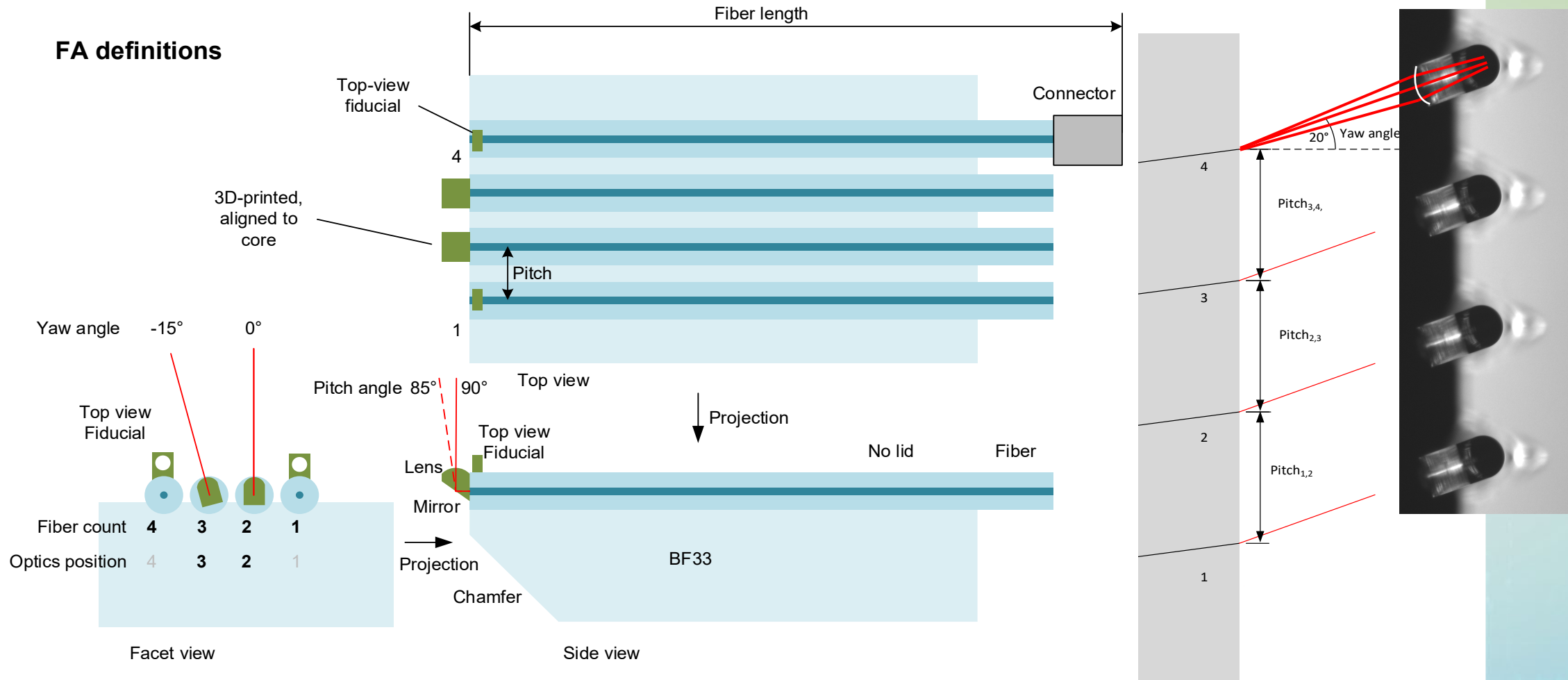




# Suitable for Double-Sided Testing



# Adapting to a Non-Standardized World



**Key Takeaway: Can adapt to most optical**

interfaces.

Philipp Dietrich

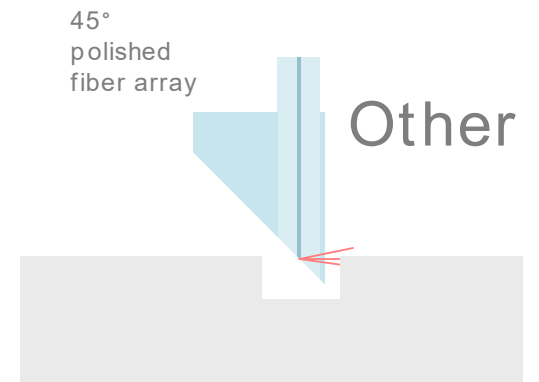
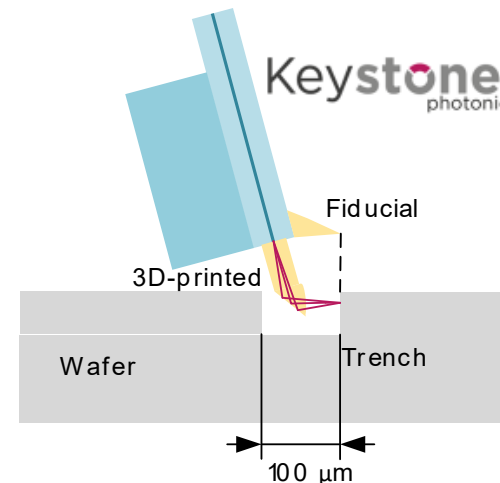
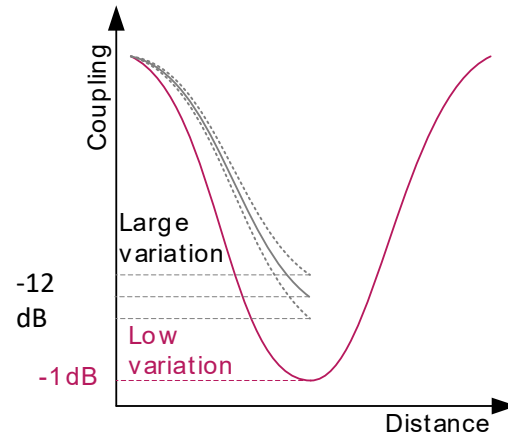
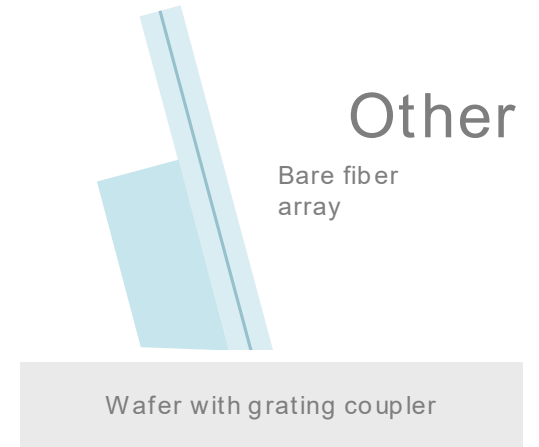
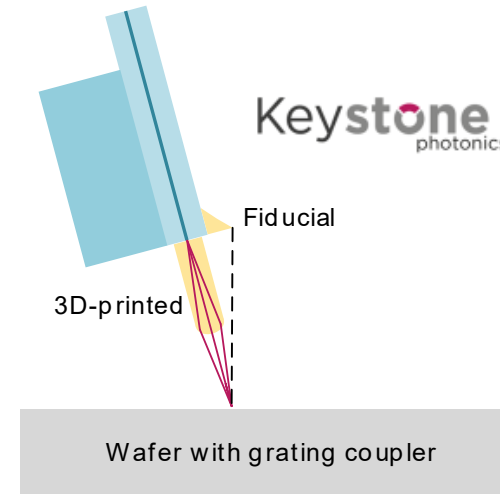
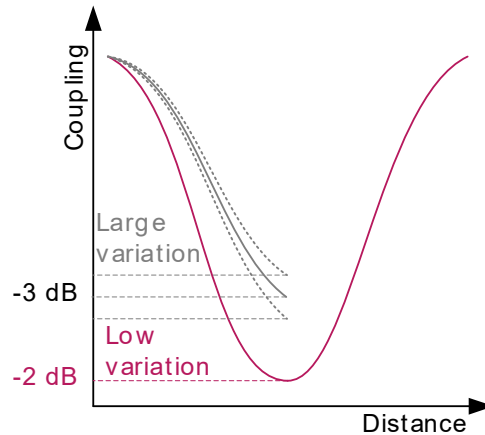
34<sup>th</sup> SWTest Conference | Carlsbad, CA, June 2 - 4, 2025

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# Comparison to Fiber Only Testing

Keystone Probes	Advantage
Reproducible	Detect device variation
Multi channel	Fast
Good coupling	BER testing
Fiducial	Simple alignment
Adjustable angle	Detect emission angle variation
PM-Option	No Pol alignment
Large working distance	Robust testing method
Micro optics	Testing of V-Grooves

**Takeaway: Order-of magnitude improvement vs. no optics**



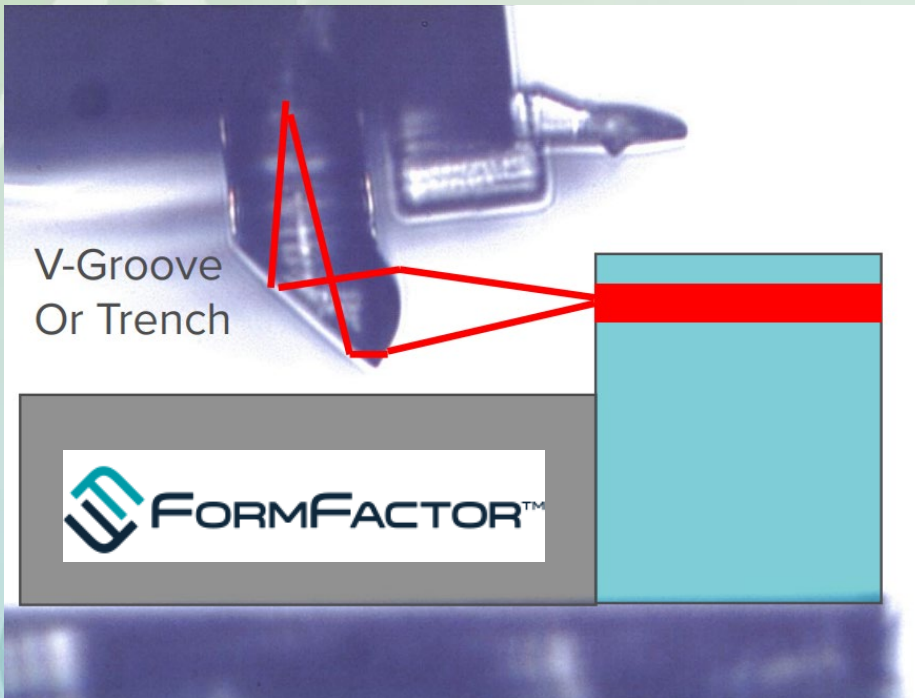


# Other Features, see SWTest 2024

- **Probe properties**
  - High surface accuracy and low surface roughness
  - High-power operation of up to 1W
  - Passes Telcordia tests including damp heat
- **Application**
  - Can be integrated in existing prober using fiducials
  - Pitch conversion down to 20  $\mu\text{m}$
  - Available on customer-specific metal carrier

# Application: Wafer-Level Testing in Manufacturing

Coupling loss is 1.47dB/facet



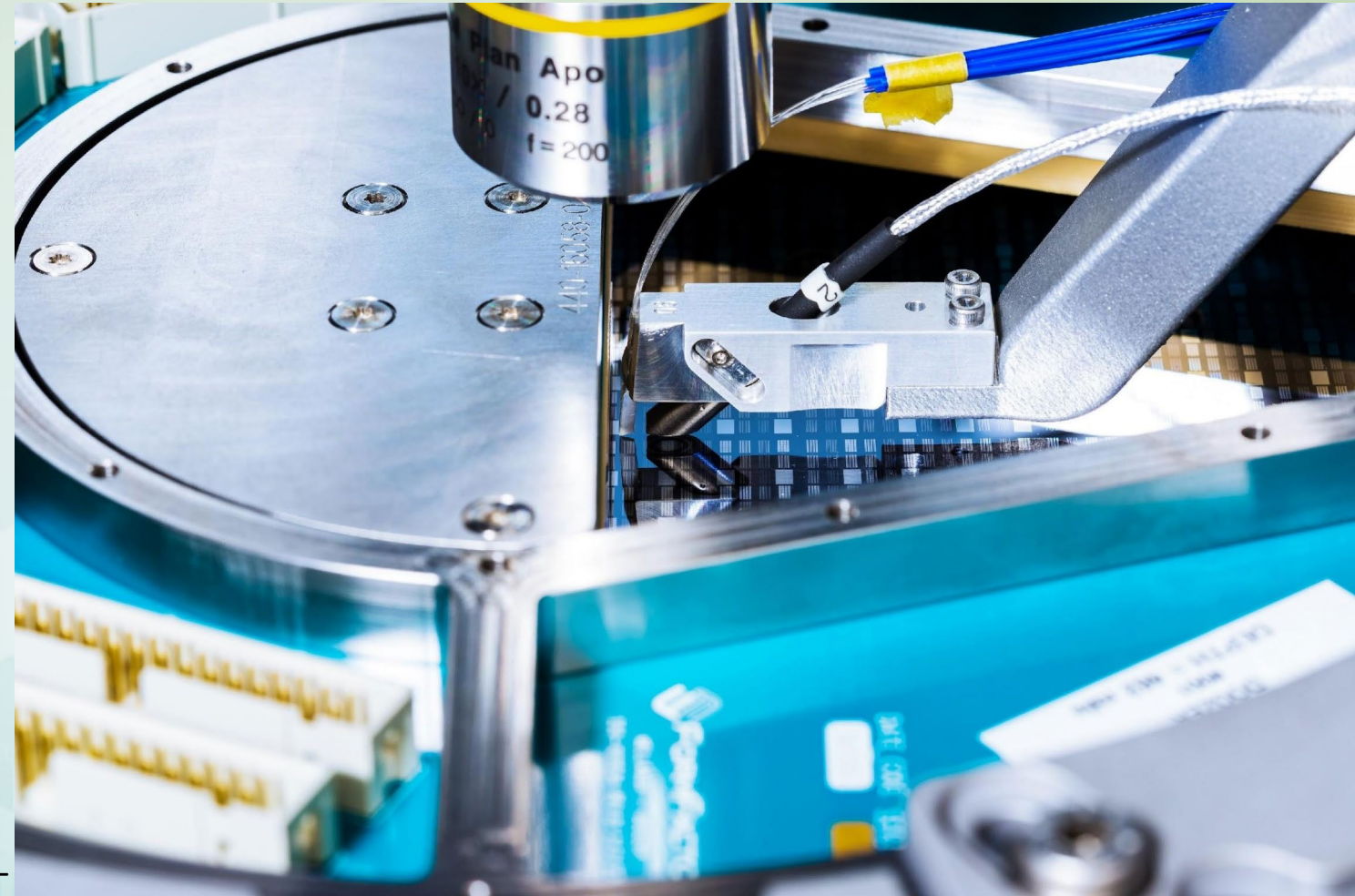
**Available from Formfactor**

[www.formfactor.com/sales-service/contact-sales/](http://www.formfactor.com/sales-service/contact-sales/)

<https://www.formfactor.com/download/fully-automated-integrated-silicon-phonic-wafer-test/?wpdmdl=82376>

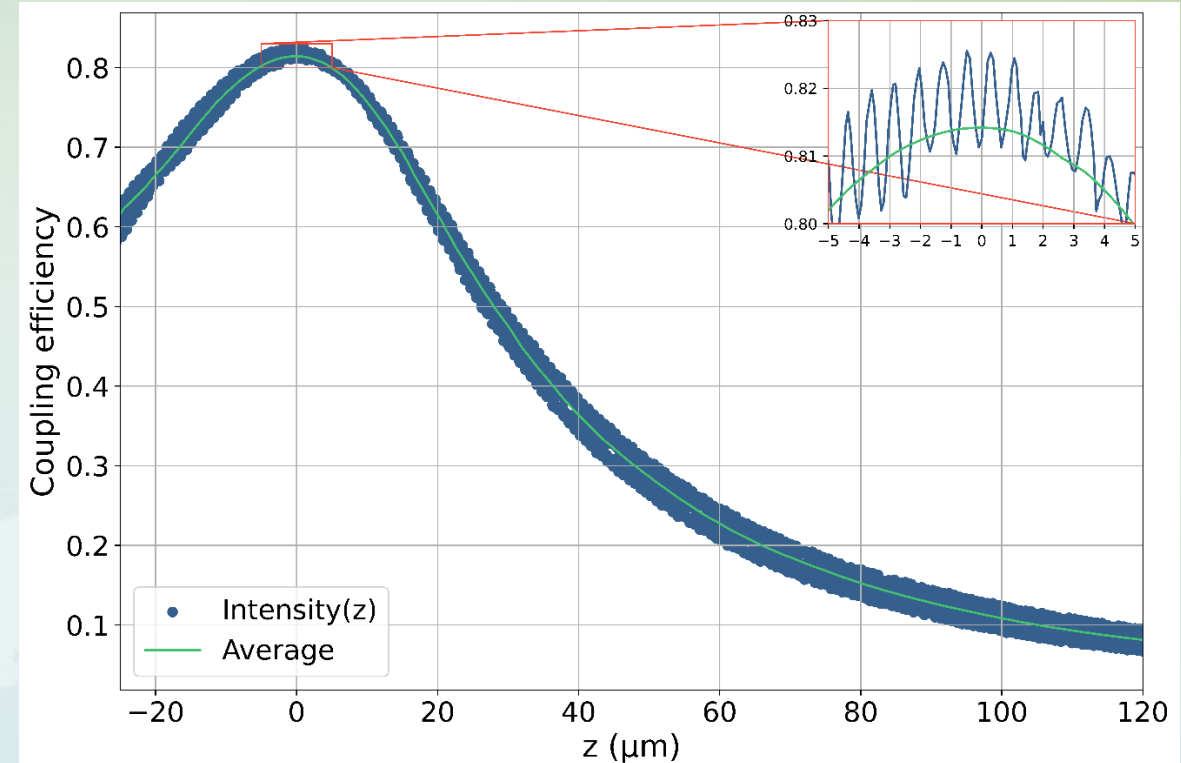
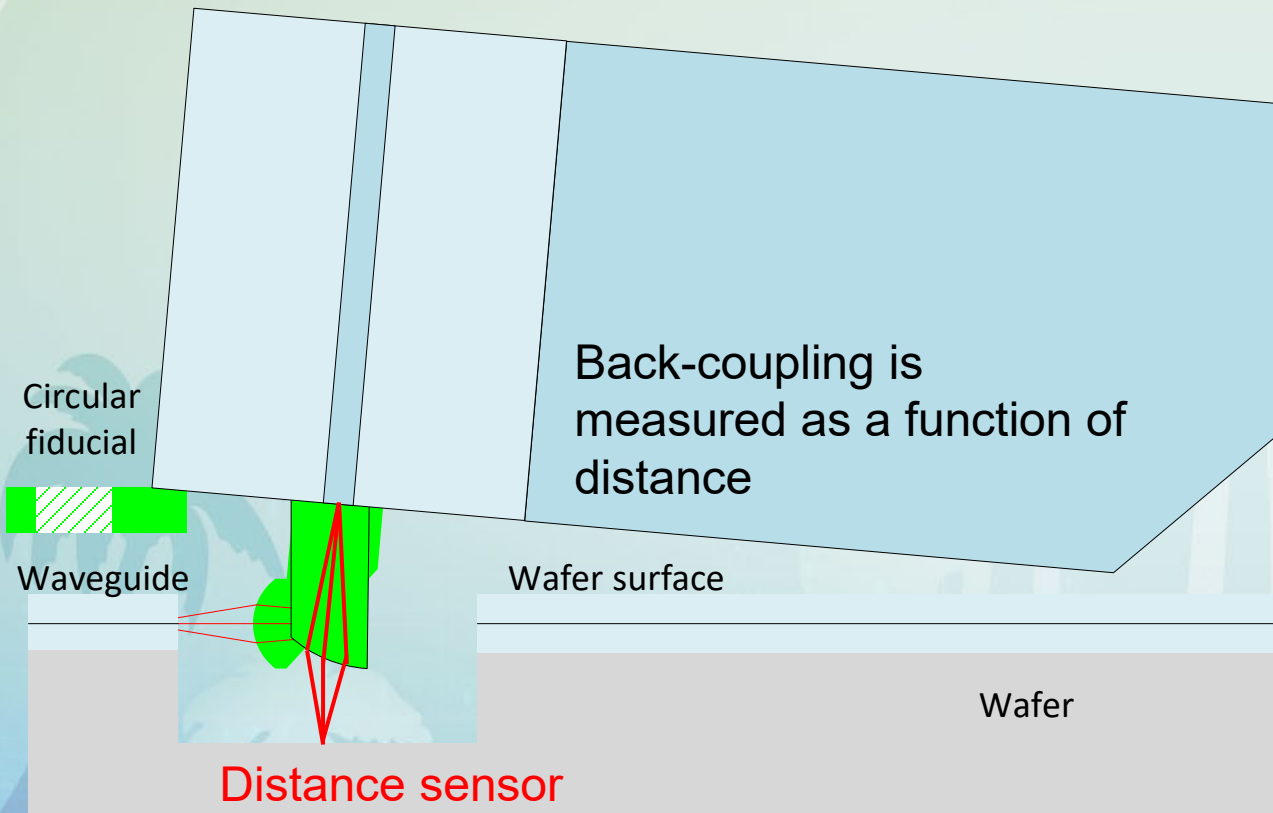
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# Wafer-Level Distance Sensor for Thin Wafer

Using additional channels for distance sensing based on a confocal principle



Measured at flat surface

# Track Record

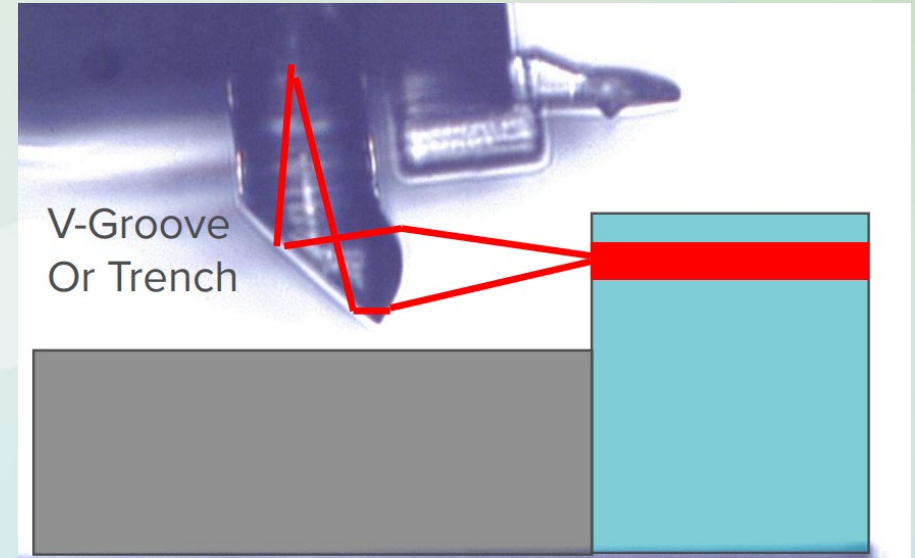
- Based on >10 years of research, basic functionality available since 2015
- First industry customer 2018
- Used in production environment since 2021
- Several thousand probes shipped
- More than 90% industry customers
- Available directly from Keystone or via most testing companies



# Formfactor OFC Release 2025



+TEL  
+Advantest



**Available from Formfactor**

<https://www.formfactor.com/blog/2025/pioneering-high-throughput-wafer-testing-for-silicon-photonics-with-triton/>

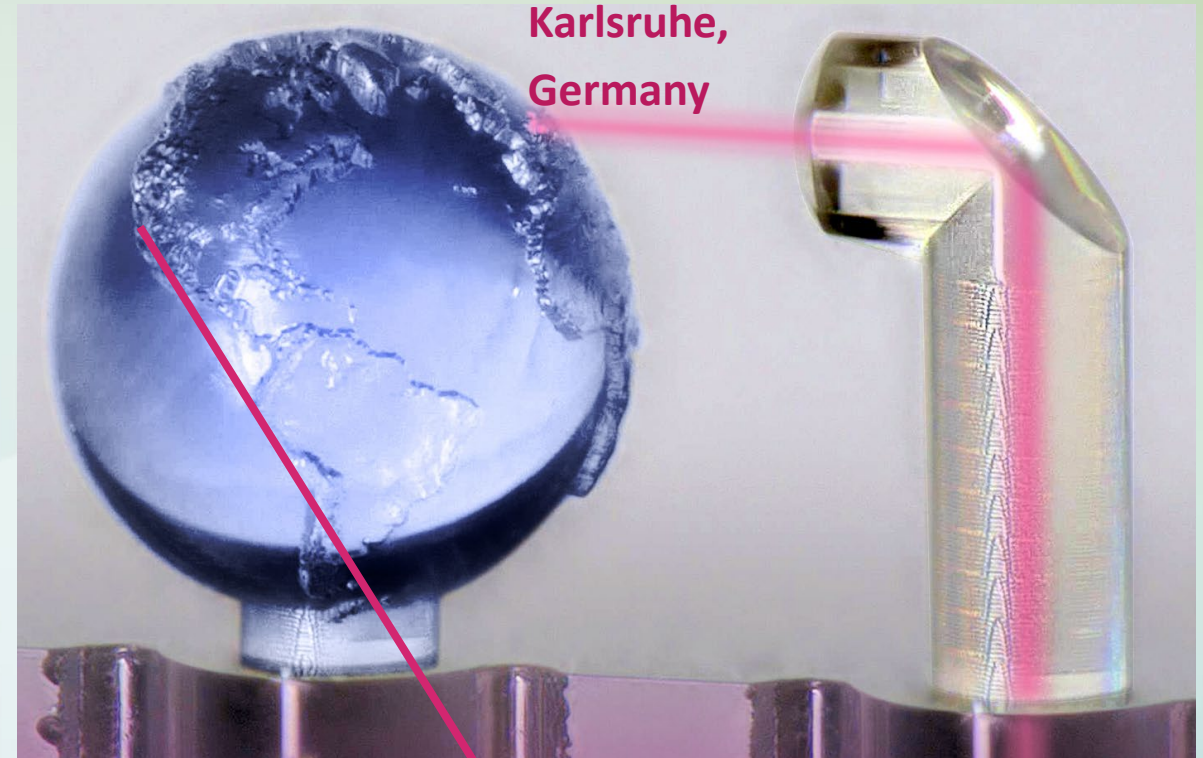
# Ficontec OFC 2025 Release



Sources; Top: Formfactor, SWTest 2024 and OFC 2025, Bottom: Ficontec, OFC 2025

# Key Takeaway

- Wafer-Level Testing plays a crucial role in photonics manufacturing
- Optical Testing always has high accuracy requirements - either angular or translational
- Keystone Photonics can provide a versatile solution for production



**Booth 103**