



SWTEST

PROBE TODAY, FOR TOMORROW

2025 CONFERENCE

Optimizing Probe Card Performance, Longevity, and Cost for Small Parametric Pads



Victoria TRAN, PhD

Director of Research and Development at Gel-Pak

Garrett TRANQUILLO

Sr. Technical Sales and Applications Engineer at Celadon Systems

Overview

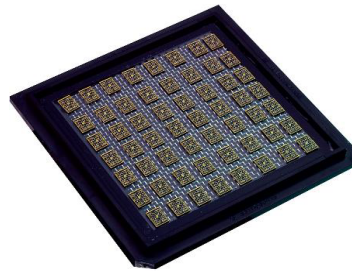
- Gel-Pak and Celadon Corporate Snapshots
- Parametric Test – Function and Challenges
- Probe Tip Cleaning – Function and Considerations
- Motivation
- Probe Cleaning Qualification Plan
- Experimental Results
- Customer Confirmation
- Cost of ownership
- Summary

Innovative Solutions that Drive OEE

Three ISO 9001-2015 Certified Manufacturing Facilities:

- Over 95,000 square feet of Materials Manufacturing
- ISO Class 10,000 Cleanrooms
- ISO Class 7 Cleanrooms
- Over 200 Employees
- Global Sales and Applications Support Network

SMALL DIE SHIPPING & HANDLING



Vacuum Release (VR) Carriers

- Automated pick & place applications for bare die and devices ranging from <250 micron to 75mm in size.
- Suitable for transport and handling MEMs Probes

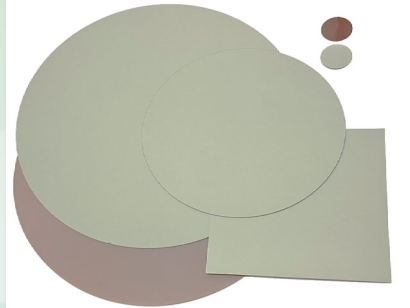
TEXTURED CARRIER PRODUCTS



Textured Device Carrier Products

- Universal Fixture for device handling in-process, singulated die testing, and shipping.

ELASTOMER PROBE CARD CLEANING FILMS



Gel-Probe Elastomer Cleaning

- Custom coating of highly engineered elastomer films for semiconductor applications.
- Customizable probe card cleaning wafer and cleaning sheet applications.

40-Years of Materials Expertise

CELADONTM

A Wholly Owned Subsidiary of MPI CORPORATION

Celadon Systems is singularly focused on providing on-wafer probing solutions of the highest quality to the semiconductor, space and defense, and medical industries.

1997
Founded

**Burnsville,
Minnesota**
Headquarters



20,000+
Probe Cards used
Globally

6,000+
High Performance
Cables used Globally

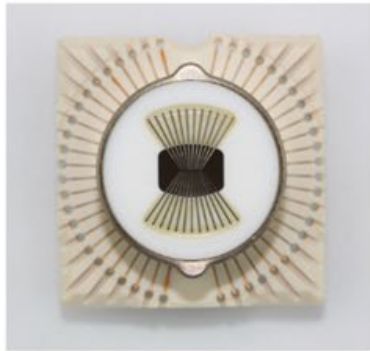
2021
Acquired by MPI
Corporation

The Home of Peace of Mind ProbingTM



Key Features

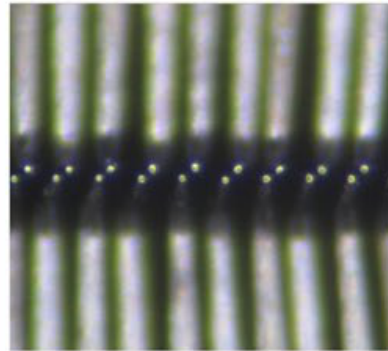
Robust with Long Lifetimes



Low Maintenance,
Low Cost of Ownership

***Millions of
Touchdowns***

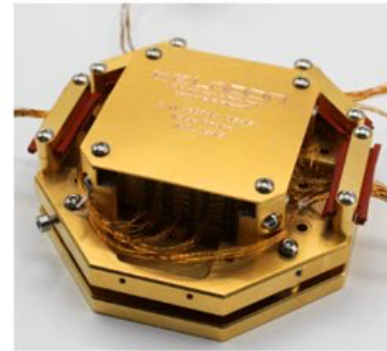
Accurate Measurements



Low Noise, Low
Leakage

***<30 μ m Pads at
Temperature***

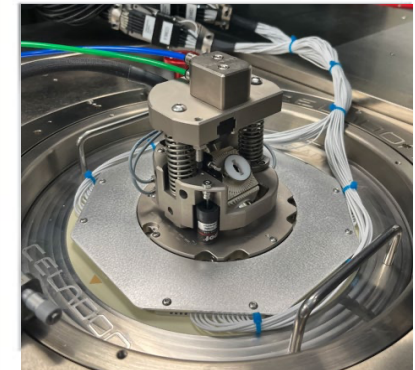
Extreme Temperatures



Widest Operating
Range

***-65C to 600C+
Down to 2 Kelvin***

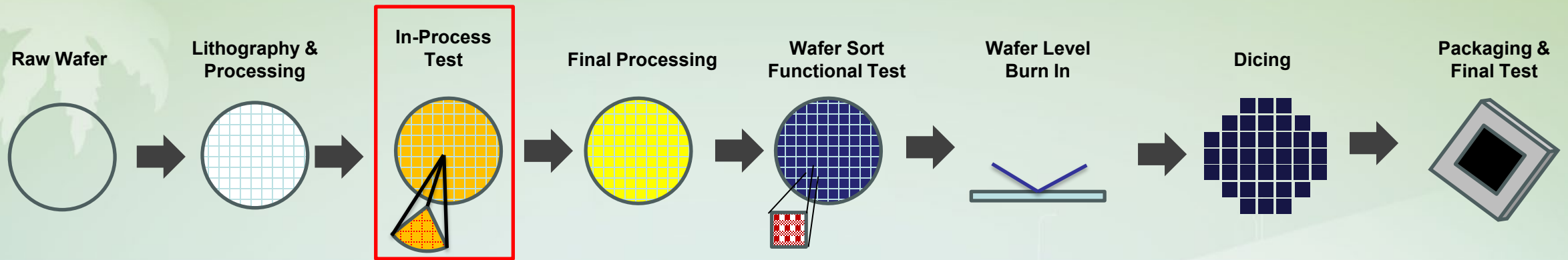
Versatility



Modular Solutions for
Labs and Production

***Fixed,
Adjustable, and
Automated***

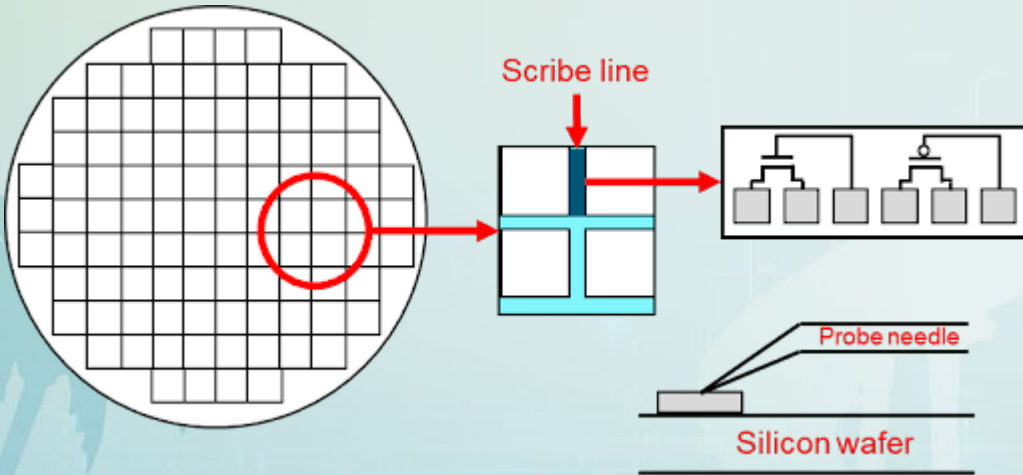
Parametric Test Background



- Performed during and after wafer fabrication
- Monitors existing in-line and end of line processes
- Identifies the performance characteristics of the device being tested
- Confirms wafers are being properly fabricated
- Checks wafer-level reliability
- Provides historical data for decision-making
- Reduces the amount of batch processing errors

Parametric Test Background

- Special test structures (capacitors, diodes, transistors and inductors) simulating actual devices are designed into the space adjacent to the devices.

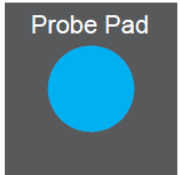


Test structures are limited by the available area in the narrow region adjacent to the devices

Pad dimensions are small – typically 40um

Source: K. Butler, MEPTEC REPORT 2021

Parametric Probing Process Considerations



- Probe needle lands inside its probe pad → pass
 - Low resistance



- Probe needle lands outside its probe pad → fail
 - High resistance



- Probe needle partially in its probe pad → pass
 - Contact resistance is proportional to the contact area
 - Should have “good” contact resistance with <100% contact



- If there's a wire next to the probe pad → pass but shorted

- Probing must be consistently within small pad to have reliable data and prevent damage to adjacent devices
- Consistent CRES Required, <1.5ohm
- Low Leakage Required

		Pad Size X (μm)									
		5	10	15	20	25	30	35	40	45	50
Pad Size Y (μm)	5	2%	12%	16%	18%						
	10	27%	63%	59%	52%		64%		59%		57%
	15	28%	77%	63%	58%		61%		55%		59%
	20	33%	66%	58%	72%	64%	65%	65%	78%	80%	85%
	25				82%	84%	82%	82%	82%	82%	82%
	30		67%	82%	82%	82%	82%	82%	82%	82%	82%
	35				82%	82%	82%	100%	100%	100%	100%
	40		69%	76%	73%	73%	73%	100%	100%	100%	100%
	45				91%	91%	91%	100%	100%	100%	100%
	50		73%	72%	82%	82%	82%	100%	100%	100%	100%

Source: Smith, Hall, and Tranquillo ICMT 2023

Cleaning Challenge | C_{RES} & Lifetime

- Probes touch the DUT, but the Current Might NOT Flow !
- Probe cleaning is a “dirty business” and critical for controlling contact.

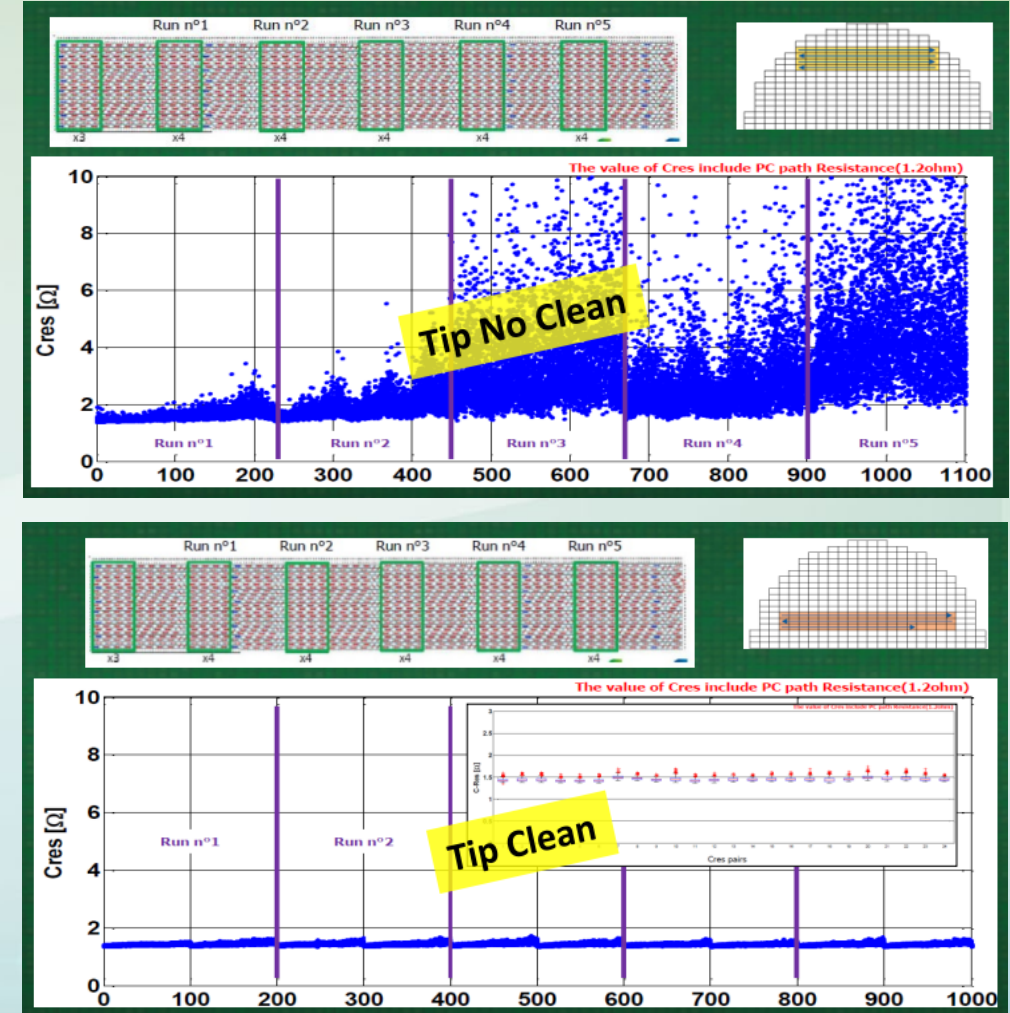
METALLIC CONTACT

$$C_{RES} = \left[\frac{(\rho_{probe} + \rho_{pad})}{4} \sqrt{\frac{\pi H}{P}} \right] + \frac{\sigma_{film} H}{P}$$

Film Resistance

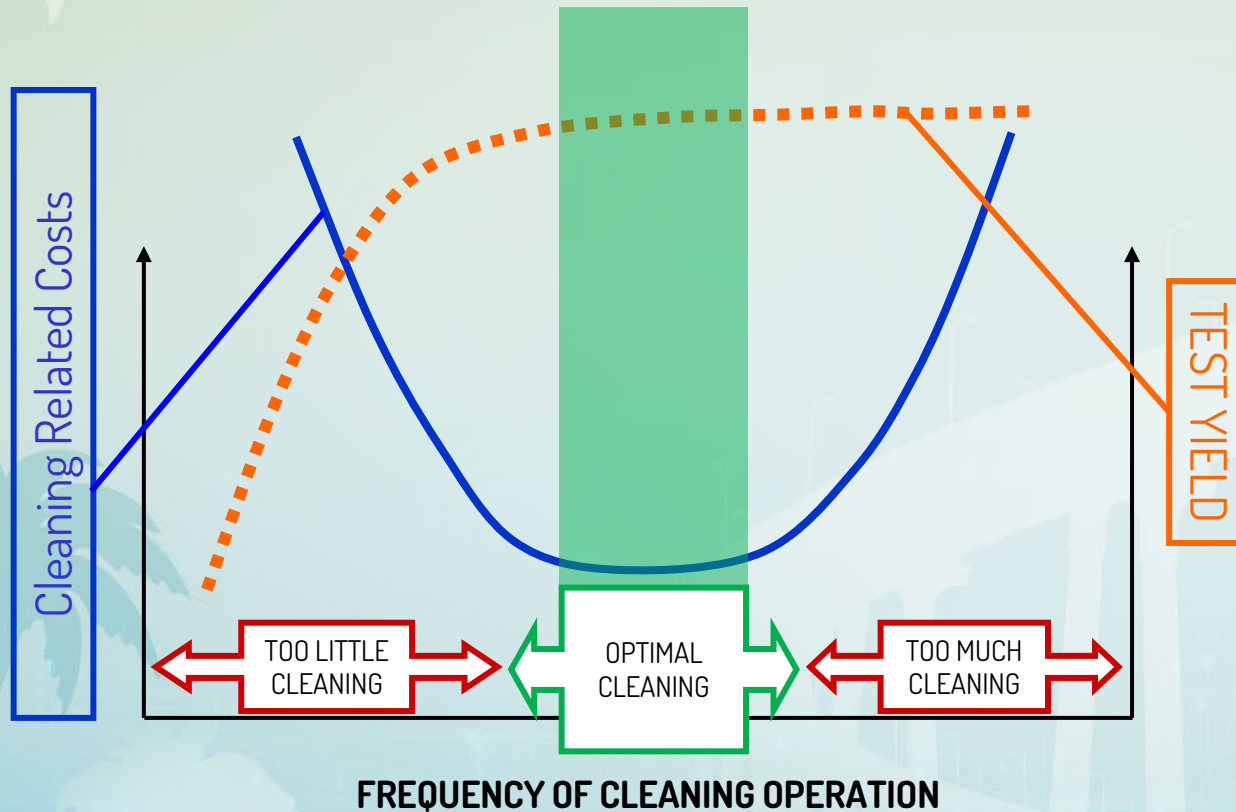
- ρ_{pad} , ρ_{probe} , σ_{film} = resistivity values
- H = hardness of the pads, bumps, pillars, etc.
- P = contact pressure applied by probe

Implement efficient cleaning
to ensure continuous and reliable electrical contact.



Source: R. Vallauri, D. Perego, M. Prea, J. Kim, and J. Yun, SWTest 2017

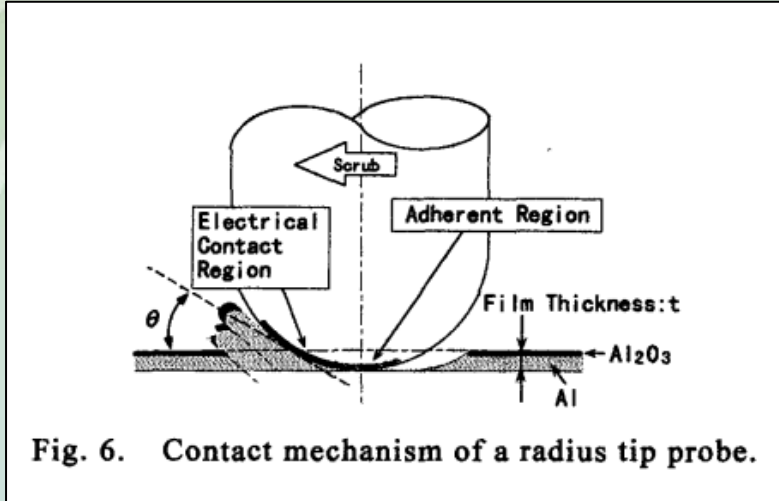
Cleaning Challenge | CRES & Lifetime



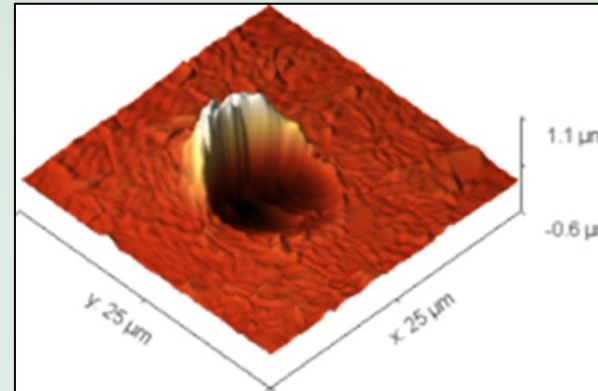
- Cleaning can consume more than 95% of a probe card lifetime.
- With aggressive cleaning test costs increase.

Source: J Broz, SWTest 2007

Tip Shape Importance

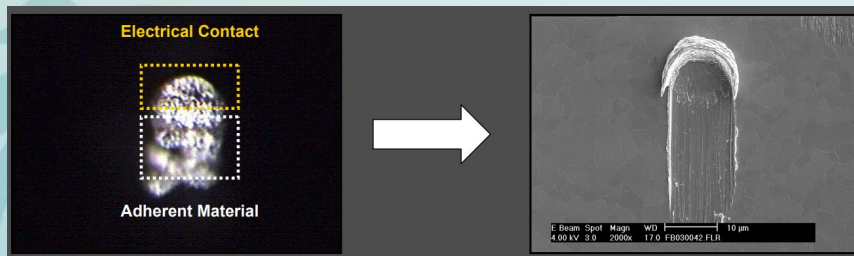


Source: S. Maekawa et al., ECTC 2000

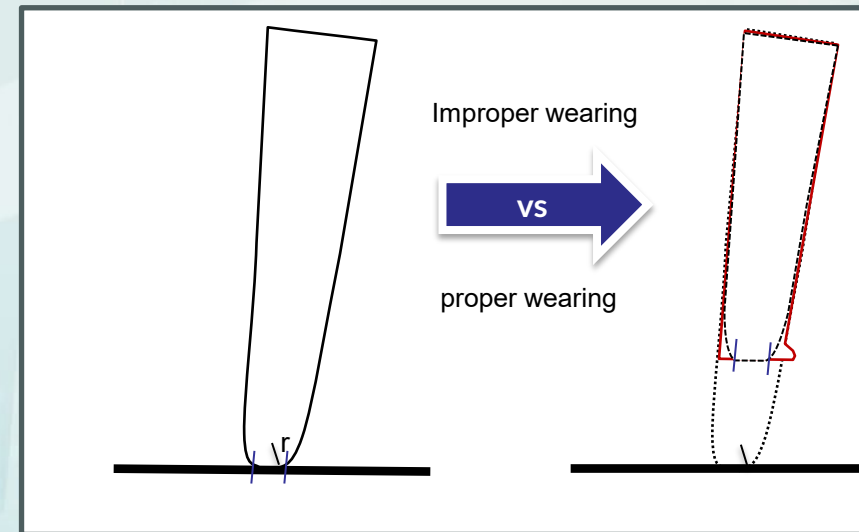


Contact resistance stability is related to contact area, probe tip diameter, and probe tip roughness

- Small, rough and round probe tips \rightarrow stable electrical resistance
- Large, smooth and flat probe tips \rightarrow unstable electrical contact resistance.

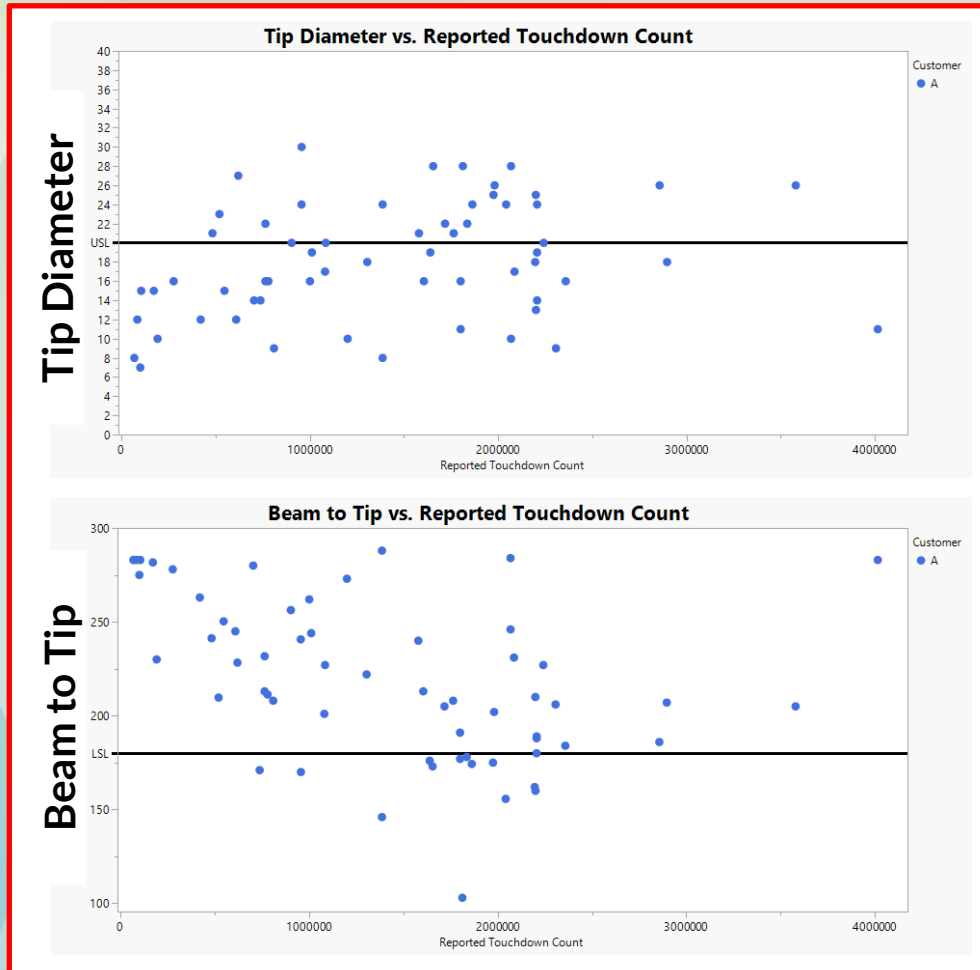


Source: Stalnaker et al., IEEE SWTW 2003



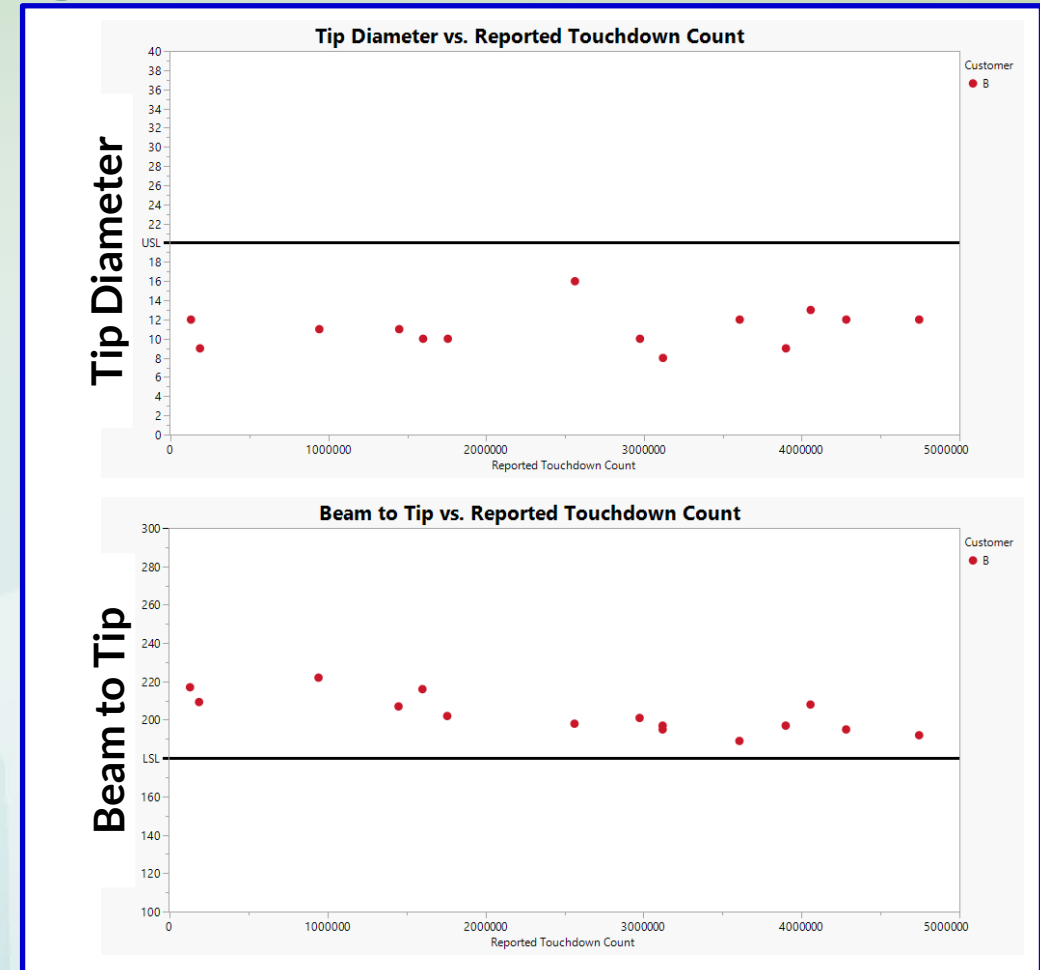
Tip shaping must retain small tip diameter especially for small pads

Proper Cleaning Importance



Customer A – Cleaning Process Not In Control

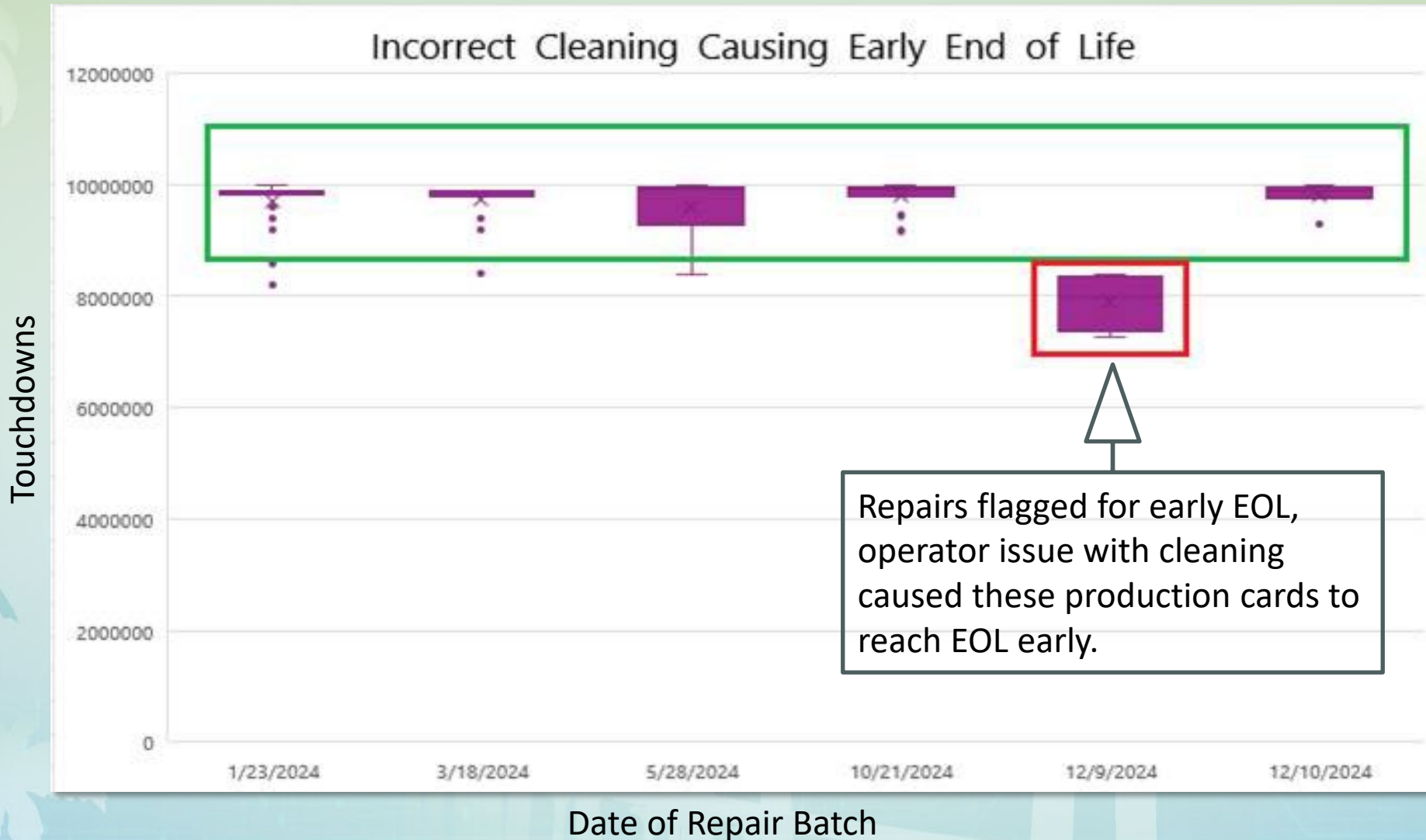
- Tip diameter and BTT loss is noisy
- Early end of life



Customer B – Cleaning Process In Control

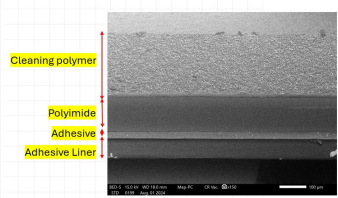


- BTT loss and diameter are steady
- Extended probe card life

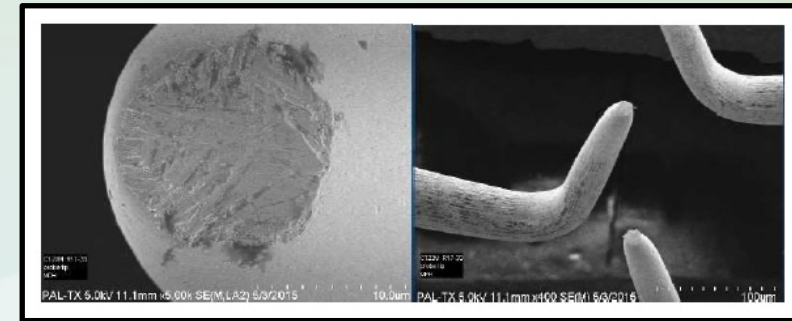
Proper Cleaning Importance



Motivation

Customer FAQ: What cleaning process should I use for my probe cards?

Polymer	Hard Clean
	
Encapsulated Abrasive	Exposed Abrasive Surface
Penetration resistant to low force probes	Scrub across surface, not applicable to shaped tips
Smooth texture imparted onto tip area	Various textures imparted onto tip area
Low Wear 	Wears quickly 



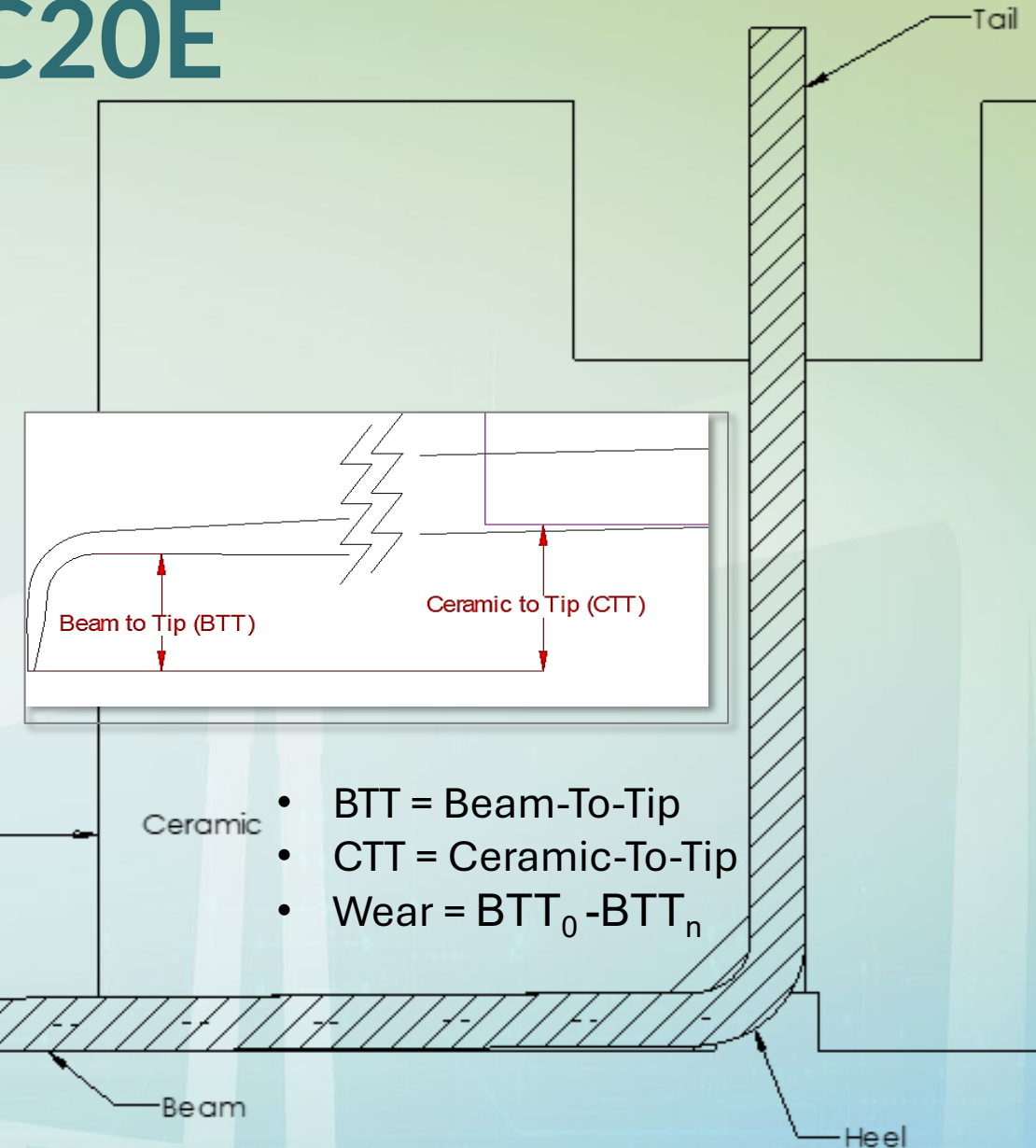
Requirements

- Clean and maintain low CRES
- Consistent Tip Shape and Texture
- Low wear and cost of ownership

Celadon VC20E

Specifications

- 48 channels with VC20E; up to 100 channels with VC43E
- Rated from -65°C to 200°C
- <5fA/V @ 10s 25C signal to signal leakage
- Up to 1.1kV; or 3kV with VC20EHV (High Voltage)



Cleaning Regimen Qualification for VC20 Advanced Cantilever

1. Mimic a customer process using a blanket aluminum wafer

- Verify elevated and unstable CRES can be achieved
- Visualize and assess scrub marks

2. Confirm CRES recovery testing with Celadon recipe

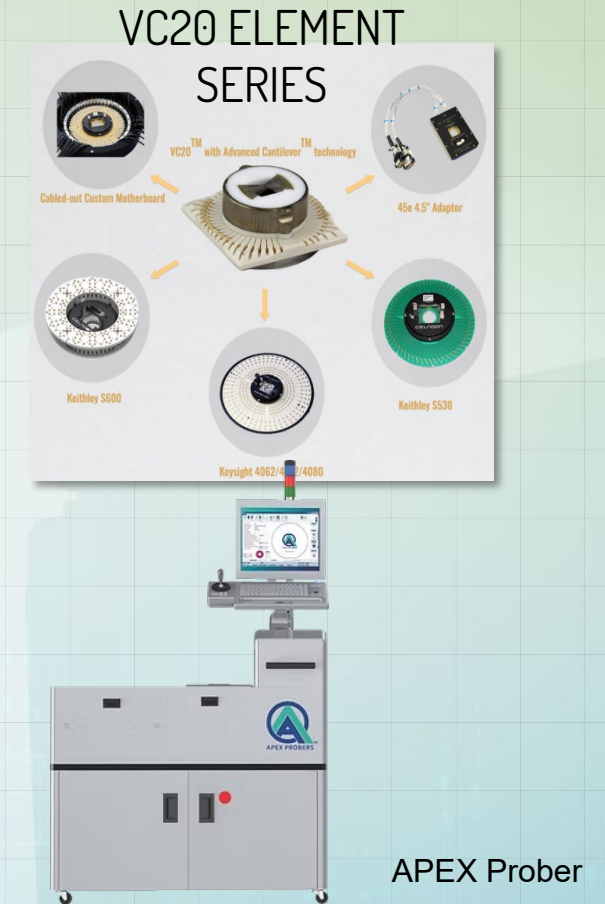
- Probe card is “made dirty” with multiple TDs
- Cleaning performance is demonstrated
- CRES recovery

3. Wear testing with cleaning execution Requirements

- “Long term” tip wear
- Tip shape change
- Exceed 10M AL-TD (with cleaning) target
- Scrub length assessment (virtual pad)

4. Qualification // Verification

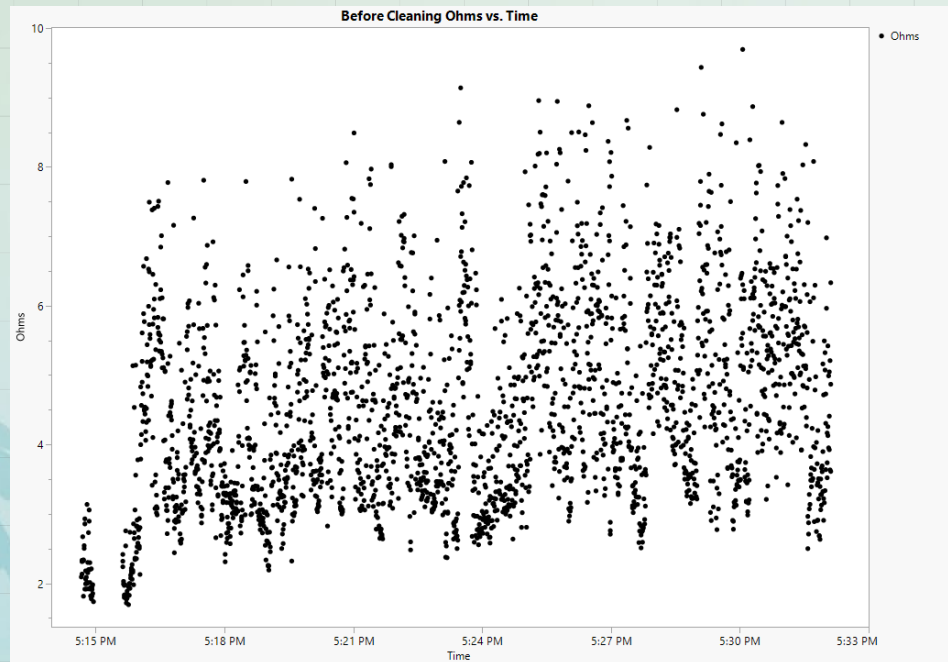
- Customer Verification



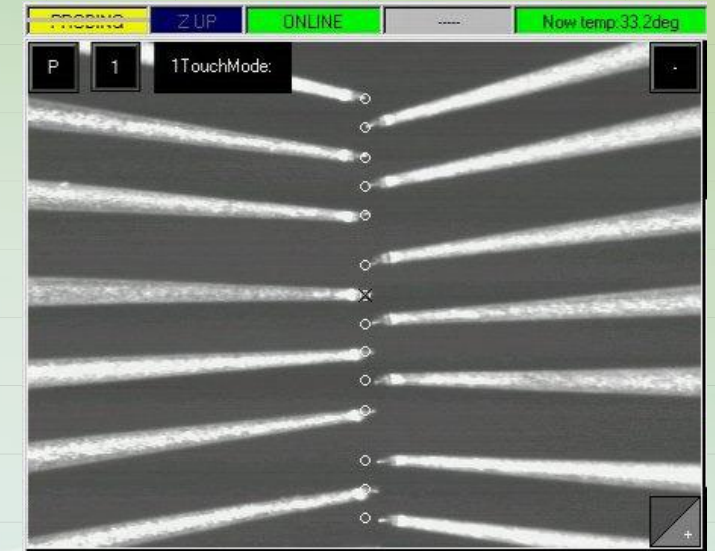
Qualification Plan

1. Mimic a customer process using a blanket aluminum wafer

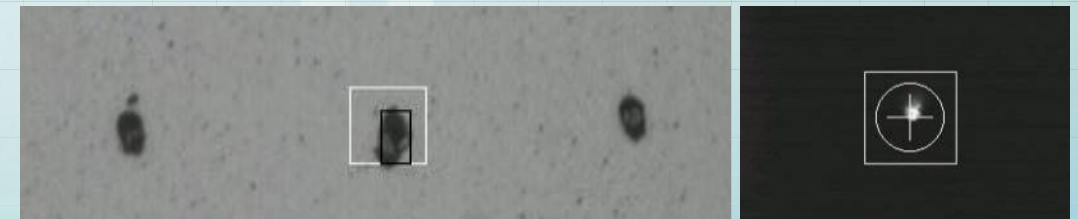
- ✓ Verify elevated and unstable CRES can be achieved.
- ✓ Visualize probes and assess scrub marks.



~2500 TD without cleaning show CRES instability



Probe 4

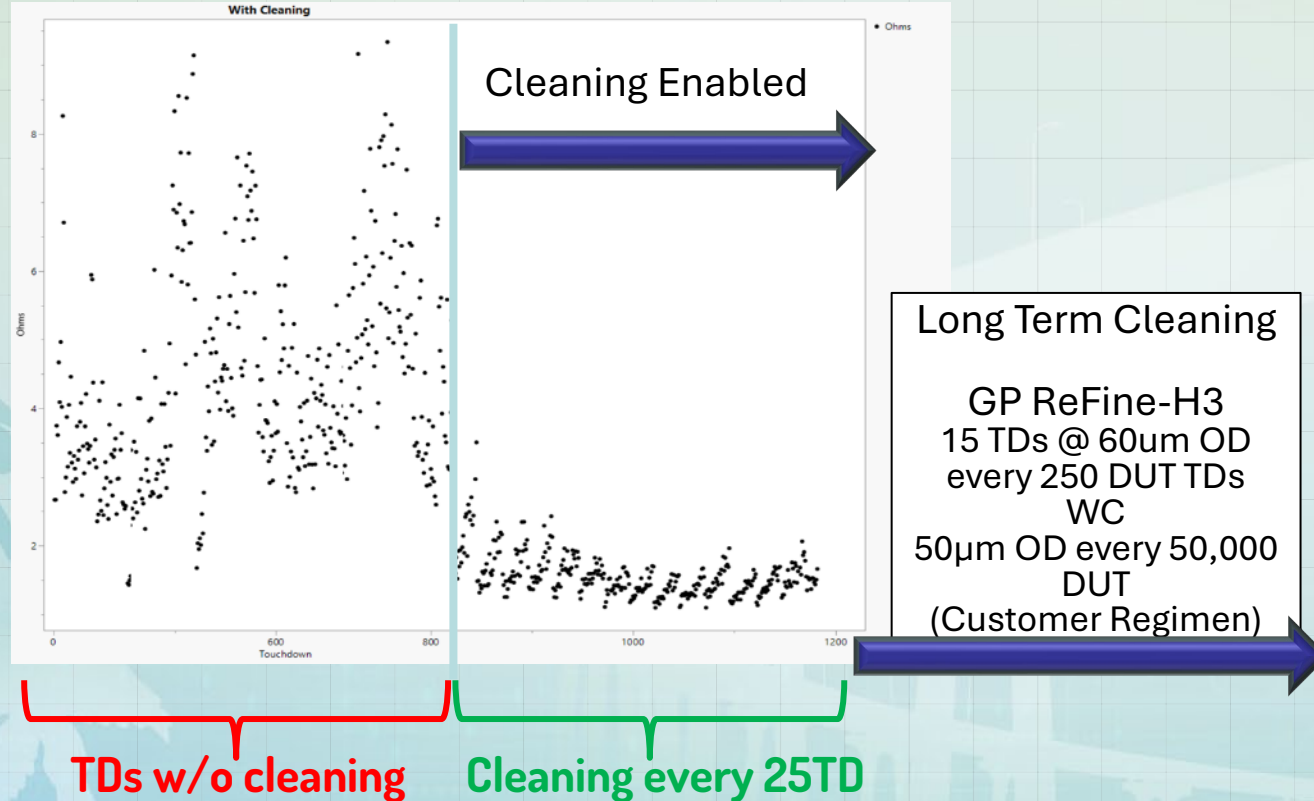


Probe 14

Qualification Plan

2. Confirm CRES recovery testing with Celadon recipe

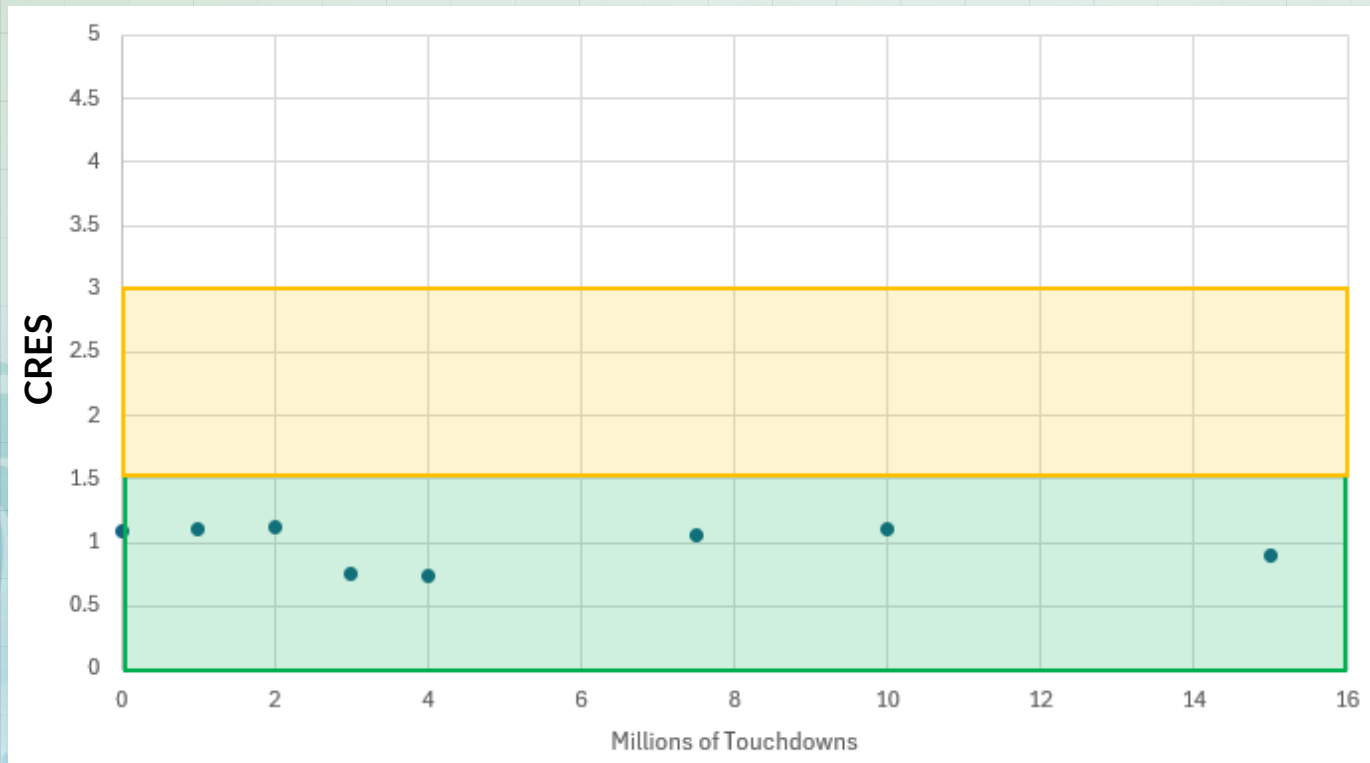
- ✓ Probe card is “made dirty” with multiple TDs.
- ✓ Cleaning performance demonstrated.
- ✓ CRES recovery



Qualification Plan

2. Confirm CRES recovery testing with Celadon recipe

- ✓ Probe card is “made dirty” with multiple TDs.
- ✓ Cleaning performance demonstrated.
- ✓ CRES recovery

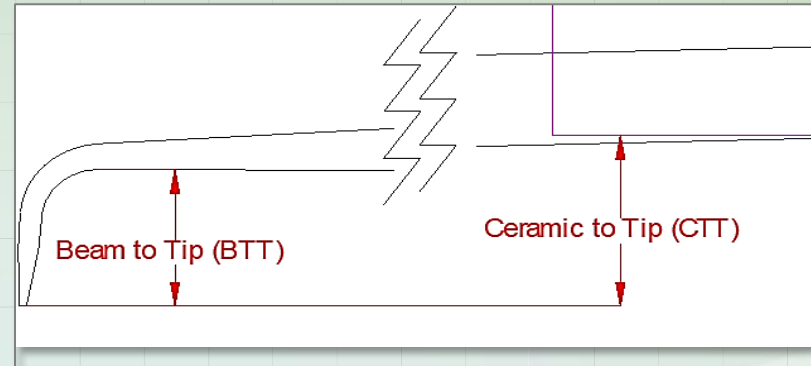


CRES Recovery verified thru
15 million touchdowns

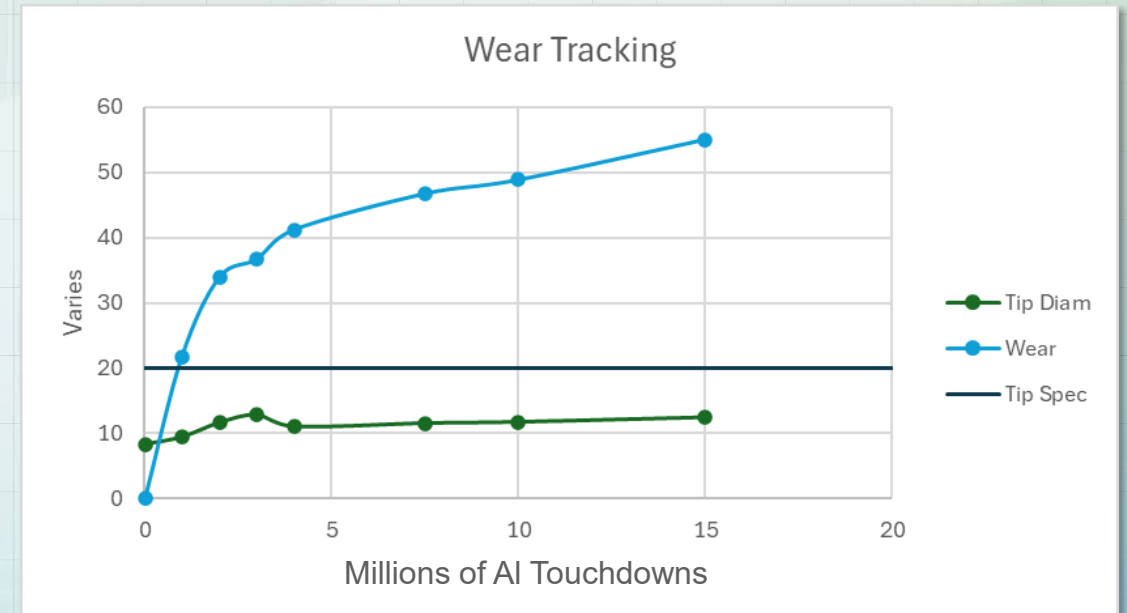
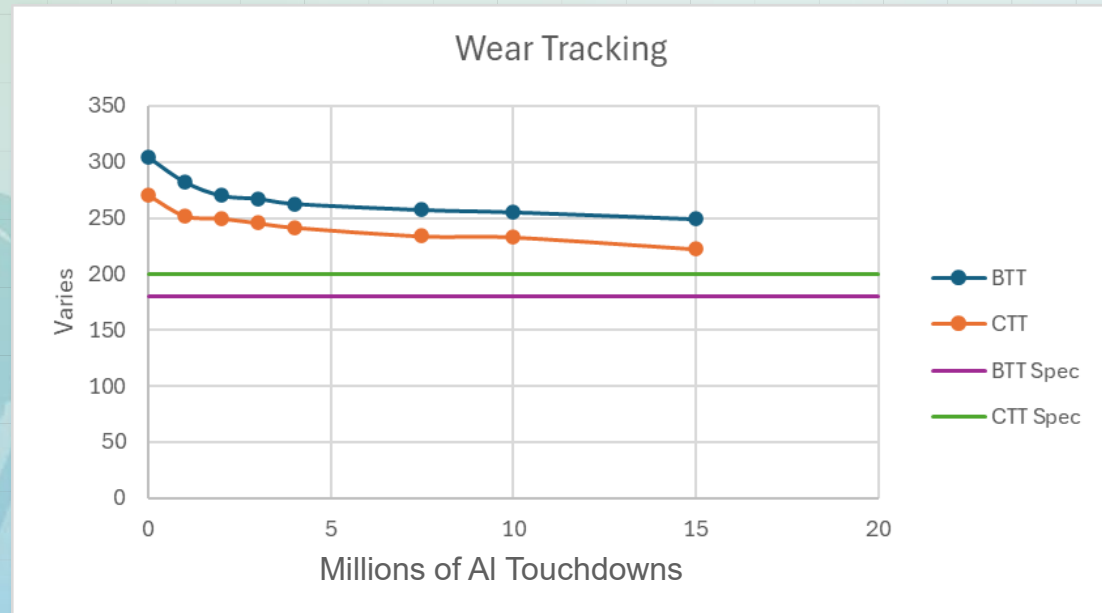
Qualification Plan

3. Wear testing on cleaning material

- ✓ “Long term” tip wear
- ✓ Tip shape change
- ✓ Exceed 10M AI-TD (with cleaning) target
 - Scrub length assessment (virtual pad)



BTT = Beam-To-Tip
CTT = Ceramic-To-Tip
Wear = $BTT_0 - BTT_n$

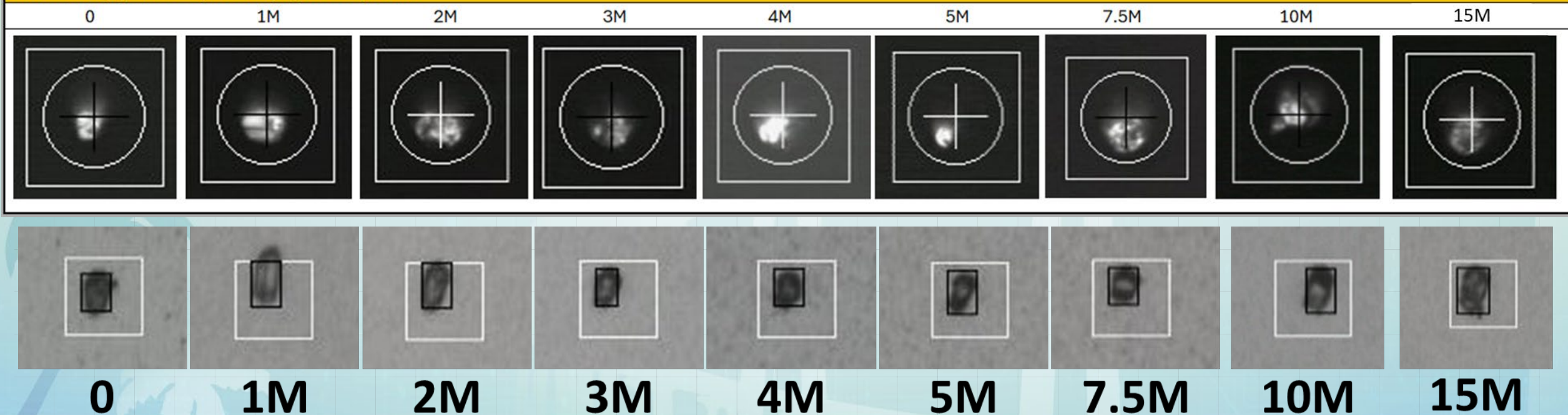


Qualification Plan

3. Wear testing on cleaning material

- ✓ “Long term” tip wear
- ✓ Tip shape change
- ✓ Exceed 10M AL-TD (with cleaning) target
- ✓ Scrub length assessment (virtual pad)

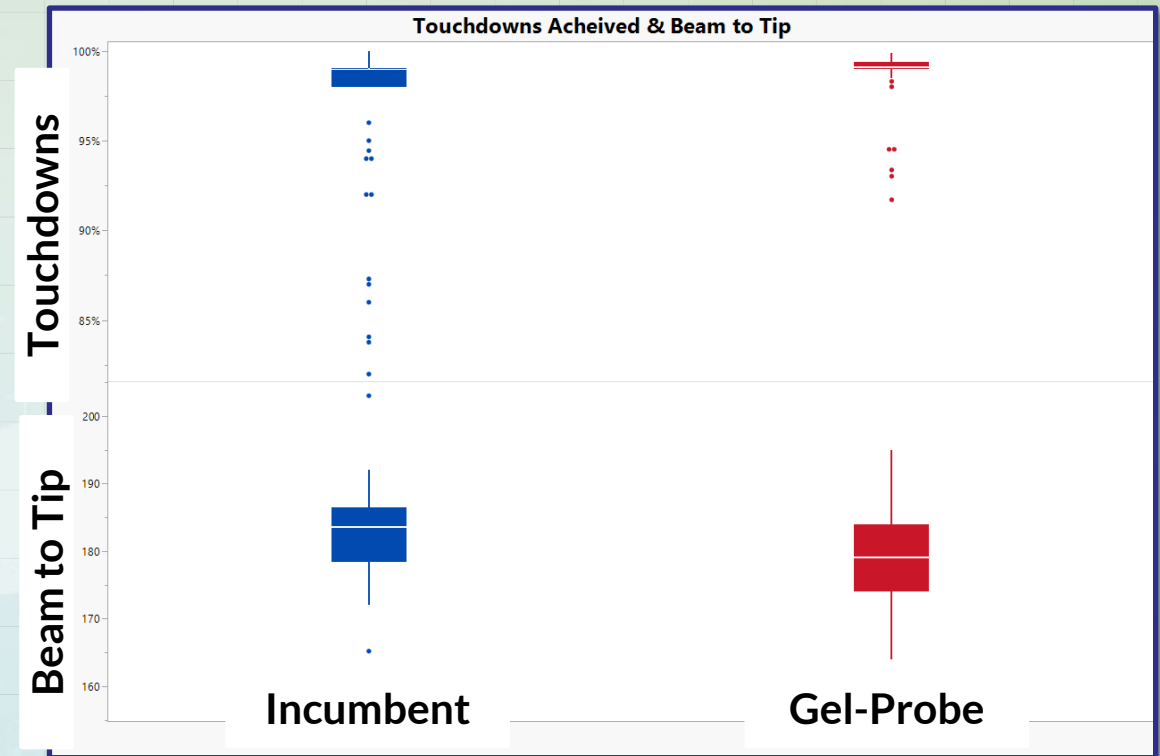
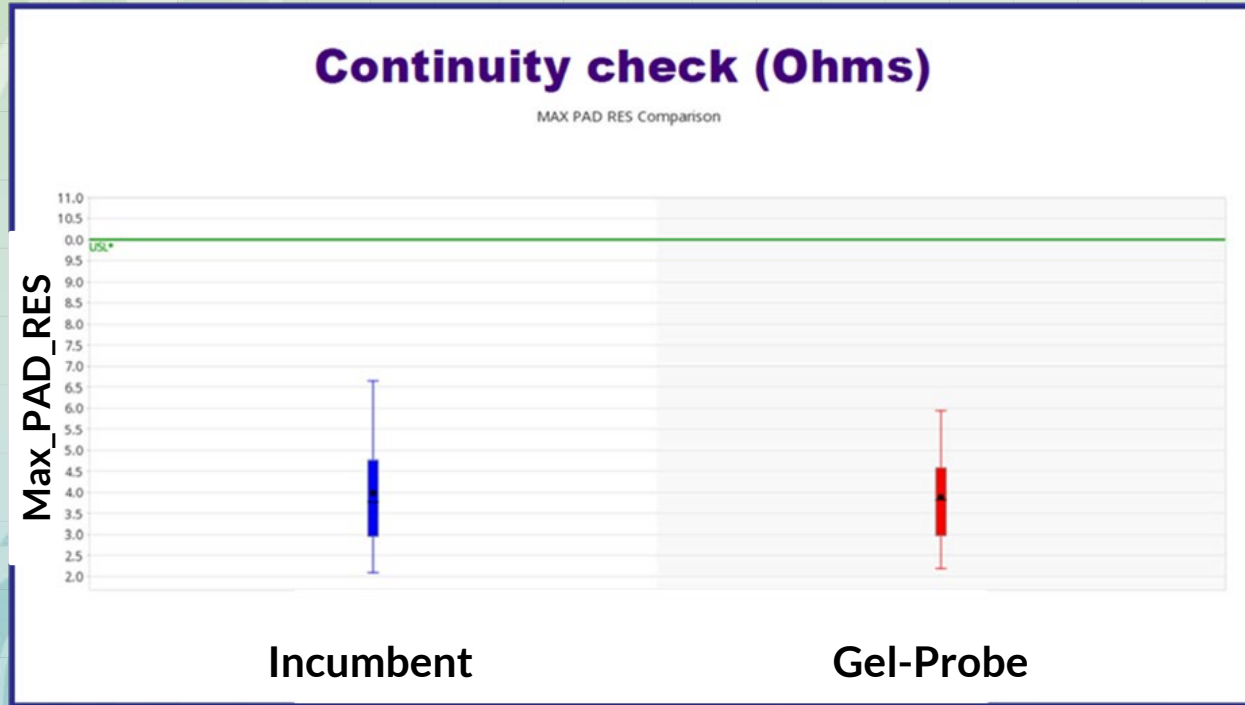
Timeline of tip pictures. Specifically tip 3 sanity check



Customer Verification

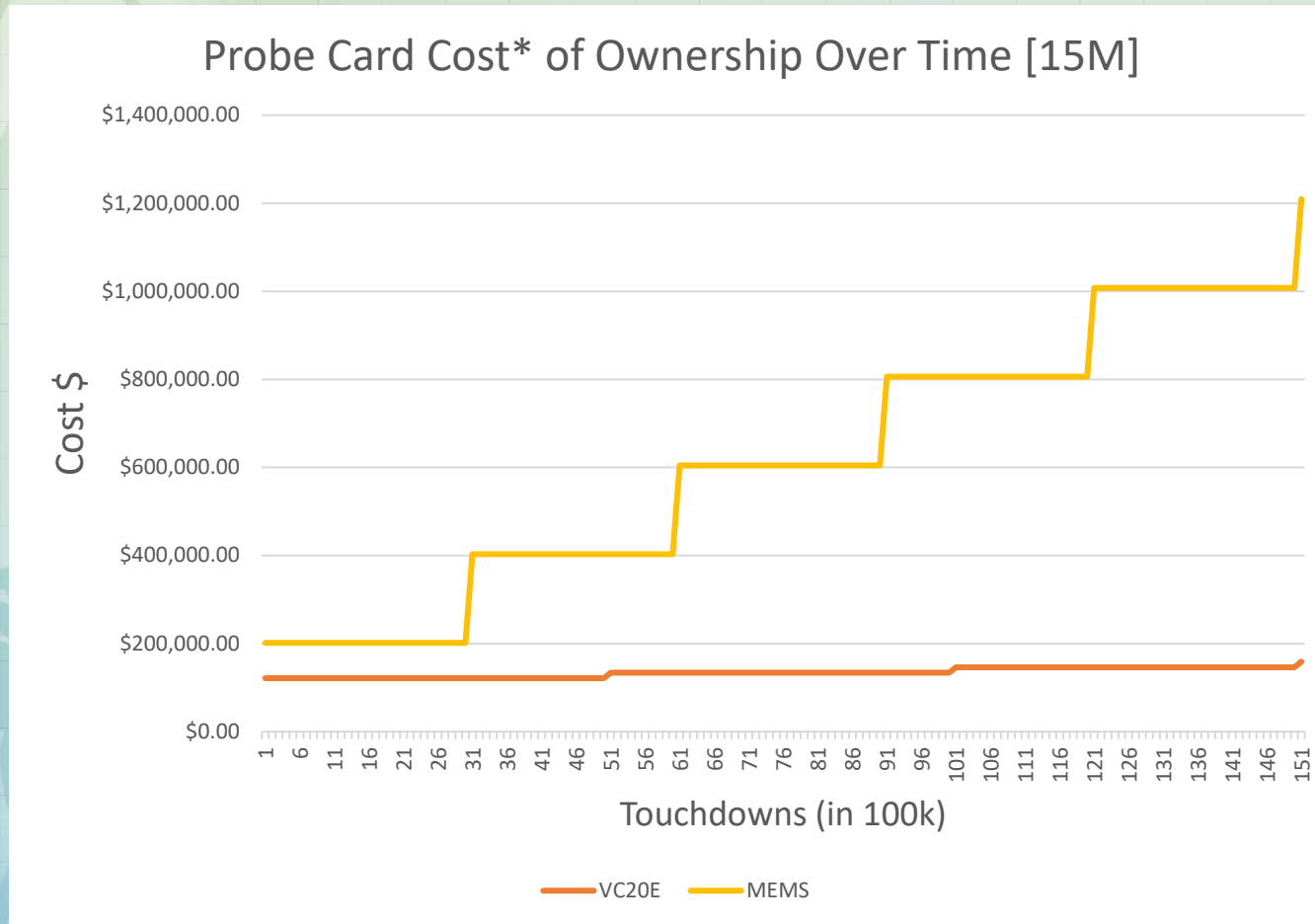
4. Qualification // Verification

✓ Customer Manufacturing Site



- Gel-Probe Refine M was used as a drop-in replacement for the cleaning regimen at GlobalFoundries
- Continuity check showed Max Pad Resistance comparable and was tighter
- Analysis of cards at end of life showed higher % reaching target number of touchdowns

Overall Cost of Ownership



VC20 with Gel-Probe cleaning regimen has low cost of ownership

- Lower initial and rebuild cost
- High number of touchdowns before rebuilds

**Calculated based on 16 testers*

Summary

Extended Lifetime Cleaning Regimen for VC20 Defined

- Effectively controls CRES
- Cleans away debris from tip
- Tip Diameter retained by gentle sharpening
- Tip designed with large excess of tip material available as tip is worn allows shape maintenance
- Ideal for small pad probing
- Probe Lifetime estimated to be ++15M Device TDs

Acknowledgements

- **Celadon Systems**
 - Dalton Roehl
- **Gel-Pak**
 - Jerry Broz
- **GlobalFoundries**
 - Jacqueline Ngo-Hatchie
 - Jung Tae Hwang
- **Complete Probe Solutions**
 - Sancho Adam
 - Mike Dean
 - Kevin Chandler