



**SWTEST**

PROBE TODAY, FOR TOMORROW

2025 CONFERENCE

# **MEMS Probe Card Solution to Address Parametric Test Challenges**



**Mukesh Selvaraj, Apoorva Dube, Judd  
Gerber, Philip Tavernier, Sanjay Bidasaria**  
FormFactor and Intel

# Agenda

- Introduction/Problem Statement
- MEMS Probe Card Requirements
- Probe Card Architecture
- Probe Design
- Probe Down-Selection
- Contact Force for Stable CRES
- Scrub Performance
- Probe Assembly; Pad Size, Layout and Pitch
- Qualification Results
  - Key Issues/Challenges
  - Contact Resistance for different pad metallurgy
  - Lifetime Results for different pad metallurgy
- Summary and Conclusion

# Introduction/Problem Statement

- Test engineers leverage parametric testing to
  - Enhance semiconductor device quality
  - Monitor and control process variations
  - Boost production yield and minimize material waste
  - Help lower overall manufacturing costs
- Parametric probe cards face increasing pressure to deliver ultra-precise, repeatable, low-damage electrical contact with high reliability
- Probe card requirements for parametric testing
  - Ensure ultra-low leakage currents for accurate measurements
  - Utilize robust contact technology to safeguard wafer integrity
  - Deliver high reliability and consistent performance over extended use
  - Support yield enhancement and waste reduction
  - Enable faster time-to-market by reducing lead time for new designs

# MEMS Probe Card Requirements

- **Smaller Pad size and Pitch**
  - $\leq 40\mu\text{m}$  pitch requires smaller probe cross section
- **Low force 2D MEMS springs**
  - Reduces risk of pad damage
- **Very low scrub ratio < 7%**
  - Low scrub marks is critical to achieve smaller pad size
- **Low particle generation**
  - Tip to beam clearance  $> 250\mu\text{m}$  is critical
- **Works across different pad surfaces**
  - Stable low CRES required for variety of pad metallurgies for Al, Cu, Inline and Solder
- **Constant probe tip length**
  - Tip size needs to be consistent across Beginning of Life (BoL) and End of Life (EoL)

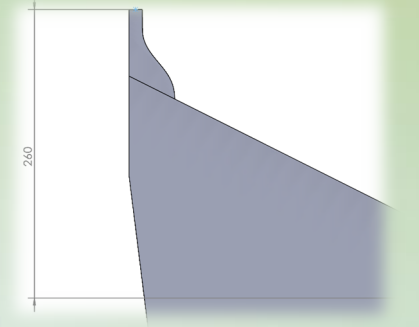


Fig. 1 – Tip to Beam Clearance

Attribute	Value
Pad Size	25x25 $\mu\text{m}$
Pitch	40 $\mu\text{m}$
Max OT	150 $\mu\text{m}$
Operating OT	100 $\mu\text{m}$
Scrub Length	<15 $\mu\text{m}$
Leakage	<0.5 pA
Pad Layout	Flexible
Pad Material	Al, Cu, Solder, Cu Pillars, Ti, Nb, etc.

Table 1 – Attribute and Value



# Probe Card Architecture

- A novel MEMS probe card architecture was designed and developed to meet the demanding parametric test requirements
- Interchangeable probe heads built with ultra high precision MEMS probes
  - Capable of exchanging different probe head designs on-site using a common PCBA
  - MEMS probes with fine pitch capability, low force, low scrub ratio and stable Contact Resistance (CRES) developed
- Key Benefits
  - Reduced lead-time
  - Flexibility of asset utilization
  - Lower cost
  - Maximizes Total Cost Of Ownership (TCOO)

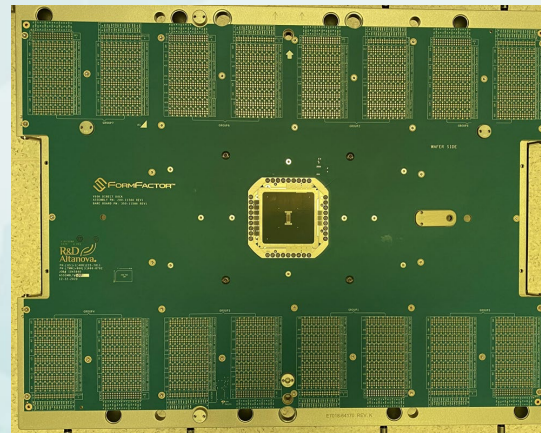


Fig. 2 – MEMS Probe Card

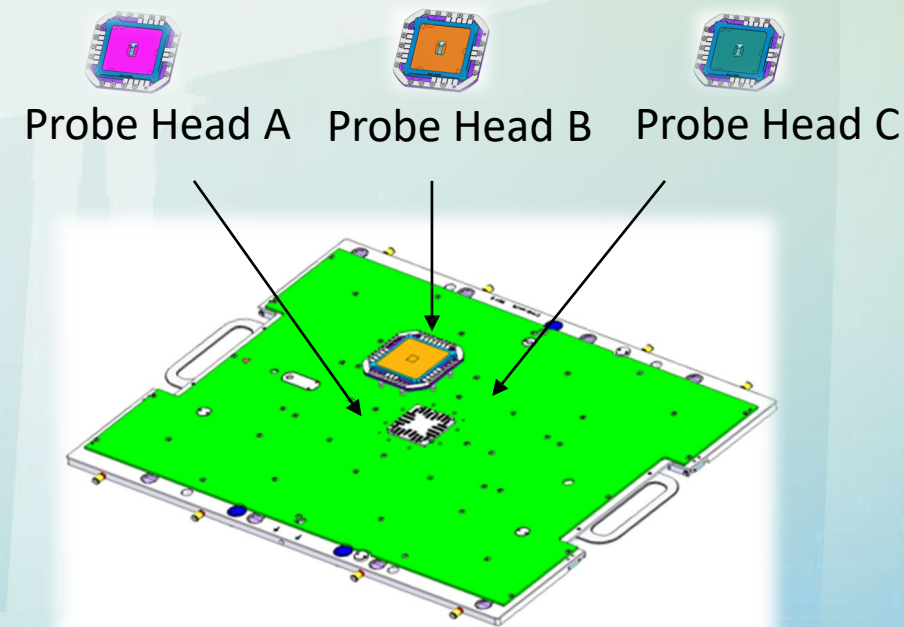


Fig. 3 – MEMS Probe Card with Interchangeable Probe Heads

# Probe Design

- **Input parameters/ factors to consider**
  - Optimal MEMS metallurgy
    - Superior thermo-mechanical properties
    - High yield strength
    - Optimal Young's modulus
  - Dimensions/size of the probe
  - Ease of fabrication
- **Output parameters**
  - Desired maximum stress at maximum Over-Travel (OT) with sufficient margin
  - Appropriate contact force ~ 2.5-4.5g at operating OT
  - Desired total scrub length ~ 12-15  $\mu\text{m}$
- **All the above parameters determined through FEA**
  - Optimized probe design selected from an iterative process
  - Best candidate was down selected for fabrication

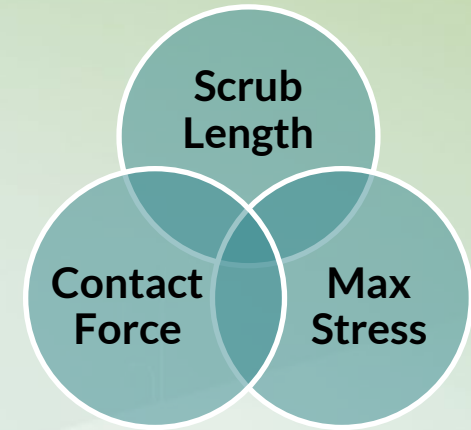


Fig. 4 – Optimum probe design criteria

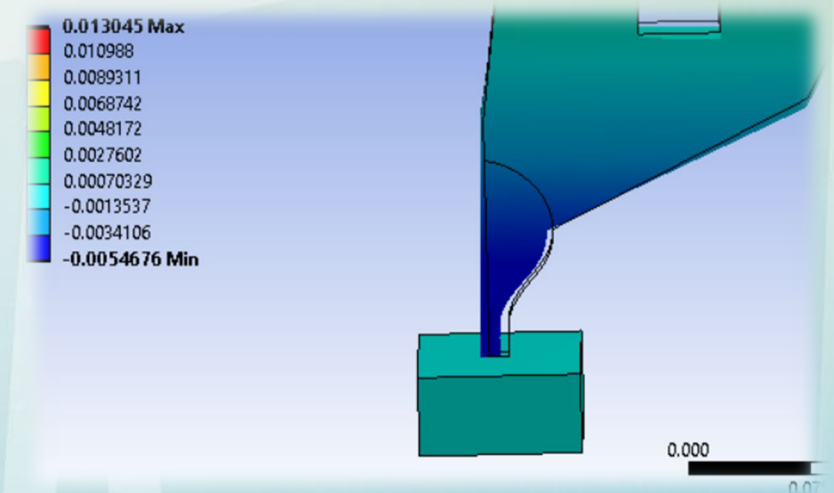


Fig. 5 – Scrub Length as per FEA

# Probe Down-Selection

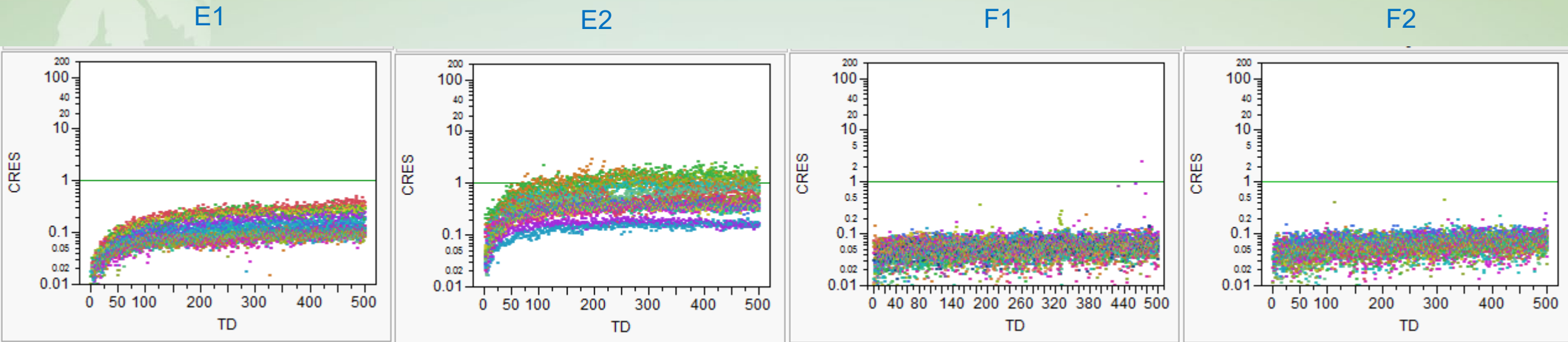


Fig. 6 – CRES data for Probe E1, E2, F1 and F2

- Contact Resistance (CRES) and Scrub mark data was collected for different probe designs at maximum Actual Overtravel (AOT) of 150 $\mu$ m
- Stable CRES was demonstrated for 500 production touchdown (TD) cycles without any cleaning
- Down selected E1 based on CRES and scrub performance
- F1 and F2 had longer scrub length which will not meet customer's small pad size requirement

# Probe Down-selection - CRES

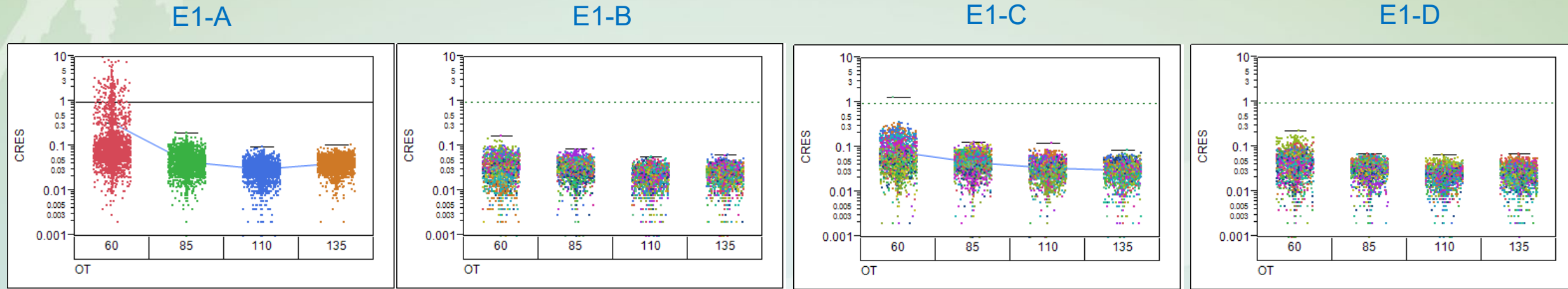


Fig. 7 – CRES data for the variants of probe E1

- Above are the 4 variants of E1
- 3 of the 4 candidates pass CRES even at 60 $\mu$ m OT
- E1-D was down-selected for Cu, Cu Pillar, Solder, Aluminum pads



# Contact Force for Stable CRES

- Contact Force needs to be optimized for low pad damage and stable CRES
  - Low contact force would lead to high CRES and hence, undesirable
  - High contact force though would provide a low CRES but could damage the customer pads
  - E1-D probe's contact force was optimized for stable CRES and low scrub ratio using FEA
- Pad material also influences the CRES performance and accordingly the probe design needs to account for the contact force
- For Titanium pad, increase in contact force is critical as shown in Fig. 8 but scrub length is similar ensuring no damage to the pad
  - E1-B was down-selected for Ti pad
- Good correlation between FEA and experimental data as shown in Fig. 9

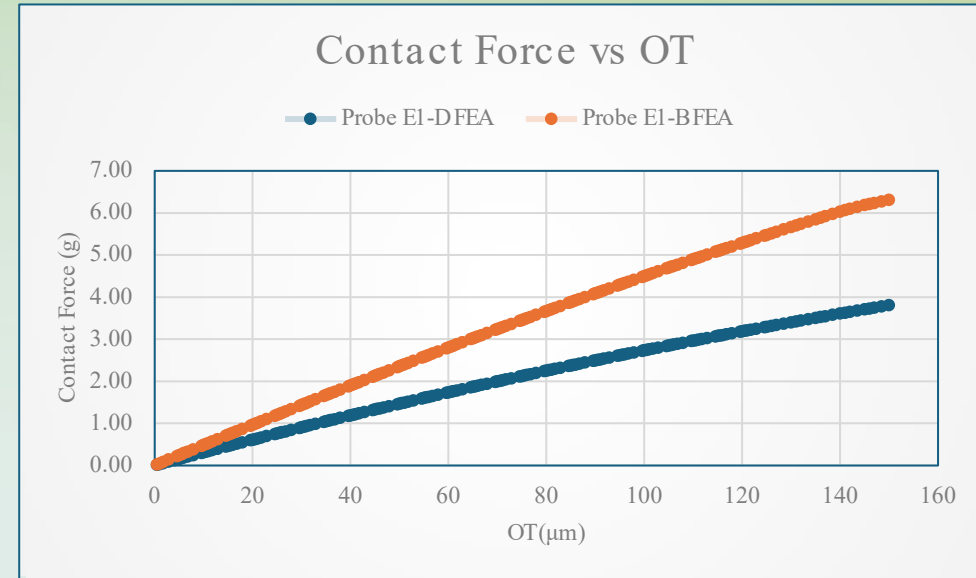


Fig. 8 – Contact Force Vs Overtravel for E1-D and E1-B as per FEA

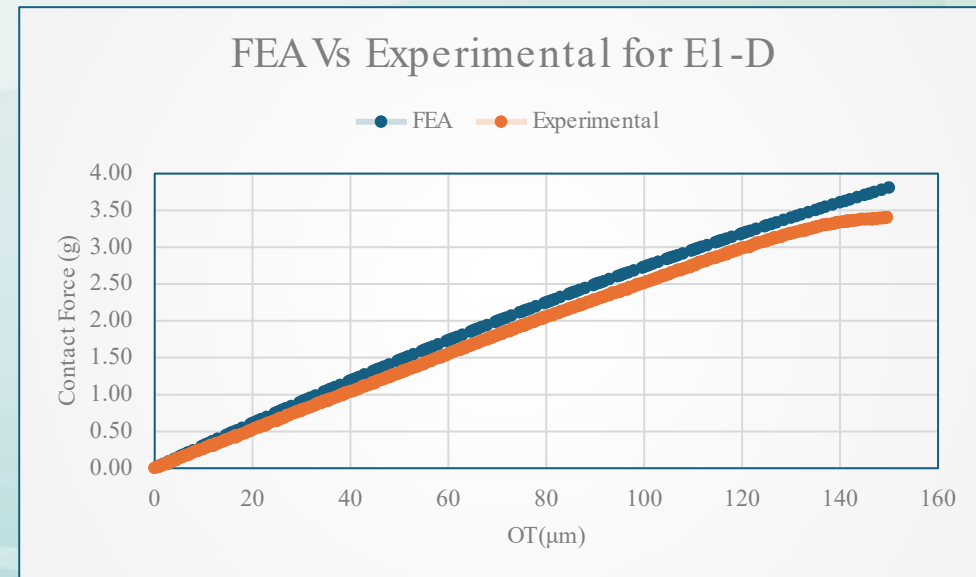


Fig. 9 – Contact Force Vs Overtravel for E1-D, FEA Vs Experimental

# Scrub Performance

- Scrub ratio refers to the scrub length with respect to the amount of overtravel
- A consistent predictable scrub ratio is critical for electrical performance
- Scrub ratio: 6.5%
- Scrub depth analysis shows very low punch through on the pad
- Low scrub ratio without pad damage is paramount for very small pad applications

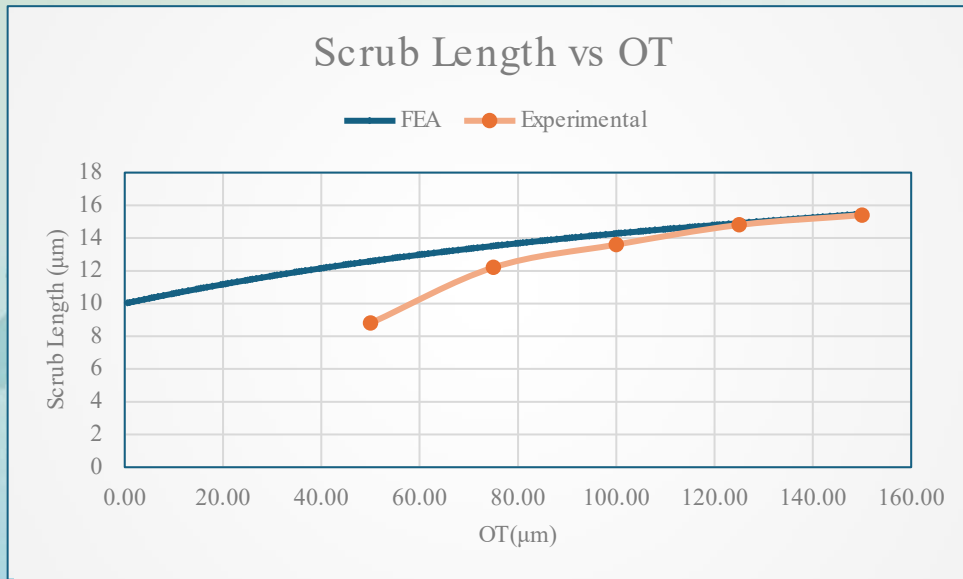


Fig. 10 – Scrub Length Vs OT for E1-D,  
FEA Vs Experimental



Fig. 11 – Scrub Length Vs OT

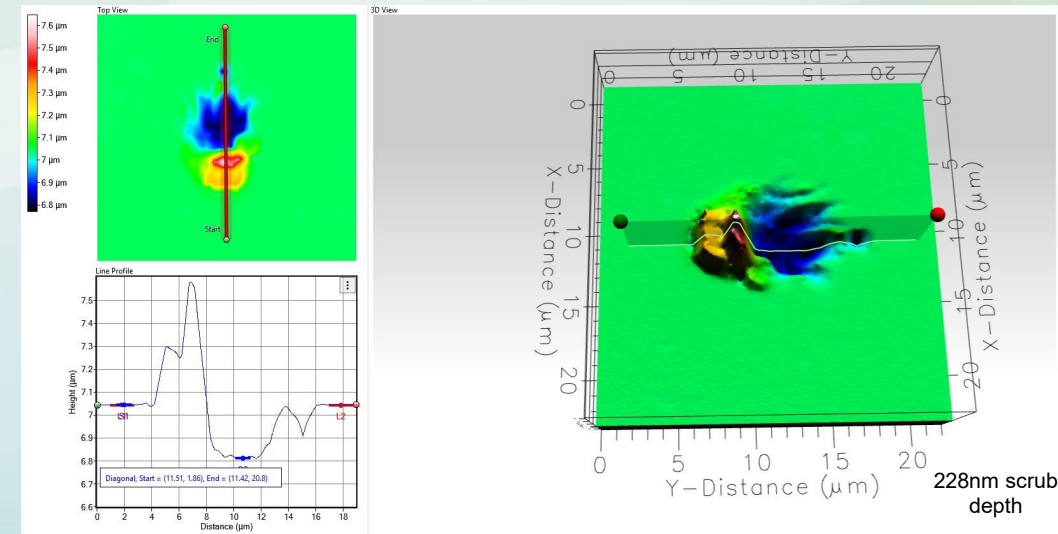


Fig. 12 – Scrub Depth Analysis

# Probe Assembly; Pad Size, Layout and Pitch

- MEMS probe assembled using ultra high precision automation tool
- Probe attachment methodology enabling fine pitch solution at 40  $\mu\text{m}$  pitch developed, 20  $\mu\text{m}$  capability in progress
- Pad head to head clearance significantly reduced to 10 $\mu\text{m}$
- Improvement in MEMS probe tip placement accuracy in X,Y and Z
- Flexibility in pad layout and enables high parallelism testing

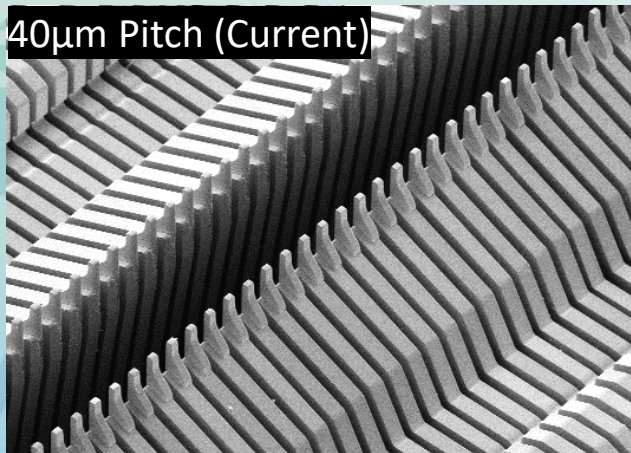


Fig. 13 – Probe Assembly; 40  $\mu\text{m}$  Pitch

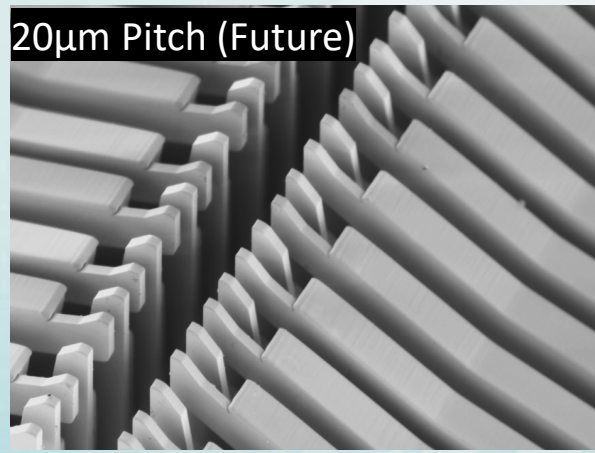


Fig. 14 – Probe Assembly; 20  $\mu\text{m}$  Pitch

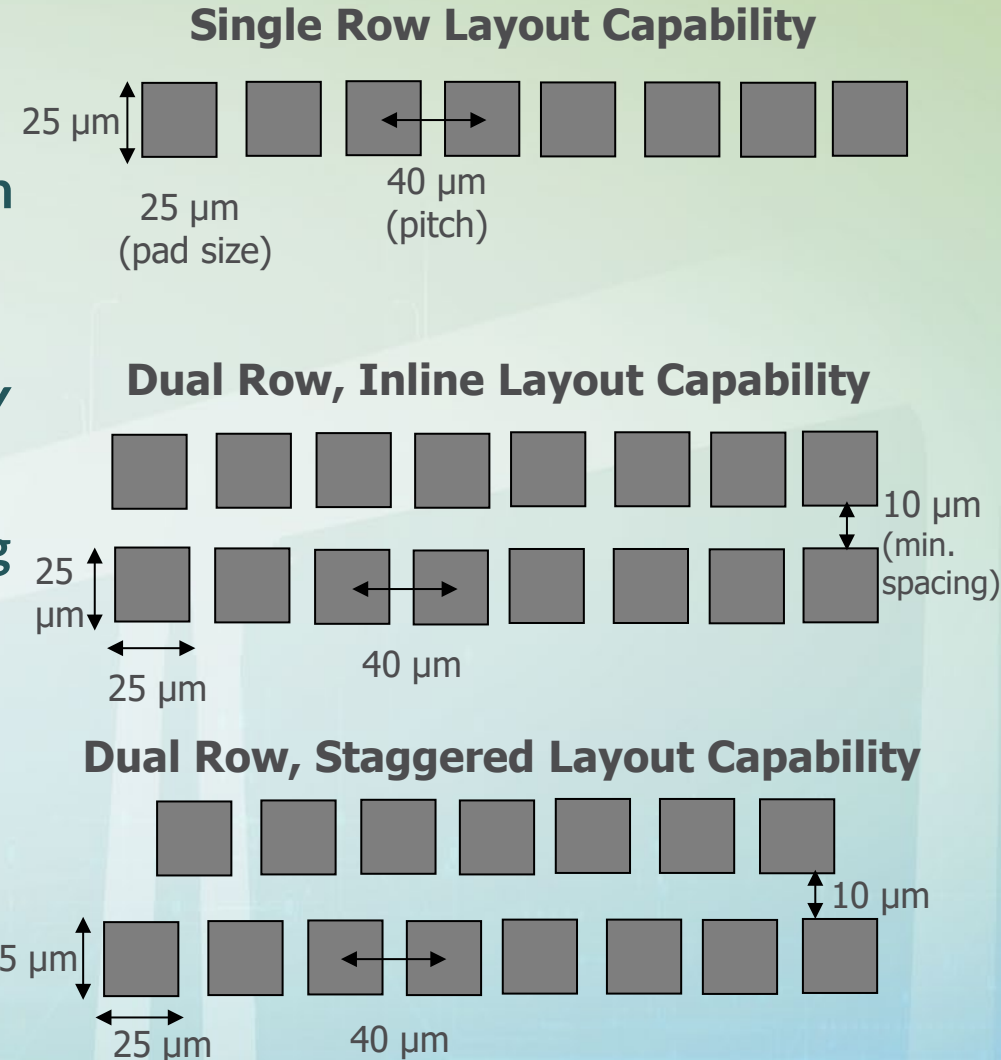


Fig. 15 – Pad size, layout and pitch

# Qualification Results - Key Issues/Challenges

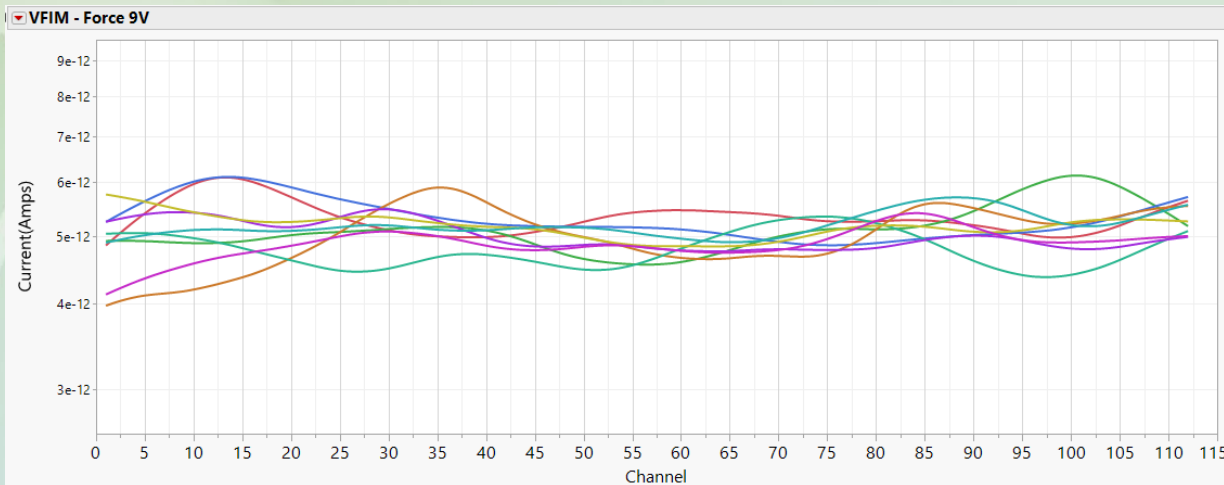


Fig. 16 – Probe Card Ultra low leakage Data

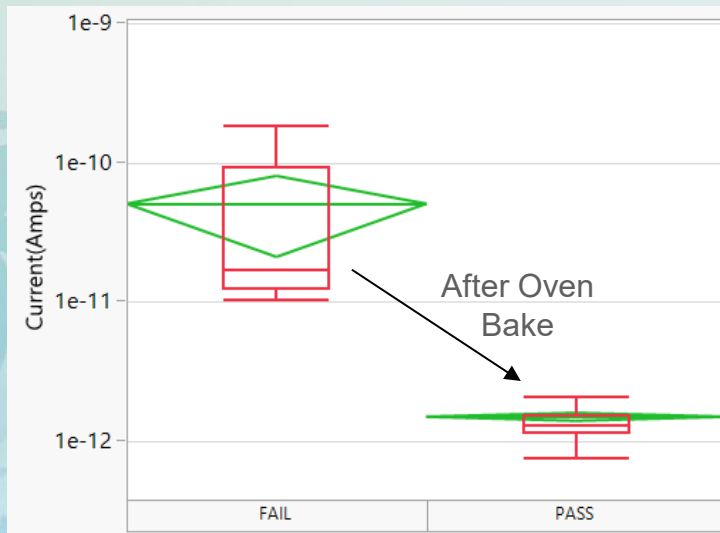


Fig. 17 – Random low leakage failure and fix

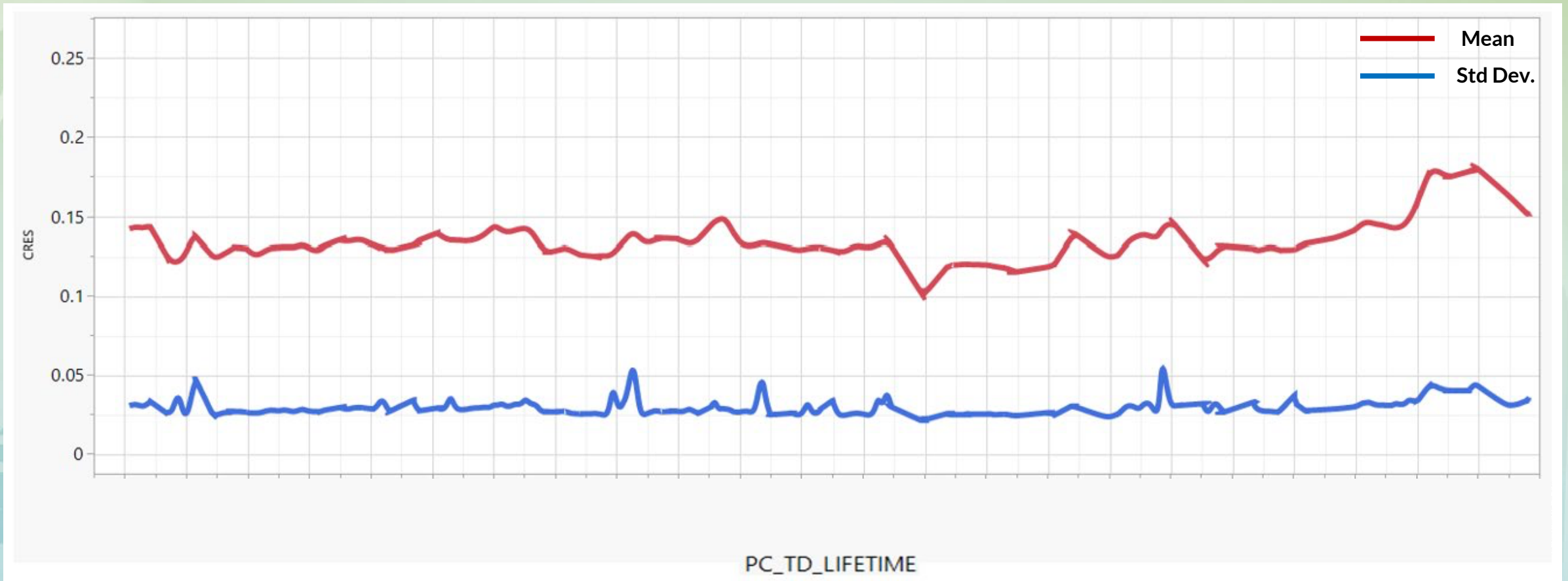
Initial evaluation samples passed Intel test requirements

## Random Low Leakage Failures

- Observed few random low leakage failures during qualification and ramp
- Low leakage was attributed to moisture build up on PHs
- Onsite oven bake on failed PHs showed that the leakage can be reduced
- Implemented outgoing bake process on PH as standard practice to reduce leakage failures
- Implemented flux-free PH process to further reduce chance of leakage failures



# Qualification Results – Lifetime Data on Copper Pillar



# Qualification Results – Lifetime Data on Copper Pad

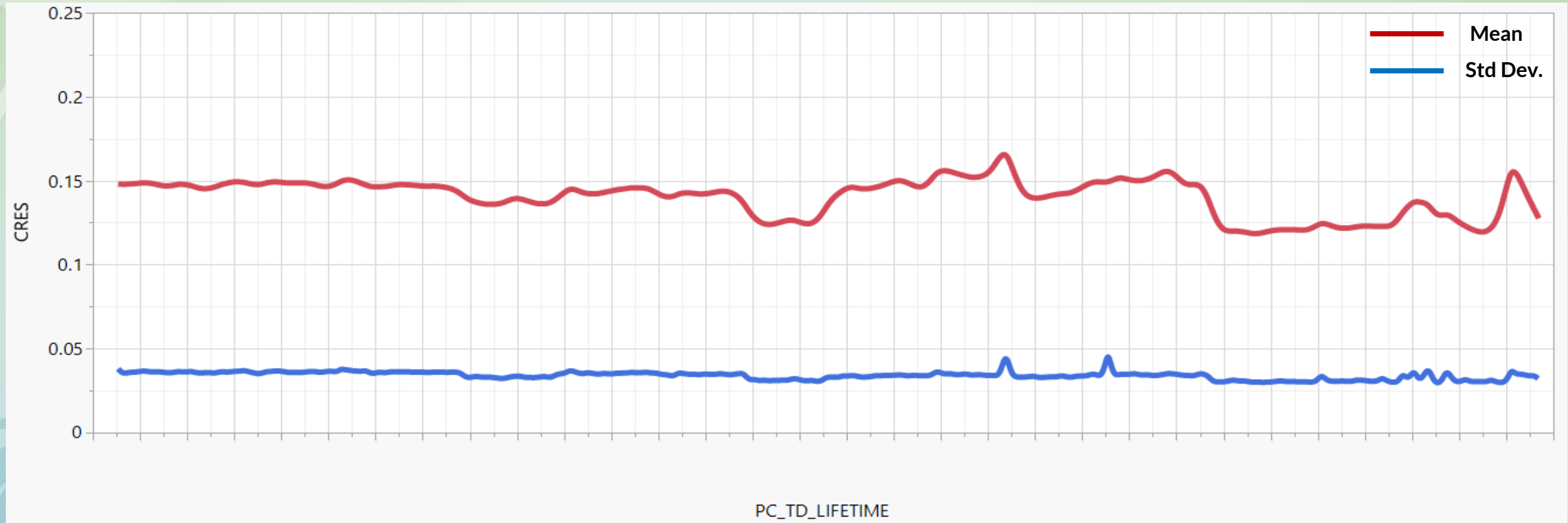


Fig. 19 – CRES and Lifetime Data on Cu Pad

- Probing surface - Cu Pads
- Lifetime > 1 million TDs

# Summary / Conclusion

- Developed an innovative interchangeable MEMS Probe Card architecture that meets Intel's demanding parametric test requirements
- Probe design with desired CRES, contact force and scrub length achieved across different pad surfaces
- MEMS probe fabrication, assembly and capability developed for varying pad sizes, layouts and pitches
- Exceptional CRES and lifetime performance demonstrated
- Future parametric test requirements
  - High temp (180 - 200°C) testing
  - Fine pitch probing <40  $\mu\text{m}$  up to 20  $\mu\text{m}$
  - Smaller pad size ~ 20x20  $\mu\text{m}$

# Acknowledgements

- **FormFactor Team**

- Jose Gonzalez, Oscar Moreno, Chintan Panchal, Nick Jansen, Xianling Yan, Wilson Kyi, Sudhin Shetty, Jesse Li, Tim Eichenseer, Arvind Sambasivan

- **Intel Team**

- Jiun-hong Lai, Tanzila Tasmin Ava