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2025 CONFERENCE

# Revolutionary SiC-based Micro-vertical Cryogenic Probing Solution Down to 2K

Nielson Scientific

CELADON™
A Wholly Owned Subsidiary of MPI CORPORATION


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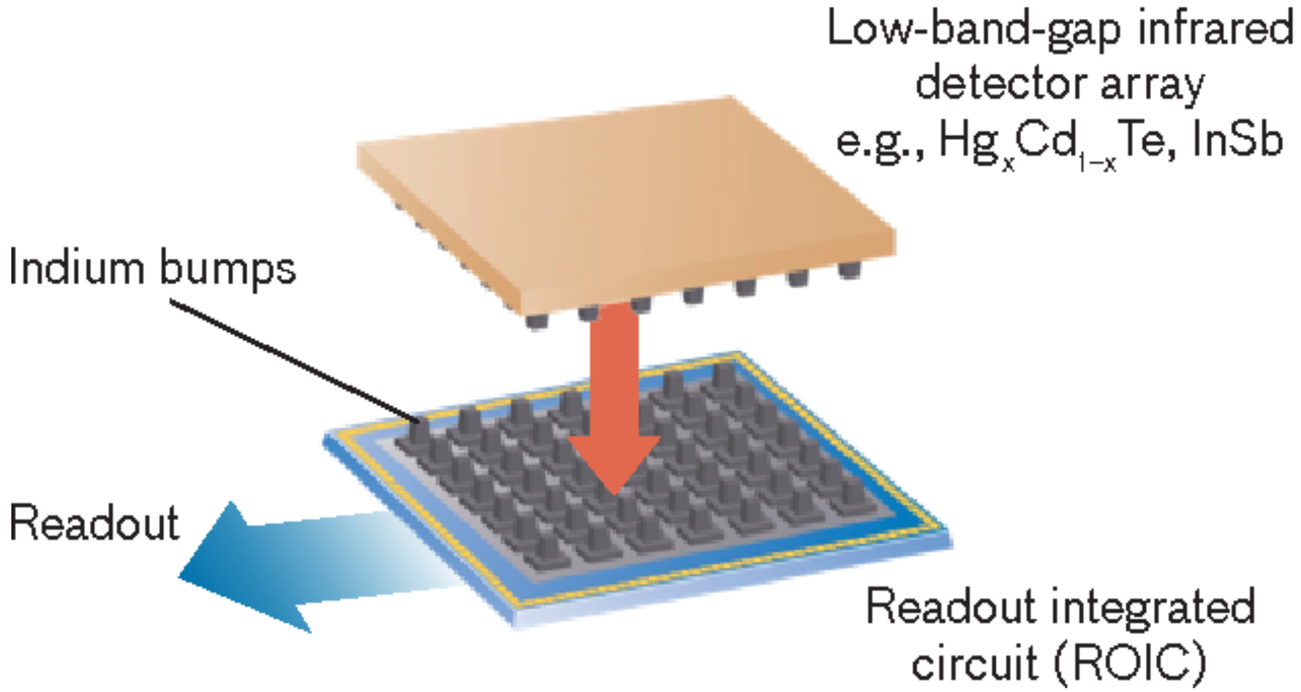
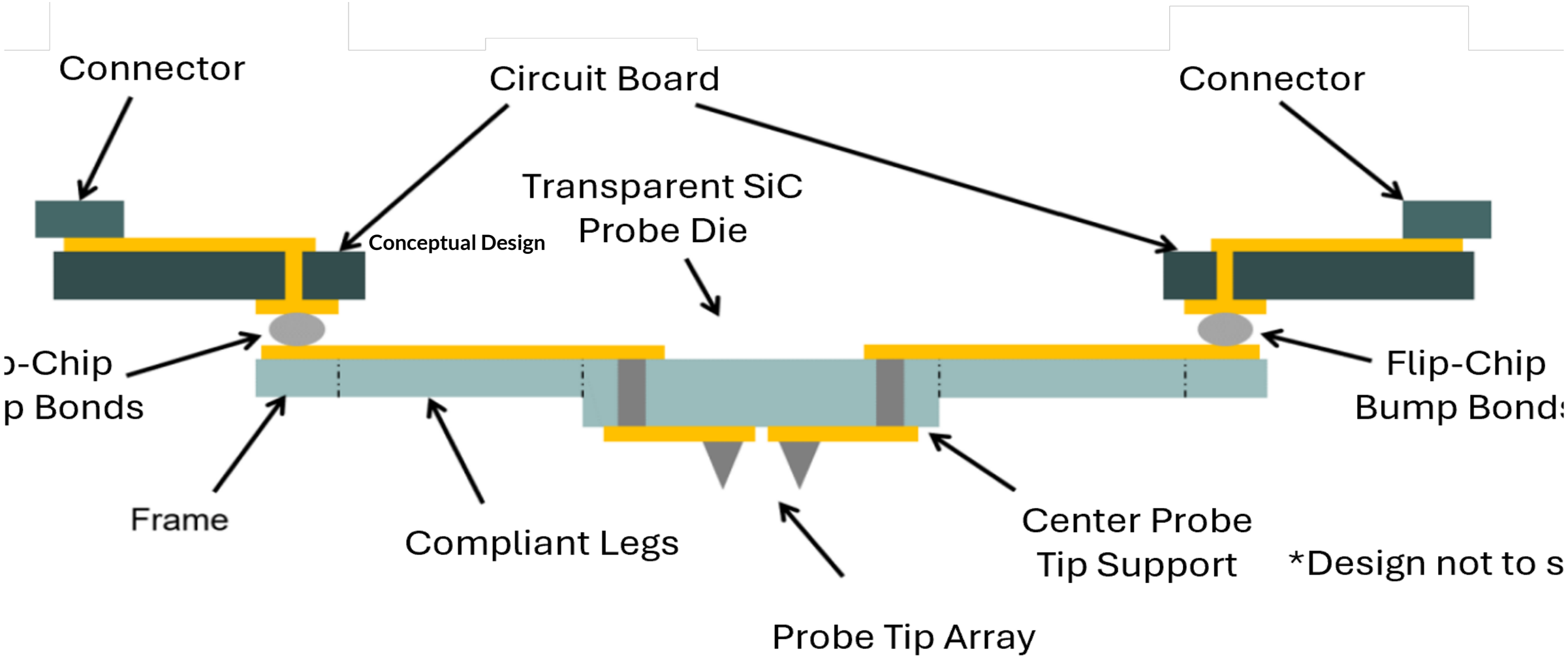
# Motivation and Technical Objectives

## Probe card for testing multiple nearest-neighbor pixels in a cryogenically cooled IR focal-plane array prior to ROIC attachment

- Cryogenic operation
- Probe tip pitch to match pixel pitch
- Transparent probe card for visual alignment
- Tip compliance behavior to match traditional probe tips
  - Tip force of 15 - 40 µN/µm²
  - Tip displacement of 25 - 75 µm at desired tip force



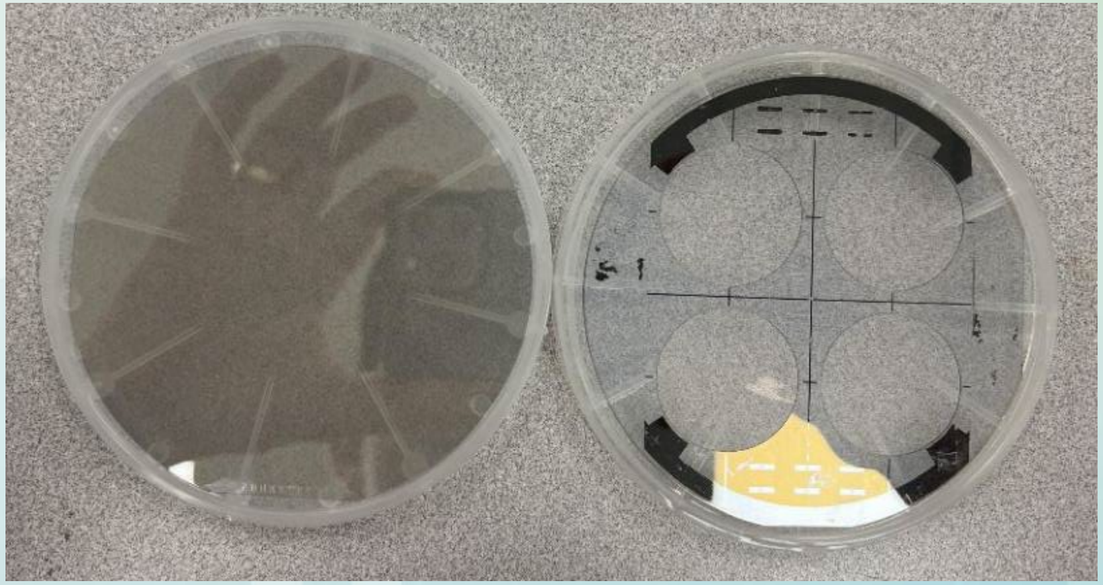
# Conceptual Design



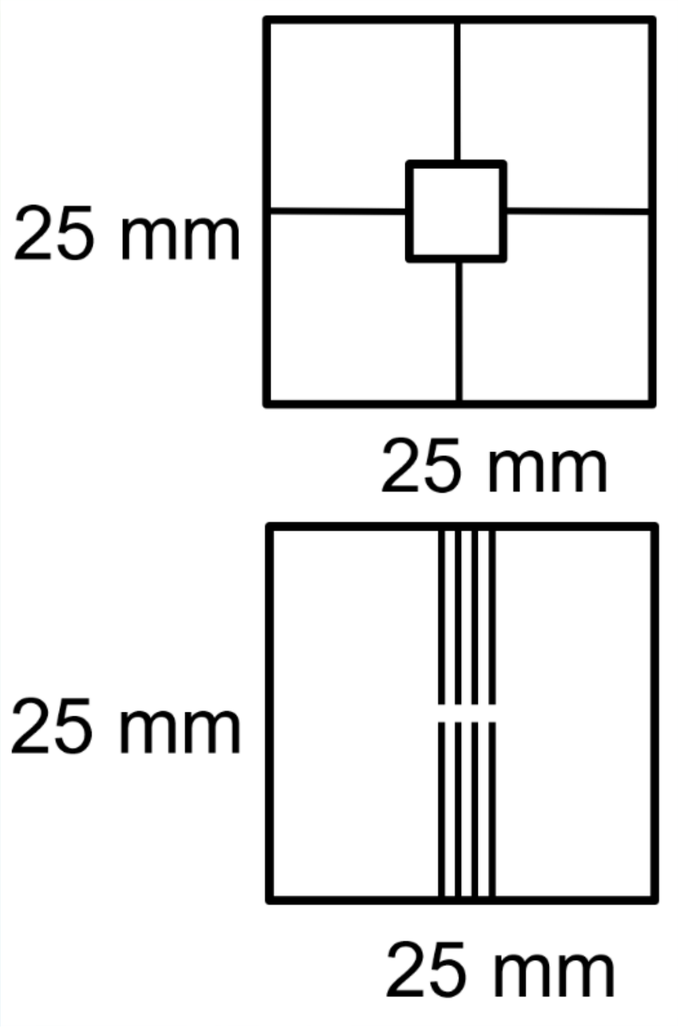
# SiC Substrate

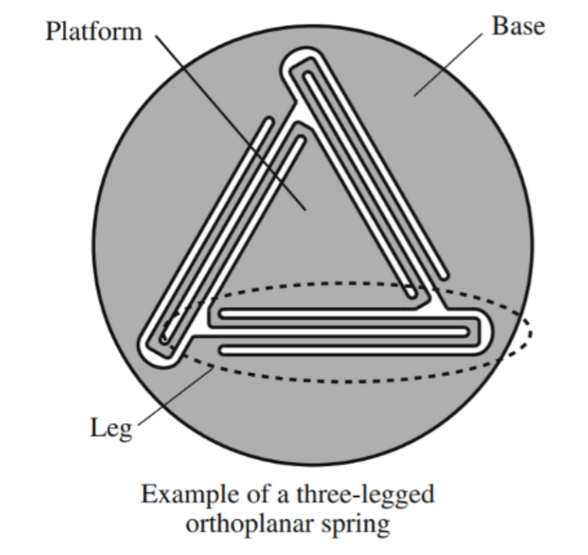
| Operating Temperature | Tensile Strength | Thermal Conductivity | Density | Young's Modulus | Poisson's Ratio |
|---|---|---|---|---|---|
| ~1800°C | 1.5 GPa | 490 W/m*K | 3.21 g/cm$^3$ | 440 Gpa | 0.2 |

- Very high thermal conductivity
- Chemically inert
- Maintains high strength through operating temperature range
- Wide bandgap semiconductor (3.23 eV)
- Transparent to visible and IR light (~2.7 optical index)
- Extremely hard (9.5 Mohs hardness)
- Low coefficient of thermal expansion
- Robust to radiation
- Very low helium diffusion rates



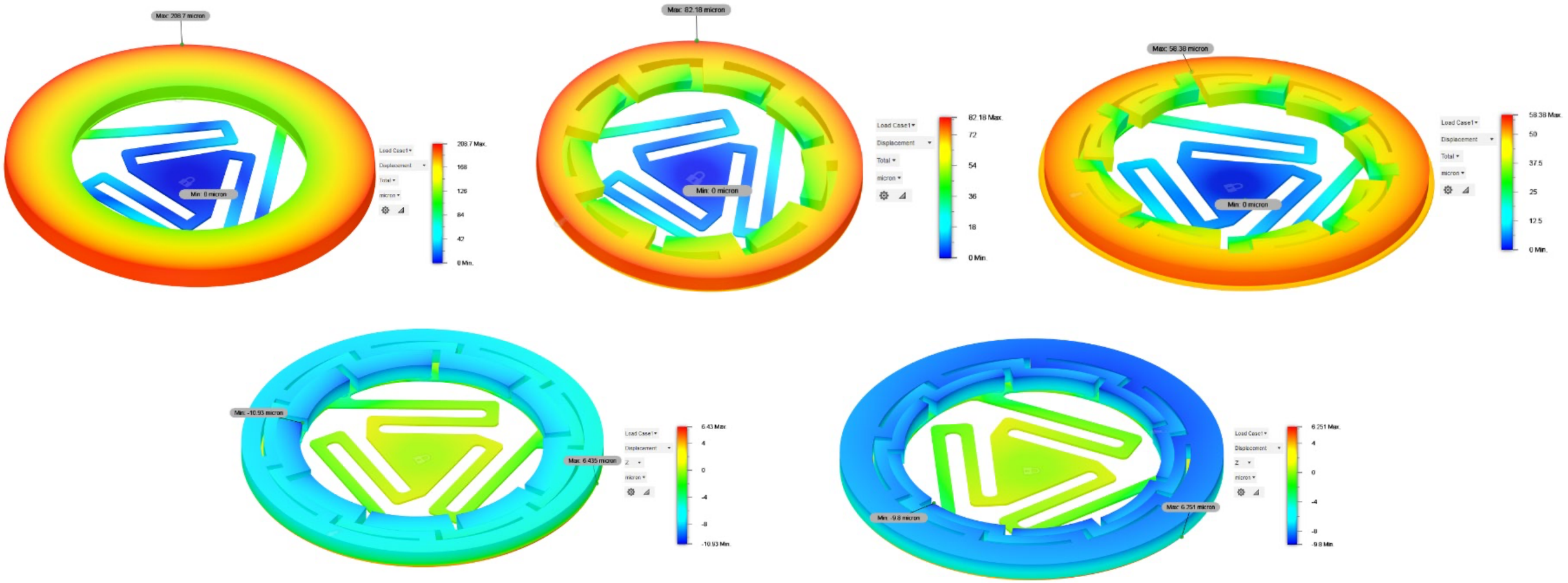
# Probe Card Mechanical Design Concepts



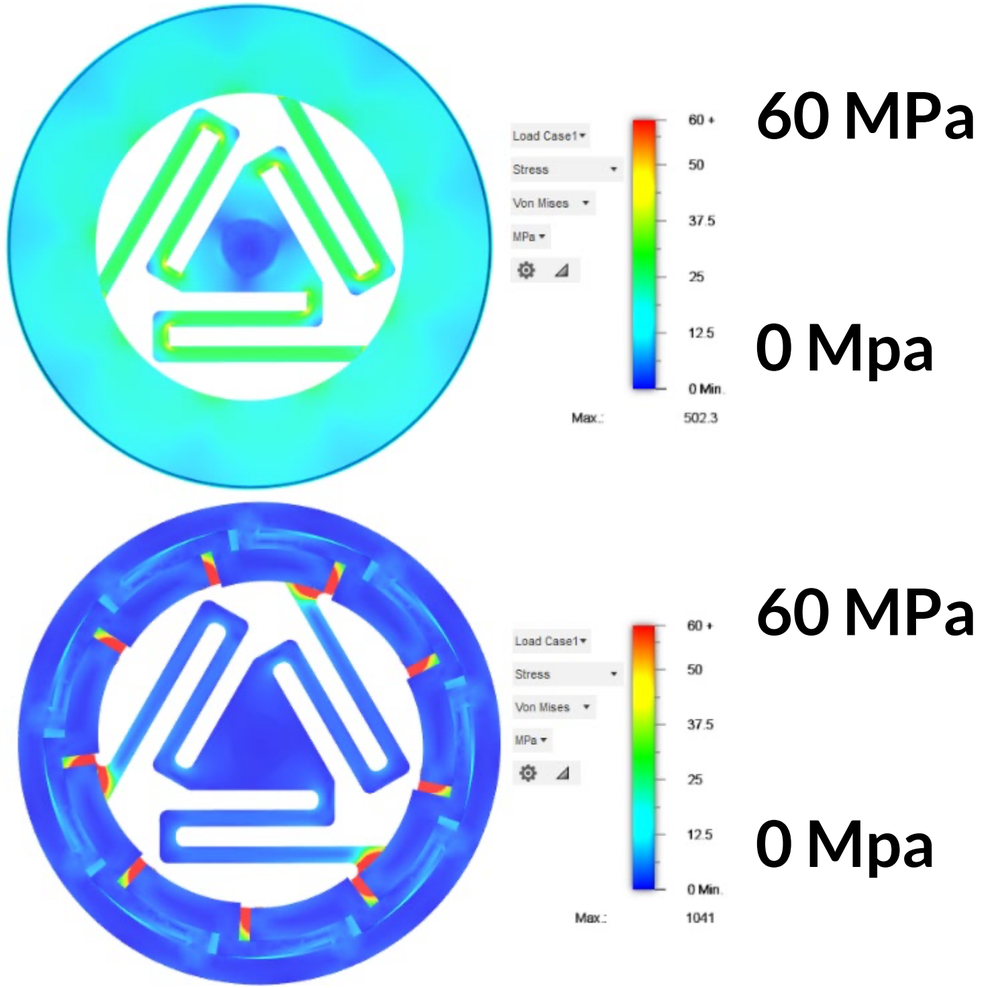
Example of a three-legged orthoplanar spring

# Thermal Cooling Displacements Due to PCB/SiC CTE Differences



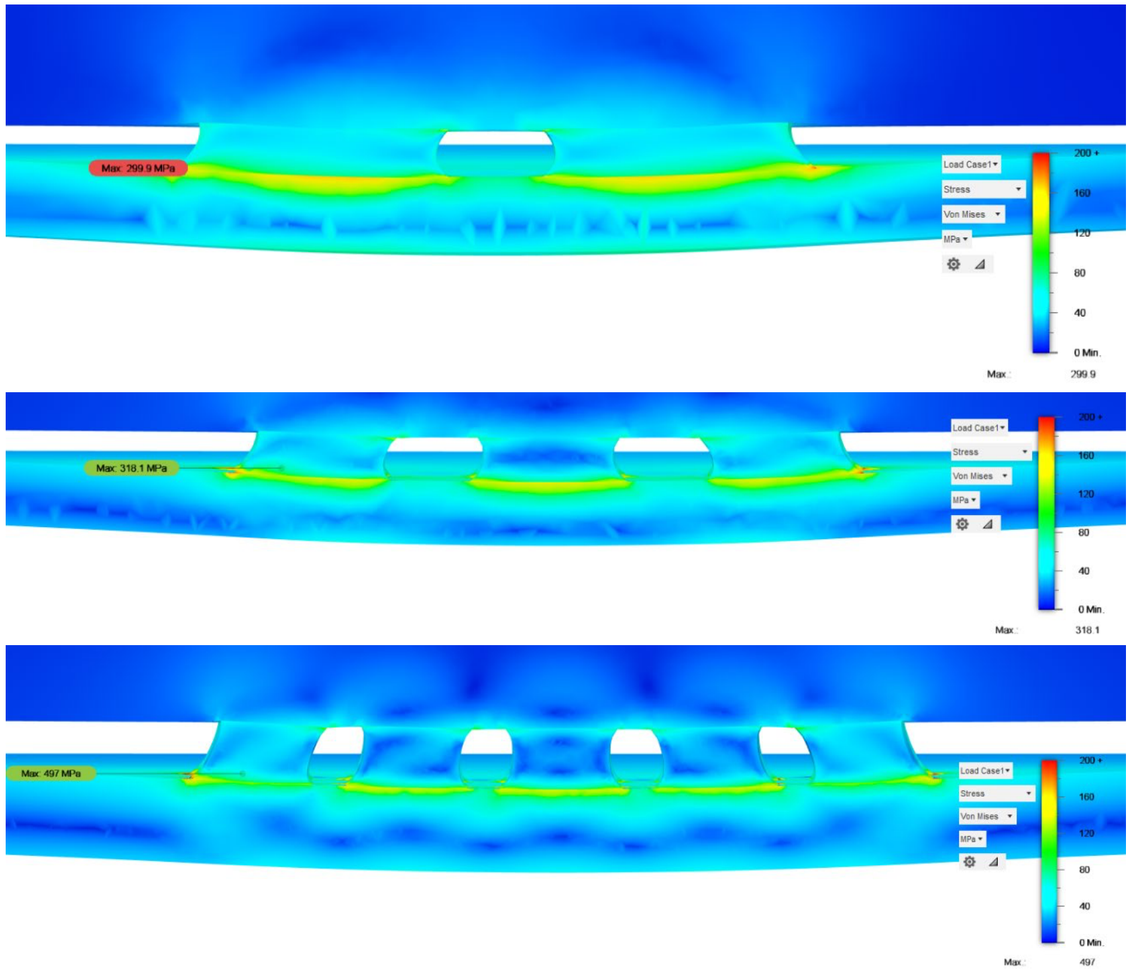
# Thermal Cooling Stress

- SiC tether stress is less than 30 MPa without flexures in PCB
- SiC tether stress is less than 10 MPa with flexures in PCB
- Max stress happens in solder due to material differences



# Solder Cooling Stresses

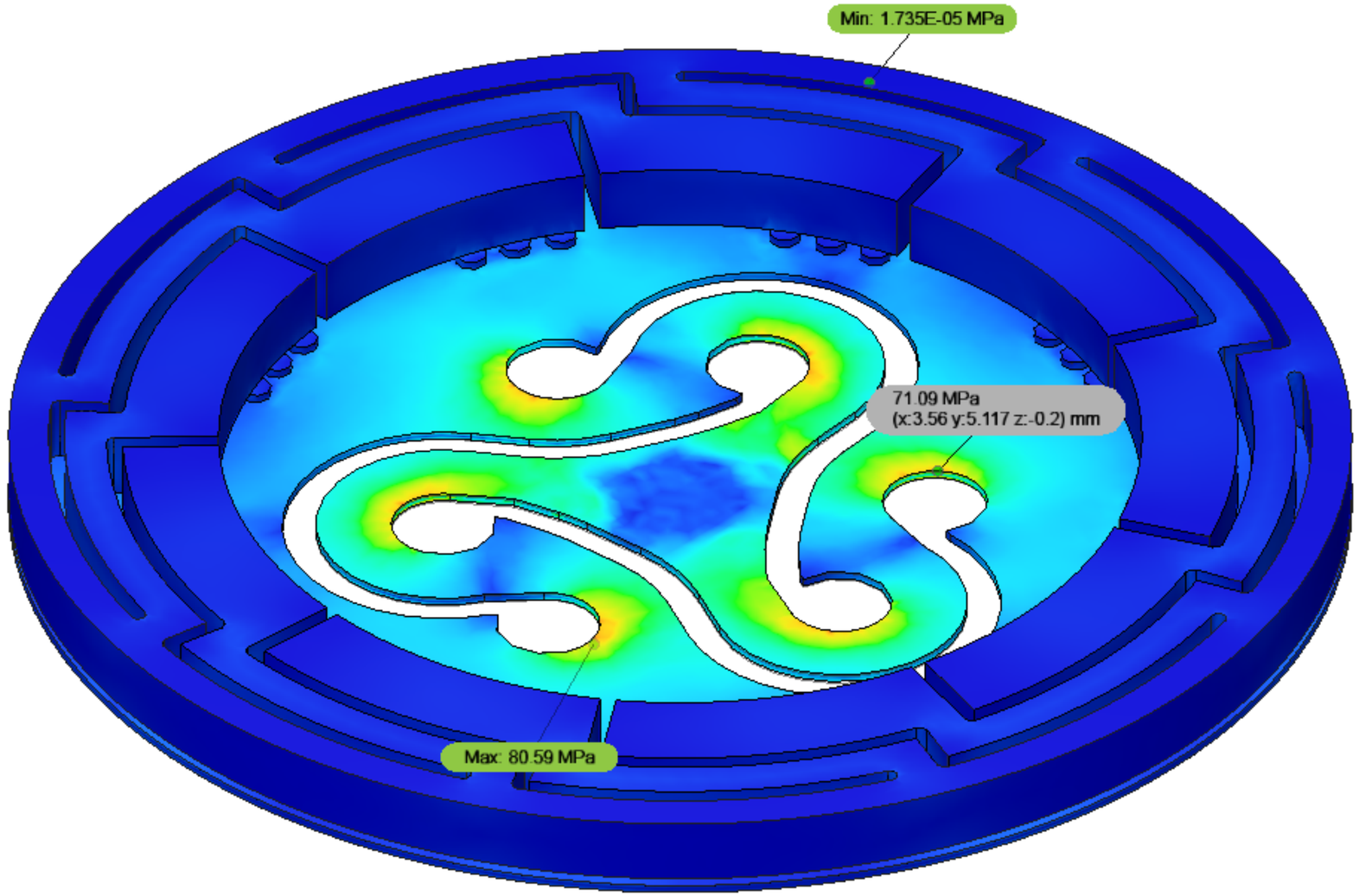
- Stress is reduced for taller, skinnier solder bumps
- Multiple small contact points improve mechanical connection robustness against thermally induced stresses

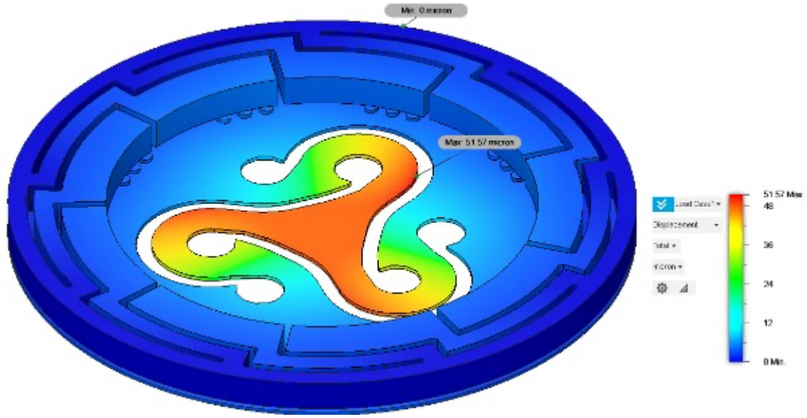


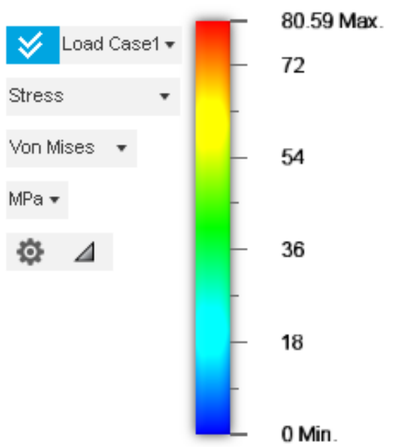

200 MPa

0 Mpa

# FEA Analysis of a 50 µm Displacement

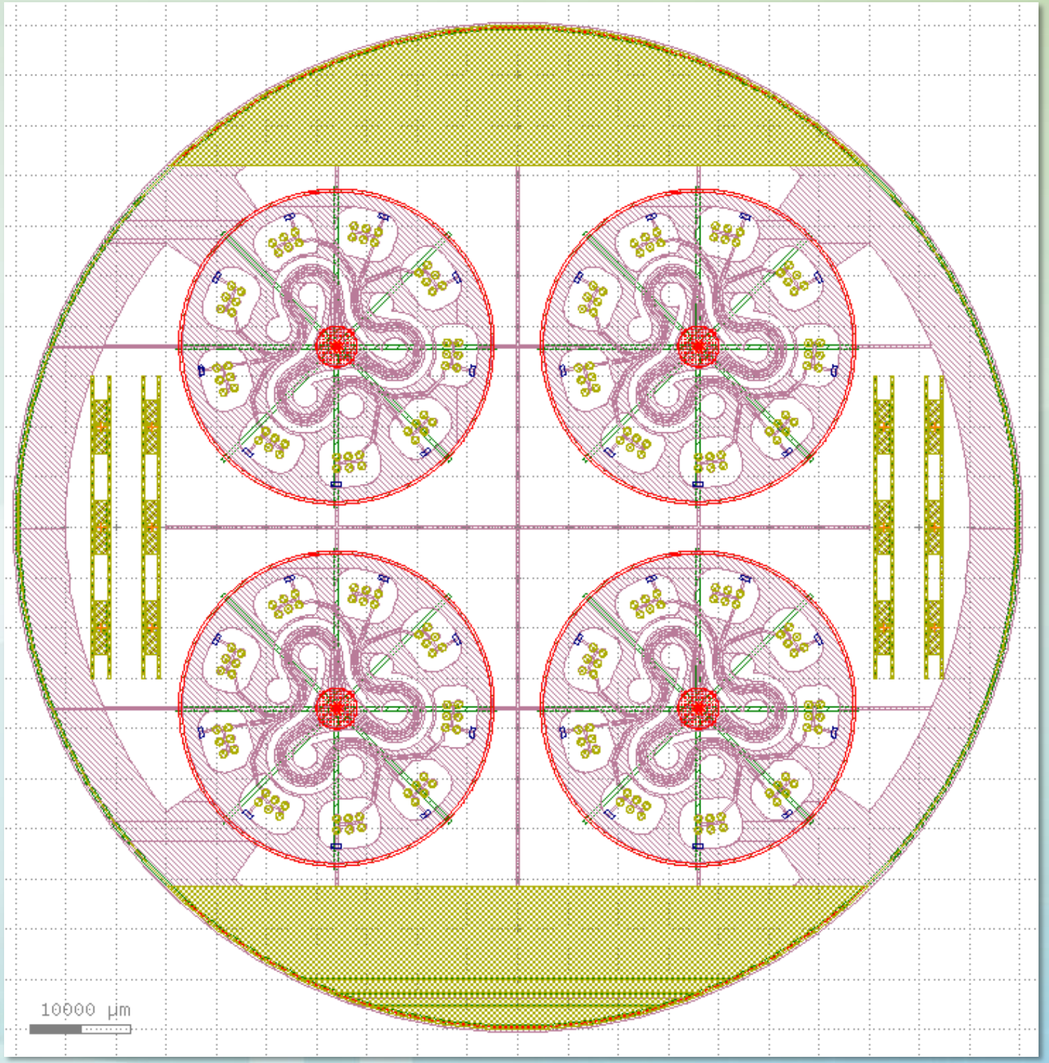


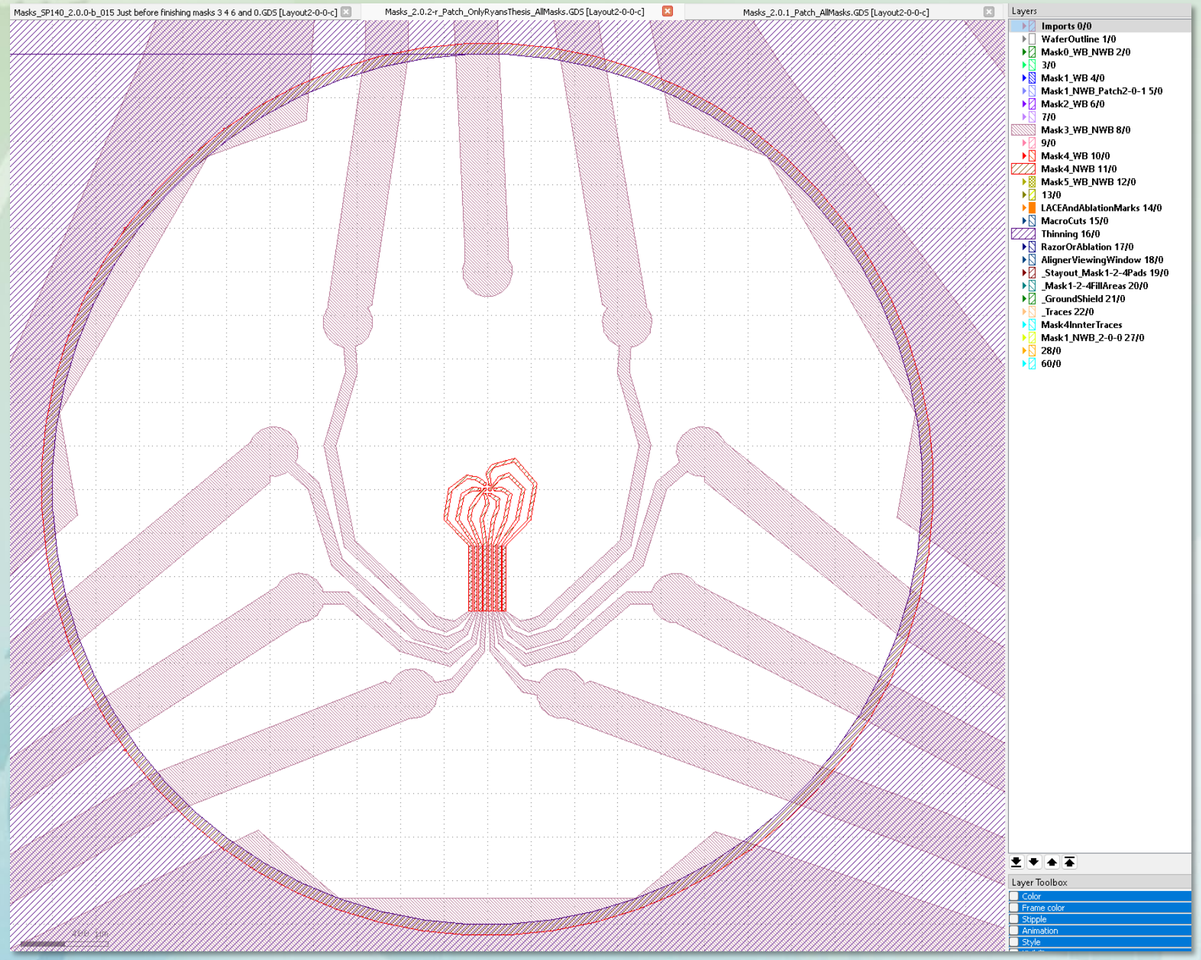



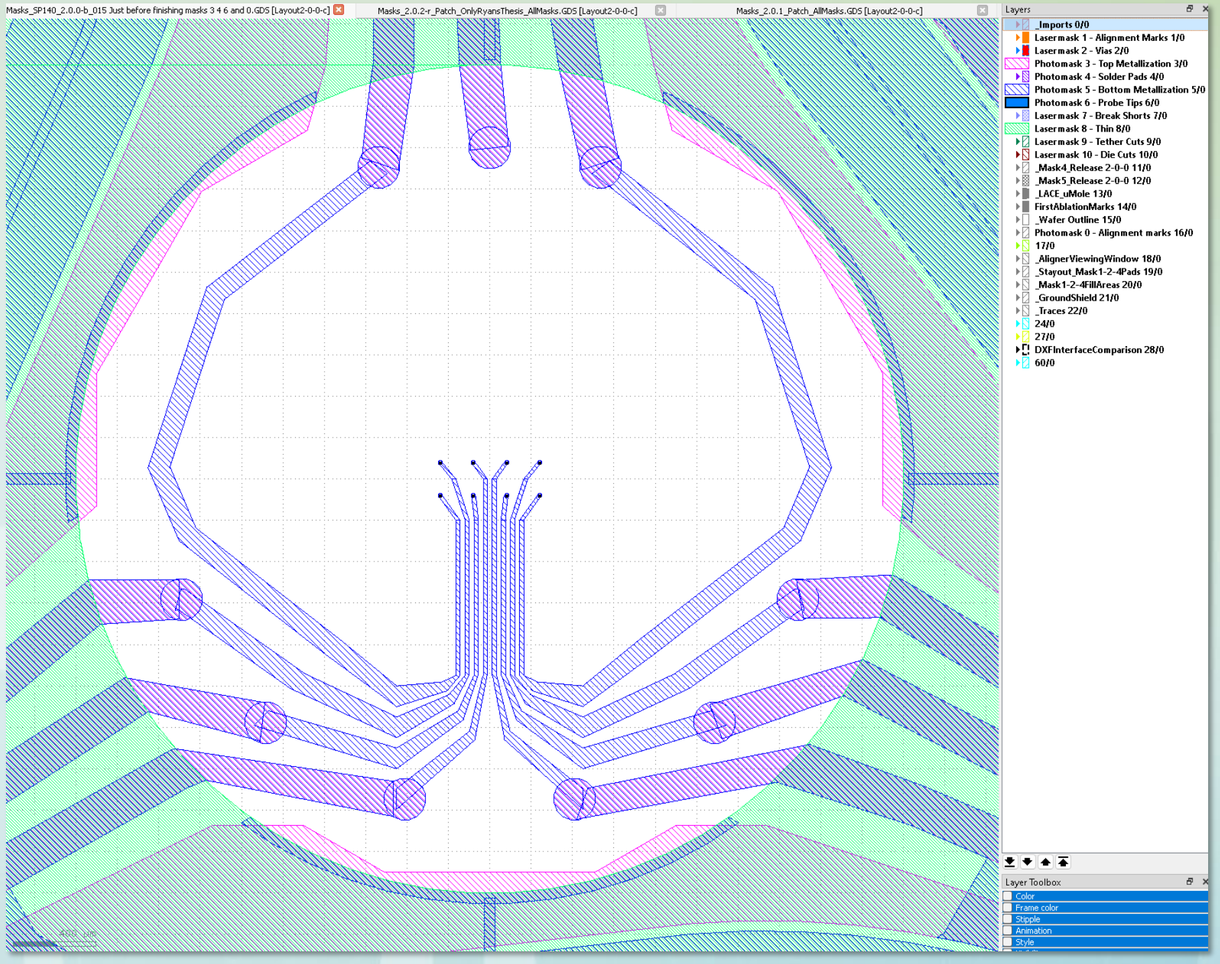
# Electrical Routing and Mask Design

- Metallization is comprised of 50 nm chrome adhesion layer, 500 nm aluminum layer, 50 nm nickel (seed layer for plating)
- Metallization (and signal routing) on front and back of wafer
- Copper plated through wafer vias connect front/back traces
- Front to back side alignment
- Combination of laser fabrication and lithography-based fabrication



# Front/Back Traces, Vias, and Probe Tips



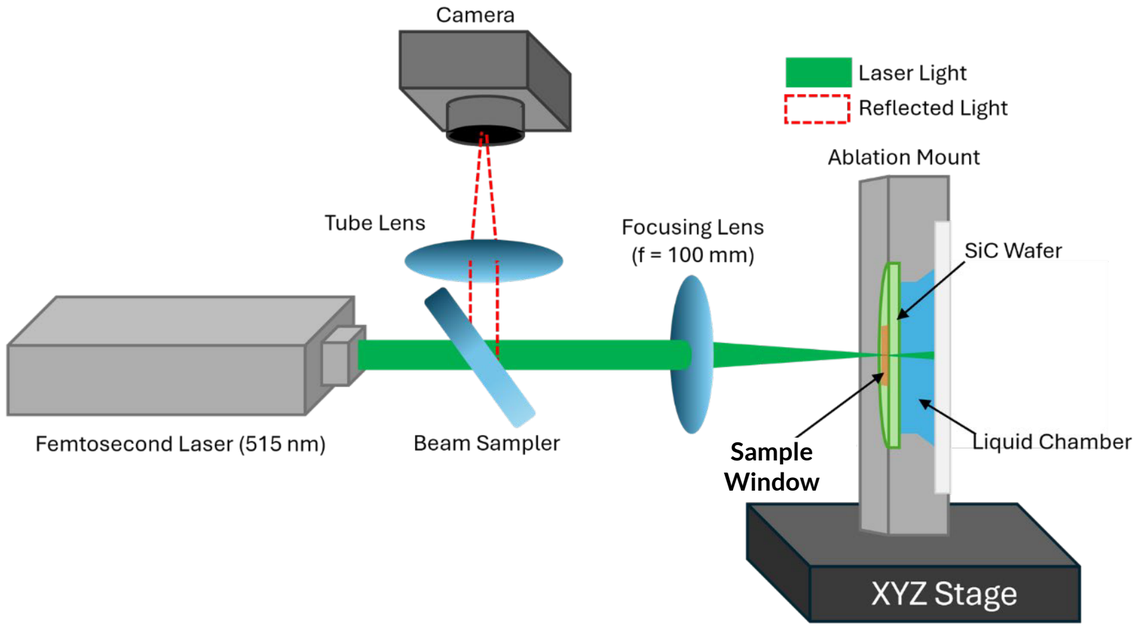
# Fabrication: Through Wafer Vias

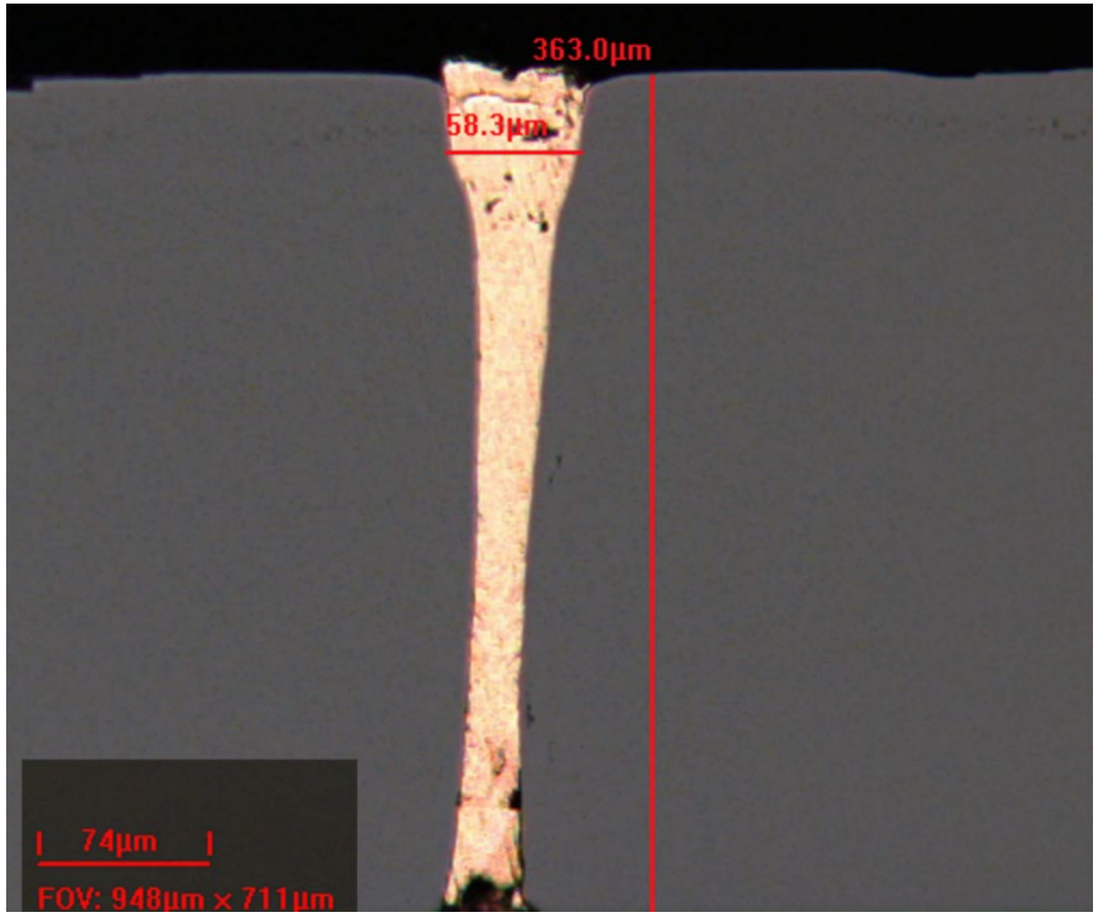
Laser fabrication of via holes

- Laser ablation: 50 µm diameter, 12:1 aspect ratio
- 2-photon laser directed 3D etching: < 2 µm diameter, > 150:1 aspect ratio, 3D microchannesl

Copper via fill

- Chrome seed layer followed by electroplated copper

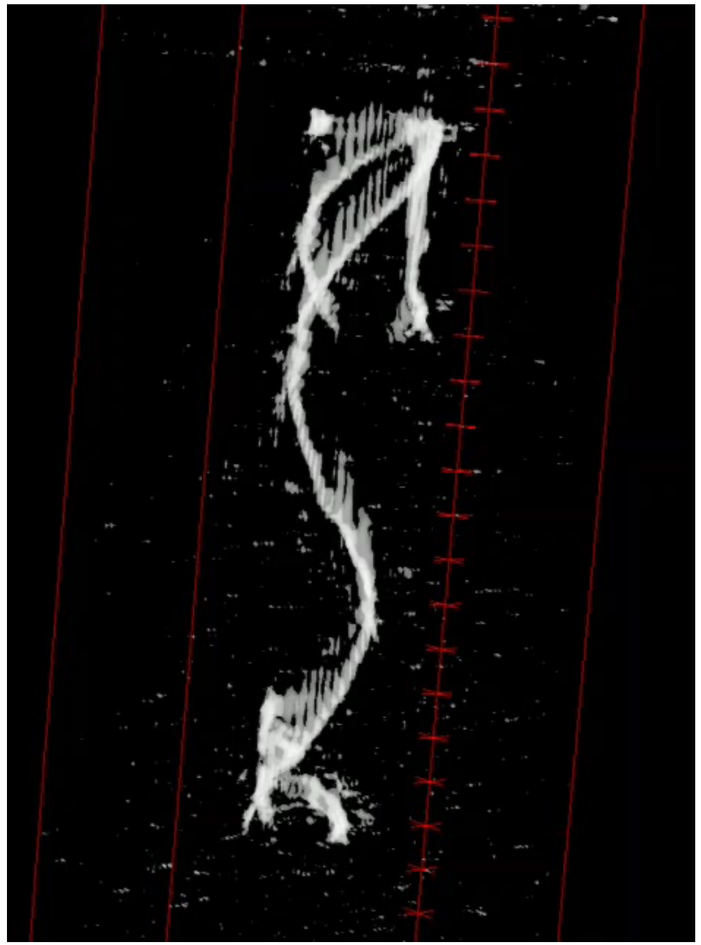


# High-Density, 3D Through Wafer Vias

## 3D two-photon directed etching of SiC

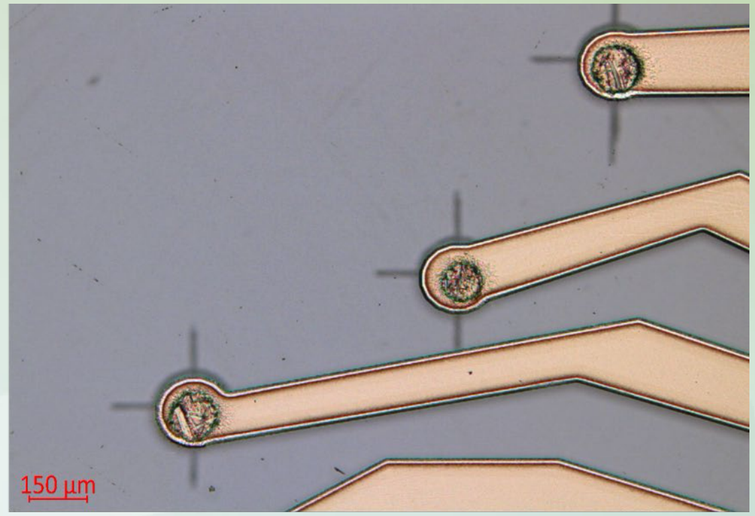
- 3D structures
- Very high aspect ratios (> 100:1)
- Features down to < 2 µm

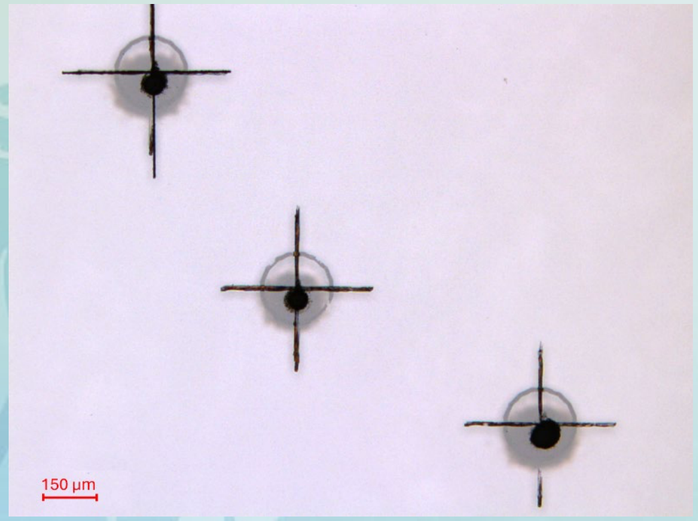


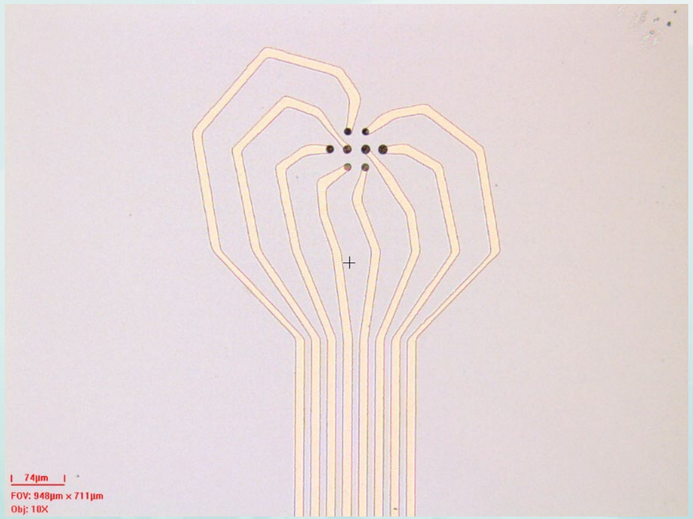
3D Xradia Micro-CT scans of through-wafer structures fabricated in 4H SiC

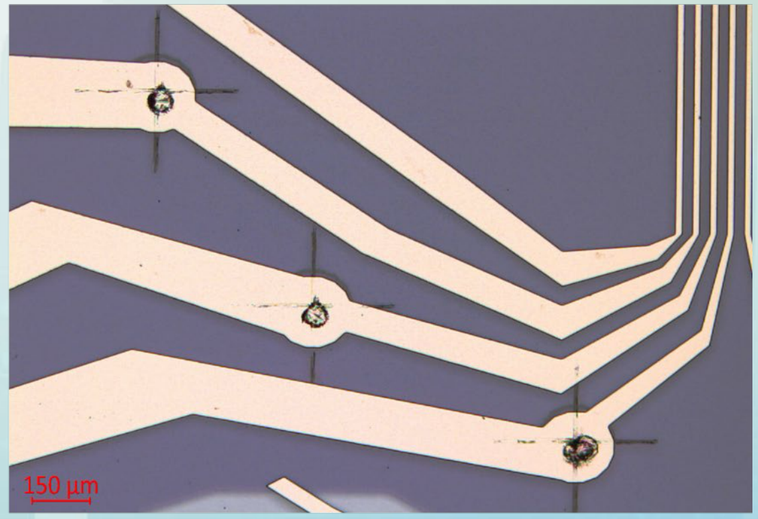
# Fabrication: Signal Traces

- Via hole and front/back trace alignment
- Metallization patterning and etching with photolithography
- Demonstrated good adhesion to SiC



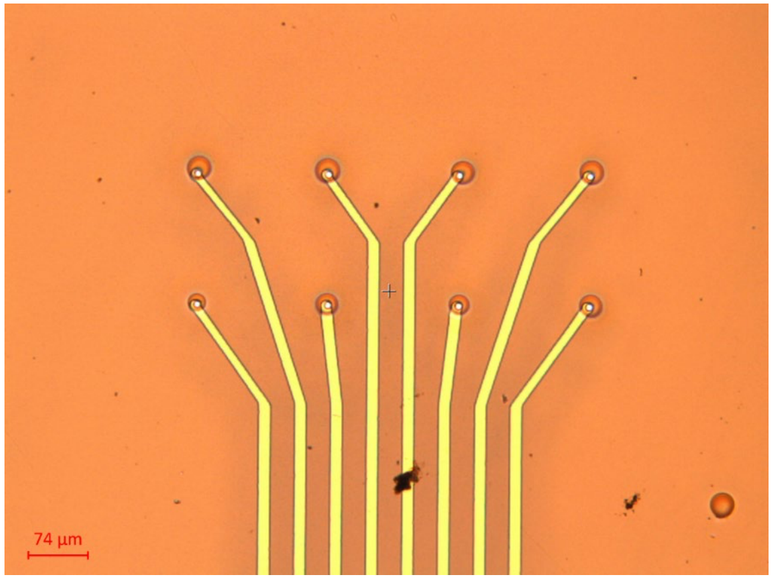



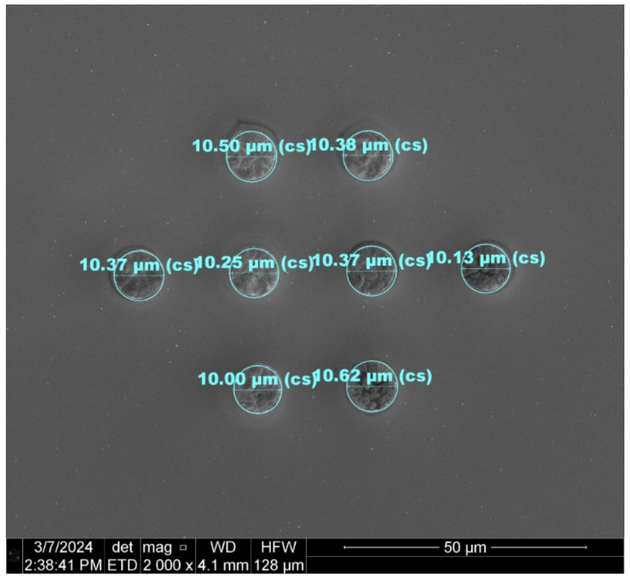



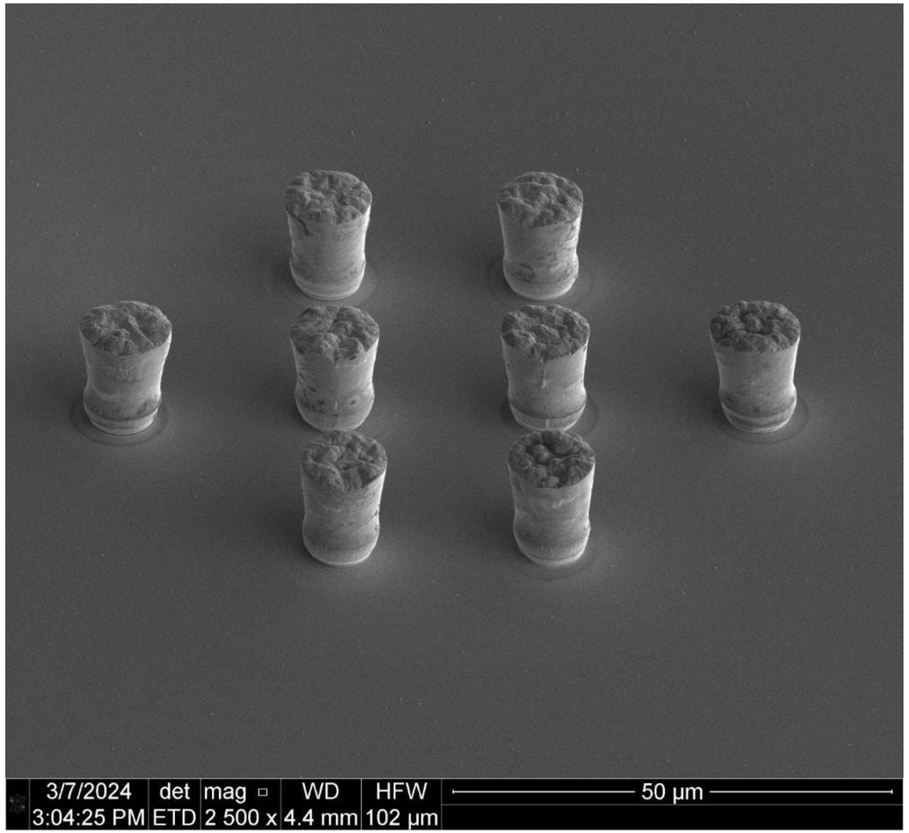



# Fabrication: Probe Tips

- Thick photoresist (10-15 µm) patterned with holes on top of probe tip traces to act as probe tip mold
- Palladium plated into the patterned photoresist
- Photoresist stripped to reveal probe tips

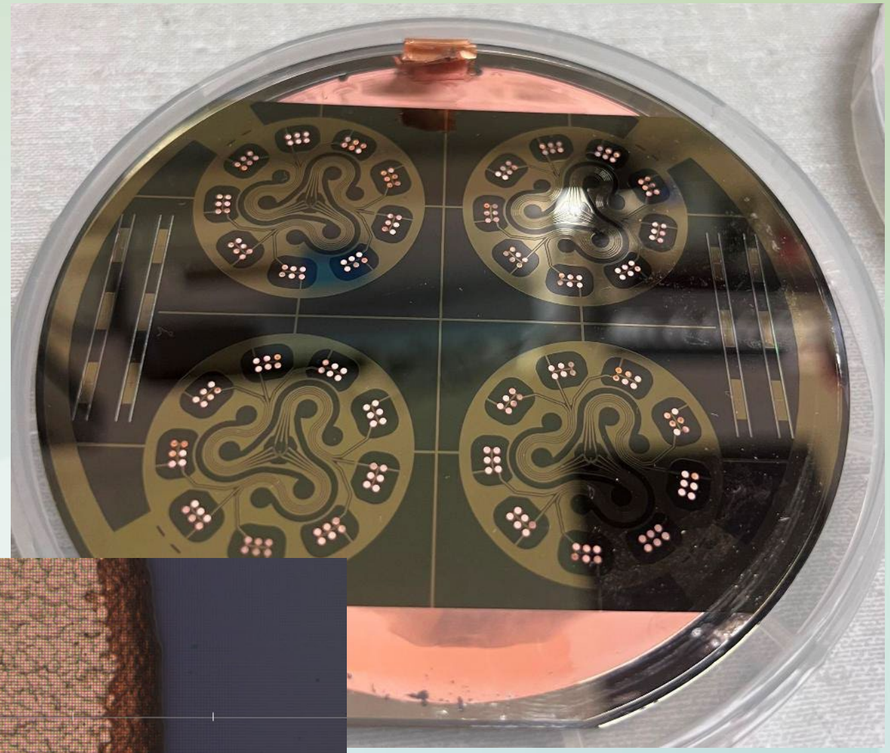


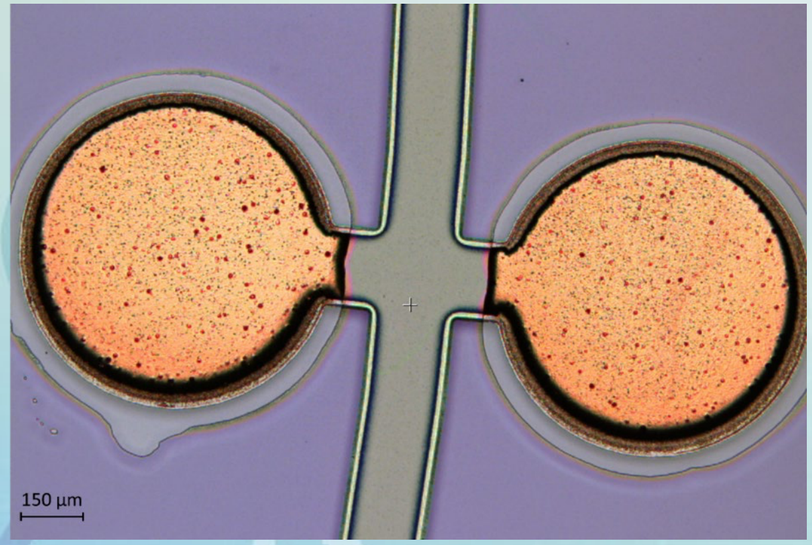



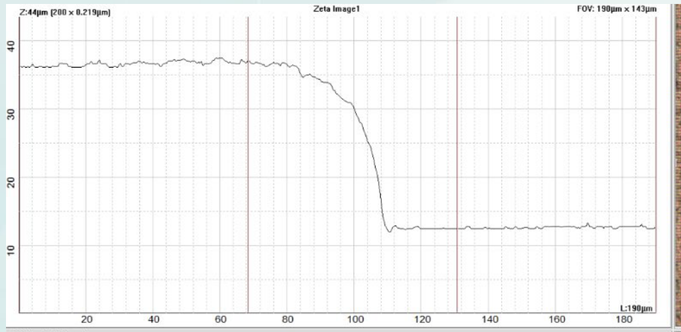



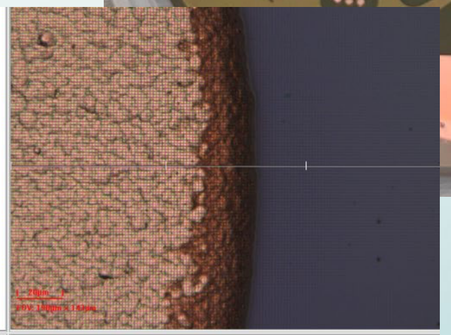
# Fabrication: Contact Pads

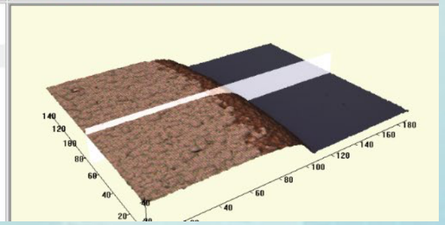
- Pad metallization has an exposed plating seed layer of nickel or copper
- Coat the wafer with a silicon oxide thin film
- Pattern and etch windows into oxide on pads
- Electroplate copper to desired thickness





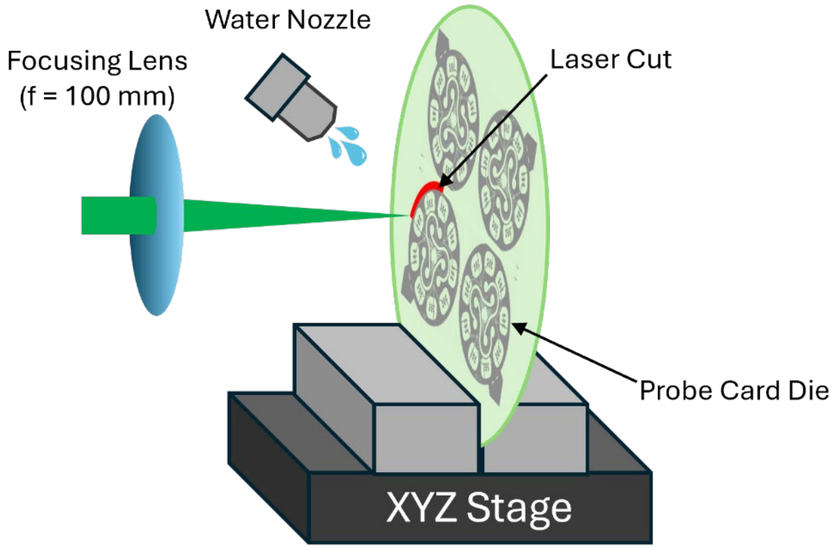



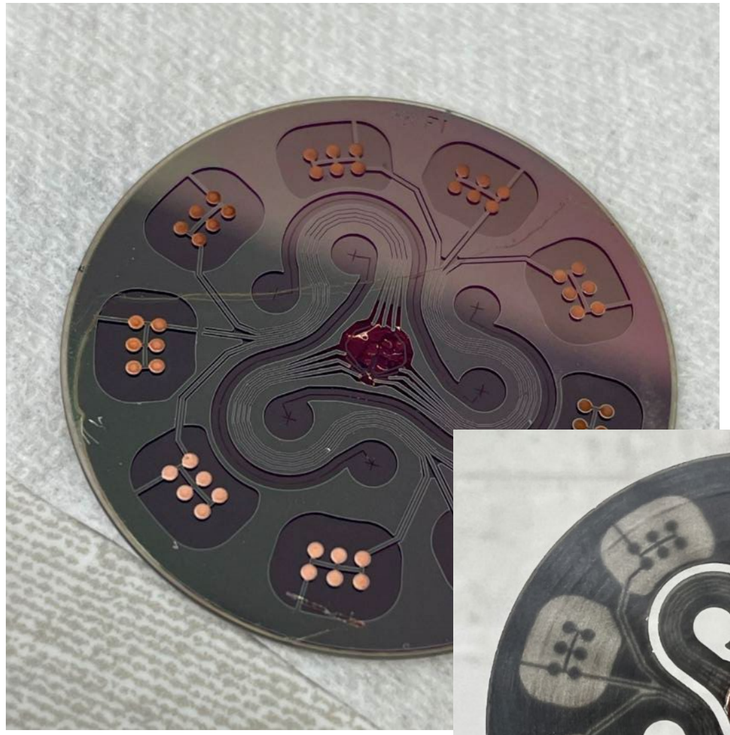



# Fabrication: Die Cutout

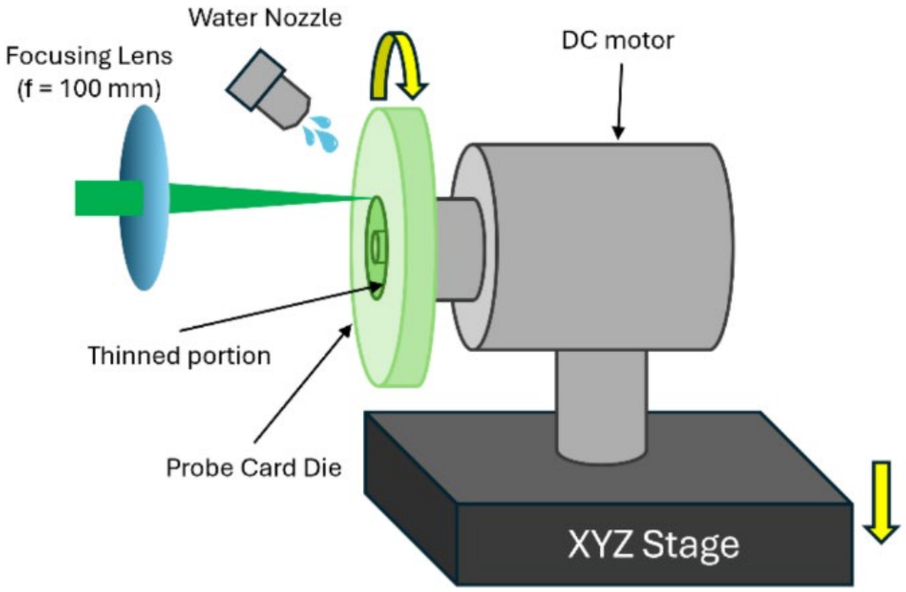
- Die cutout and flexure formation created with precisely controlled laser ablation
- Probe tips protected with a drop of photoresist
- Outside die cut first, then the die is thinned, then the flexures are cut

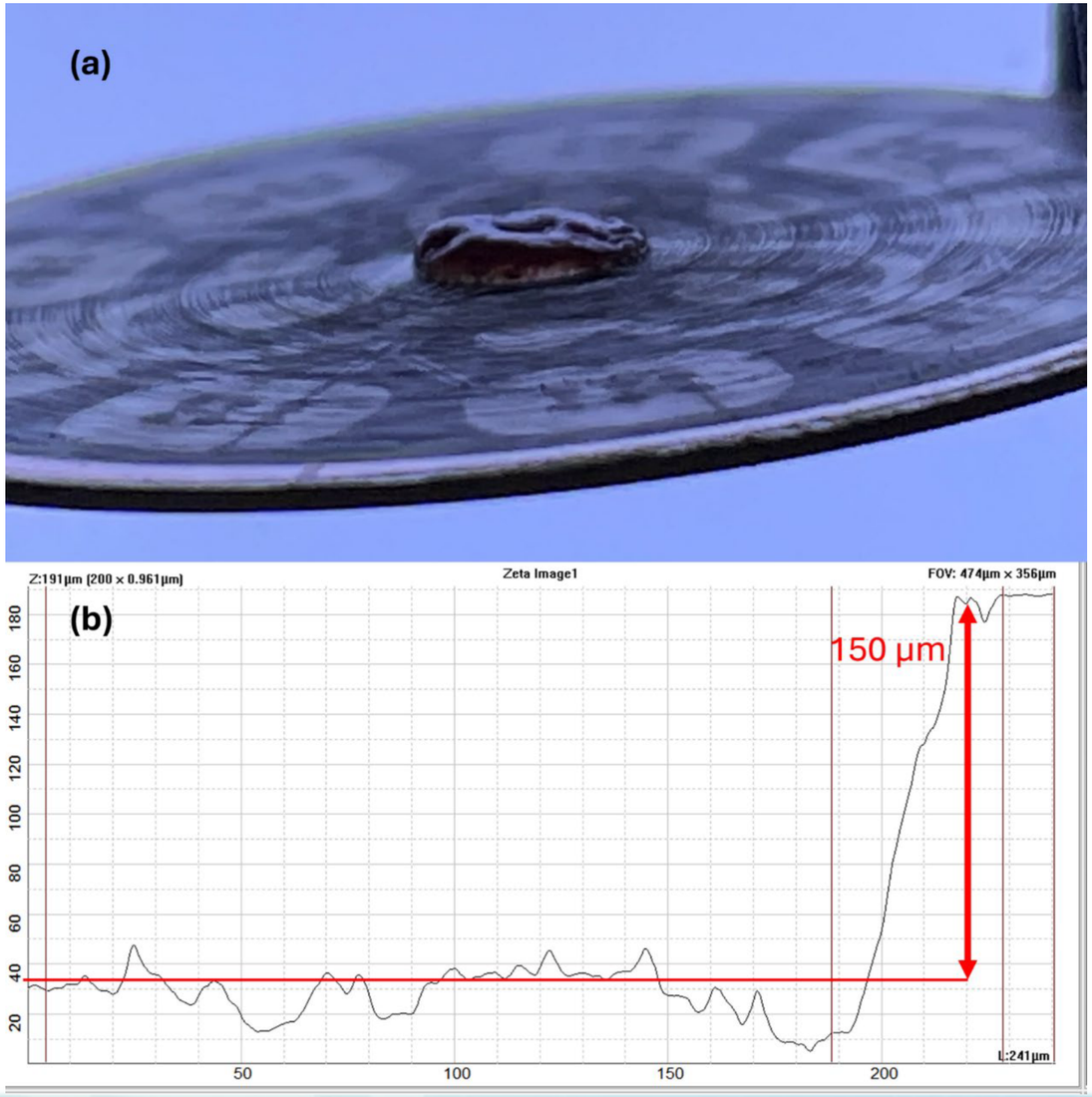


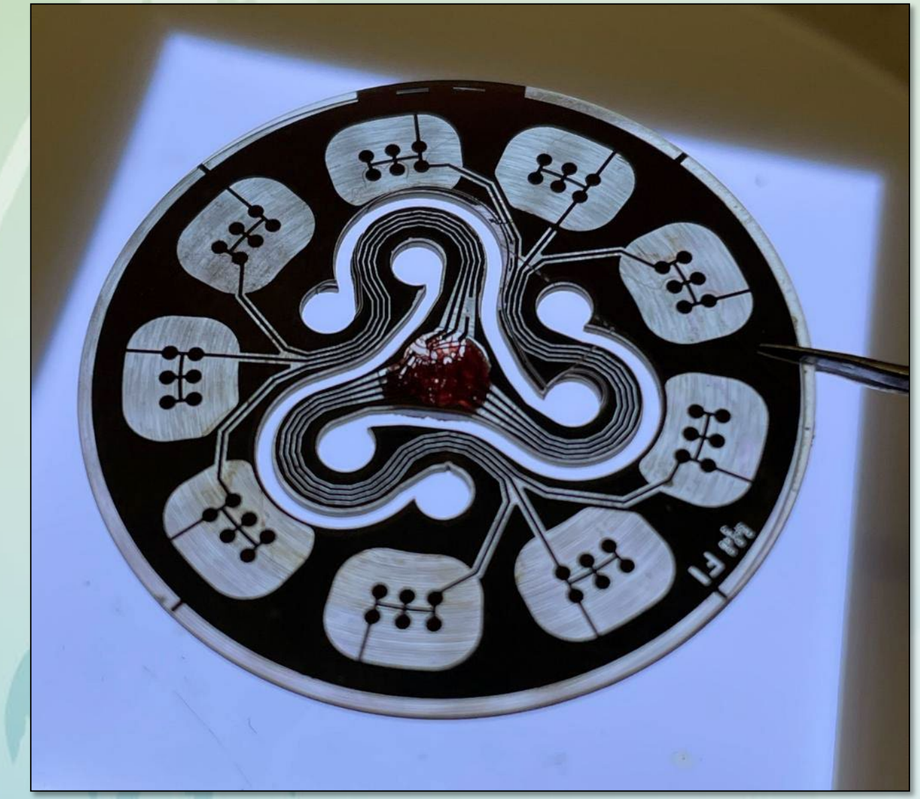
# Fabrication: Die Thinning

- Die thinning is required to provide clearance for the probe tips
- Thinning is accomplished with a “laser lathe” technique



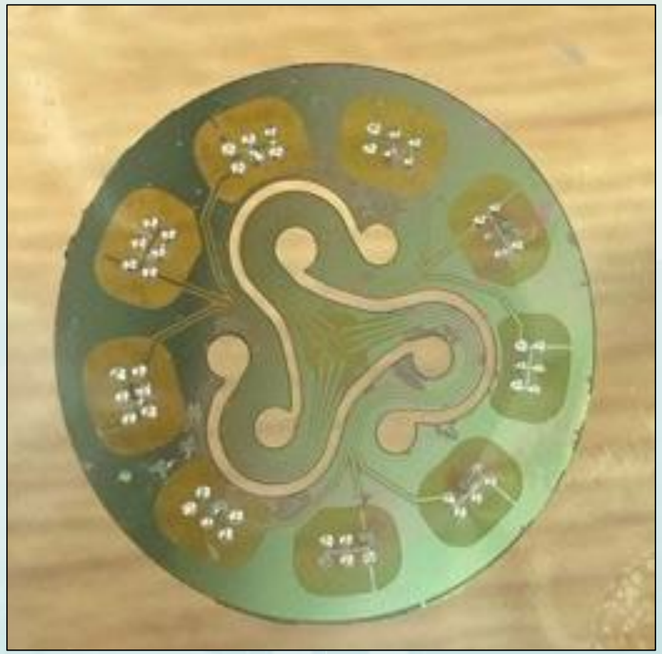
# Final SiC Die



# PCB Attachment

- The Flexure PCB is attached to the SiC die using a low temp solder to form a mechanical and electrical connection.
- The flexures within the PCB mitigate the radial mechanical stress from the cryogenic shrinkage.
- The 6-point solder positions provide a strong yet flexible connection.

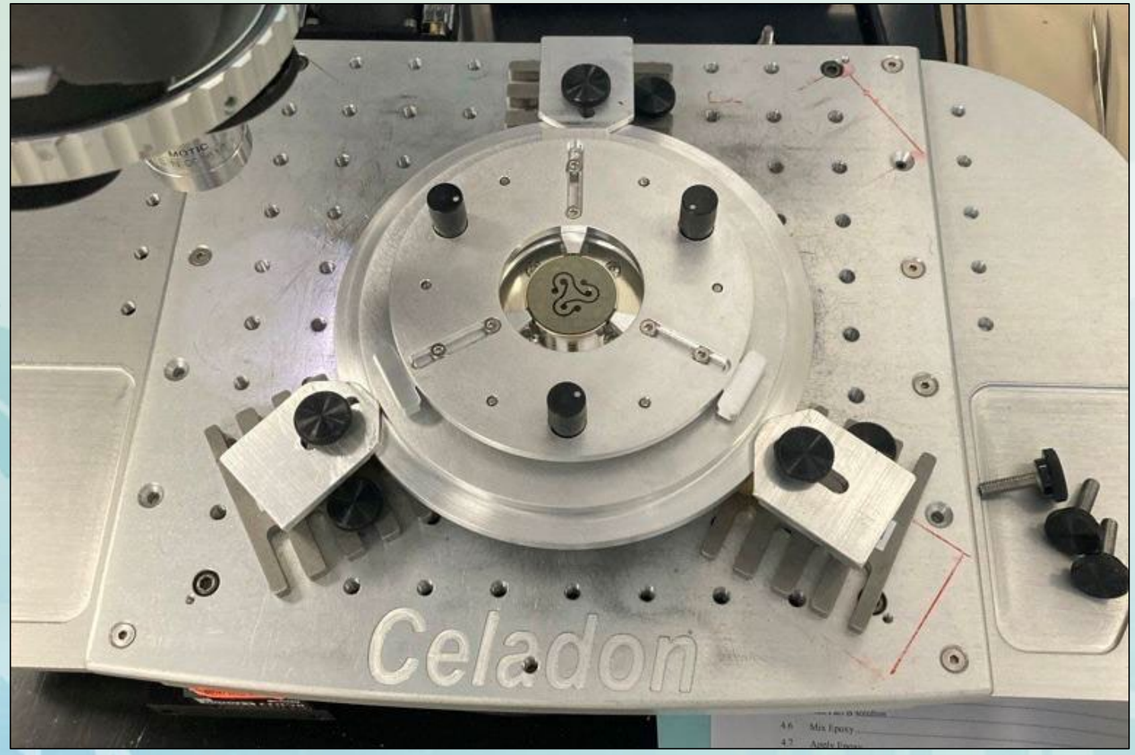
Flexure PCB

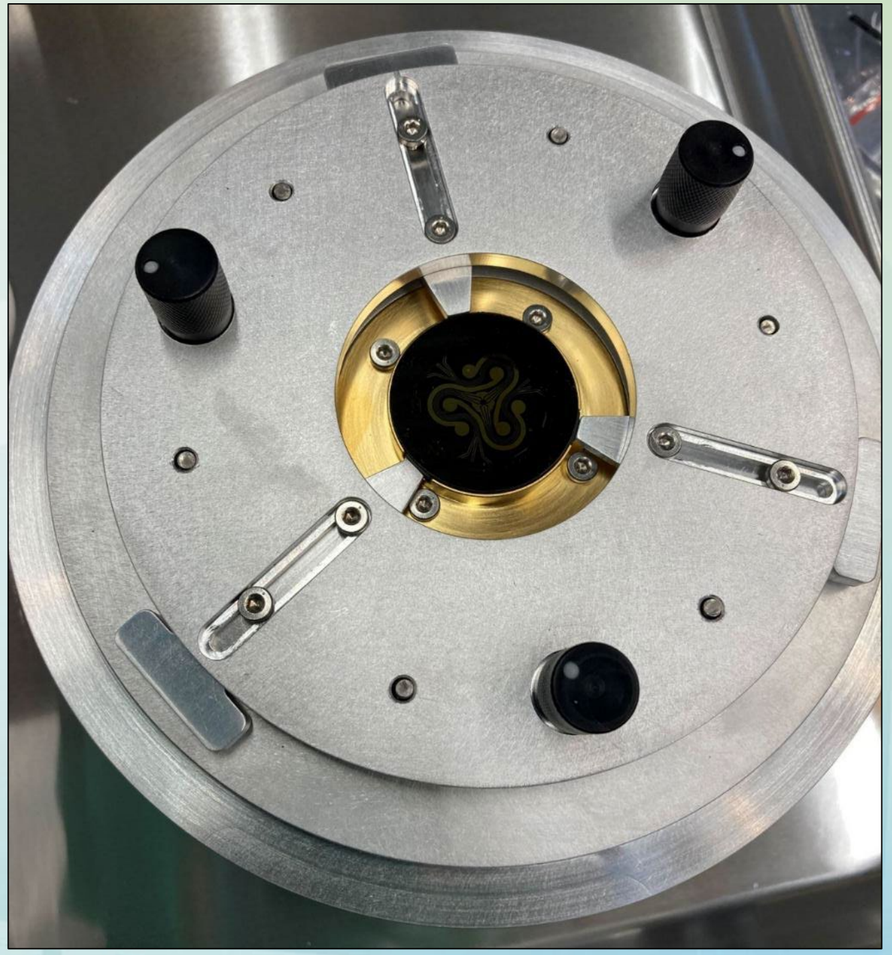


SiC Die

# Chassis Planarization

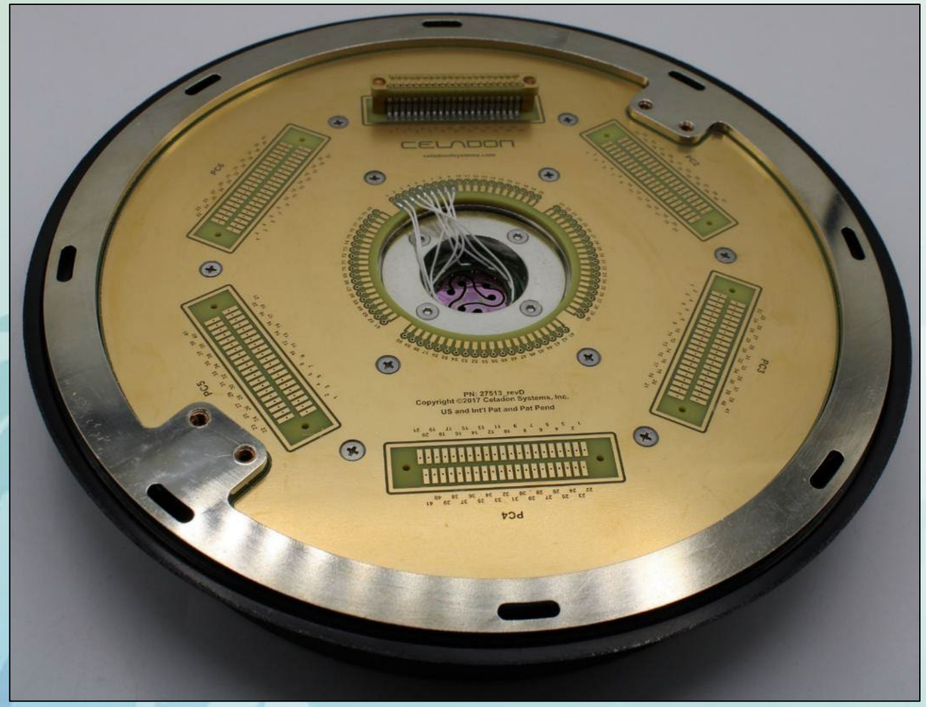
- The Flexure PCB is epoxied into the chassis of the probe card and planarized to within ± 5 µm to ensure proper contact to the wafer.
- This planarization is done on the Celadon Alignment Stations.

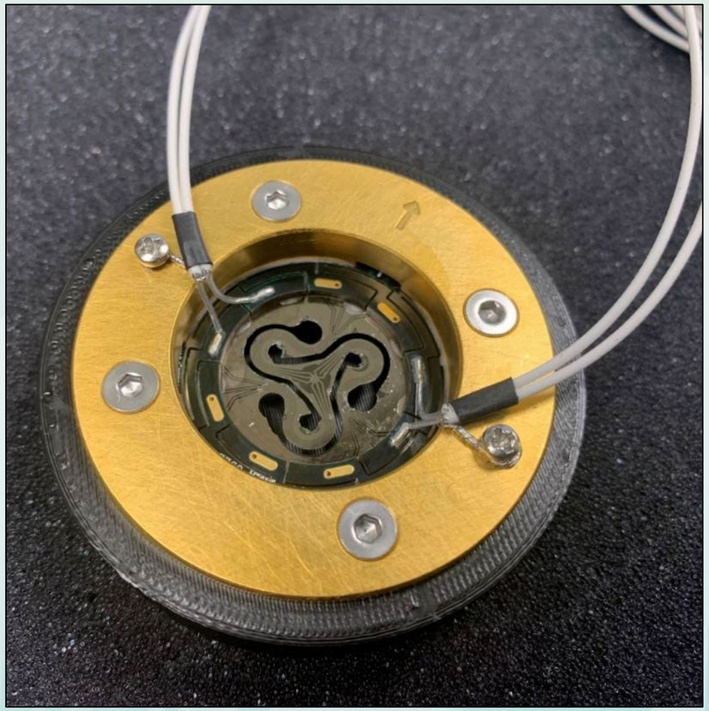


# Final Assembly

- The finishing process for the product is to terminate the Flexure PCB to a usable interface.
- This has been done by either direct cable out, or to a larger PCB.

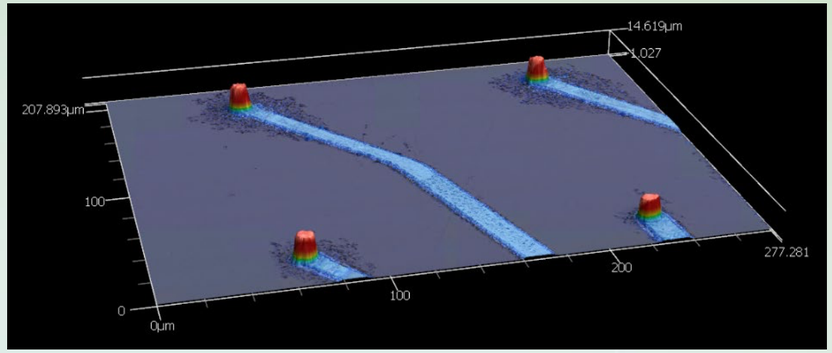


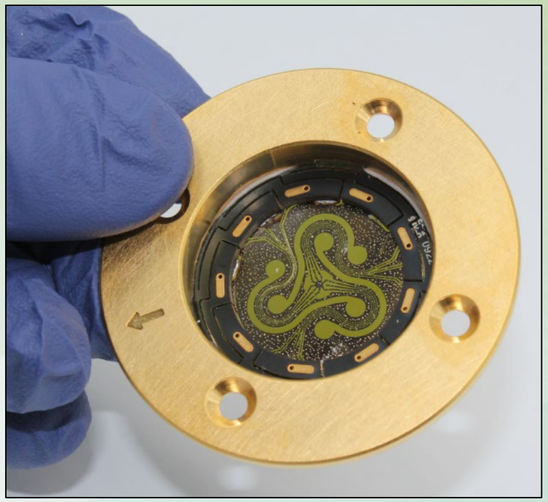



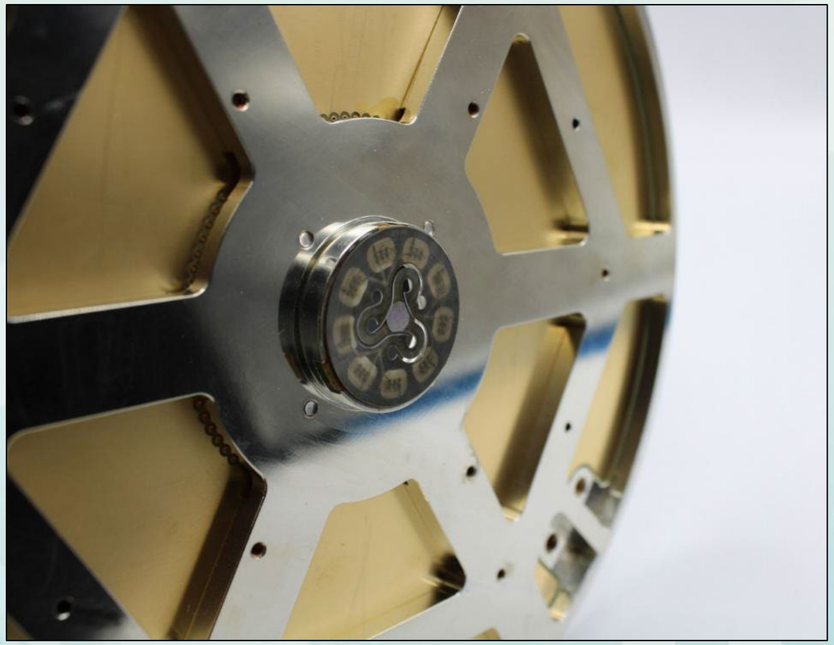
# Finished Product

## Key Features

- Cryogenic Probing expected down to 2K
- Clear Optical Path for top-down alignment “See-through”.
- MEMS style probes for pad arrays.
- Small probe tips at 8 µm diameter
- Extremely tight pitch down to 20 µm.
- Future plan for hundreds of probes.





# THANKS

## For Your Attention