SWTEST

PROBE TODAY, FOR TOMORROW

2025 CONFERENCE

A Novel Approach for Increased Probe Card Parallelism Utilizing Device Package Substrates

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Agenda

Motivation of Work — Market Drivers

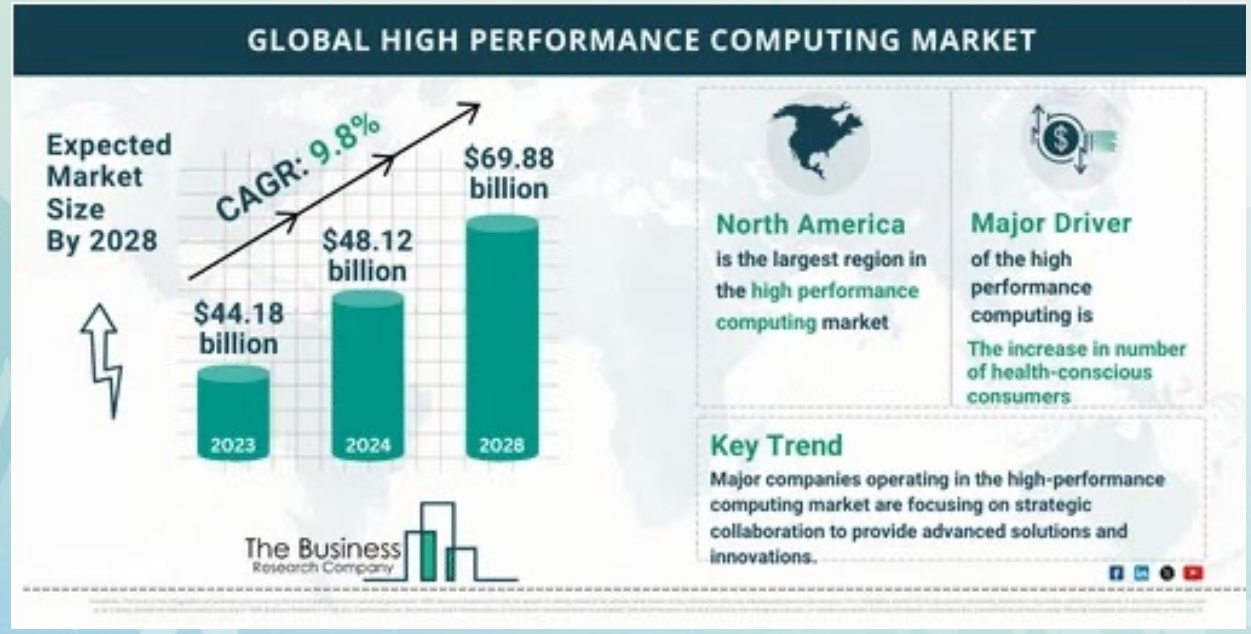
Development Strategy Overview — Customer Challenge; Solution Approach

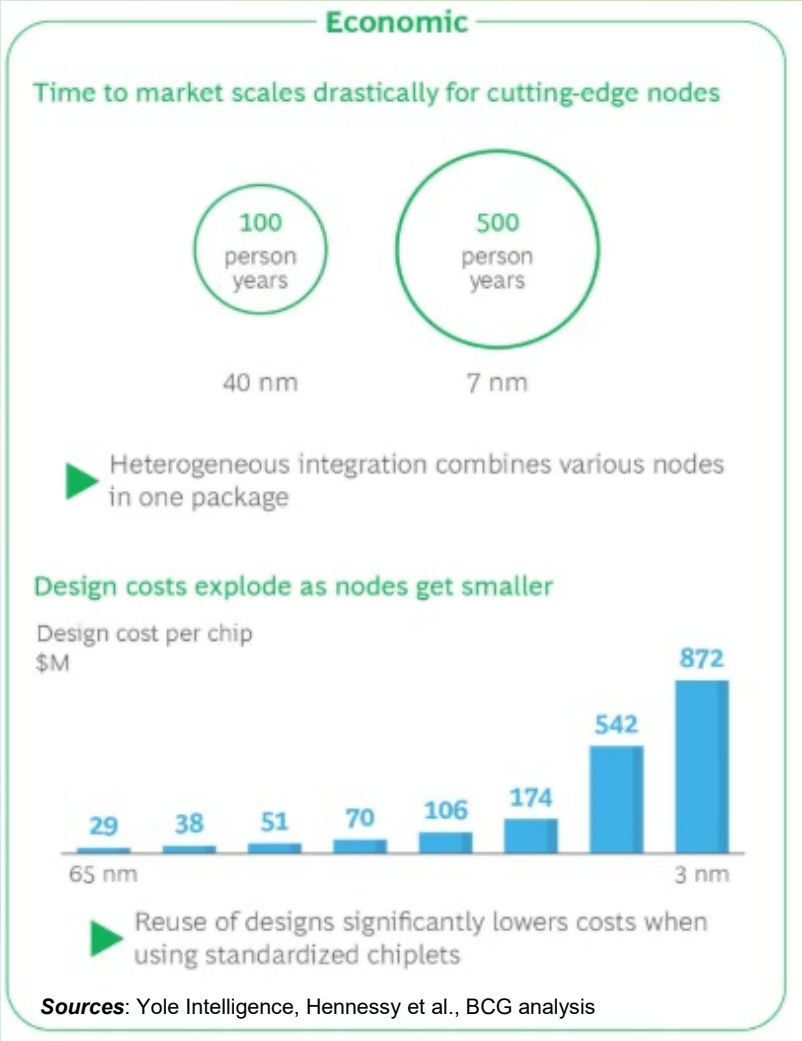
Product Validation Results — Confirmation of Solution Approach

Summary and Acknowledgements

High Performance Compute (HPC) Device Market Trends

- The costs of introducing next generation devices and process technologies has exploded
  - In addition, chip design costs have increase 30x going from a 65nm design to a 3nm design
- At the same time, the market is rapidly expanding
  - CAGR: ~10% from 2023 to 2028

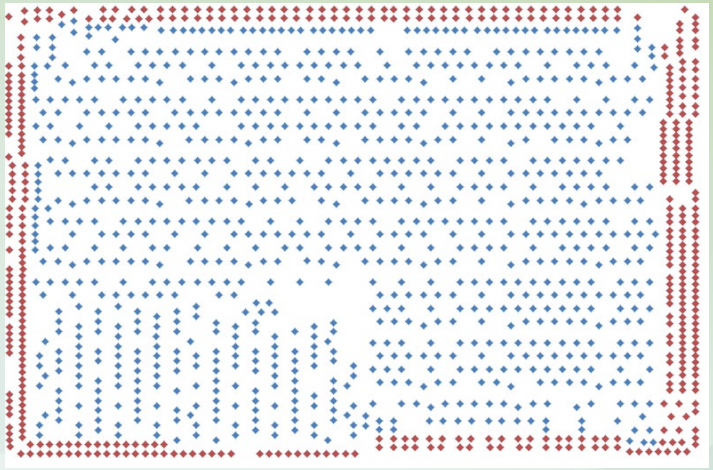


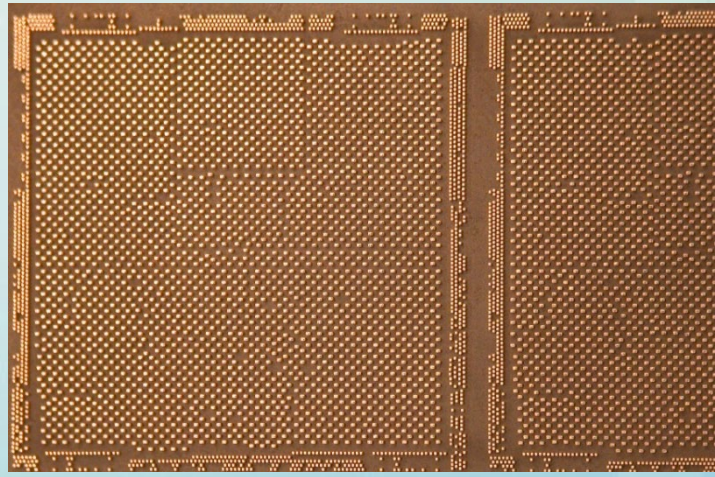


Sources: Yole Intelligence, Hennessy et al., BCG analysis

HPC Device Wafer Test Challenges

- Increased I/O and Power & Ground connections points → increase pin counts per DUT
- Critical to maintaining and improving signal fidelity to achieve entitled yields
  - Aligning SI/PI performance to device to minimize signal loss and reduce re-test rates
- Relentless drive to reduce cost of test is increasing wafer test parallelism and strategies
- Expanding test temperatures increases the thermodynamic challenges
- Probe card design strategies
  - Monolithic vs. Singulated substrates





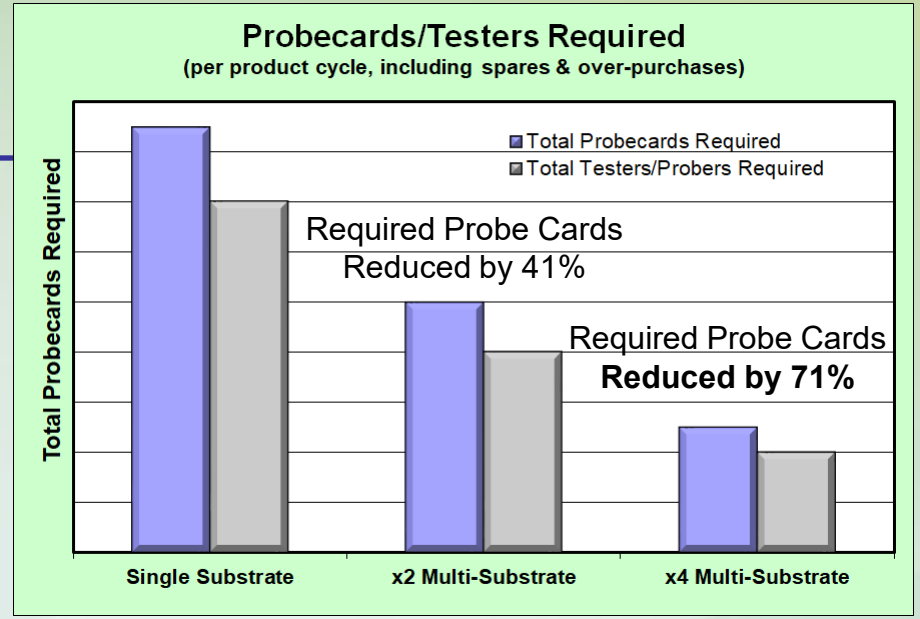
Meeting Cost of Test Reduction Challenges – Considering Package Substrates as Space Transformer

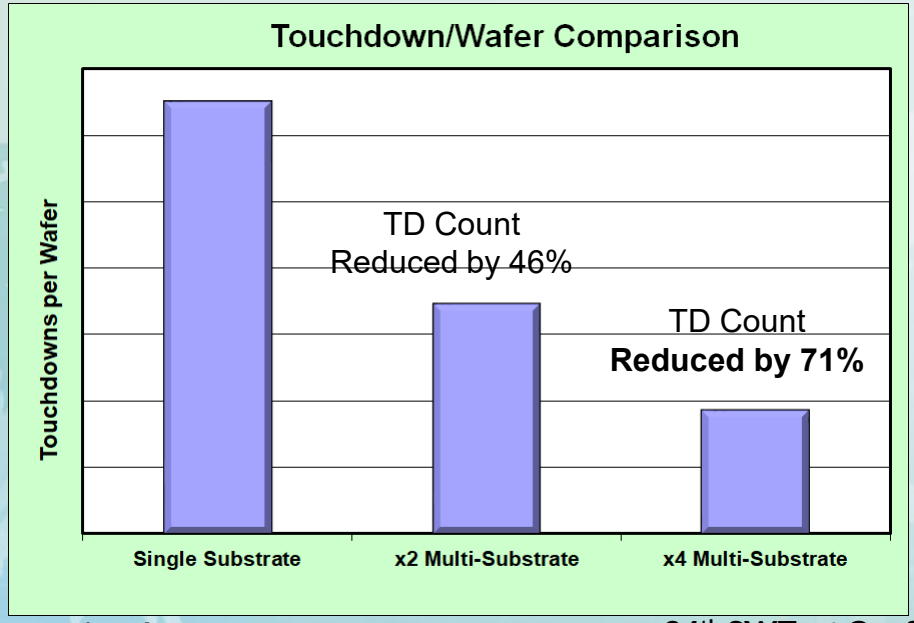
	Advantage	Disadvantage
Traditional Monolithic MLO	- Higher Parallelism → reduced TD count - Better manufacturability - Solid array is possible for lower parallelisms	- Challenges to aligning SI/PI to DUT - Higher MLO costs/DUT tested - Slower to redesign, limited modularity
Package Substrate	- SI/PI better aligned with DUT - Built in DFT - Lower substrate (MLO) costs - Expect test results closely matched to end use applications	- Requires skips for multi-DUT - Limited parallelism for comparable monolithic area - Additional manufacturing challenges

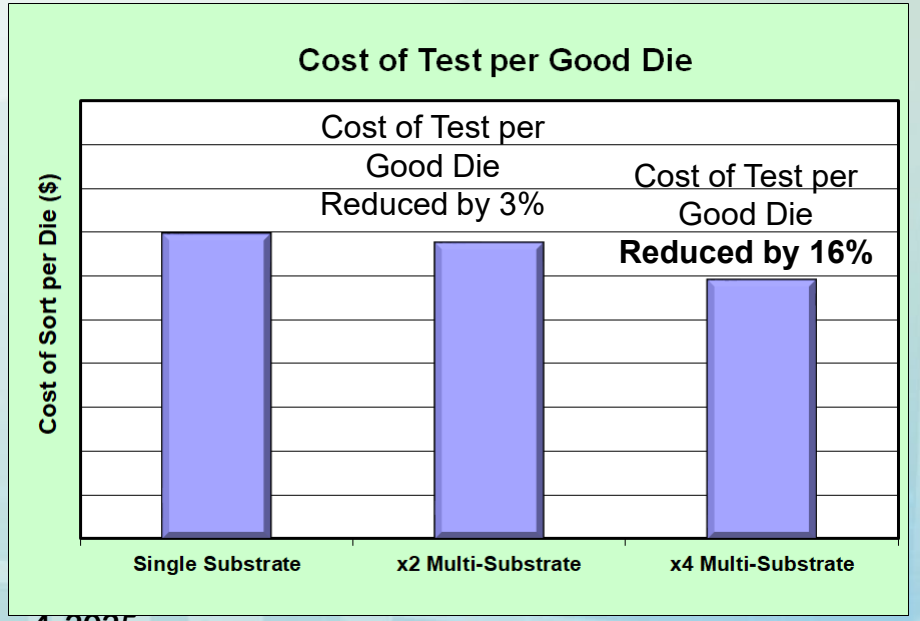
Supporting Cost of Test Reduction

-TCOO Analysis (500 wspm): Single Substrate vs. Multi-Substrate

- **Objective:**
  - Reduce cost of test with increased parallelism
- **Assumptions:**
  - 300mm wafer, ~350 die, 500 wafers per month (wspm)
  - Test time, retest %, and cleaning cycle remain unchanged
  - No increase in required tester count



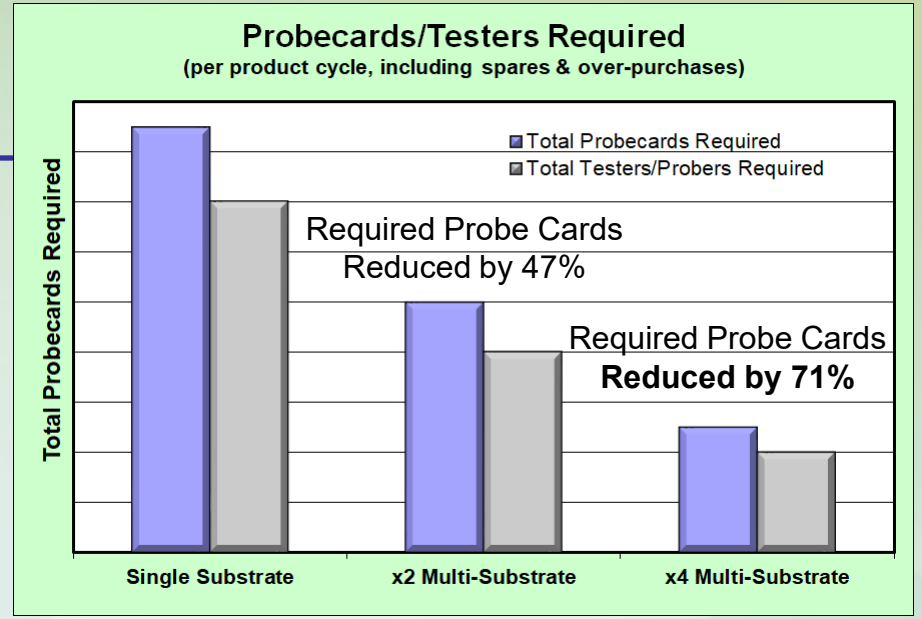


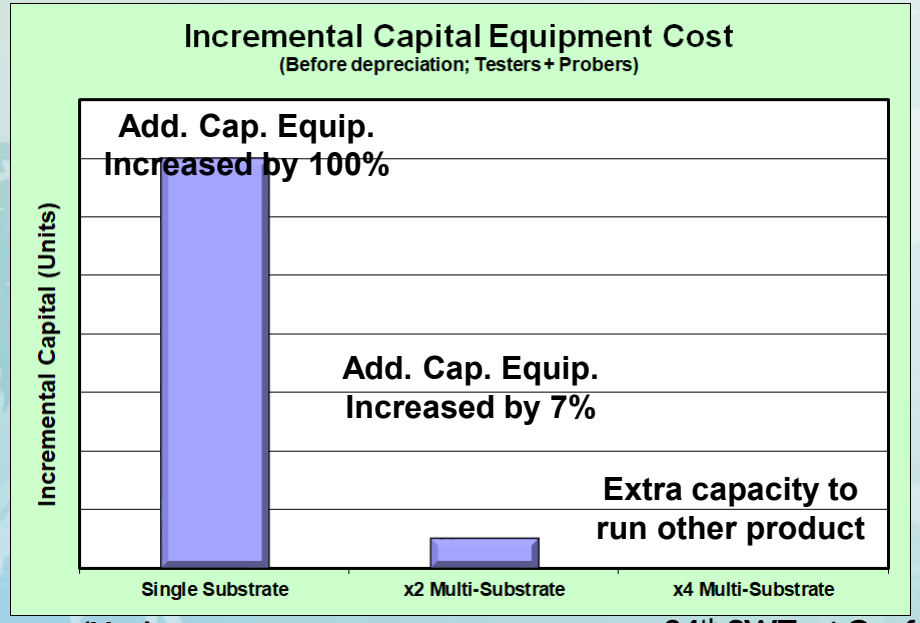


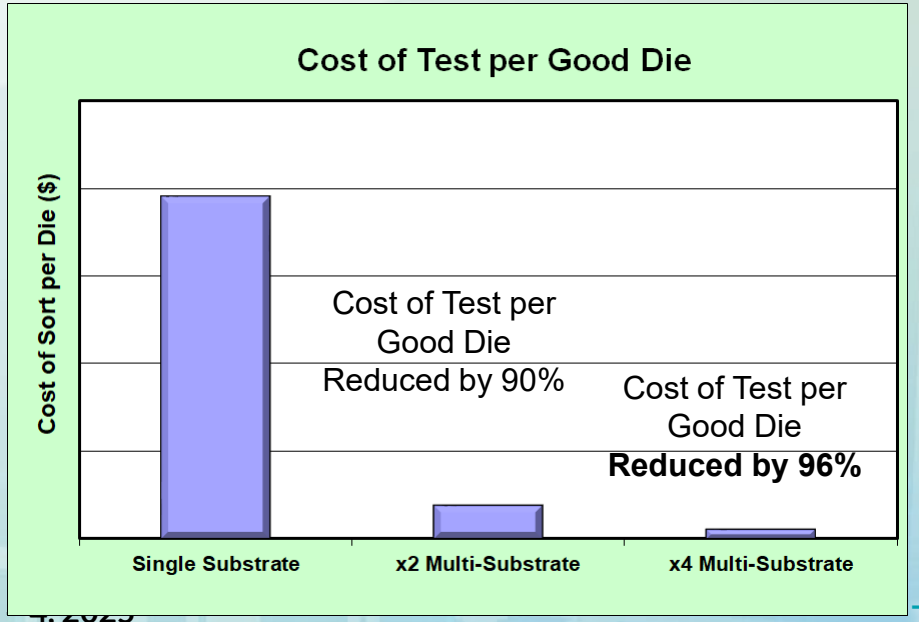
Supporting Cost of Test Reduction

-TCOO Analysis (1,000 wspm): Single Substrate vs. Multi-Substrate

- **Objective:**
  - Reduce cost of test with increased parallelism
- **Assumptions:**
  - 300mm wafer, ~350 die, 1,000 wafers per month (wspm)
  - No Change to test time, retest %, and cleaning cycles
  - 14 additional testers needed to support demand





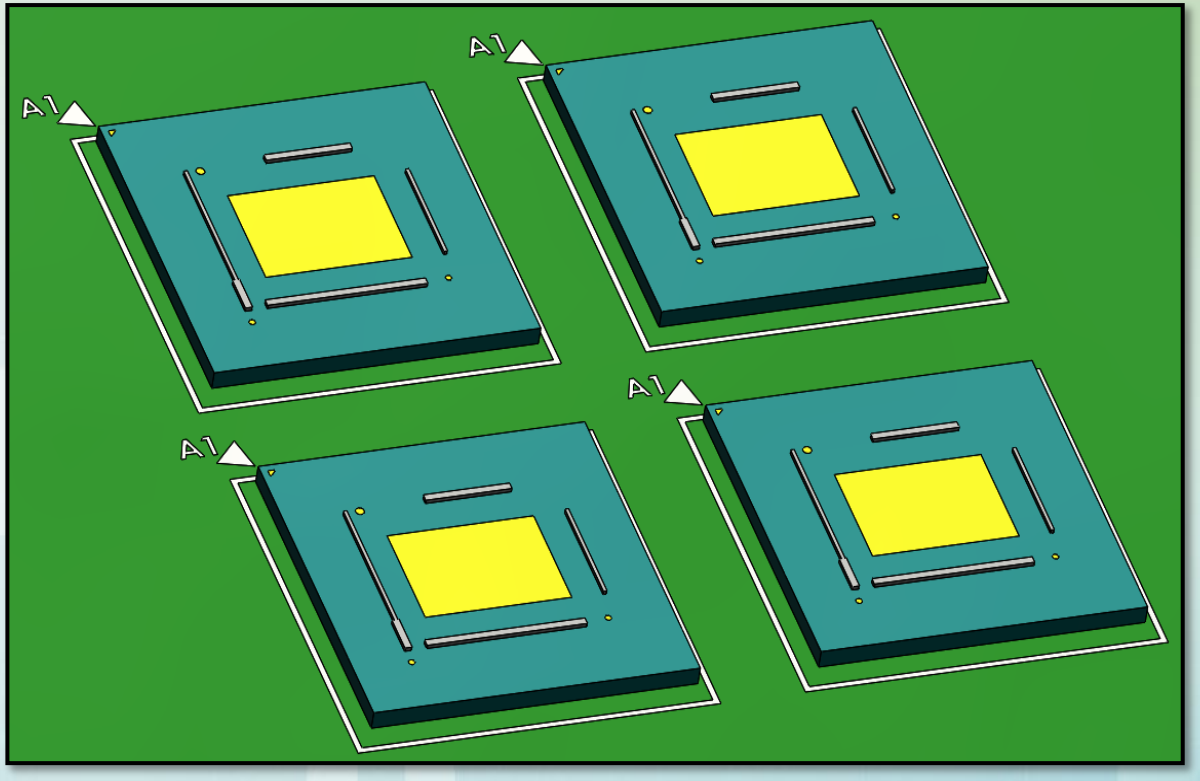


Agenda

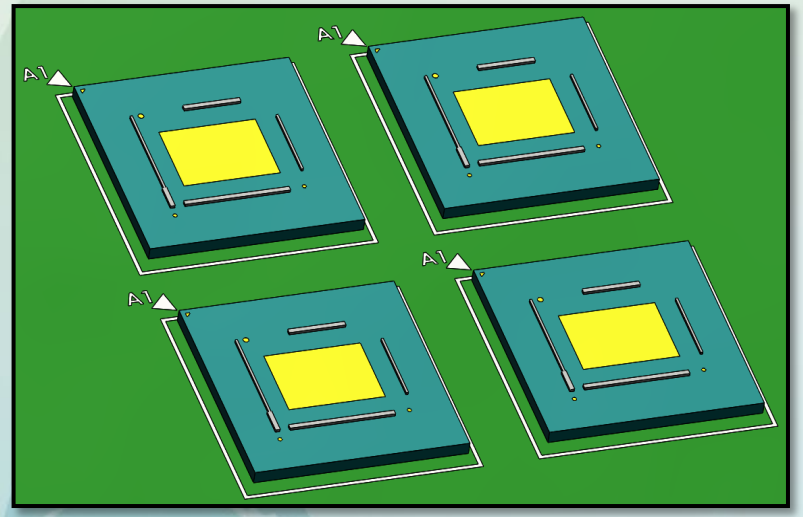
- **Motivation of Work** — Market Drivers
- **Development Strategy Overview** — Customer Challenge; Solution Approach
- **Product Validation Results** — Confirmation of Solution Approach
- **Summary and Acknowledgements**

Multi-Package Substrate Placement Challenges
- What are the key specifications and challenges?

- **Define Criteria for HVM:**
  - Electrical reliability
  - Multi-substrate co-alignment
  - Stable assembly processing across the full temperature range.



Multi-Package Substrate Placement Challenges
- What is the Test-Plan?



Determine Baseline	Can current BKM achieve required results?
Theoretical Modeling	Can a theoretical model reliably predict final outcomes based on in-line processing behavior?
Validate Modeling	Do experimental results confirm model accuracy and alignment trends?
Optimize Placement	What process changes improve alignment accuracy and reduce variability?
Determine Repeatability	Can the optimized process deliver consistent, scalable performance?

Multi-Package Substrate Placement Challenges
- What defines our current baseline capabilities?

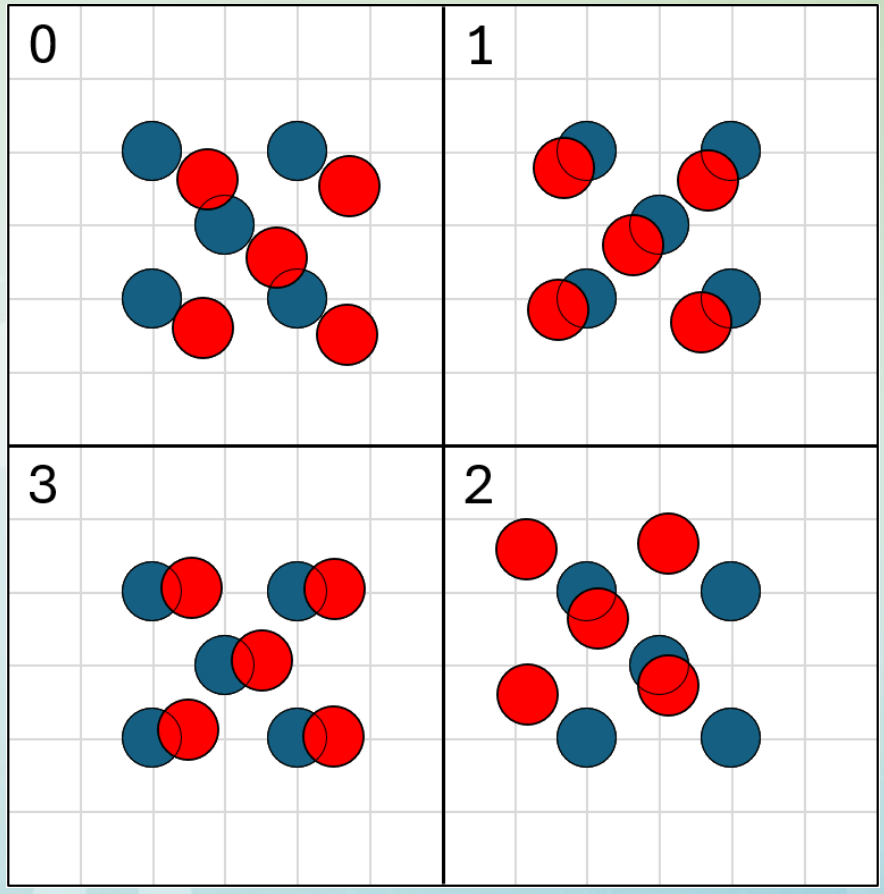
- **Objective:**
  - Evaluate if current methods meet co-alignment requirements
- **Passing Criteria:**
  - Accurate positioning within/across substrates
  - Alignment to local and global targets
- **Summery of Results:**
  - No consistent alignment between substrates
  - Post-reflow results exceeded tolerance limits.

Alignment Results

DUT	Location	Dispo
0	TL	FAIL
1	TR	FAIL
2	BR	FAIL
3	BL	FAIL

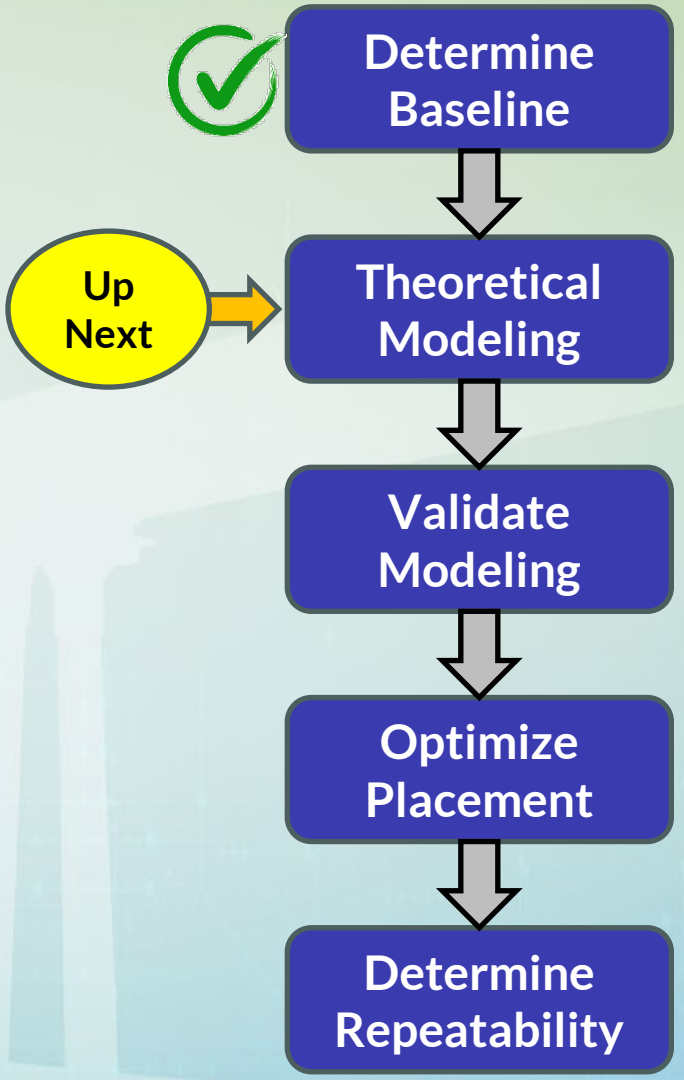
Nominal
Measured

Baseline Co-alignment Results



Multi-Package Substrate Placement Challenges
- What are the key take-aways from BKM?

- **Key Take-Away:**
  - Current methods yield inconsistent co-alignment and exceed tolerance limits.
  - Alignment to local and global targets remains unreliable
  - Tighter control and better placement are ***required*** for scalable, high-yield production.



Multi-Package Substrate Placement Challenges
- What is the criteria for the theoretical model?

- **Boundary Conditions:**
  - POR constraints limit flexibility and impact co-alignment consistency
  - Process variation must be managed through targeted adjustments
- **Control Strategy:**
  - Leverage controllable steps to mitigate process-induced variation and enhance repeatability
- **Modeling Setup:**
  - Build a predictive model using the proposed control strategy under optimized process conditions

Multi-Package Substrate Placement Challenges
- Can a theoretical model predict final substrate alignment?

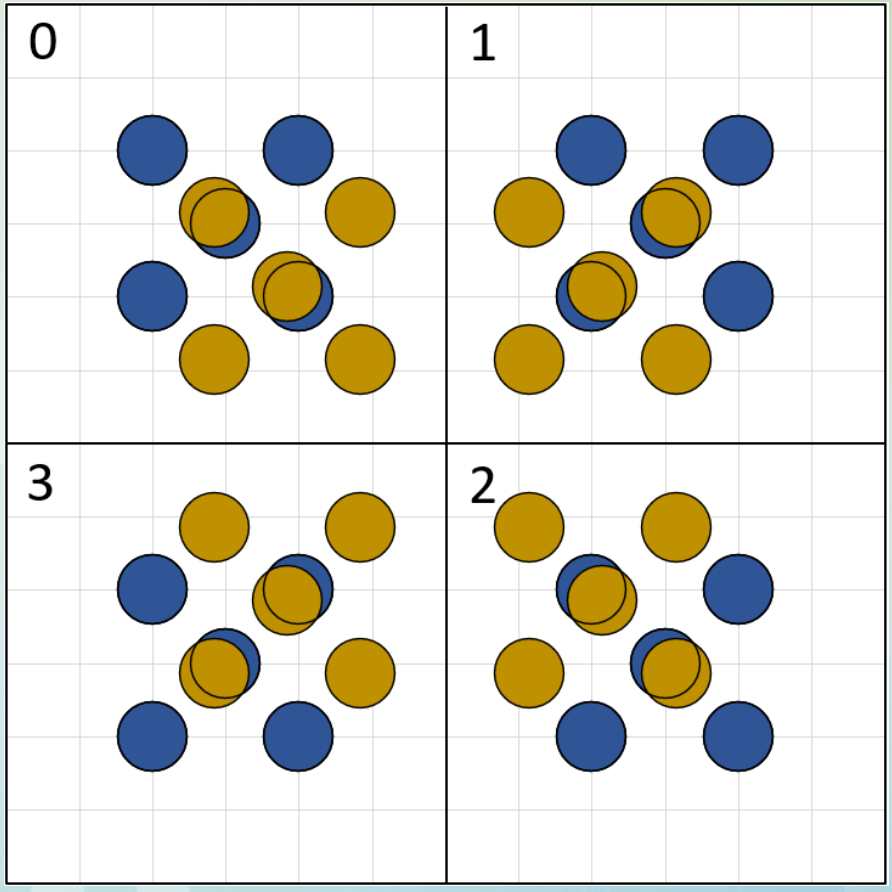
- **Objective:**
  - Validate if simulations and optimized processing predict final co-alignment
- **Summary of Results:**
  - Model shows uniform radial offset beyond spec range

Alignment Results

DUT	Location	Dispo
0	TL	FAIL
1	TR	FAIL
2	BR	FAIL
3	BL	FAIL

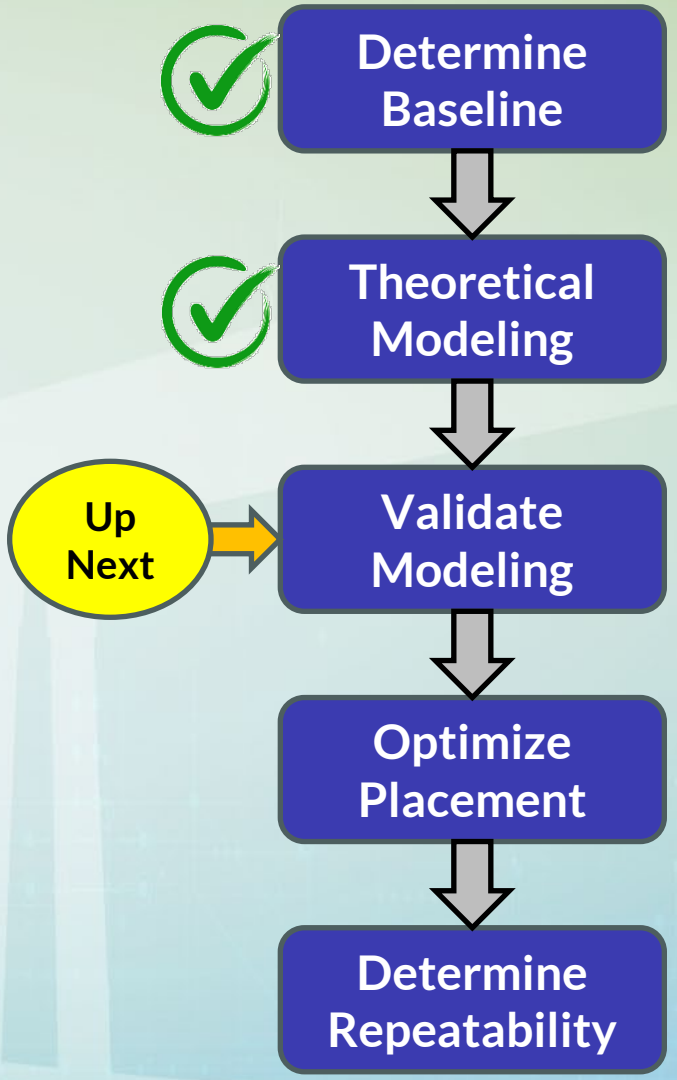
Nominal
Theoretical

Theoretical Co-alignment Results



Multi-Package Substrate Placement Challenges
- Can we predict misalignment with thermal modeling?

- **Key Take-Away :**
  - Multi-substrate assemblies need added process control to maintain co-alignment
  - Assembly process induces directional shifts that affect final alignment.
- **Next Steps:**
  - Empirically validate if the optimized control strategy accurately predicts final alignment
  - Use experimental data to identify and address remaining process gaps



Multi-Package Substrate Placement Challenges
- Can a modified process approach improve co-alignment?

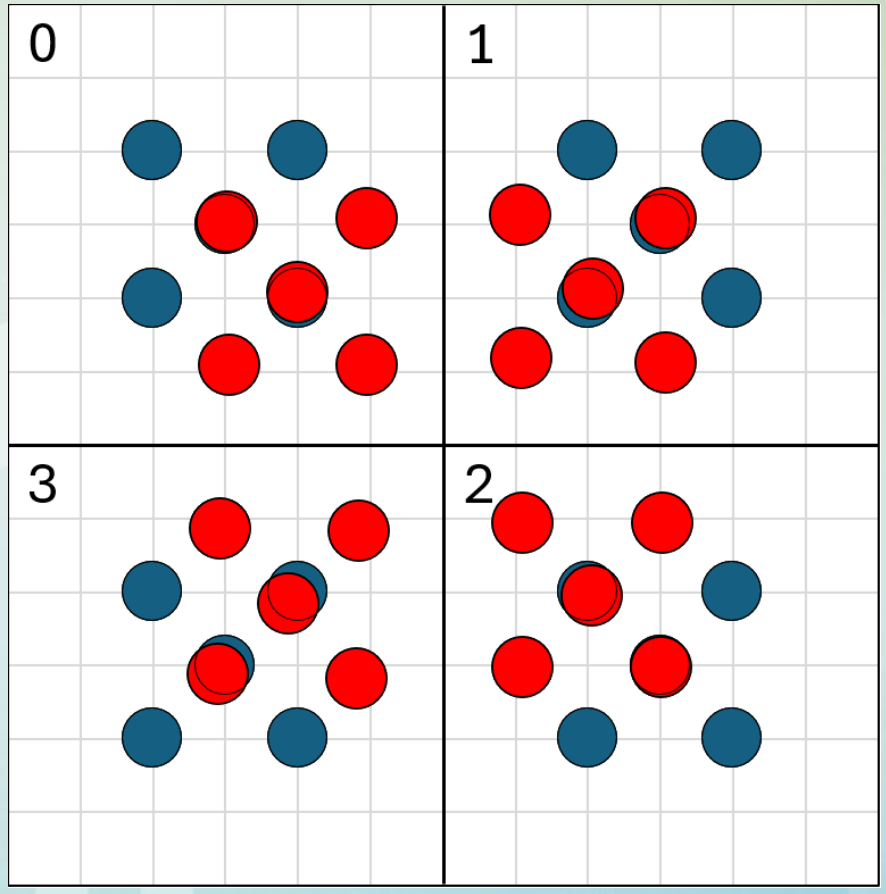
- **What is the Gameplan?**
  - Control key assembly factors to replicate modeled results
  - Design for consistent outcomes with process control and adaptability
- **Summary of Results:**
  - Co-alignment was repeatable
  - Radial shift aligned with model predictions.

Alignment Results

DUT	Location	Dispo
0	TL	FAIL
1	TR	FAIL
2	BR	FAIL
3	BL	FAIL

Nominal
Measured

Co-alignment Results



Multi-Package Substrate Placement Challenges
- How well did the thermal modeling predict substrate placement?

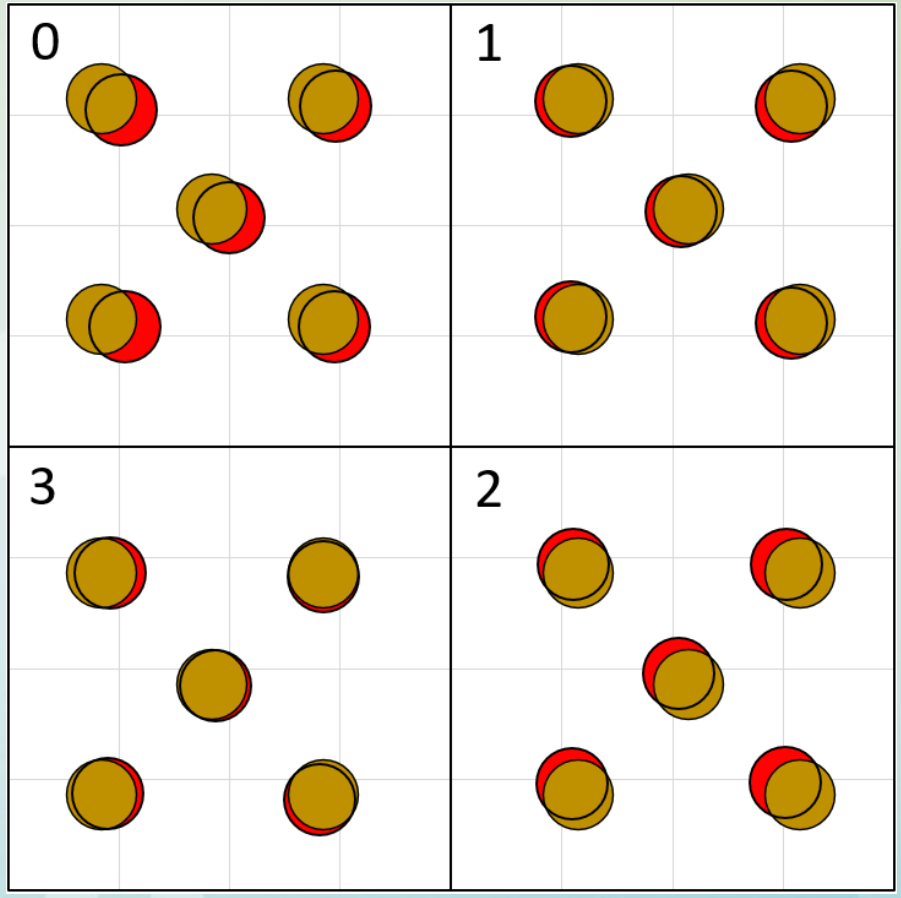
- **Key Take-Away:**
  - Simulation aligned with measured results with tolerance range.
  - Model accuracy validated for real-world assemblies.

Alignment Results

DUT	Location	Dispo
0	TL	PASS
1	TR	PASS
2	BR	PASS
3	BL	PASS

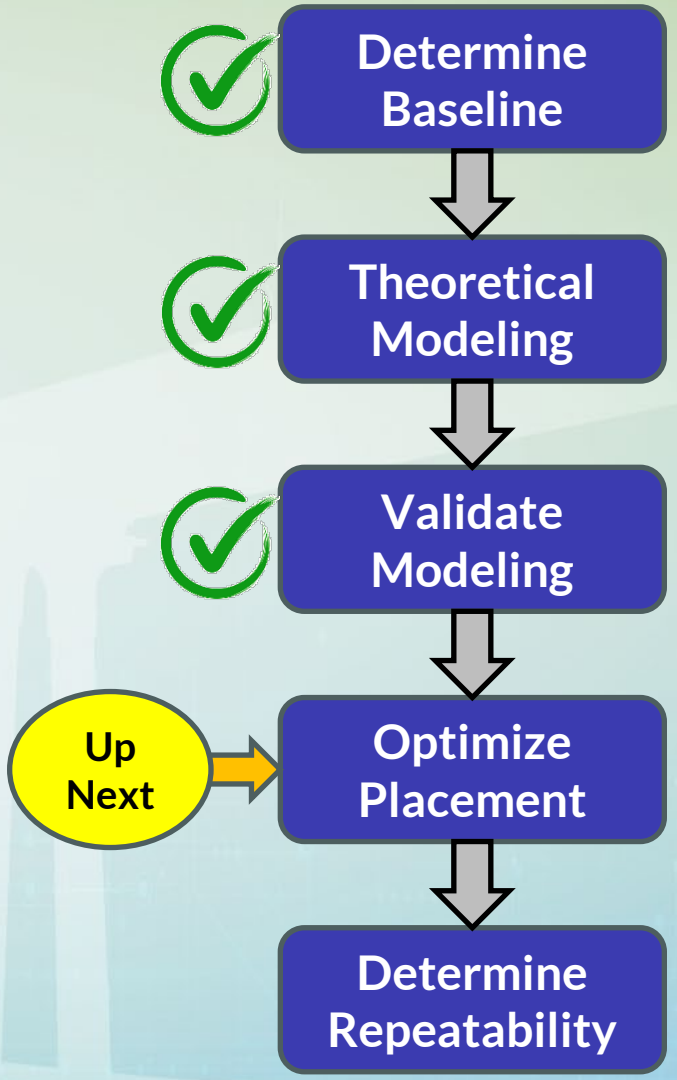
Theoretical
Measured

Theoretical vs. Actual



Multi-Package Substrate Placement Challenges
- Can we predict misalignment with thermal modeling?

- **Assumptions:**
  - In-line processing induces positional drift at final assembly.
  - Empirical results confirm simulation-predicted behavior.
- **Next Steps:**
  - Refine process setup and parameters to minimize drift.
  - Control positional variation.
  - Improve final placement accuracy.



Multi-Package Substrate Placement Challenges
- Does the optimizing process setup meet co-alignment requirements?

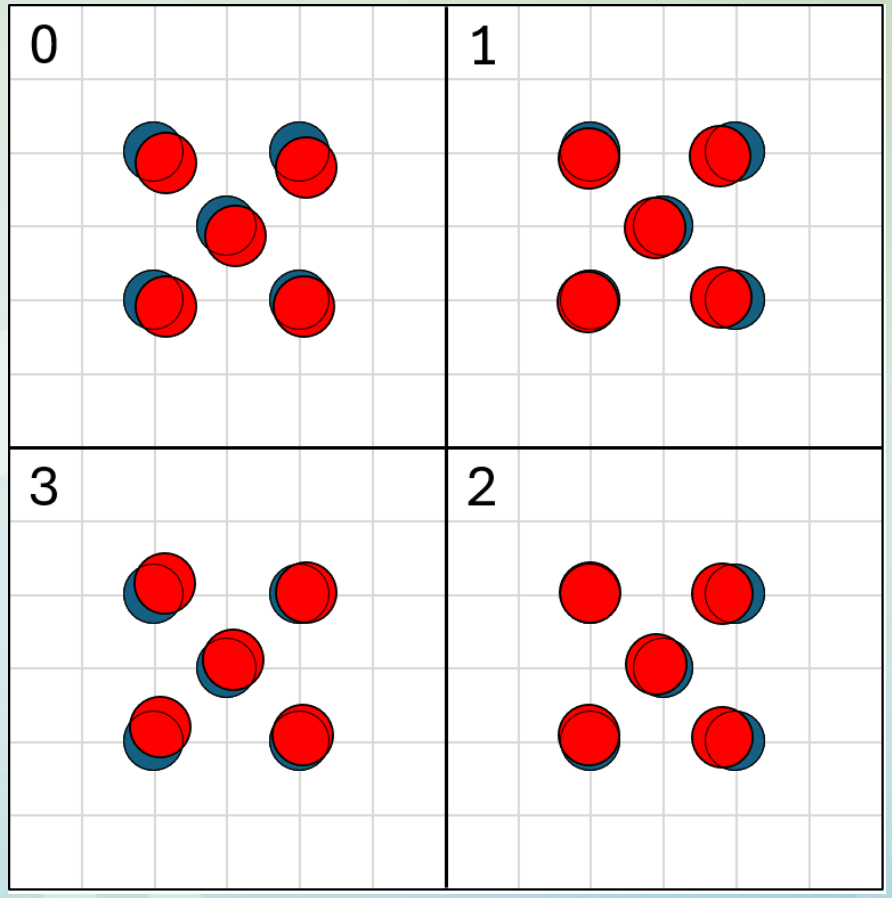
- **Objective:**
  - Confirm if the optimized process produces required co-alignment results
- **Summary of Results:**
  - Co-alignment at final assembly is well within spec

Alignment Results

DUT	Location	Dispo
0	TL	PASS
1	TR	PASS
2	BR	PASS
3	BL	PASS

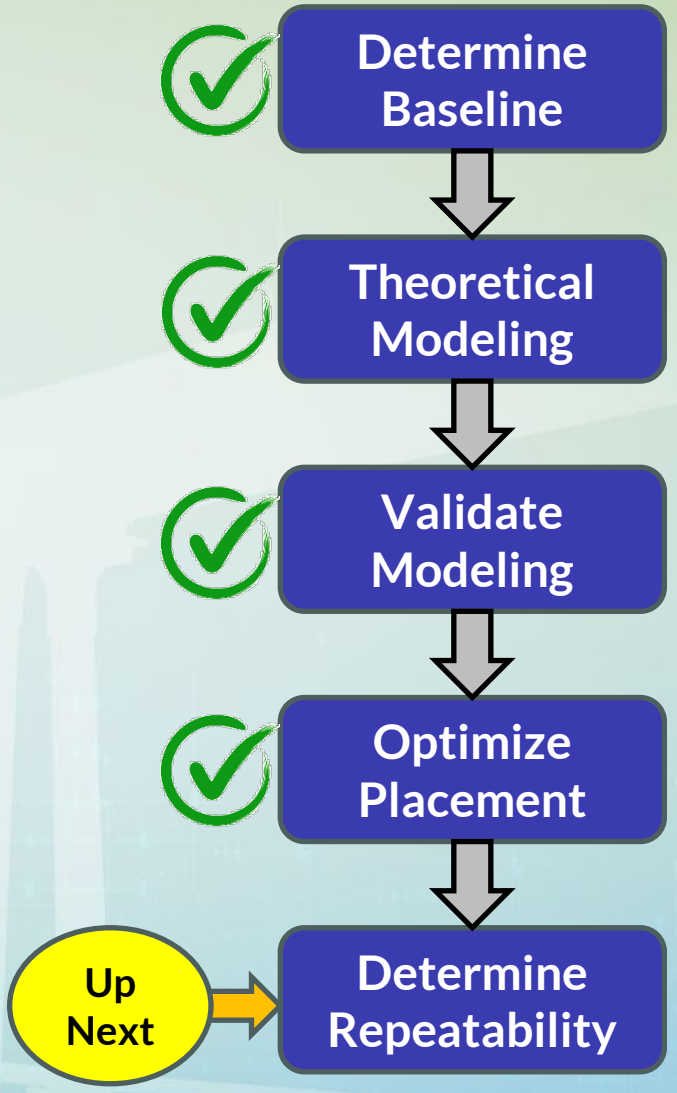
Nominal
Measured

Co-alignment Results



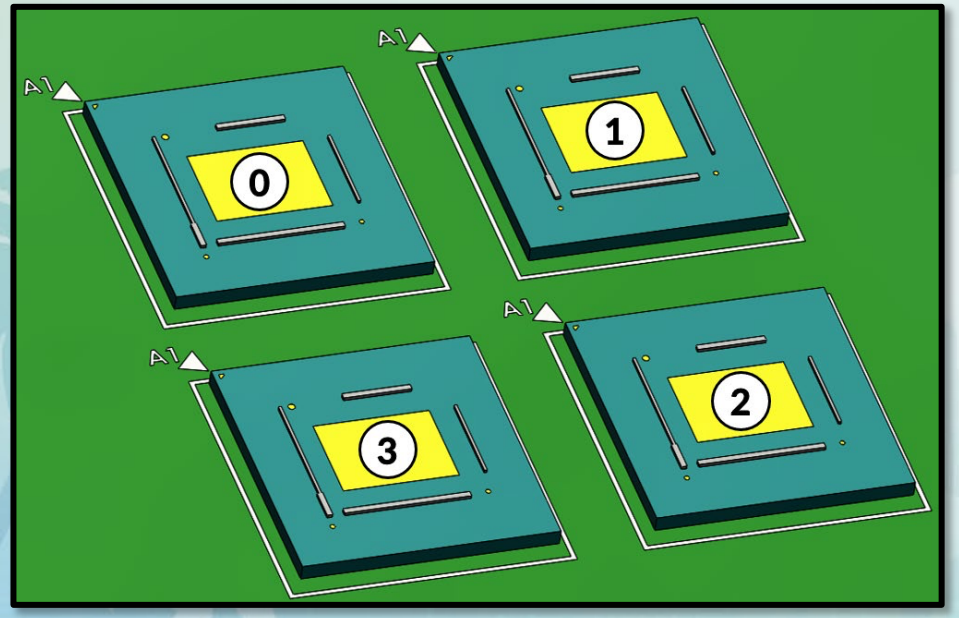
Multi-Package Substrate Placement Challenges
- Can we compensate misalignment with the optimized process setup?

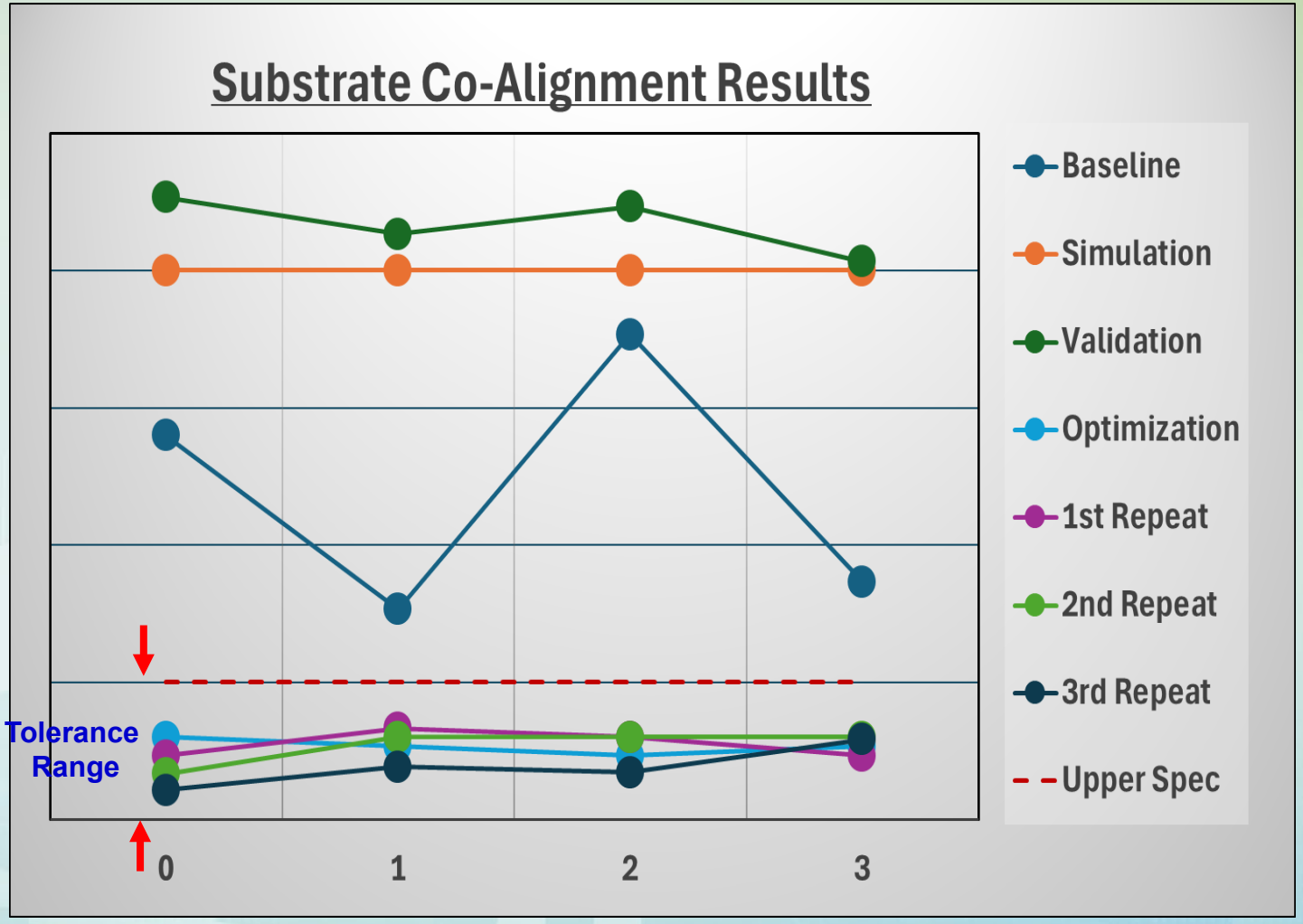
- **Key Take-Away :**
  - Optimized setup reliably manages variation and achieves co-alignment within tolerance range.
- **Next Steps:**
  - Conduct repeatability study



Multi-Package Substrate Placement Challenges
- How repeatable was the optimized solution?

- **Key Take-Away:**
  - Consistent alignment was achieved
  - Stable and repeatable results.





***Engineering test runs were converted to production product shipped to customer

Summary/Conclusion

- **Capability Assessment**
  - Baseline evaluation identified areas to improve process control for co-alignment
  - A predictive model guided process optimization and alignment assessment
  - Experimental validation confirmed the model's effectiveness for multi-substrate applications
- **Concept to Product**
  - Process refinement led to consistent, repeatable co-alignment results
  - Outcome builds confidence in the updated setup for future builds
- **Customer Commitment**
  - FFI successfully delivered a validated solution on time to meet customer needs

Acknowledgements

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Martin Hinajosa
Sr. Manufacturing Specialist
PC Assembly Support

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Director, Mechanical Design Engineering
Mechanical Design

Andy Kontic
Manager, Manufacturing Engineering
Pick and Place & Reflow Development

Robert Mendoza
Sr. Principal, Product Engineer
Feasibility

Mike Stadt
Sr. Principal Applications Engineer
Customer Interface

Thank You