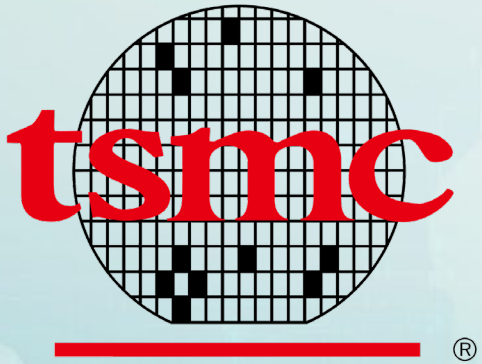
SWTEST
PROBE TODAY, FOR TOMORROW
2025 CONFERENCE

Effective Solutions for Large Form Factor Testing Challenges in High Parallelism HPC Device Testing



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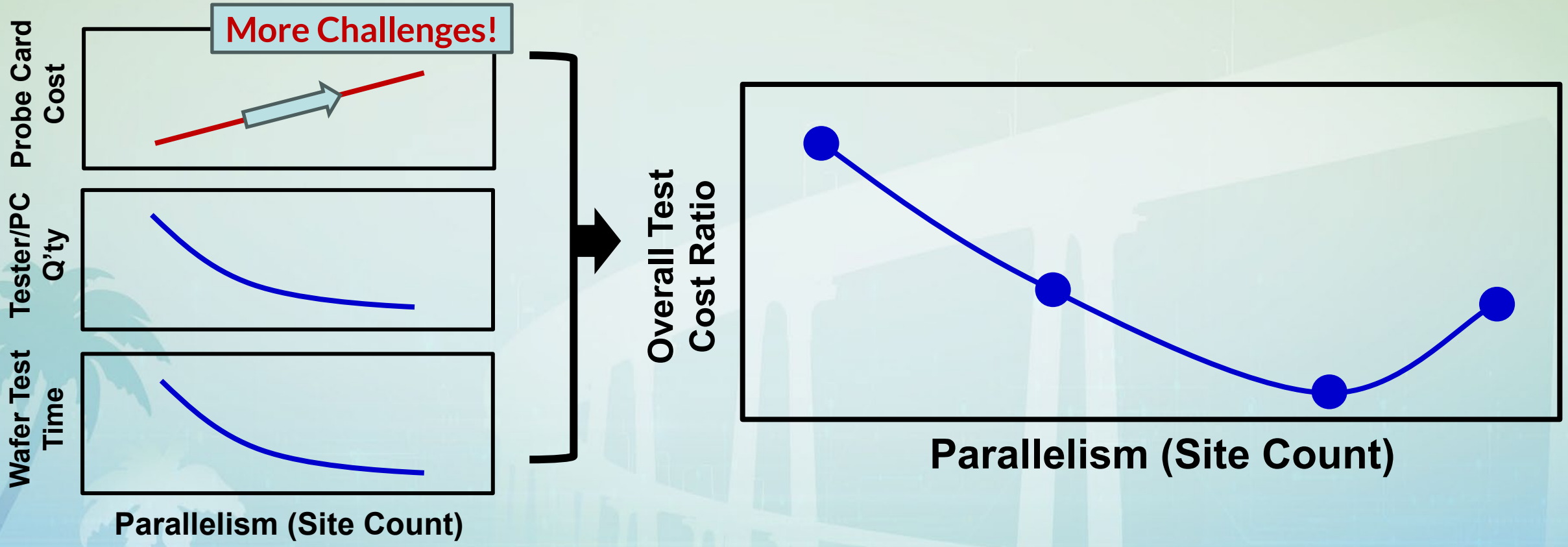
Oscar Lee

Overview

- Introduction
- What's the Challenges and How to Solve?
  - High Pin Count
  - Large Probing Area
  - Thermal
- Summary

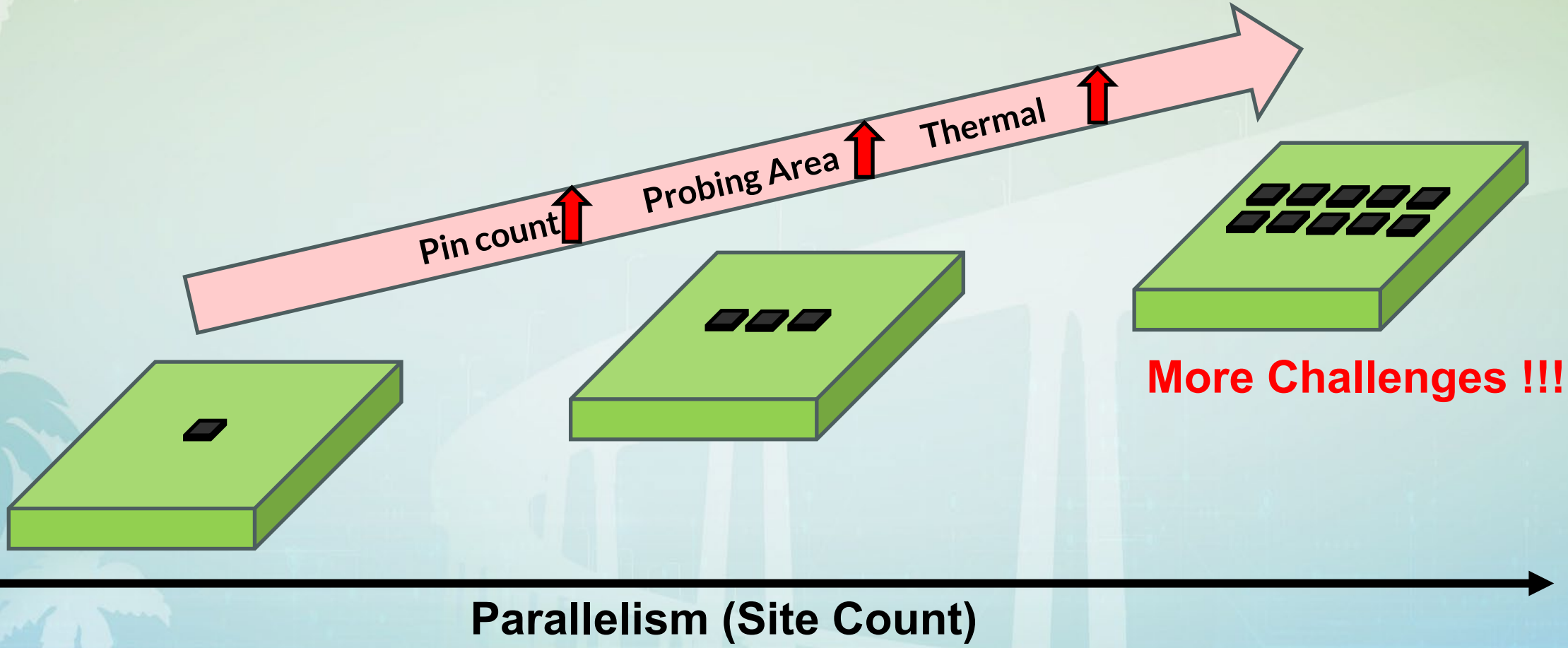
Introduction

- Why High Parallelism?
  - Time is Money. Find the sweet point design.



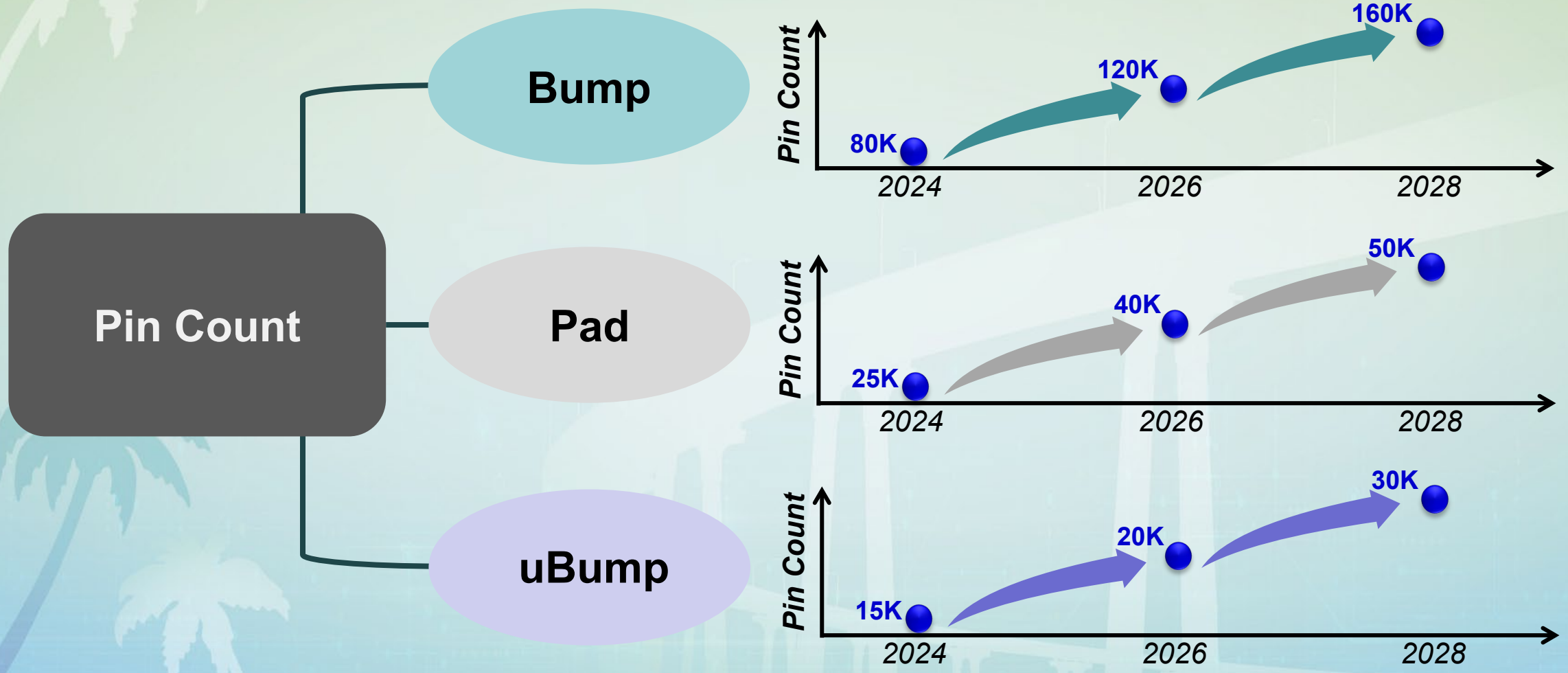
What's the Challenges in High Parallelism?

- Pin count, probing area, and thermal will increase with high parallelism.



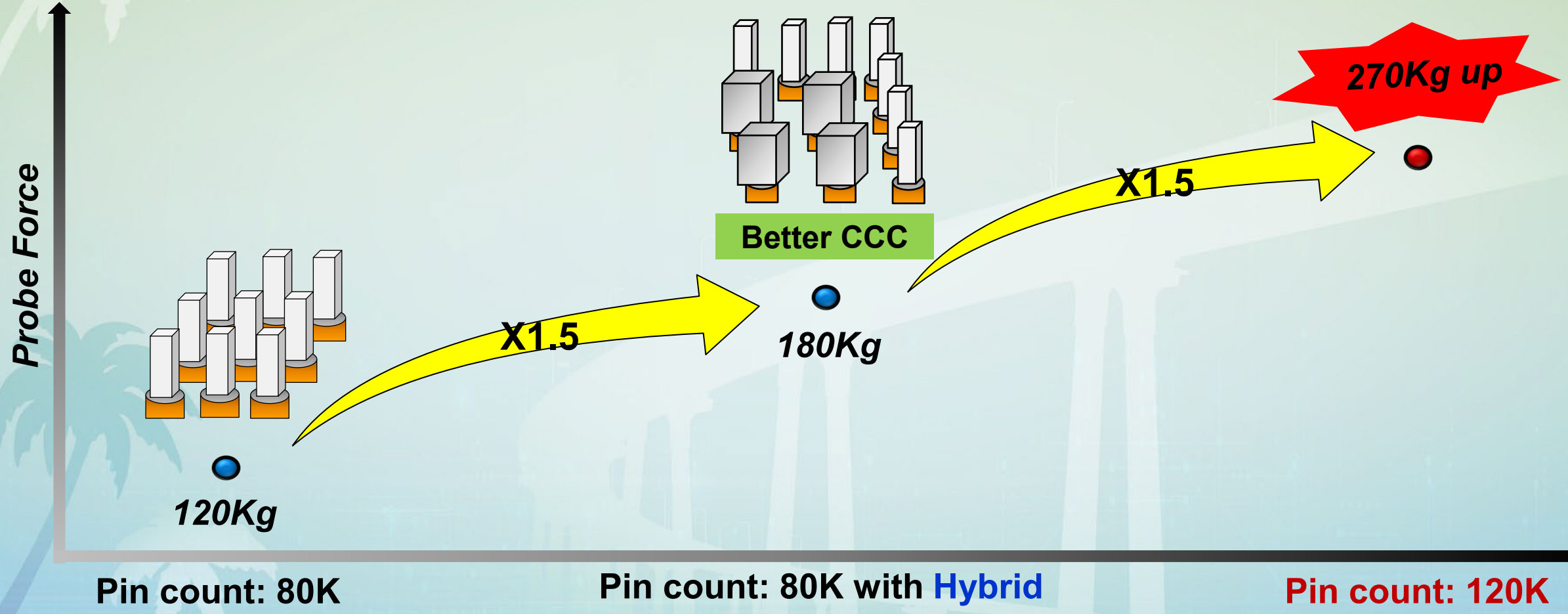
Challenges 1 High Pin Count

- Bump device is still the device with highest pin count.



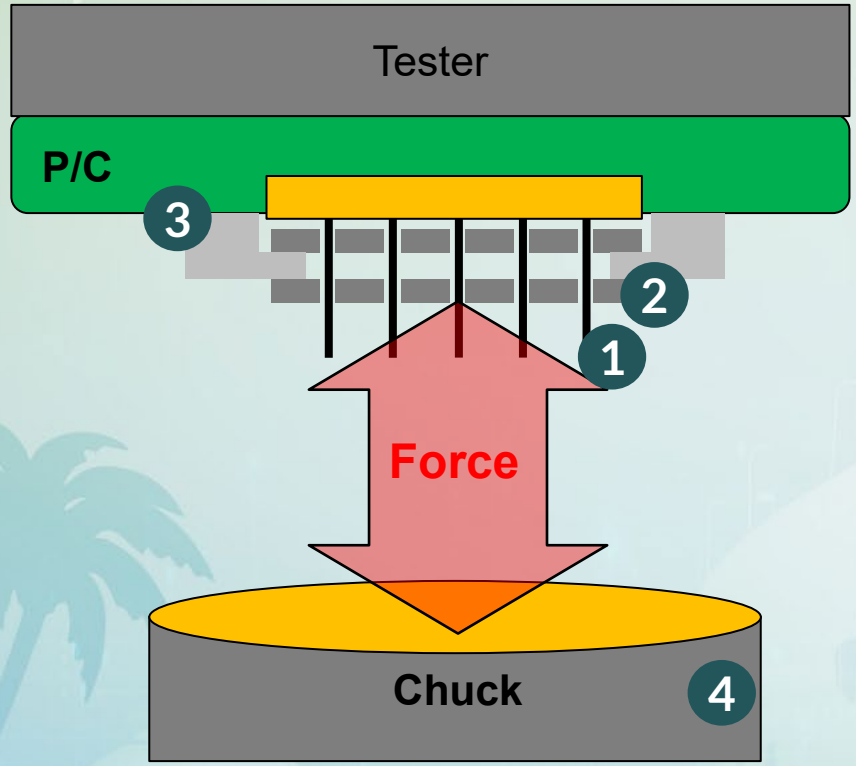
Challenges 1 High Pin Count

- The probe force will be up to 270Kg with 120K pin count.



Challenges 1 High Pin Count

- Developments to overcome high probe force.



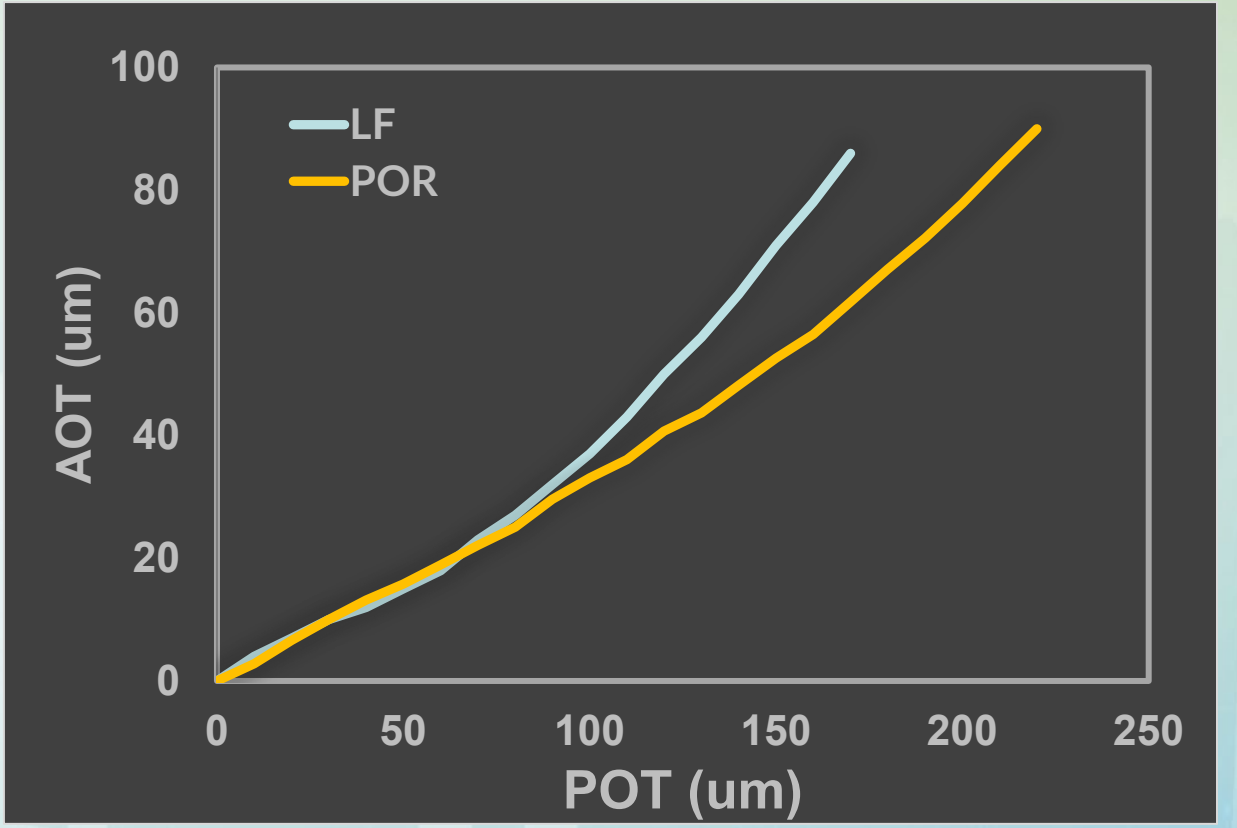
Category	Items
Probe Card	1 Low Force Probe Development
	2 Advanced Ceramic with High Strength
	3 Simulation & Probing Recipe
Tester/ Prober	4 Rigid Chuck/WAPP

Challenges 1 High Pin Count

- Develop low force probe to support higher pin count.

	Pitch 80 um	
Probe	POR	Low Force
Force	1.5 -27%	1.1
CCC	1	1.2

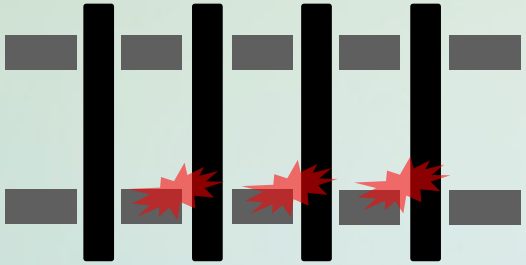
	Pitch 100 um	
Probe	POR	Low Force
Force	2 -25%	1.5
CCC	1.6	1.6



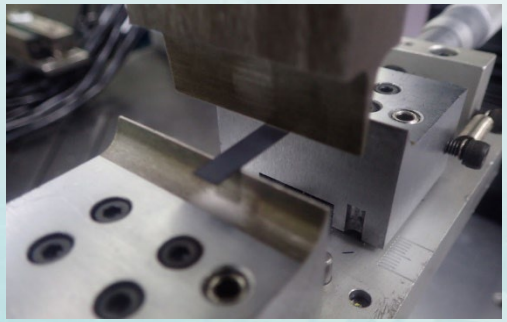
Challenges 1 High Pin Count

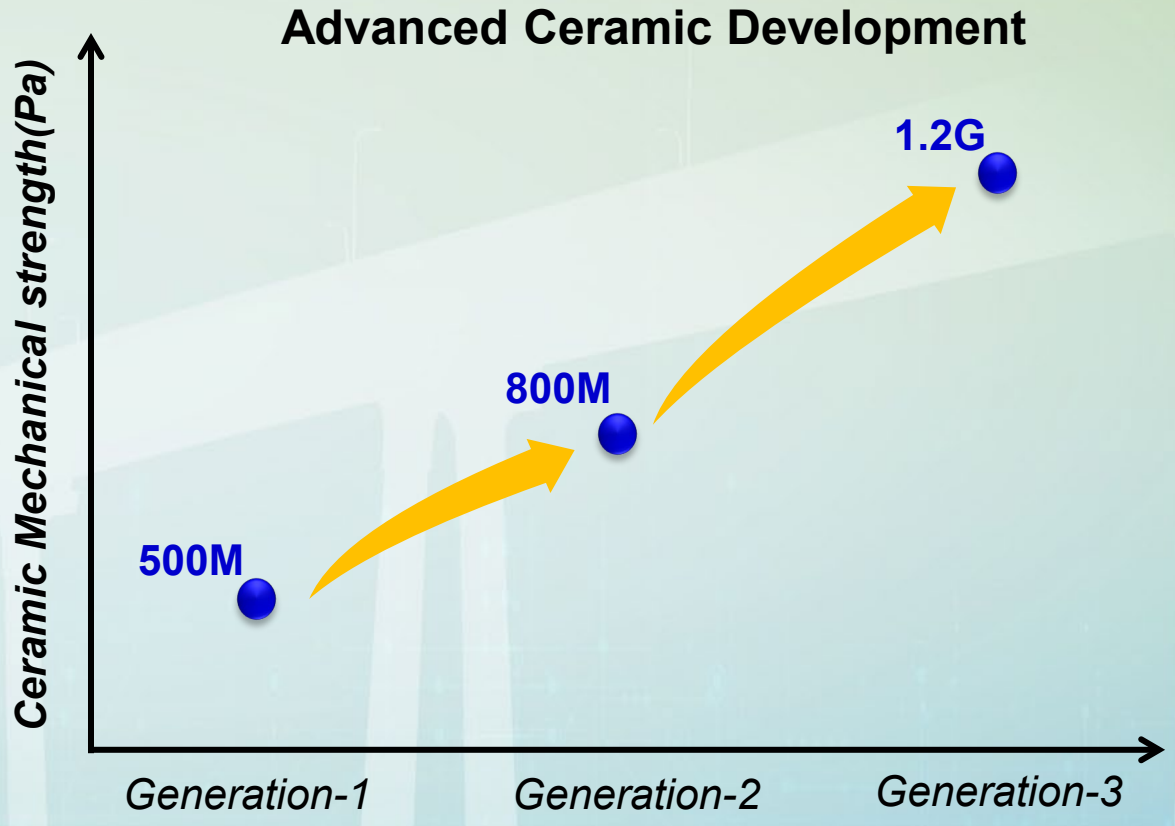
- Develop advanced ceramic to endure higher stress.

Ceramic crack due to high stress



Ceramic stress test

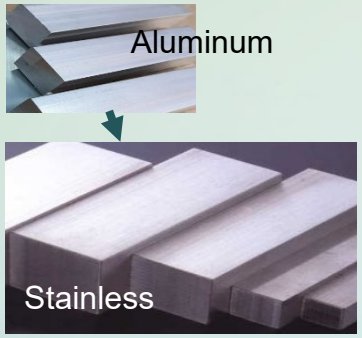


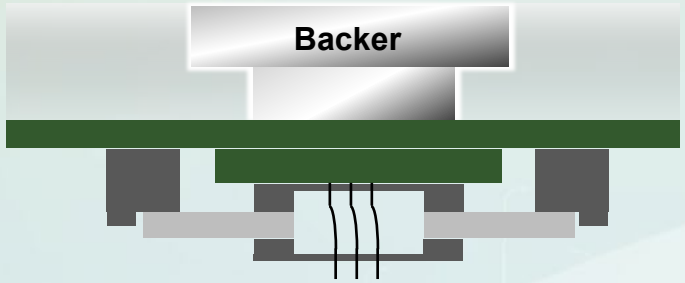


Challenges 1 High Pin Count

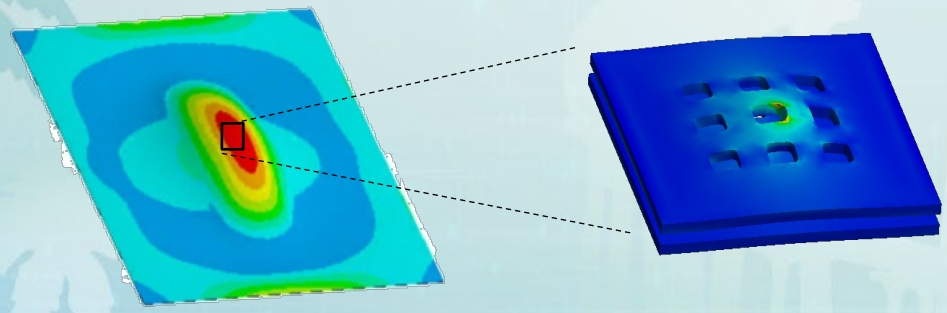
- Mechanical Simulation and Recipe Optimization

Material and Structure

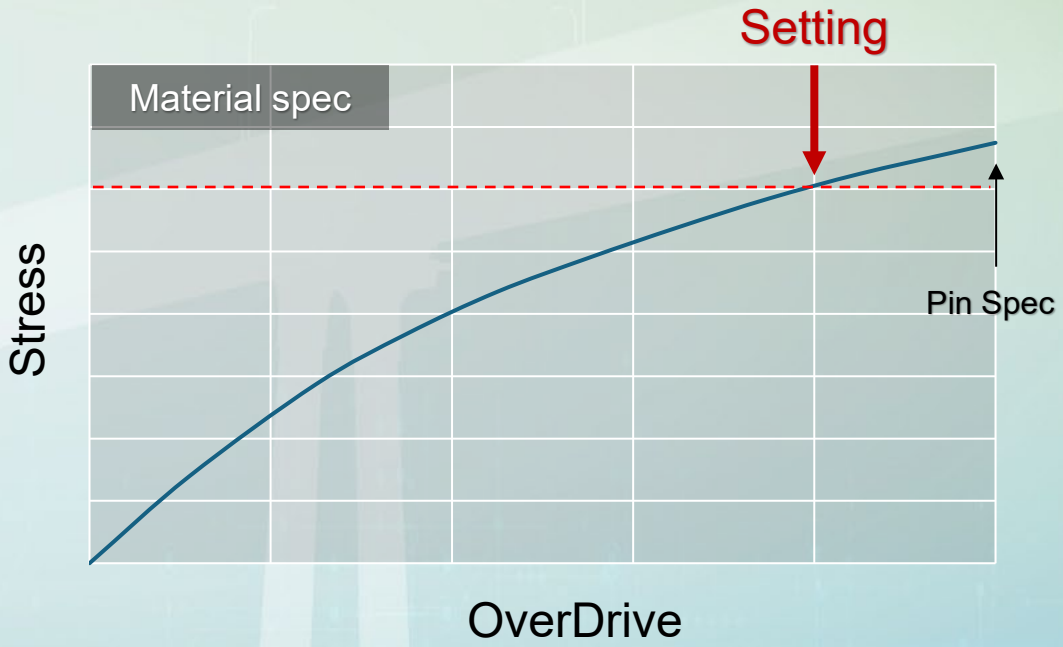




Stress Simulation



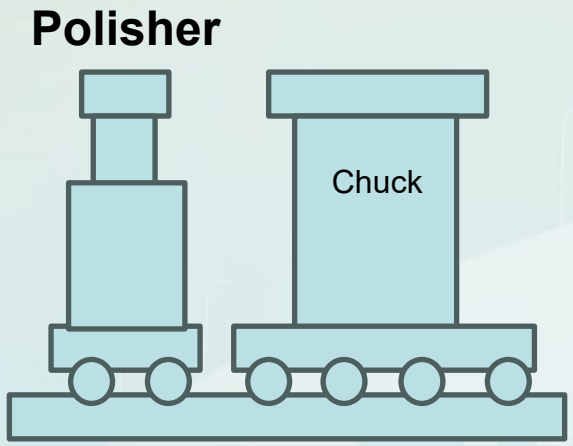
Recipe setting



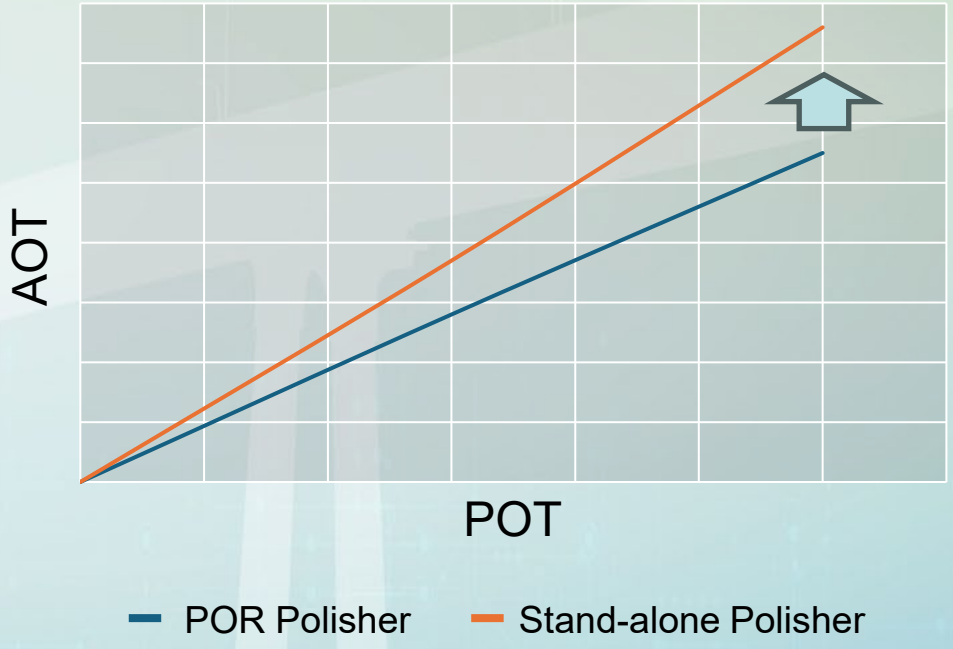
Challenges 1 High Pin Count

- Develop high rigid chuck/polisher to support higher pin count.
- Enhance ATE strength to minimize the offset.

Rigid Chuck

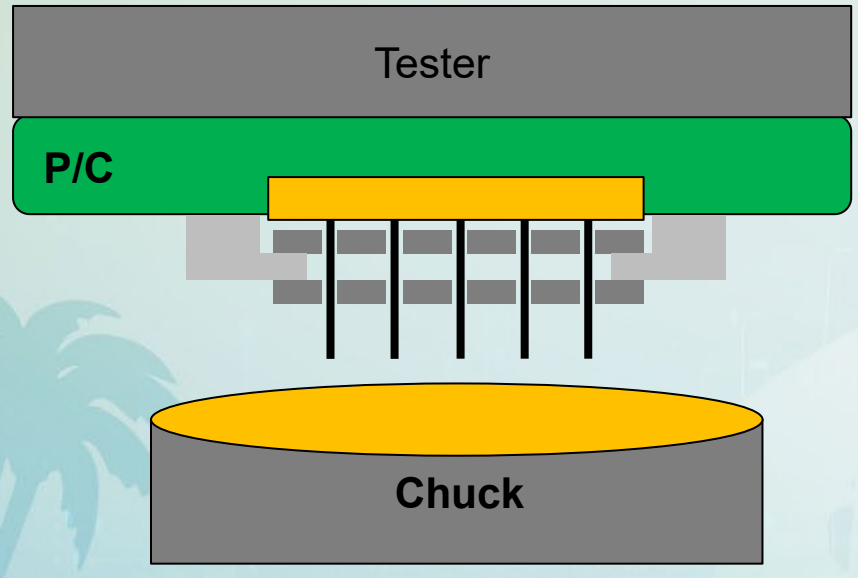


Stand-alone Polisher

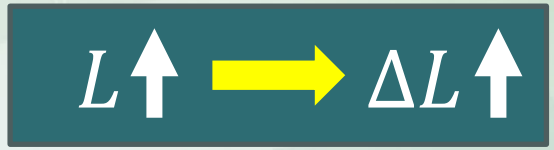


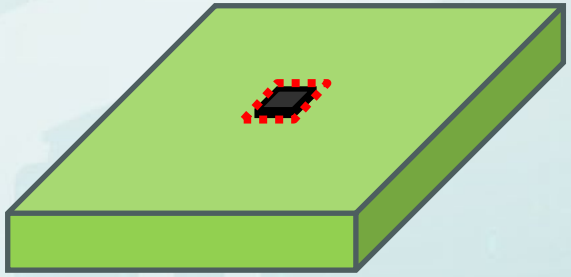
Challenges 2 Large Probing Area

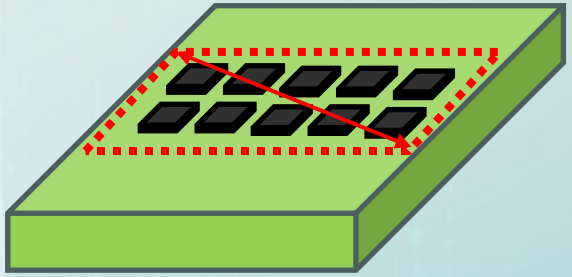
- The alignment between material interface is critical due to CTE (Coefficient of Thermal Expansion) difference , especially for high-parallelism probe card.



$$\Delta L = L \times \Delta T \times CTE$$







5 times L → 5 times ΔL !!!

Challenges 2 Large Probing Area

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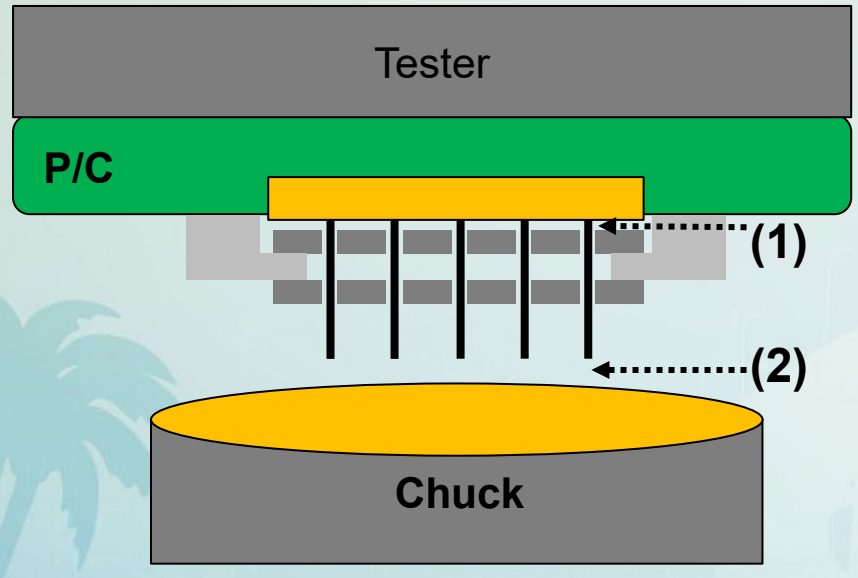
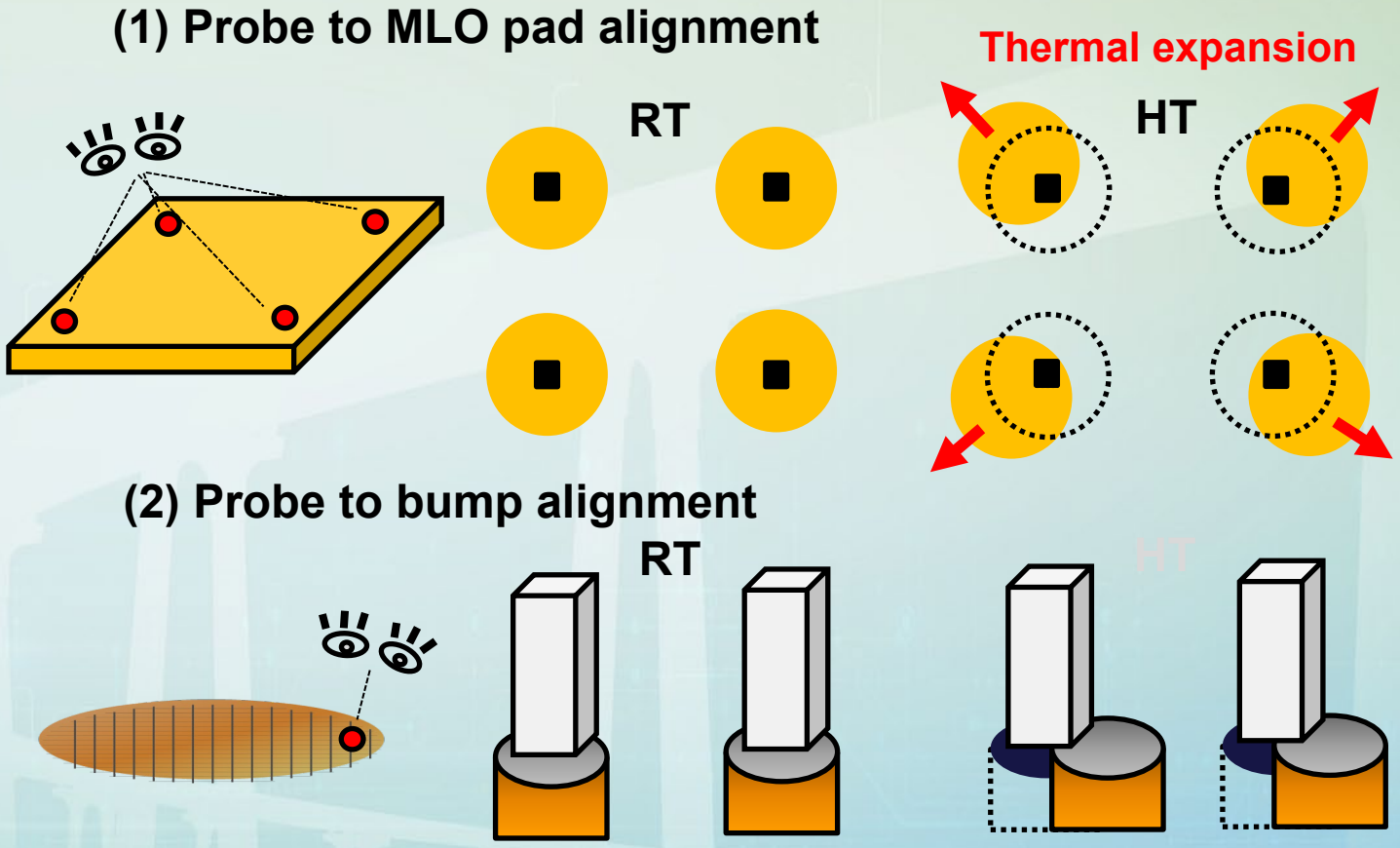
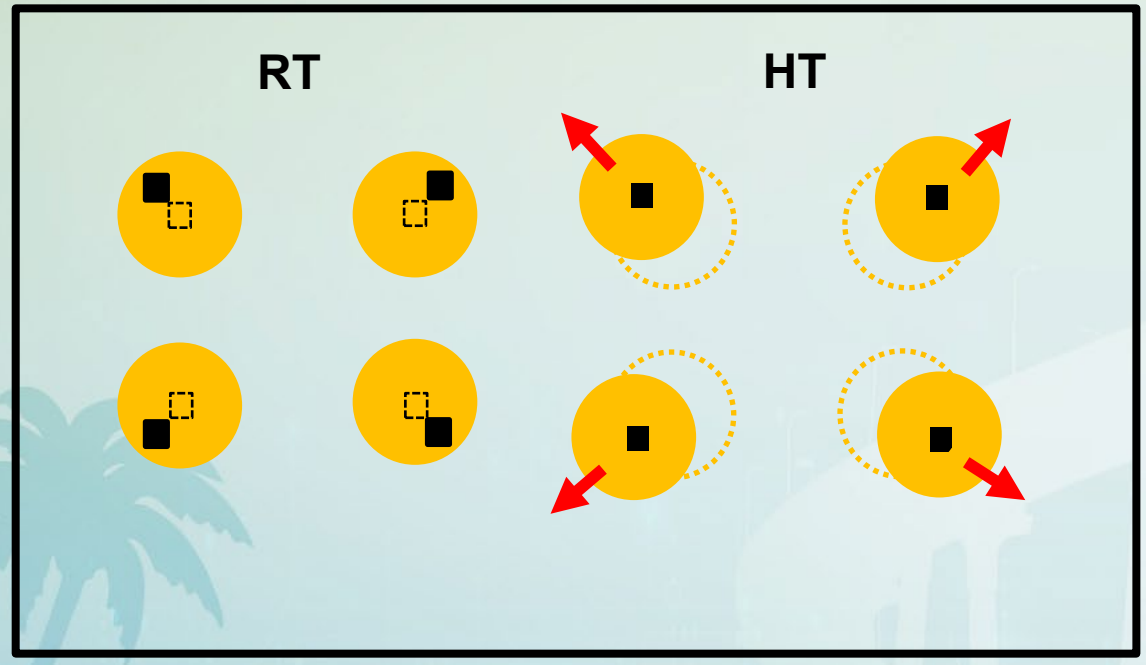


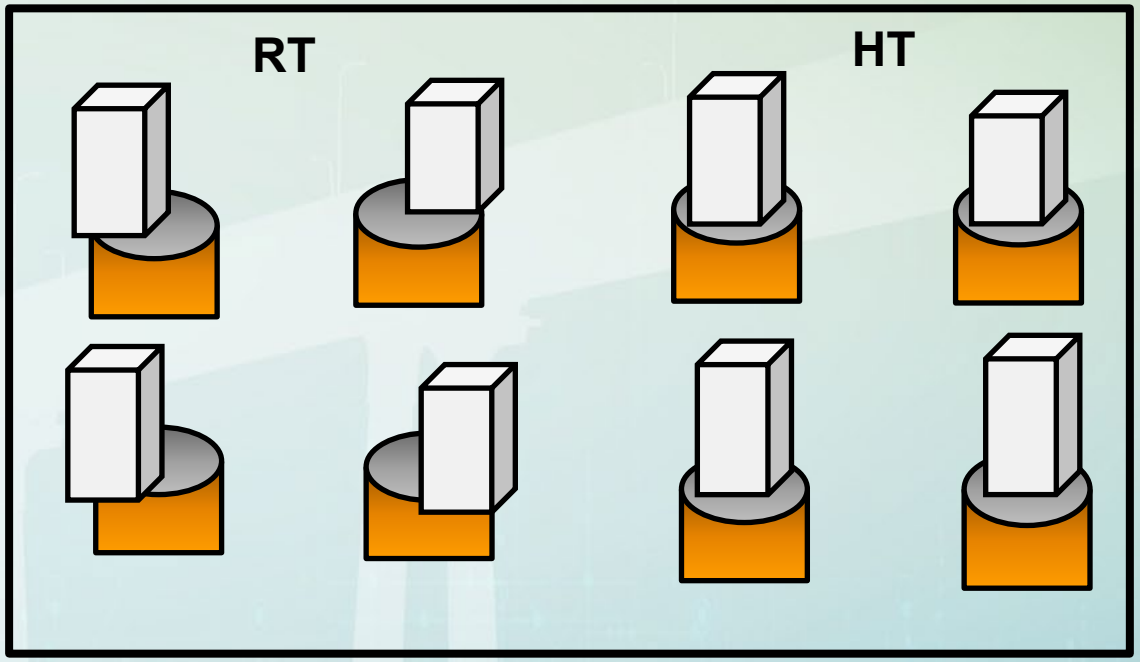


Challenges 2 Large Probing Area

- Scaling to compensate the expansion/shrinkage in advance in design phase.



Design scaled UD to compensate
Probe-to-MLO pad alignment

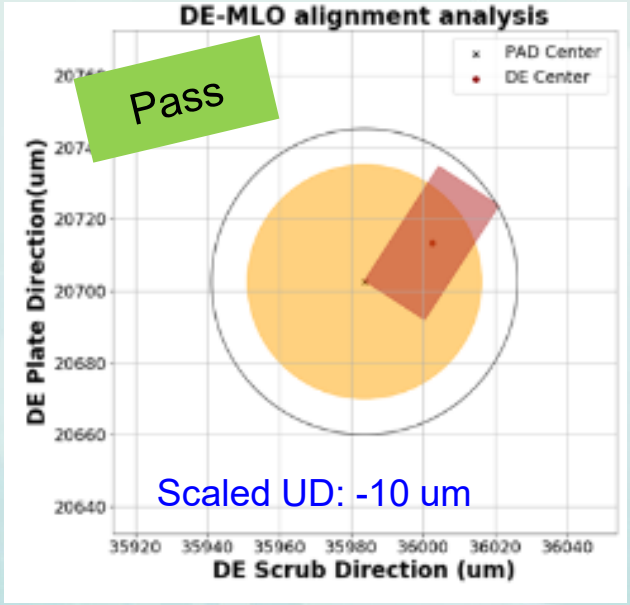
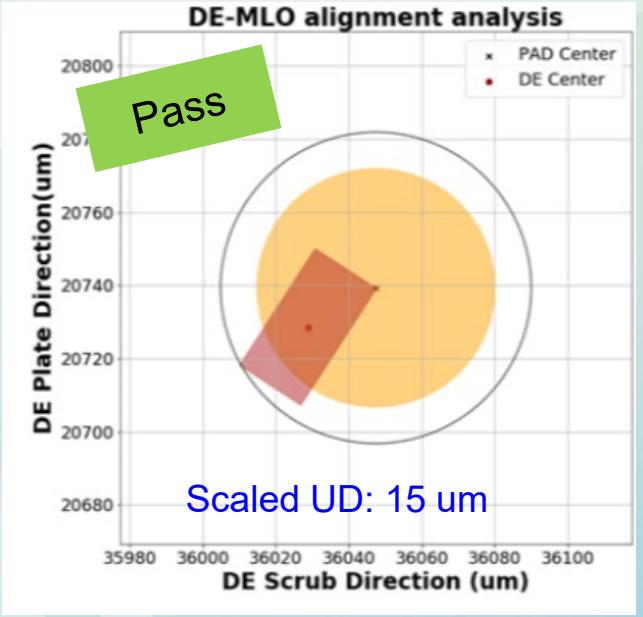


Design scaled LD to compensate
Probe-to-Bump alignment

Challenges 2 Large Probing Area

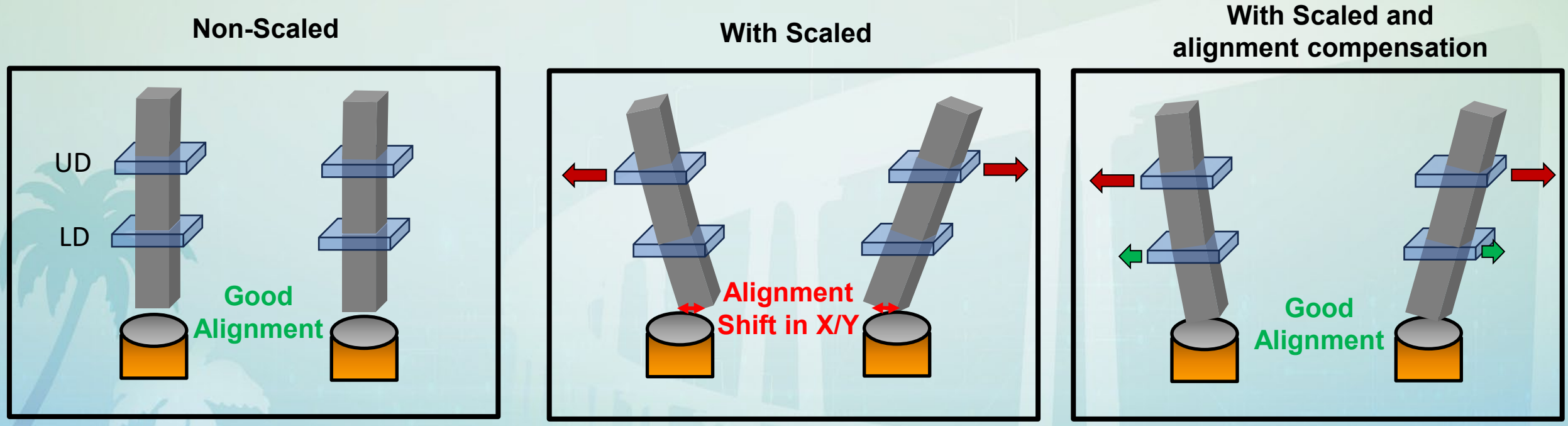
- Develop simulation tool to predict the alignment across temperature range.
- Separate P/C type for high & low temp testing.
  - Expansion/ Shrinkage scaling for high/low temp testing.

Simulation Condition
Temperature
Pitch
Pad size
Probing area
Probe type (DE size)
MLO manufacturing tolerance
MLO CTE
UD CTE
Define Scaled UD value

Low temp P/C	High temp P/C
	

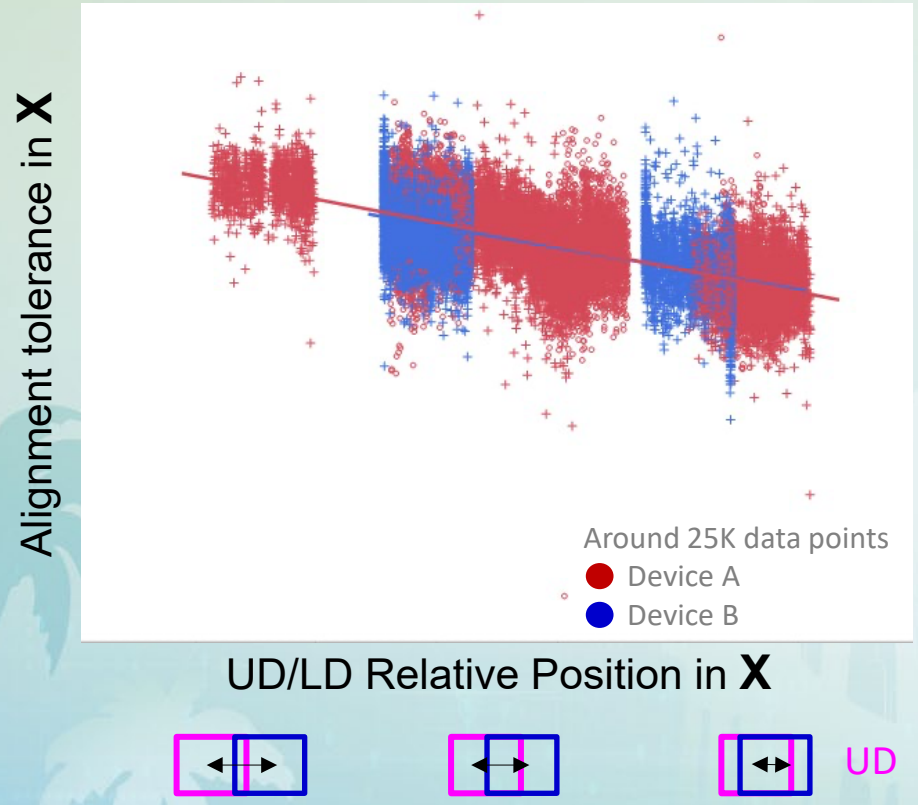
Challenges 2 Large Probing Area

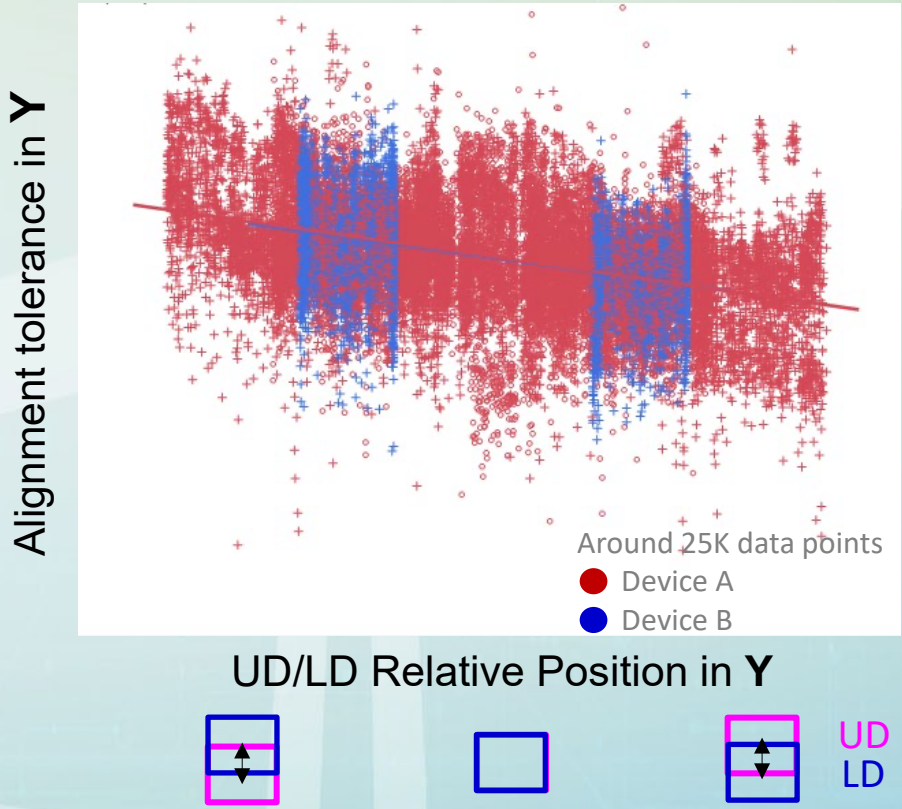
- With scaled UD, the alignment accuracy might shift due to probe tilt.
- The alignment accuracy can be compensated by scaling LD accordingly.



Challenges 2 Large Probing Area

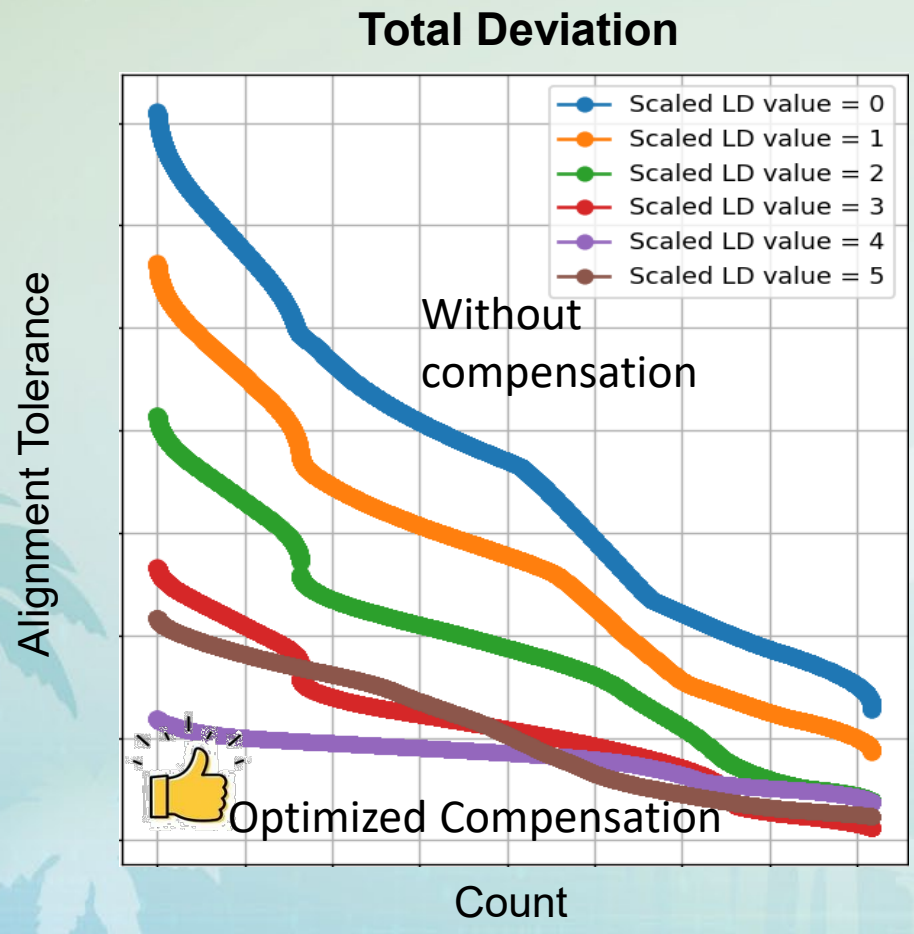
- The compensation value can be analyzed by high-volume alignment data.

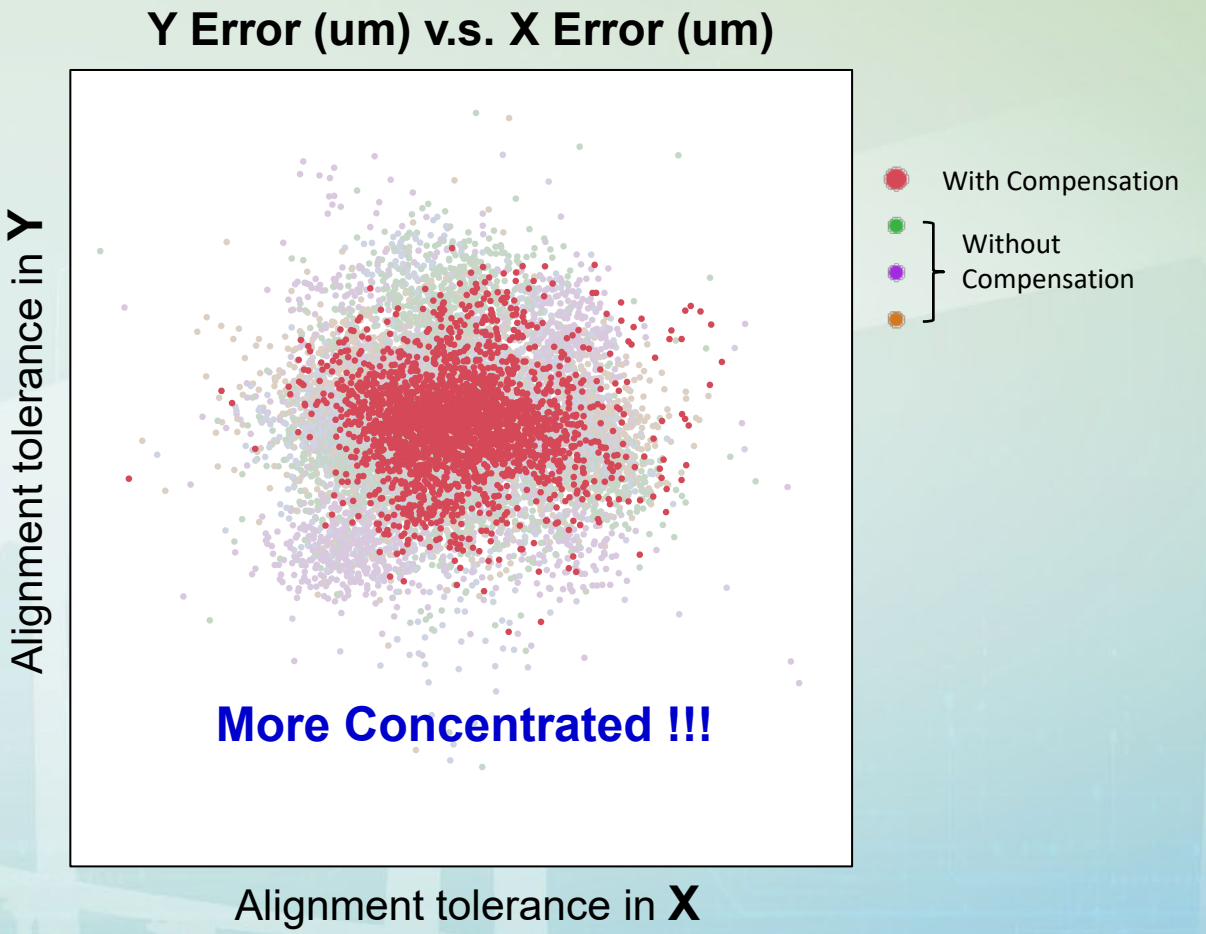




Challenges 2 Large Probing Area

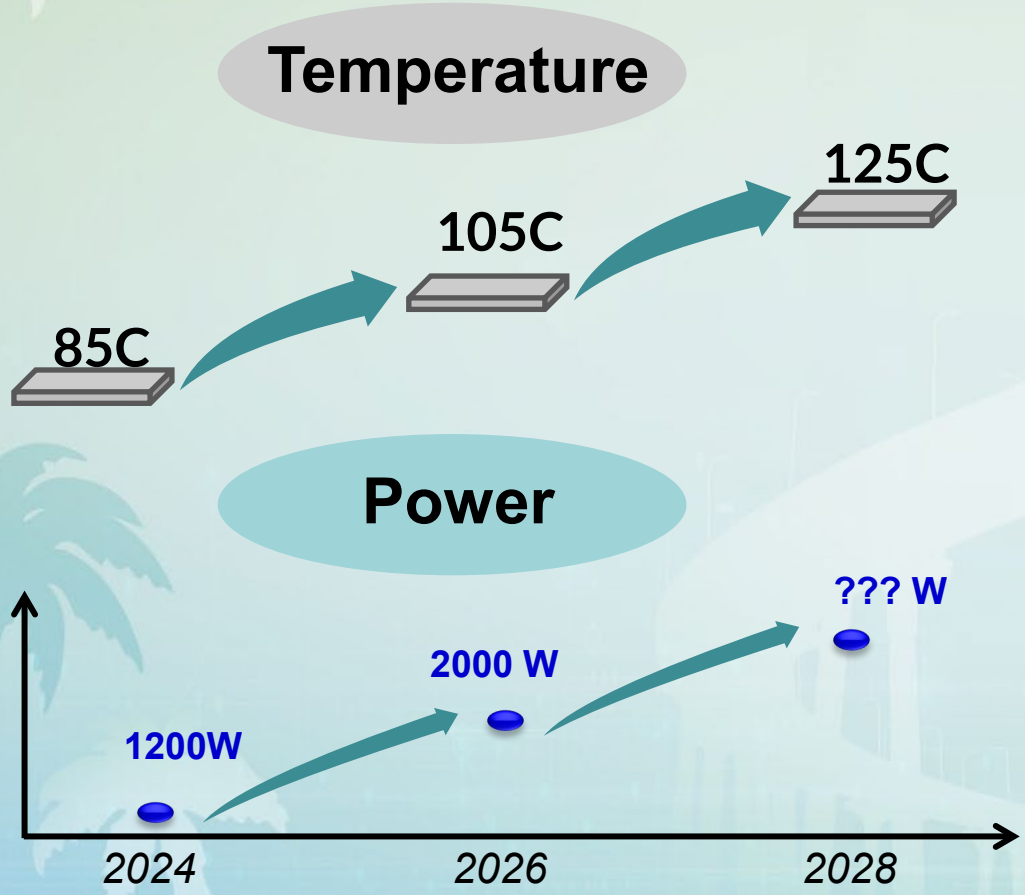
- With compensation, the alignment accuracy can be improved.

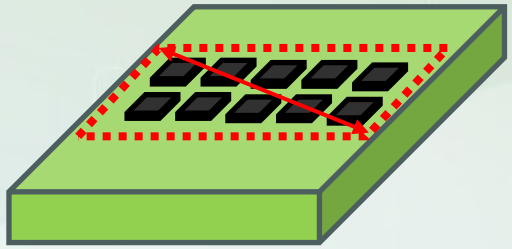




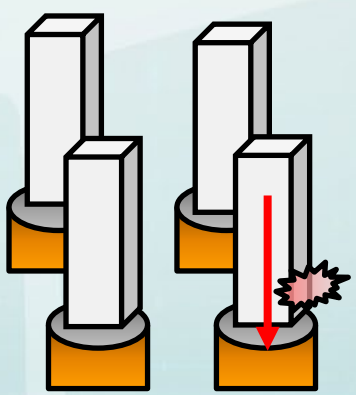
Challenges 3 Thermal Dissipation

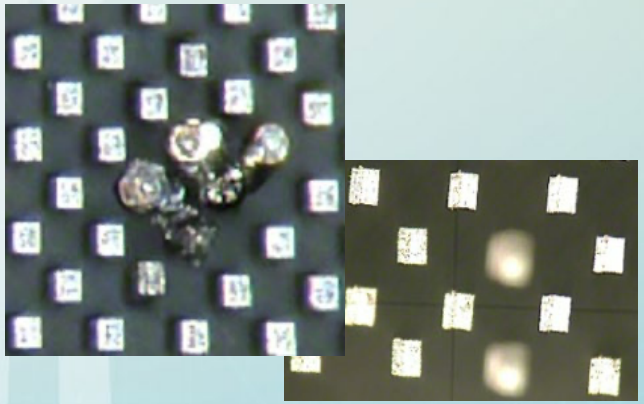
- As HPC grows rapidly, the test temperature and power consumption are increasing. High parallelism may cause larger thermal expansion and thermal accumulation resulting in tip burnt.





Thermal expansion

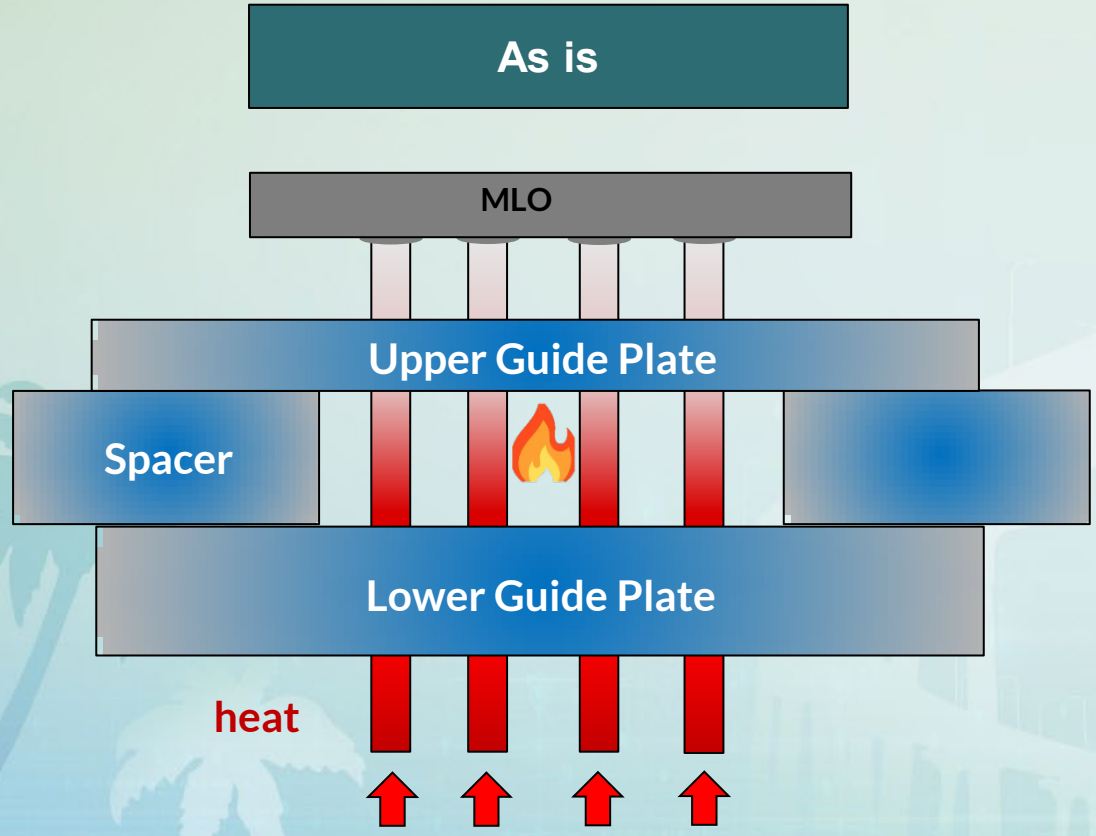


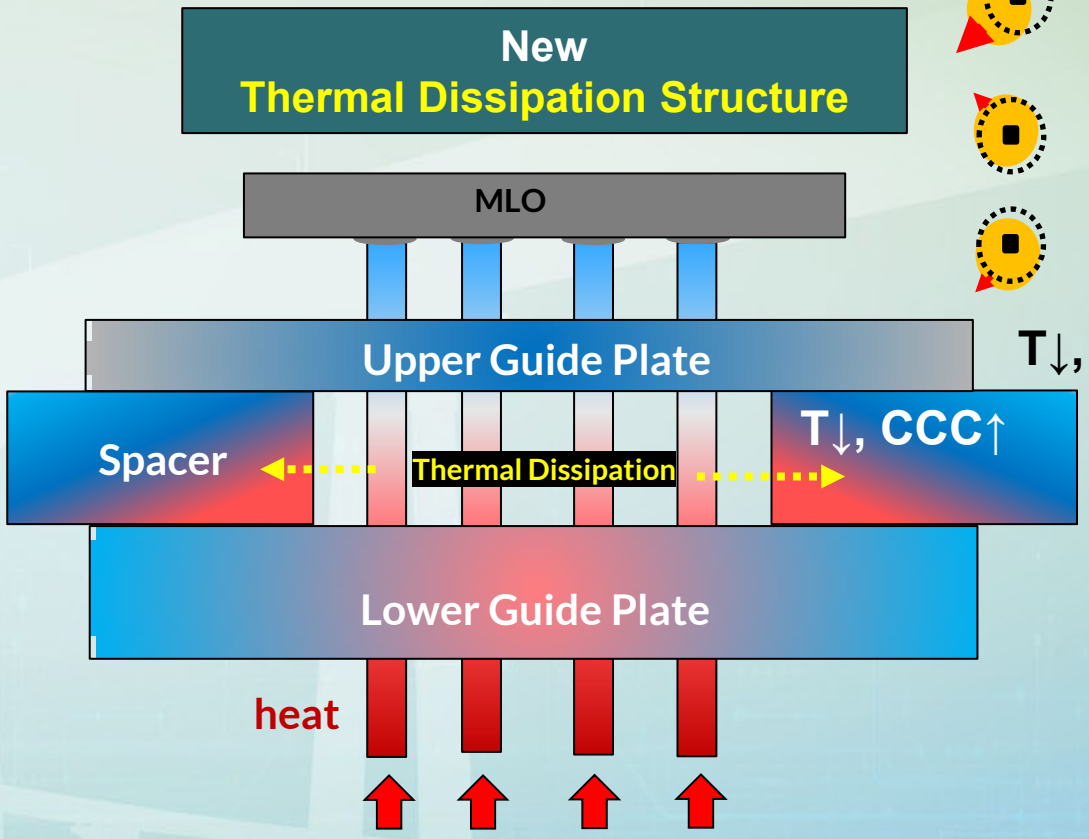


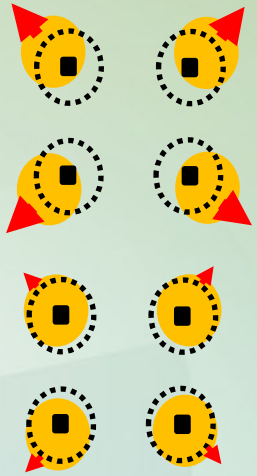
Current > CCC (Current Carrying Capability)

Challenges 3 Thermal Dissipation

- High thermal conductivity housing helps to dissipate heat. It improves CCC by >10%.







Summary

- Effective solutions are proposed to address the challenges posed by high-parallelism testing including high pin count, larger probing area, and thermal dissipation issue.
- With the development of low-force probe, high-strength ceramic, and probing recipe optimization, we overcame the challenges of high pin count testing.
- Alignment accuracy is crucial for large probing area P/C, and various solutions are provided to address this challenge.
- The innovative high thermal conductivity material enhances thermal dissipation, leading to improved probe CCC.