SWTEST
PROBE TODAY, FOR TOMORROW
2025 CONFERENCE

Enabling 100+ GHz Launches for 448G Signals

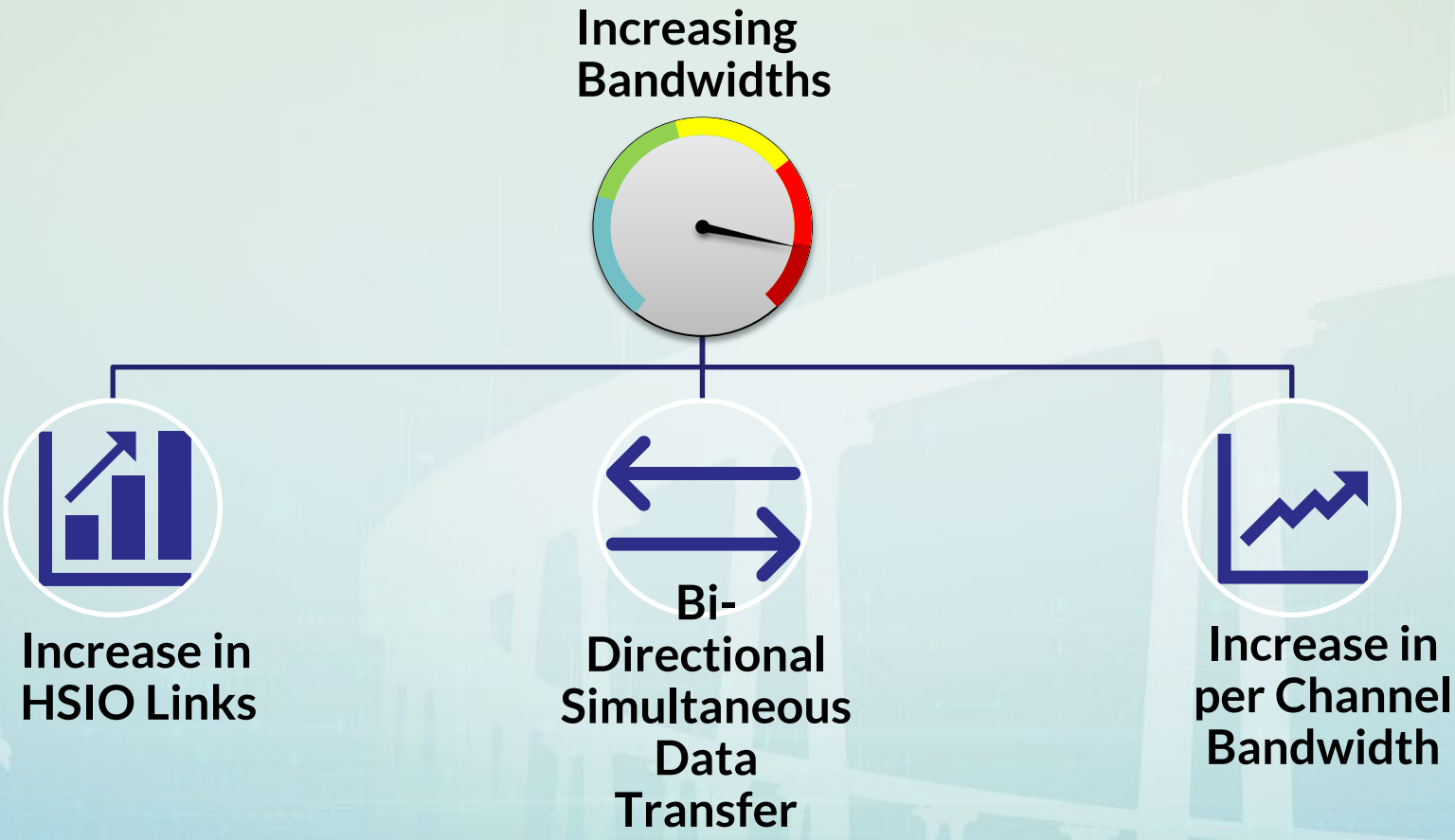
M. Hameem Ur Rahman/
Quaid Joher Furniturewala
R&D Altanova/Advantest

Agenda

- Exponential bandwidth progression
- 448G transmission
- 448G PCB launch challenges
- Through loss, reflected loss, phase and cross talk at higher frequencies
- Super structure: Special Probe via structure (IP)
- Test Vehicle
- Simulations
- Measured results / correlation
- Conclusion

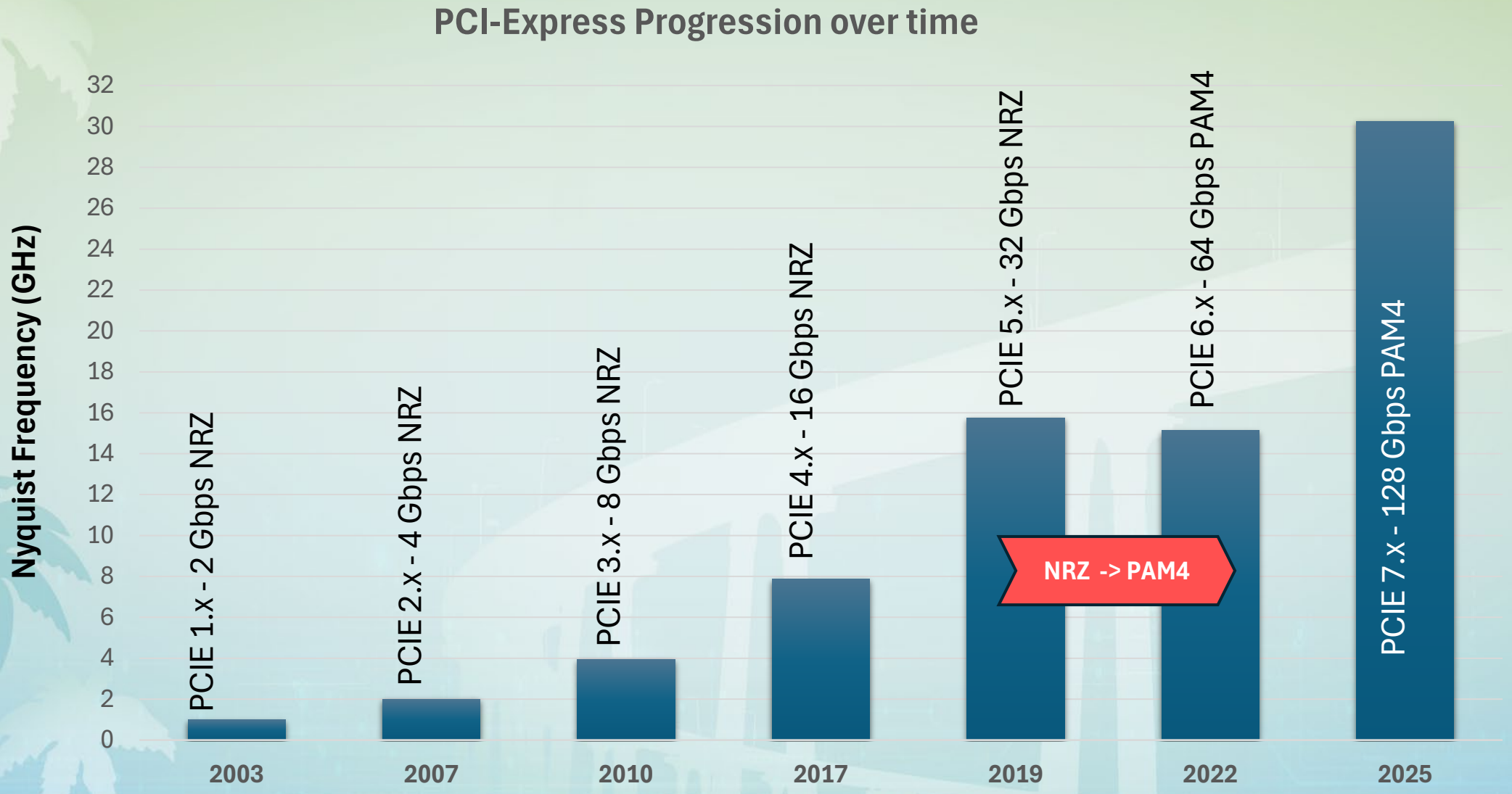
Exponential Bandwidth Growth

- ✓ Exponential growth in data transfer is seen in the last two decades
- ✓ 448G era for highspeed signal transfer is inevitable



NVLINK Bandwidth Progression

PCI-Express Bandwidth Progression



448G Transmission is a Challenge

448G

Discussion Topic!

PCB Technology

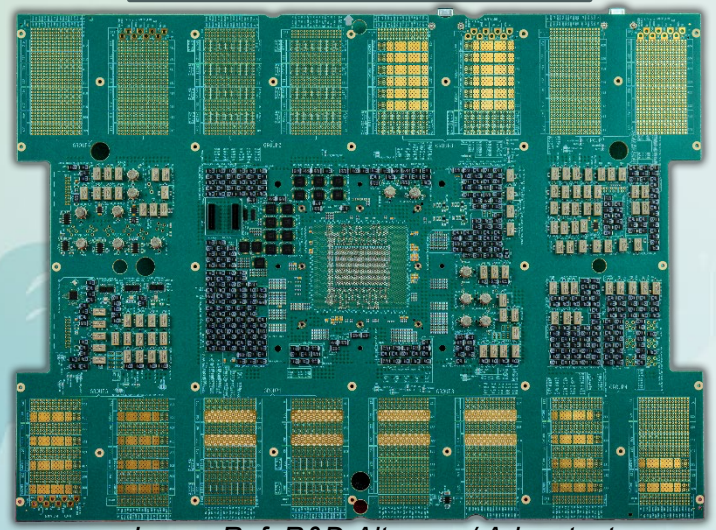


Image Ref: R&D Altanova/ Advantest

Co-Packaged Technologies

Co-Packaged Copper

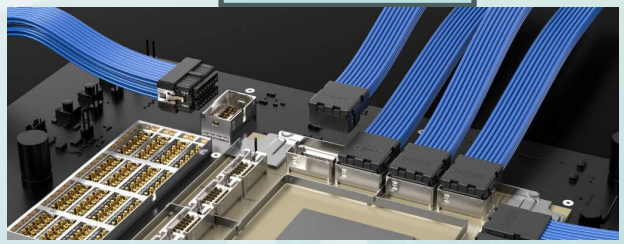


Image Ref: Samtec Inc.

Co-Packaged Optics

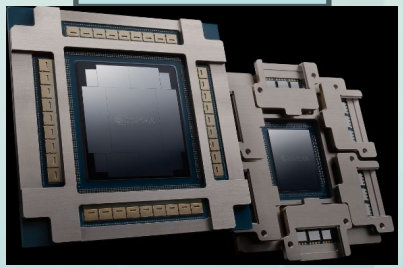


Image Ref: NVIDIA

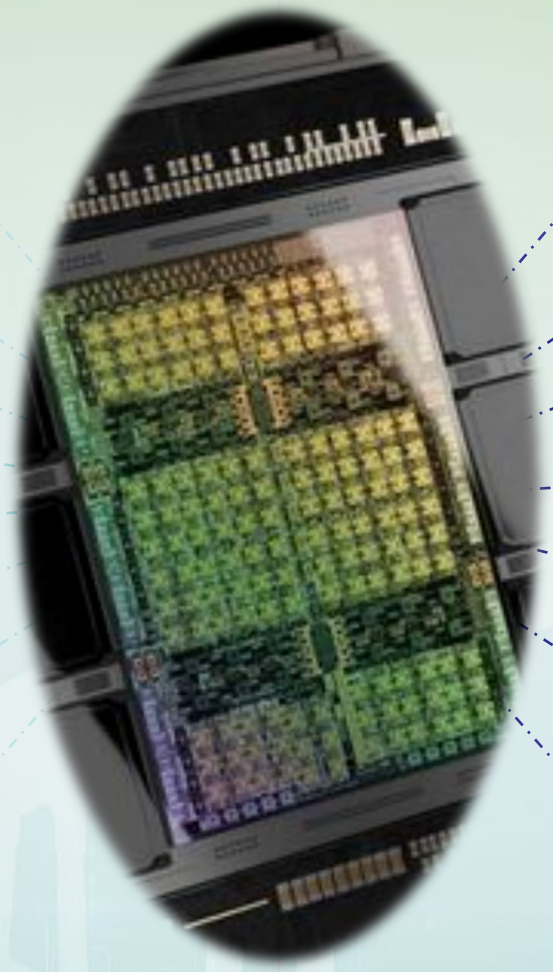
**** Near Package Optics/ Near Package Copper are technologies comparable to PCB launches since they launch into the printed circuit boards***

448G data transmission through a traditionally designed PCB is extremely challenging

HPC Challenges

CHALLENGES

- Impedance Control
- Back-Drills
- Drill Accuracy
- Material Registration
- Plating
- Feature Control
- Materials
- Density



TECHNOLOGIES

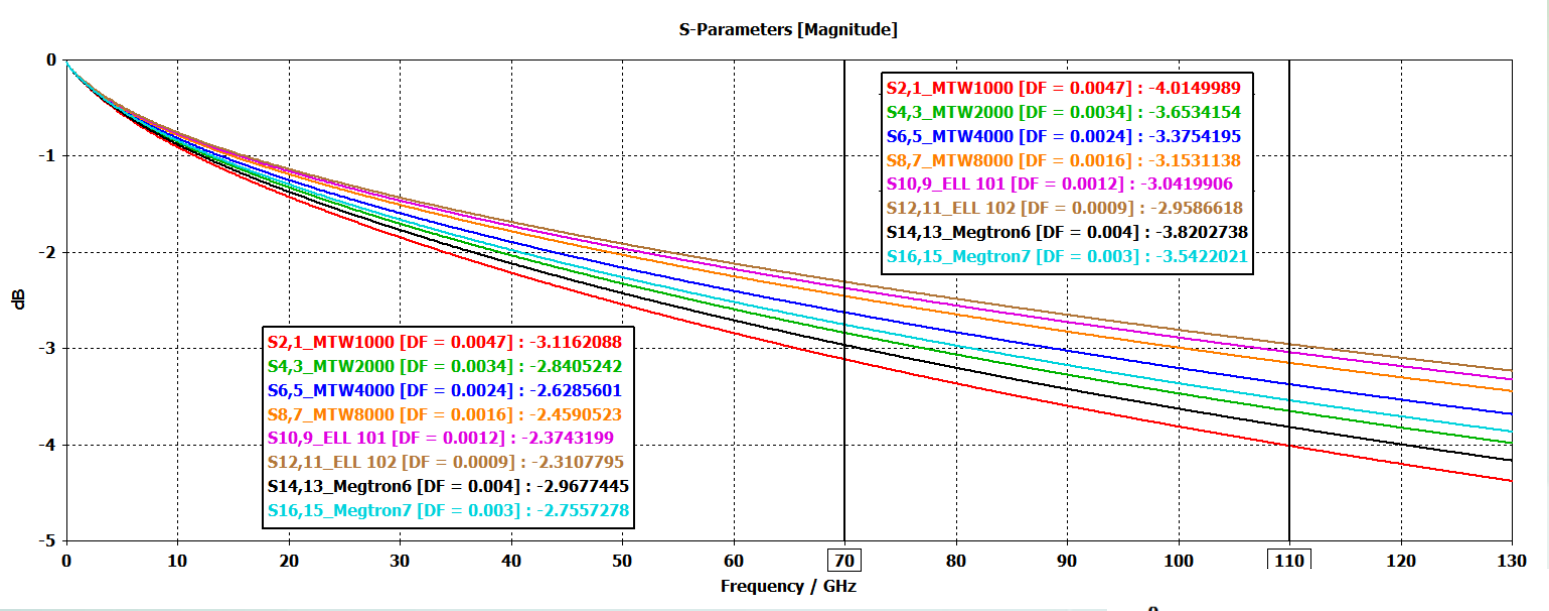
- Sintering
- Premium Materials
- Coaxial Vias
- +/-2 % Impedance
- HDI / Buildup
- 2 – 4 mil Stub Drill
- Ultra Thick Boards

PCB Challenges

What are the current challenges for performance

- Skin loss vs dielectric loss (dielectric loss gets smaller with frequency)
- Impedance Control
  - Material properties and how to reduce impedance discontinuities
  - Via tuning and via structures – special structures to reduce losses

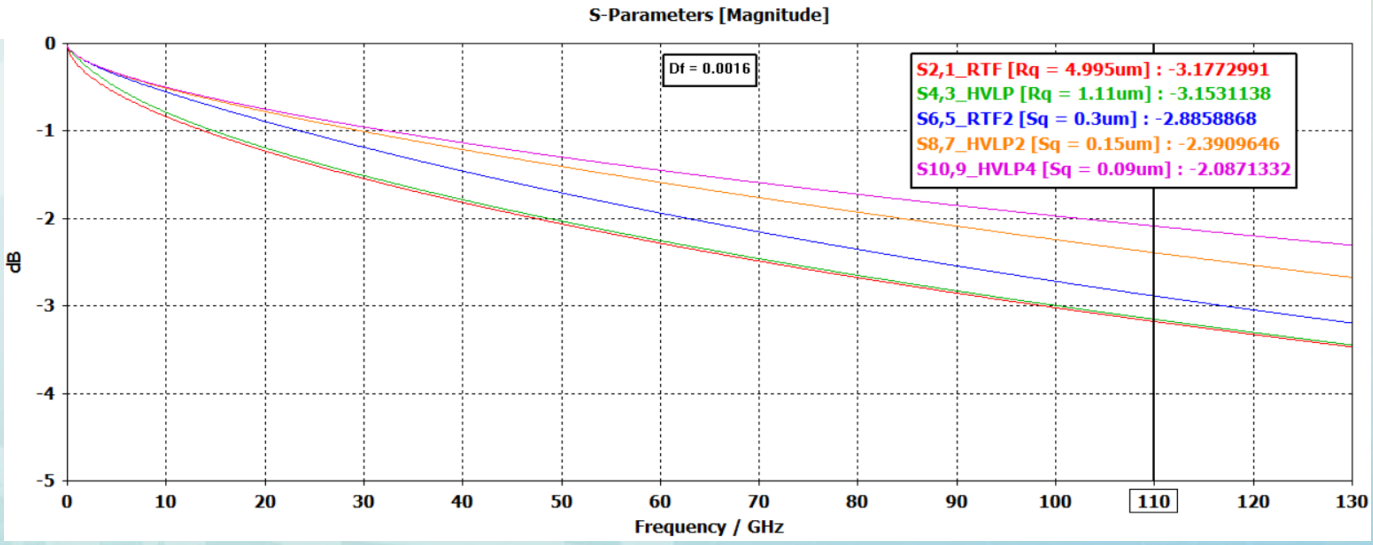
Skin loss vs dielectric loss



Skin loss dominates more vs dielectric loss

- Trace width= 4.25mils
- Length 1inch
- Minor change in IL from Df=0.0016 to 0.009

- Surface roughness contributing directly to skin effect



Impedance Control: Material properties

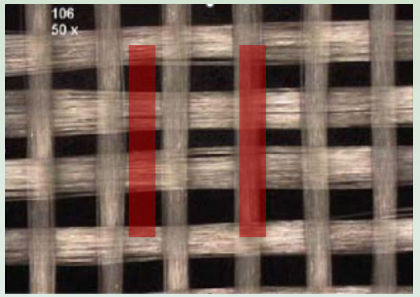
Material properties to consider and how to reduce impedance discontinuities

Material selection

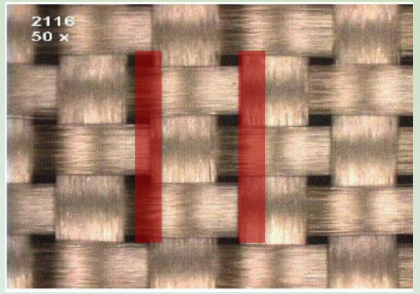
- Glass Fiber vs. Resin
  - Ex: what is 1078 [73%]
  - Tighter weaves; yields better SI performance
- Panel Rotation to mitigate Fiber Weave Effect
  - Helps reduce impedance discontinuities and propagation delays on a differential line
- Tighter impedance control required!

Surface Roughness

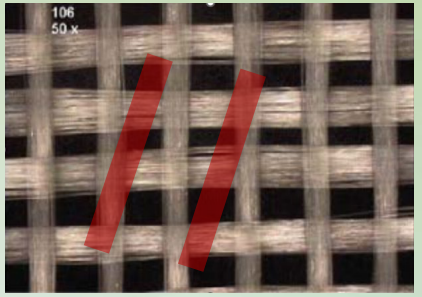
- RTF vs VLP/HVLP at higher frequencies
- Using surface roughness parameters in simulations



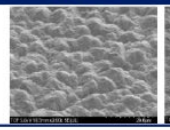
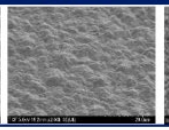
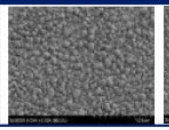
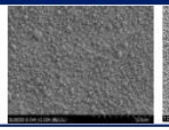
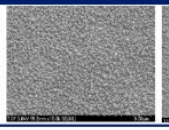
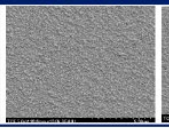
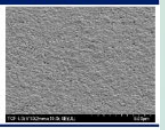
106 weave



2116 weave

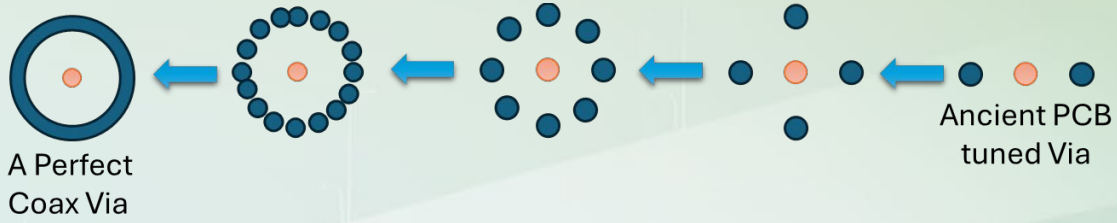


Rotation

	RTF2	RTF4*	HVLP	HVLP2	HVLP3	HVLP4	HVLP5*
							
Thickness (oz)	H / 1 / 2	H / 1 / 2	H / 1 / 2	H / 1 / 2	H / 1	H / 1	H / 1
Roughness, Sa (µm)	0.3	TBD	0.22	0.15	0.10	0.09	0.07

Impedance Control: Via tuning and via structures

- More tuning return via → Structure goes closer to Coax via structure
  - True Coax vias are great due to less complex C-L-C structure
  - Challenge is layout and manufacturing



- Minimizing structure size by half would approximately double the bandwidth

Coaxial via tuning				
ID (d) [mil]	OD (D) [mil]	Dk	Z0 (Ohms)	Cut-off (GHz)
4	19	3.5	49.91	174.62
5	23.5	3.5	49.57	140.92
7.9	38	3.5	50.31	87.50
9.8	47	3.5	50.22	70.71

$c \approx 300'000\ km/s$

$$f_c \approx \frac{2 \times c}{(D + d) \times \pi \times \sqrt{\varepsilon_r}}$$

** Data taken from Test ConX 2025 for reference*

Factors Affecting Data Transmission

Insertion loss, return loss, cross talk and phase mismatch can all contribute to poor performance of the link

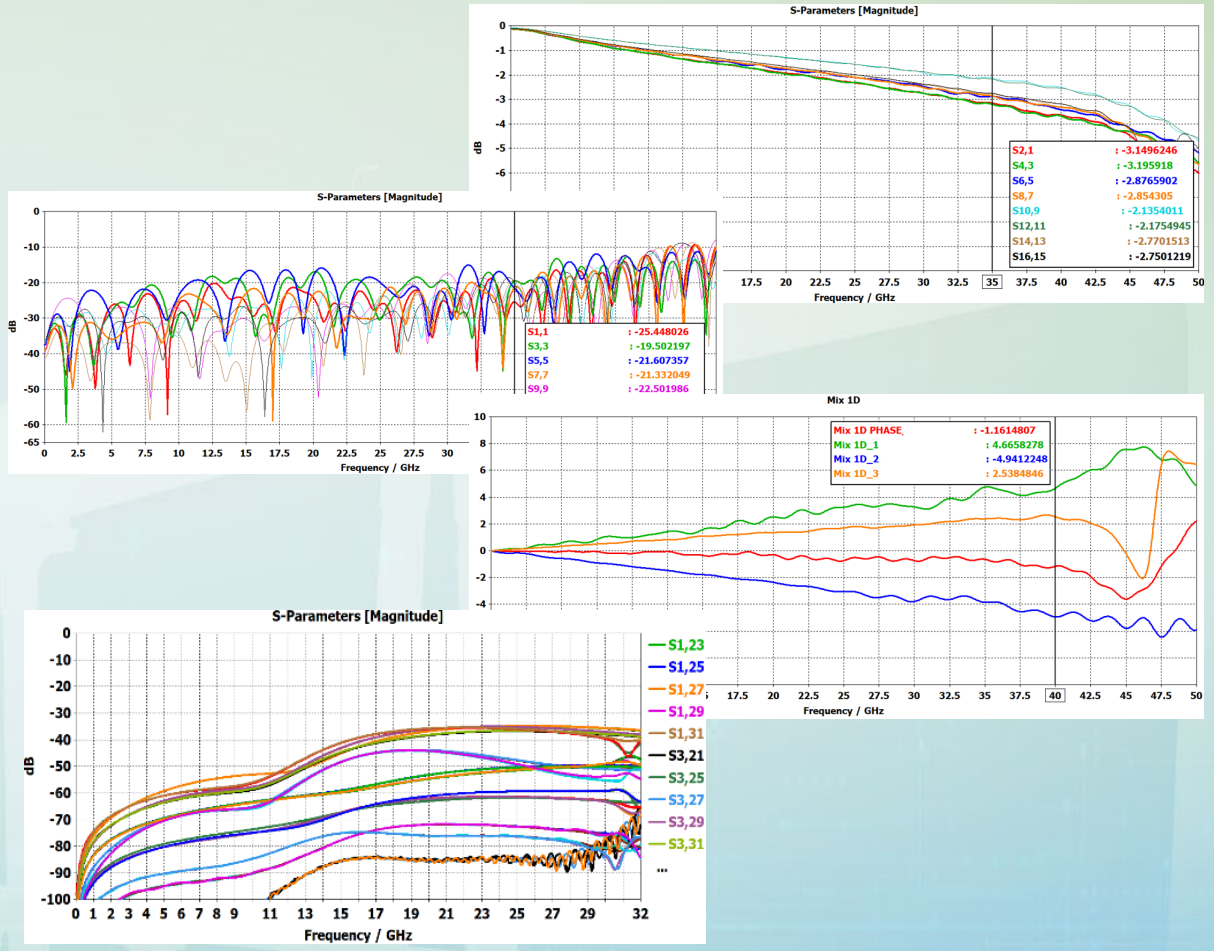
Insertion loss: aka transmission loss – Is a loss observed on transmitted energy

Return loss: aka reflection loss – measurements of reflected energy back into the transmission port

Phase Mismatch: Mismatch observed between phase of P/N signal of a differential output port compared with Input phase

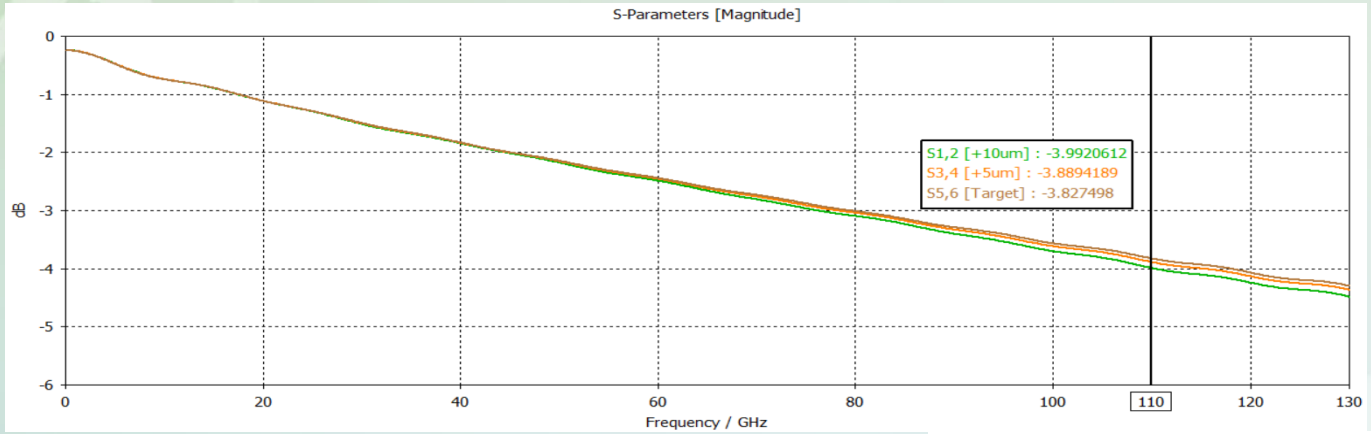
Cross talk: Energy coupled between two links due to improper isolation between the links

Managing these factors becomes significantly challenging at frequencies beyond 50GHz



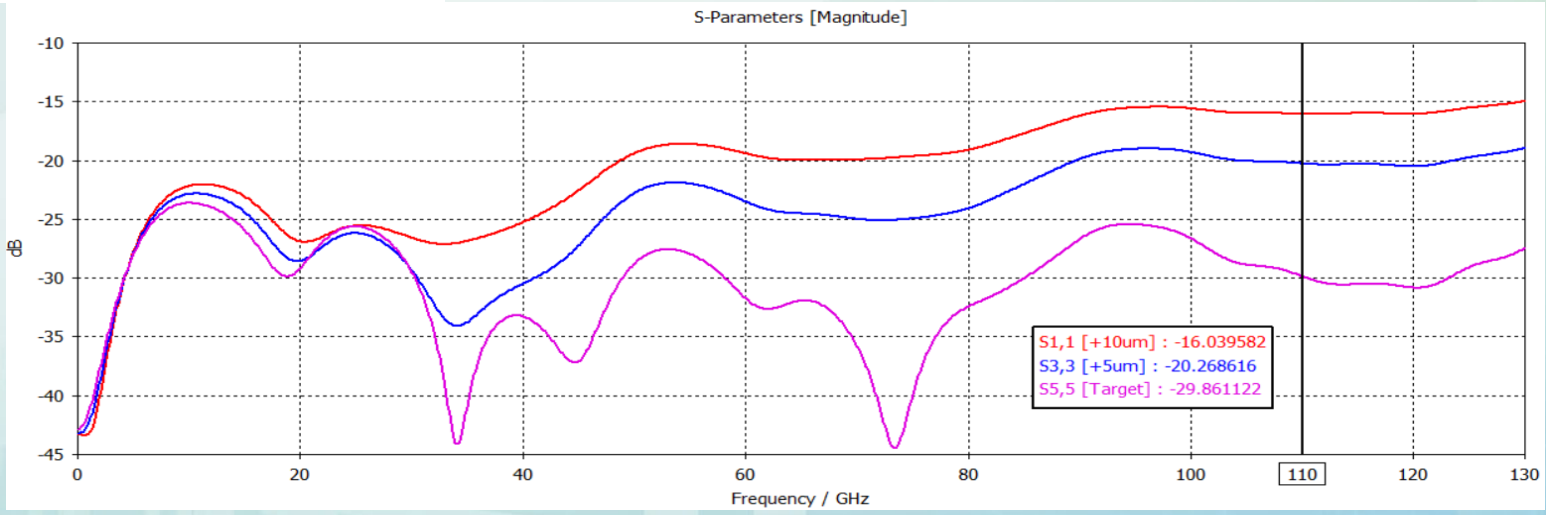
Super Structure: Special probe via IP

- Tight impedance controlled vias



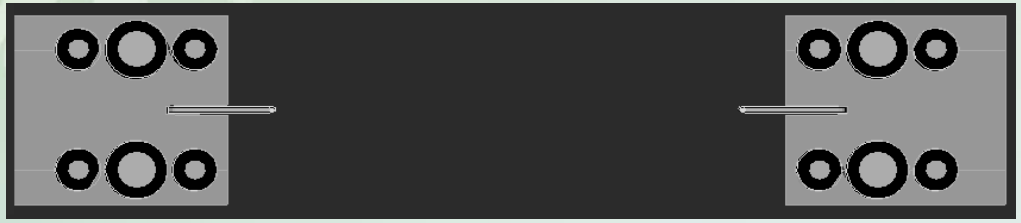
- Modeled with a Full 3D solver [CST Microwave Studios]
  - Focused on the via-tuning
  - Copper roughness accounted

- Ensures tight impedance control on the stripline
- Provides necessary isolation to address cross-talk at 100GHz+ Nyquist
- Remedies the biggest challenge for higher frequency launches – via tuning



Test Vehicle Design

Measurement Structures



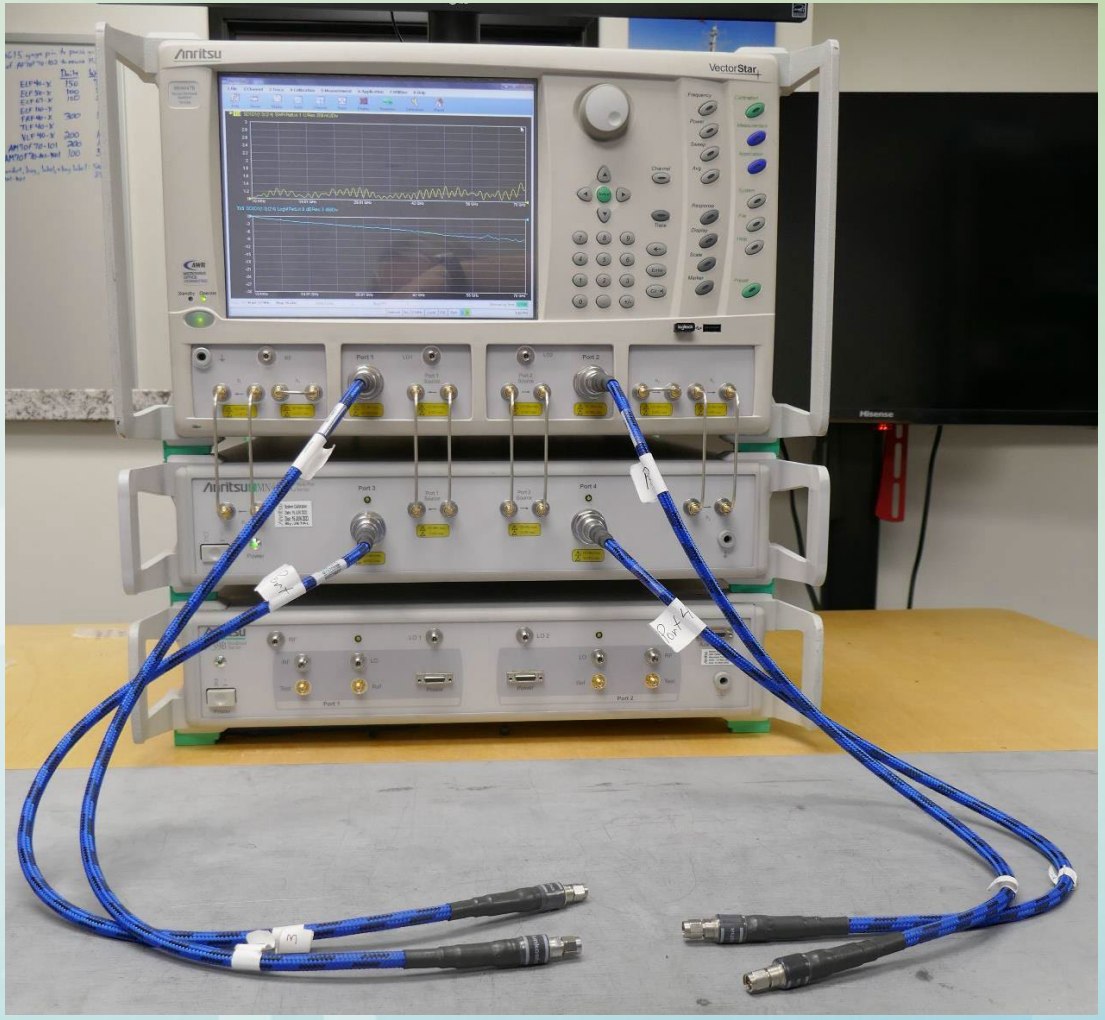
Connector → microstrip →"super structure" →stripline → "super structure" → microstrip →connector

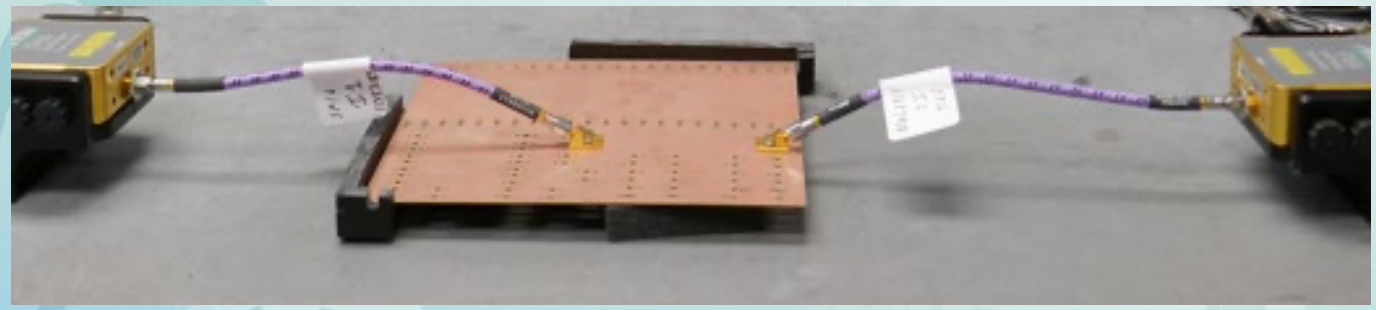
- Test vehicle designed for Probe application
- Multiple structures per routing layer
  - Varied via-impedance
  - Varied line-widths [21um, 48um, 203um]
  - Varied impedances (48, 50, 52 Ohms)
  - Varied line-length [1-inch, 2-inches]
- Repeatability: Tested 2x boards

Imp	Lyr	Copper Weight (Gr)	Family	Image	Foil	Thk (µm)	Type	Plt	Er
	SMT					25.4			
1xΩ	L1, TOP	1.98446	Substrate Foil		0.07oz	15.0114	Mixed	0	0.00
			GL102			26.2446			2.47
	L2, RDL1	1.98446	Substrate Foil		0.07oz	15.0114	Mixed	0	0.00
			GL102			26.2446			2.47
	L3, RDL2	1.98446	Substrate Foil		0.07oz	15.0114	Mixed	0	0.00
			GL102			26.2446			2.47
6xΩ	L4, RDL3	1.98446	Substrate Foil		0.07oz	15.0114	Mixed	0	0.00
			GL102			26.2446			2.47
	L5, RDL4	1.98446	Substrate Foil		0.07oz	15.0114	Mixed	0	0.00
			GL102			17.1846			2.47
	L6, INR1 L7, INR2	1.41748 1.41748	E705G		0.05oz 0.05oz	109.982	Mixed Mixed	29... 29...	4.20
			GL102			17.1846			2.47
	L8, RDL5	1.98446	Substrate Foil		0.07oz	15.0114	Mixed	0	0.00
			GL102			26.2446			2.47
6xΩ	L9, RDL6	1.98446	Substrate Foil		0.07oz	15.0114	Mixed	0	0.00
			GL102			26.2446			2.47
	L10, RDL7	1.98446	Substrate Foil		0.07oz	15.0114	Mixed	0	0.00
			GL102			26.2446			2.47
	L11, RDL8	1.98446	Substrate Foil		0.07oz	15.0114	Mixed	0	0.00
			GL102			26.2446			2.47
1xΩ	L12, BOTTOM	1.98446	Substrate Foil		0.07oz	15.0114	Mixed	0	0.00
	SMB					25.4			

Validation Setup

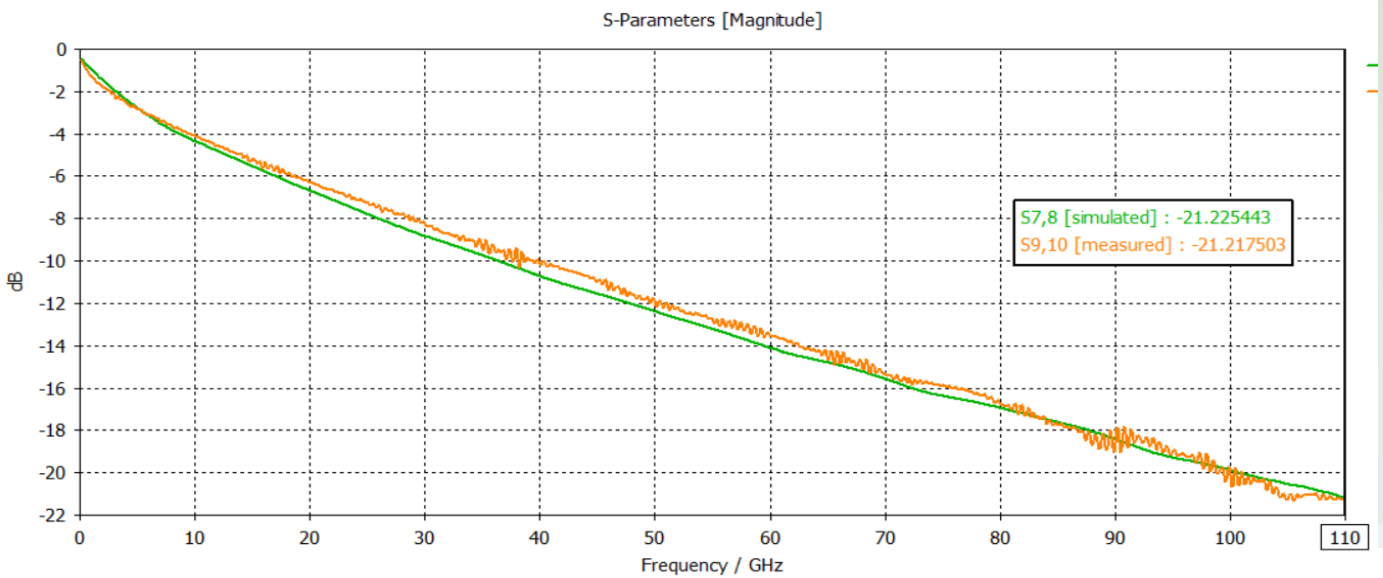
- Anritsu 70GHz VNA with 130GHz frequency extender
- Calibrated up to 1.00mm VNA cables [rated up to 100GHz]
- Connector P/N: 01K80A-40ML5 [1.00mm]
- Test Vehicle Board

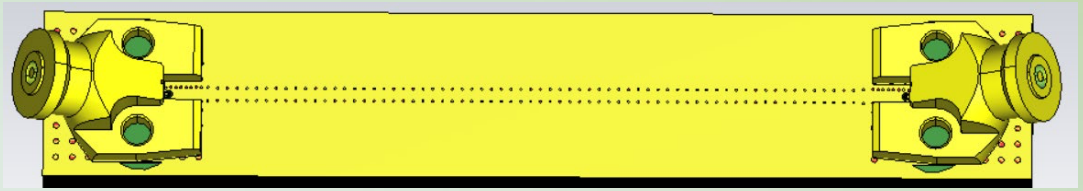




Measurement vs Simulation Results

Insertion loss & Return loss plots

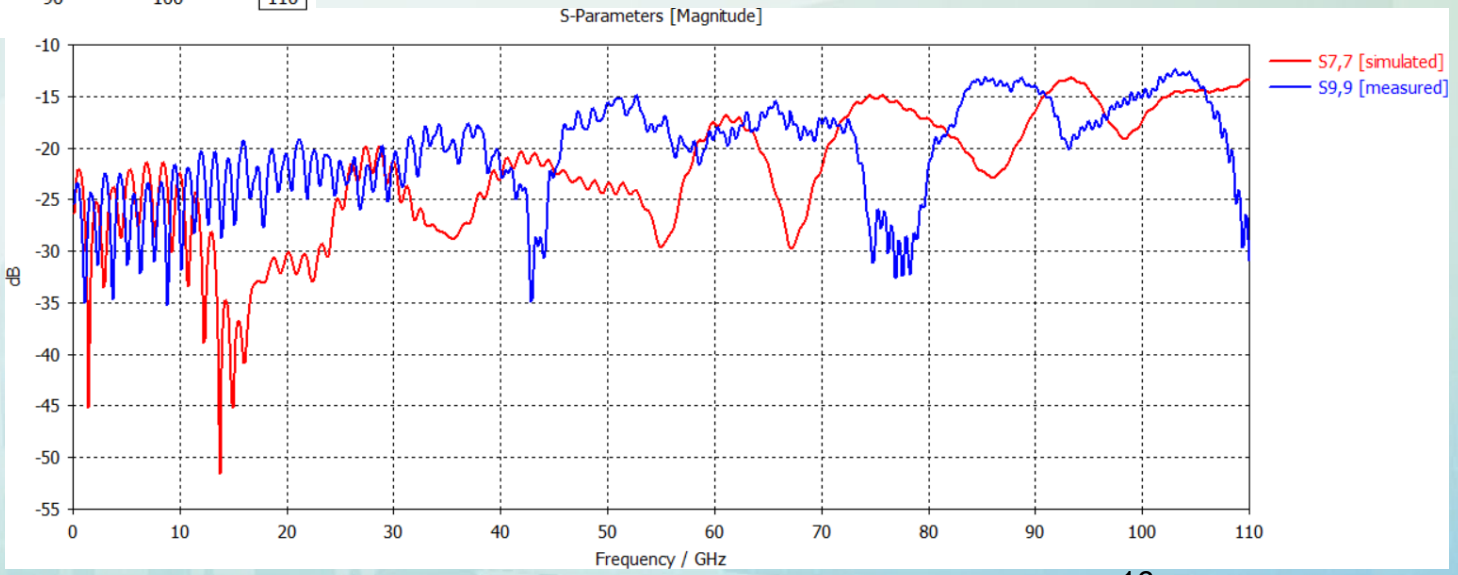




Disclaimer: The picture above is a close representation of the actual structure

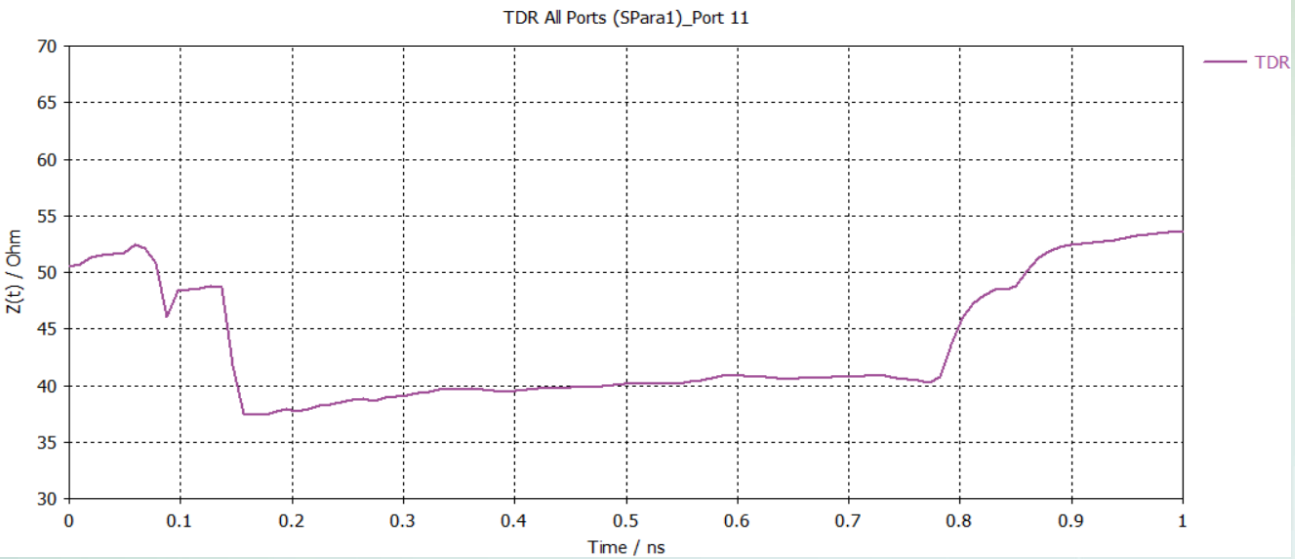
RPC-1.00	SMD Connector jack	01K80A-40ML5
Electrical data		
Impedance		50 Ω
Frequency		DC to 110 GHz
Return loss		≥ 21 dB, DC to 26.5 GHz ≥ 19 dB, 26.5 GHz to 40 GHz ≥ 17 dB, 40 GHz to 70 GHz ≥ 12 dB, 70 GHz to 100 GHz ≥ 10 dB, 100 GHz to 110 GHz
Insertion loss		≤ 0.05 x $\sqrt{f(GHz)}$ dB

- Measurements include RPC-1.00mm connectors
- Insertion loss is linear up to 110GHz
- Return loss looks good up to 110GHz
- Simulation and measurement shows good correlation

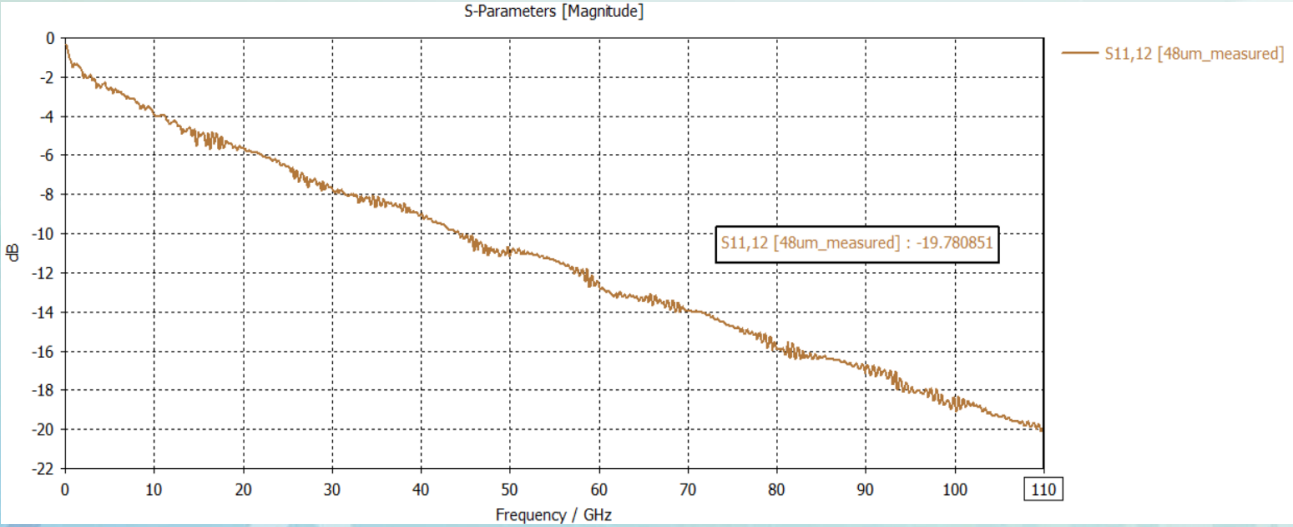


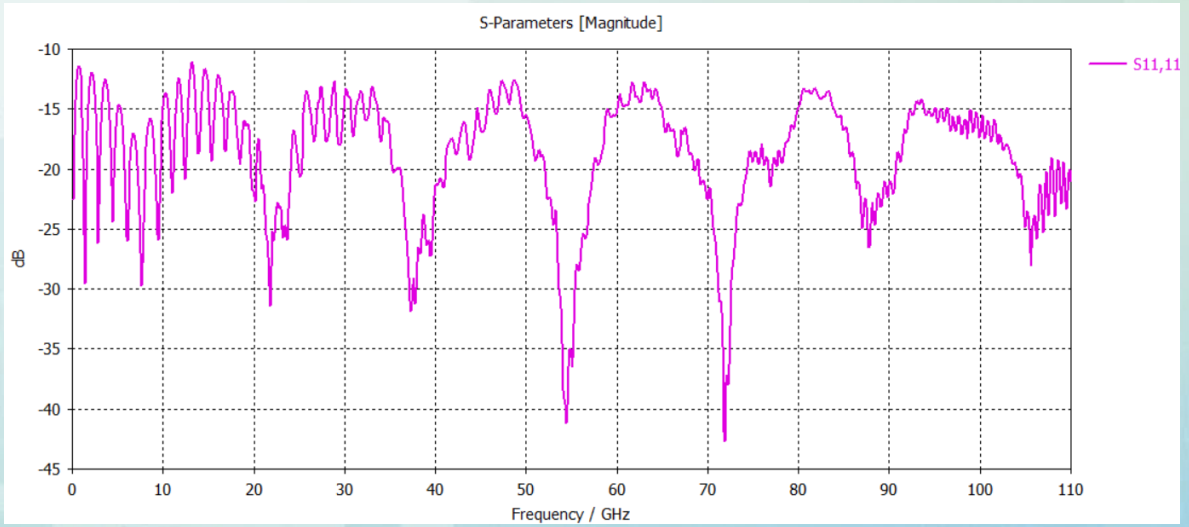
Additional Measurements

TDR, Insertion loss & Return loss plots



- Measurements include RPC-1.00mm connectors
- Trace impedance ~40Ohms +/- 2ohms
- Overall impedance drift from 50Ohm target produces decent performance
- Variation in trace impedance profile should be minimized to < +/-5%





Conclusion

- PCB technology should be able to handle 100GHz+ launches with the application of right technology
- Selecting low loss material is not enough
- Working with FAB houses is essential to dial down control and optimize per the factors discussed
- Standardizing Stack-ups will help with repeatability
- Via-tuning is the most critical parameter to achieve good performance, at higher frequencies
- “Super structure” or alike via optimization/controls essential to enable 448G+ data rates

Questions?