SWTEST
PROBE TODAY, FOR TOMORROW
2025 CONFERENCE

How High-Speed Probe Cards Accelerate Time-to-Market

micron

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Outline

- Introduction / Background
- Accelerating Cycles of Learning
- High-Speed Probe Card Definition and Use Cases
- Advancing High-Speed Probe Technology
- Key Challenges for High-Speed Probing
- Summary / Conclusion

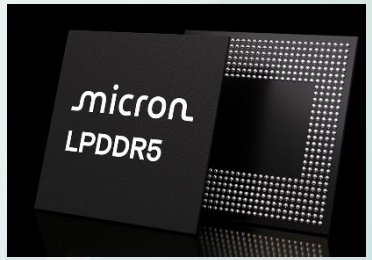
Introduction / Background

- **Problem statement:**
  - Memory manufacturers in a race to release newest technology to market (e.g.: DDR6).
  - Full cycles of learning require months from tape-out to packaged part testing.
  - Once detected, designers need to fix circuit errors, tape-out new reticle, start more wafers.
  - How to detect and fix circuit errors faster?

Does Design Meet Specifications?

- Verilog simulation
  - Not all circuit errors detected

- Physical application testing
  - Errors not caught in simulation identified by physical testing
  - Testing Methods:
    - High-Speed Package test



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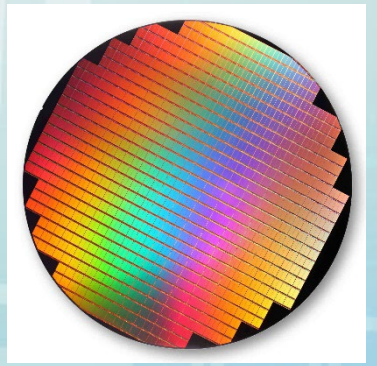
-or-

- High-Speed Wafer test



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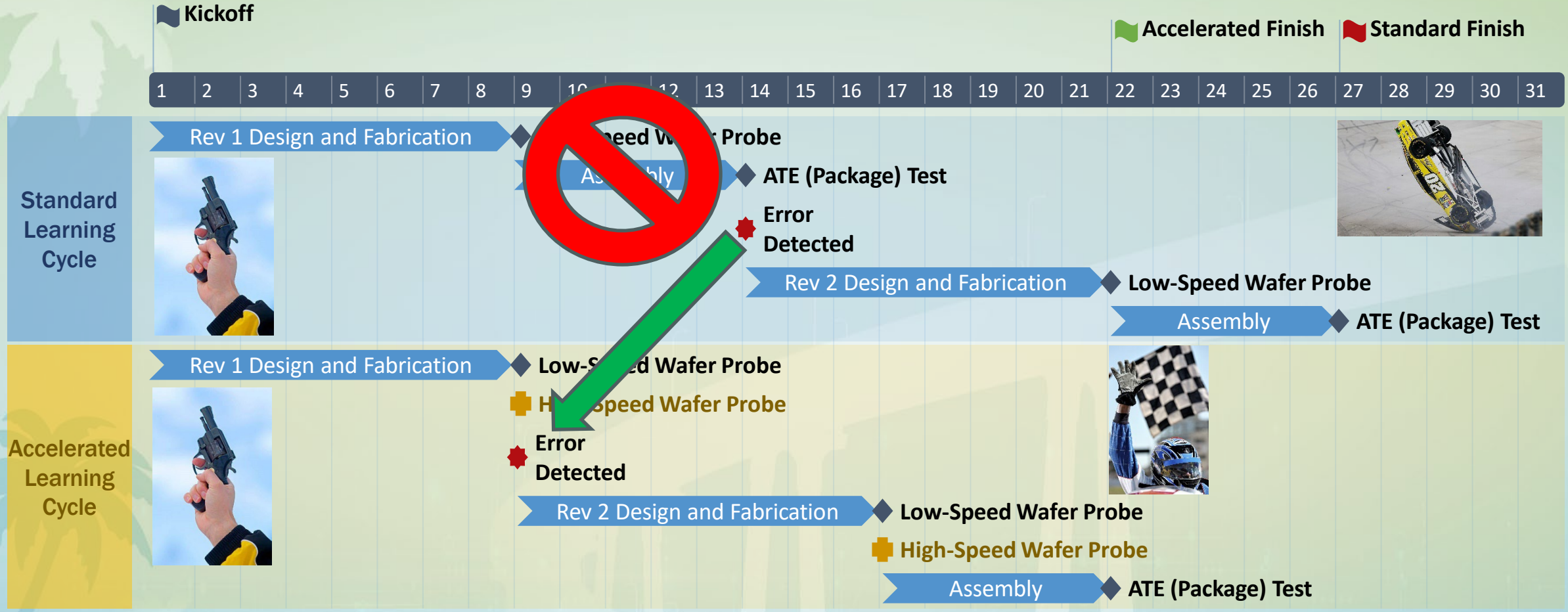
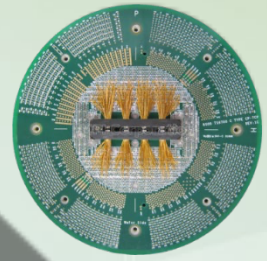
Accelerating Cycles of Learning



Time-to-market savings realized!

High-Speed Memory Probe Card Definition

- DRAM Datasheet Speed
- All signal & many PWR/GND pads probed
- Capable of native, customer mode testing
- Full datasheet range of voltages and register combinations
- Card circuitry optimized for signal and power integrity
- Full wafer automated probing for volume data



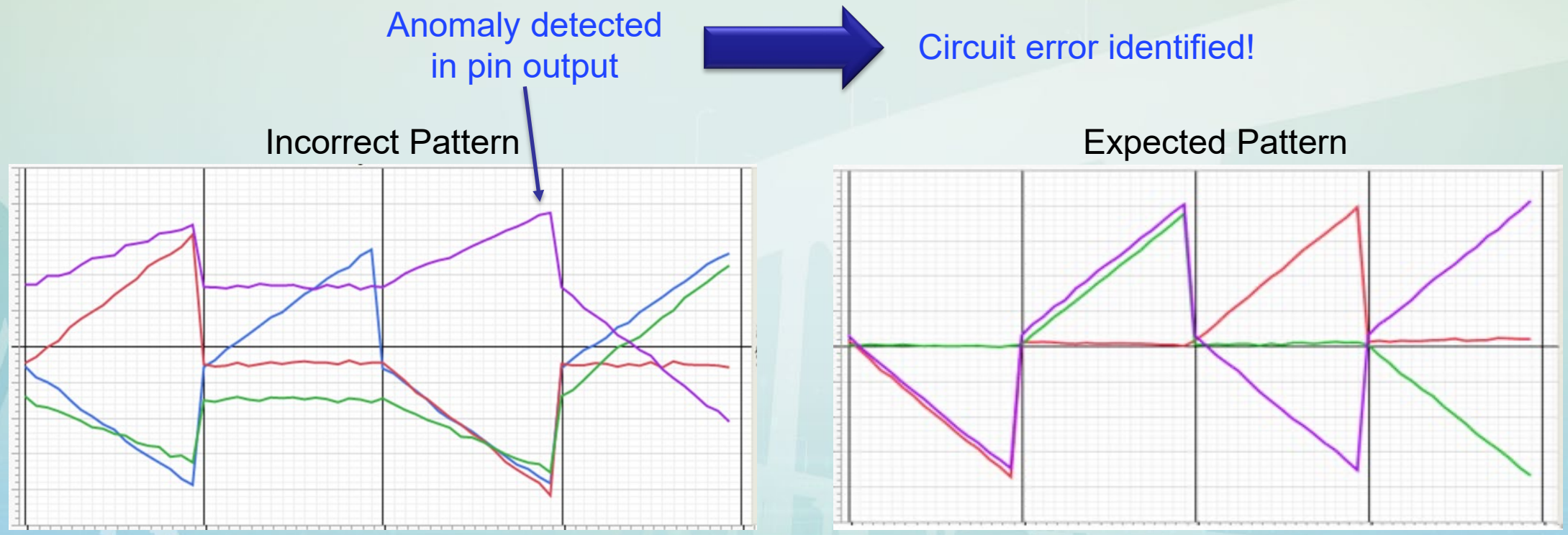
Just emulate package testing flow!

High-Speed Probe Card Use Cases

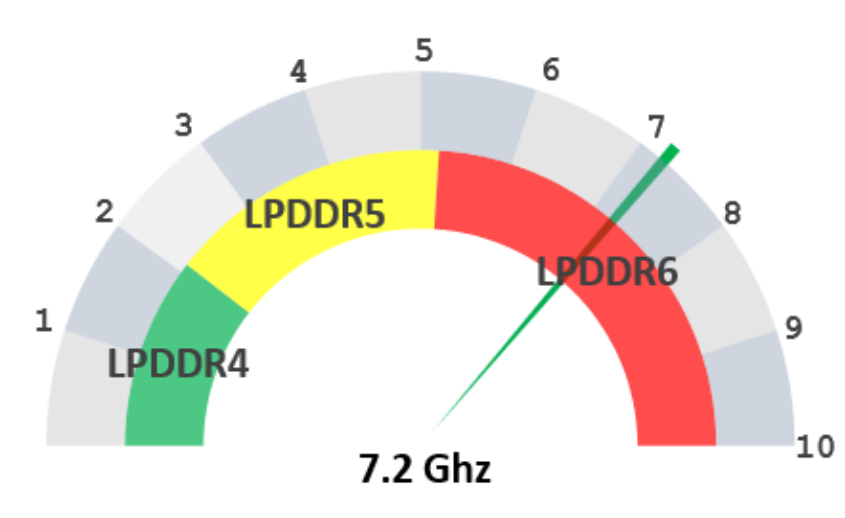
- Accelerate design revision
  - 1st Silicon debug
  - New Reticle verification
- Regular line sampling
  - Silicon health monitoring (speed yield, datasheet char)
- *Bench-level speed characterization on wafer*
  - *Single die, engineering only*

Case Study: Duty Cycle Adjust Circuit Error

- Package test flow emulation using low-speed testers is challenging
- High-Speed wafer tester can evaluate all DRAM circuitry
- Duty Cycle Adjust (DCA) circuit error found using High-Speed tester:



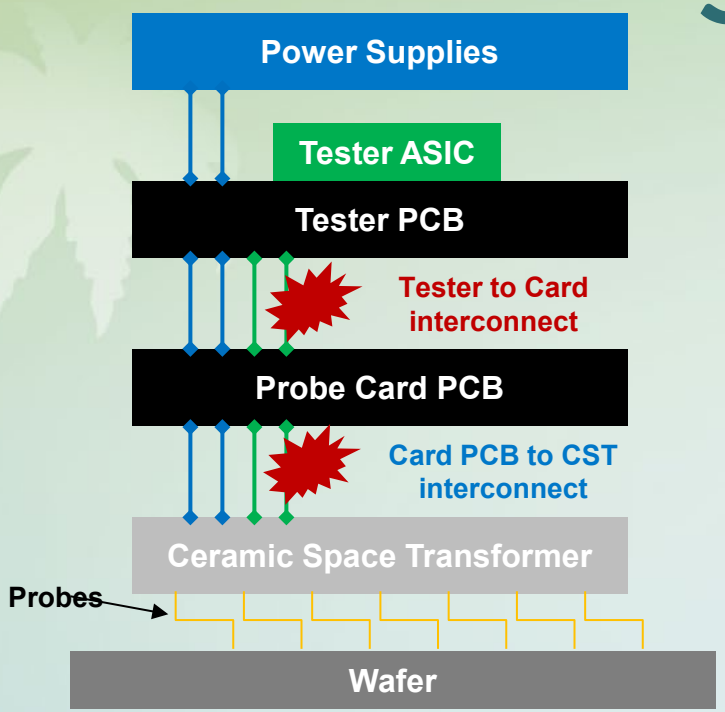
Advancing High-Speed Probe Technology

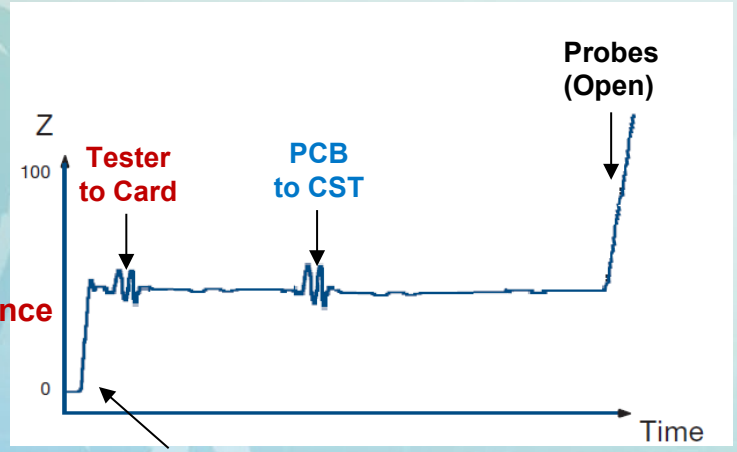


- Solutions:
  - Tester and test program development
    - Signal training, termination, etc.
    - Hardware improvements
  - Signal and Power Integrity improvement:
    - Reduction of *return loss*
    - Reduction of *insertion loss*
    - Maximization of *power probe count*
    - Supplier collaboration for Probe Card optimization
- Results:
  - Comparison of *Data Eye shmoo* for wafer vs. package
  - *Statistical Comparison* of wafer vs. package results

Solution: Return Loss Reduction

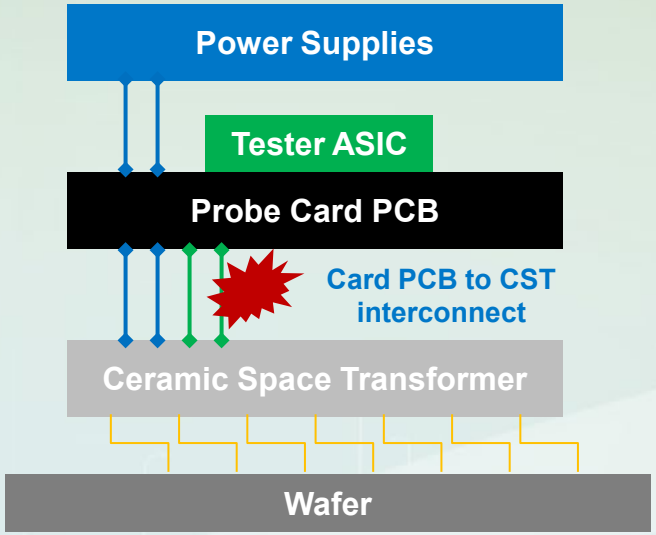
Worst Case

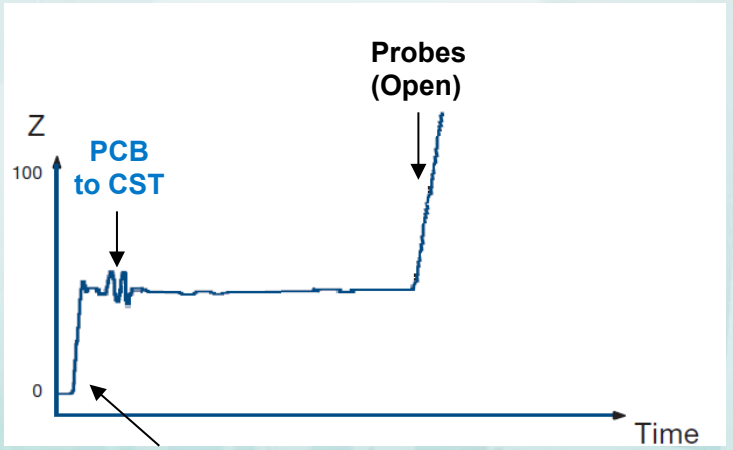




Improved

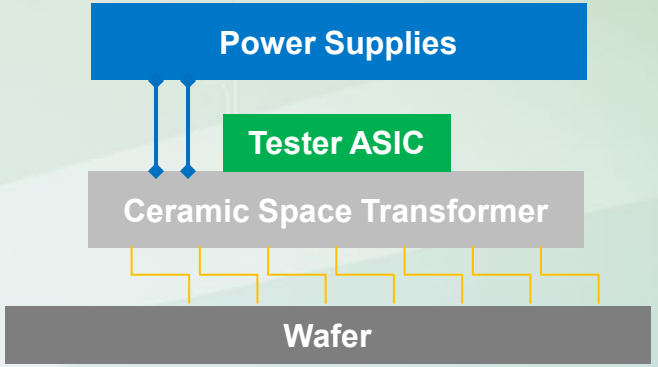
- One interconnect eliminated

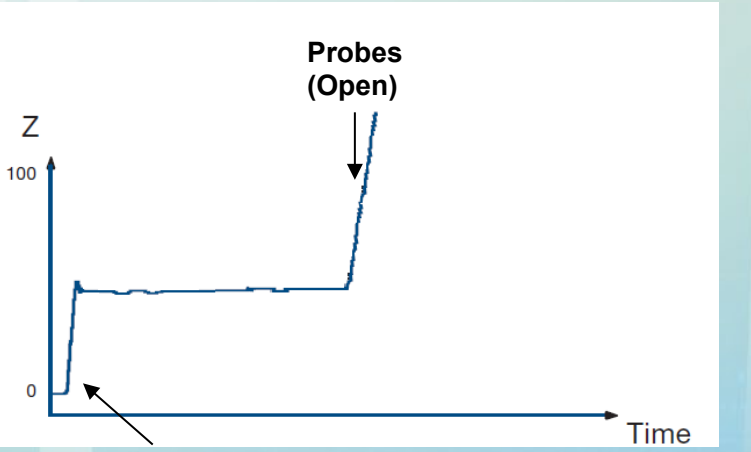




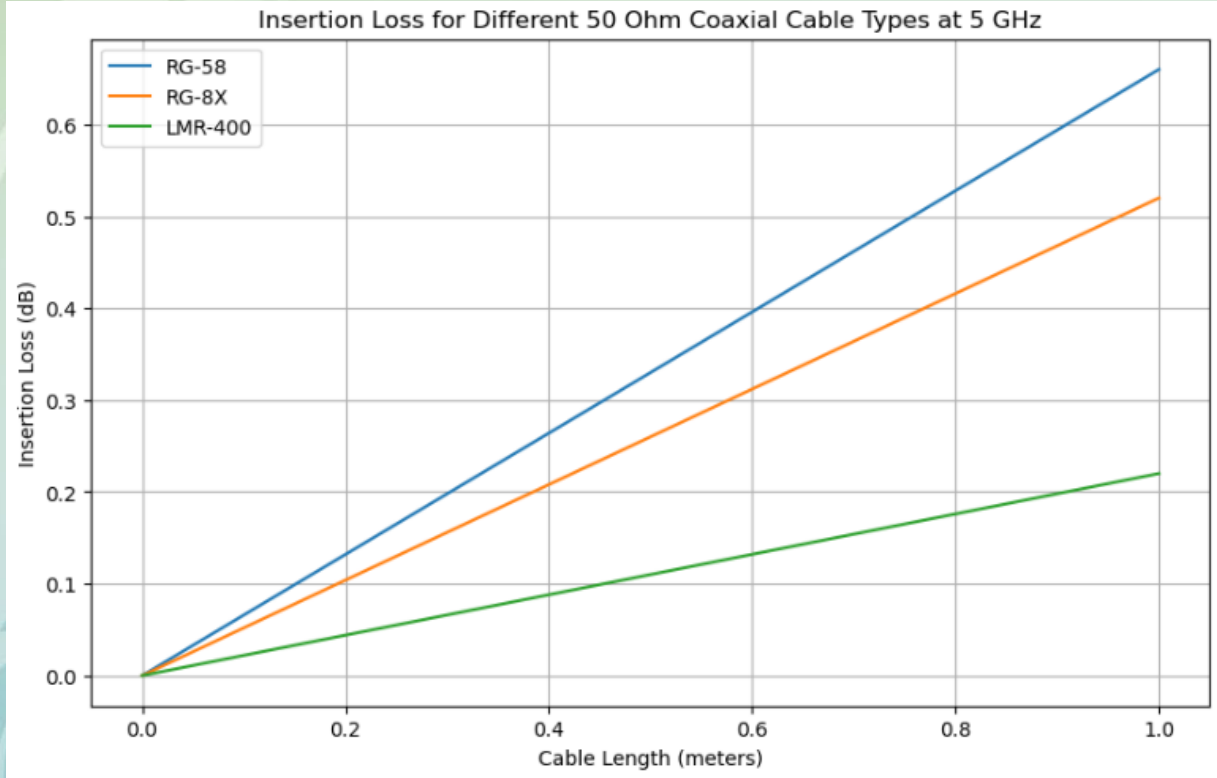
Ideal

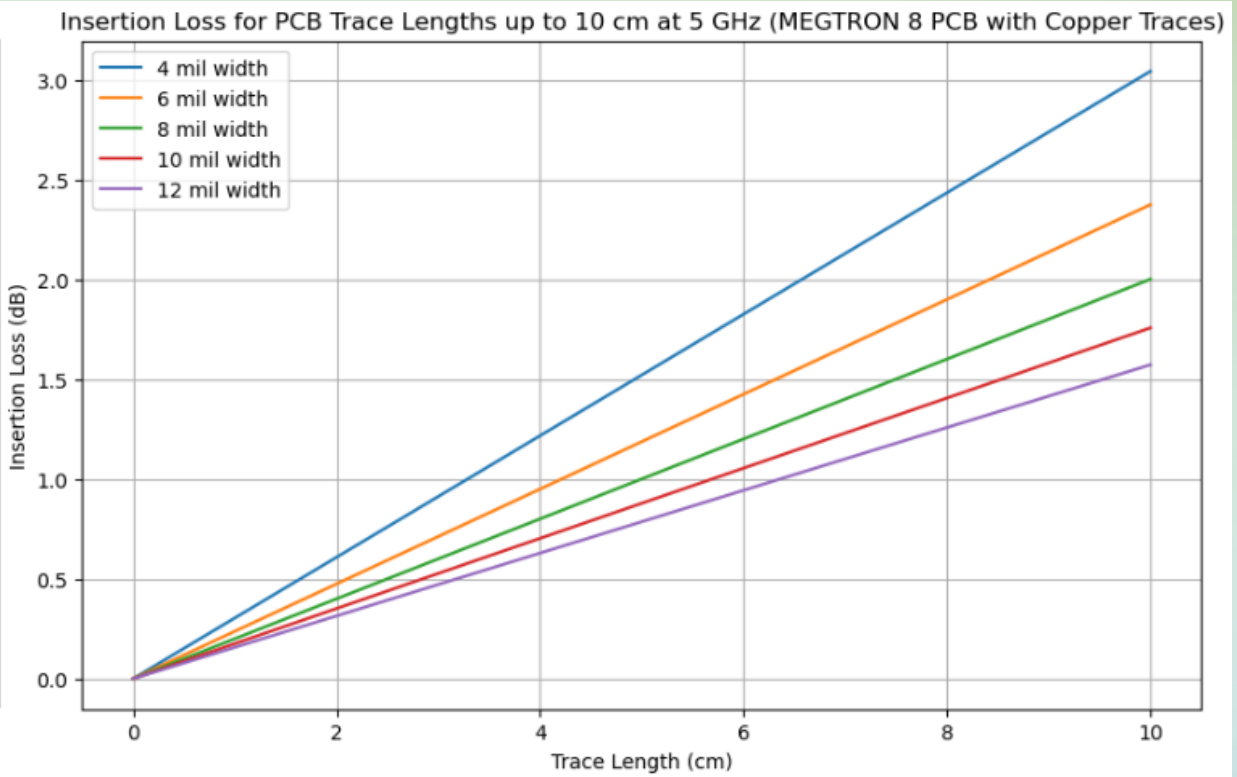
- Two interconnects eliminated
- No PCBs





Solution: Insertion Loss Reduction





Eliminating cables, shortening PCB traces = less insertion loss!

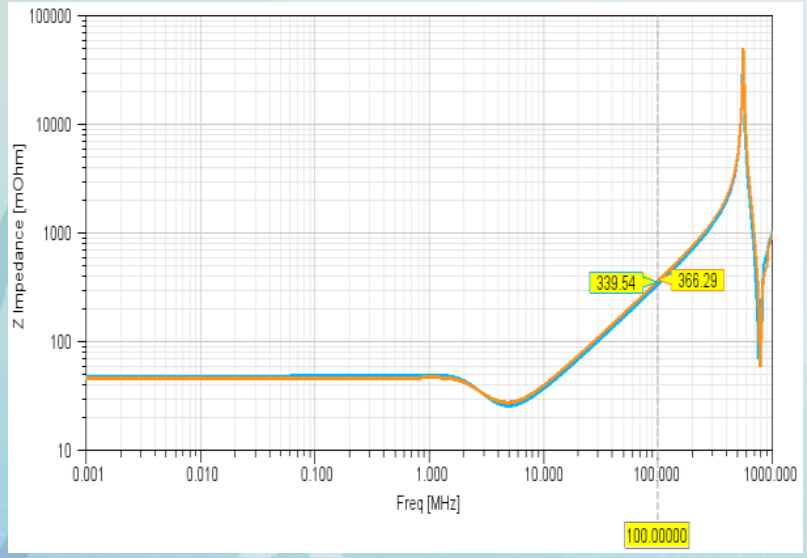
Solution: Maximize Power Probe Count

- E.g.: Target Impedance = 500 mOhms @100Mhz
- 2 ports tested (near and far)
- 3X more probes ≈ 35% lower impedance

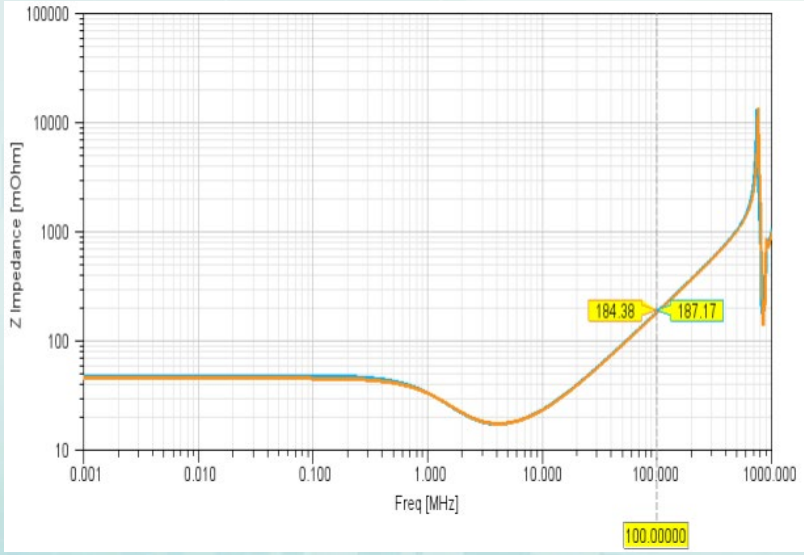
$$Z_{target} = \frac{(V_{max} \times Vdroop_{max}\%)}{I_{max}}$$

- **Where:**
  - Vdroop max = 3%
  - E.g.: 1V * 3% / 60mA = **500 mOhms**

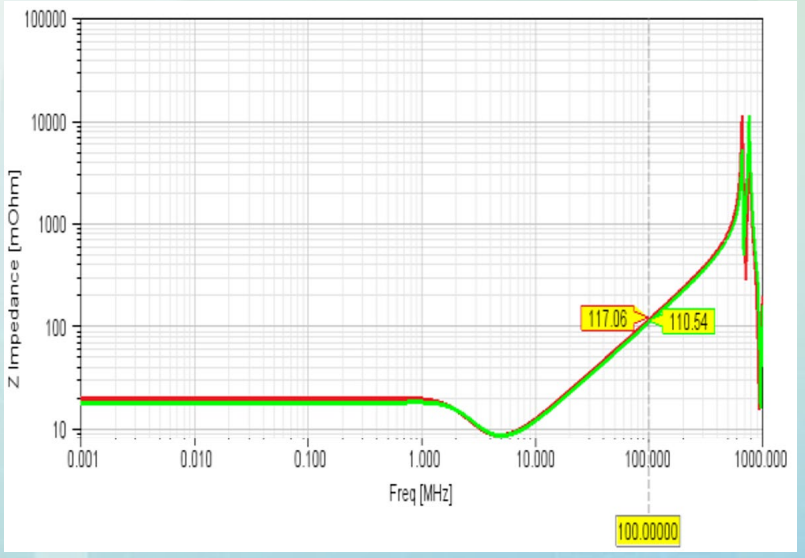
12 probes, 2x1uF caps
366.29 mOhms



12 probes, 6x1uF caps
184.38 mOhms



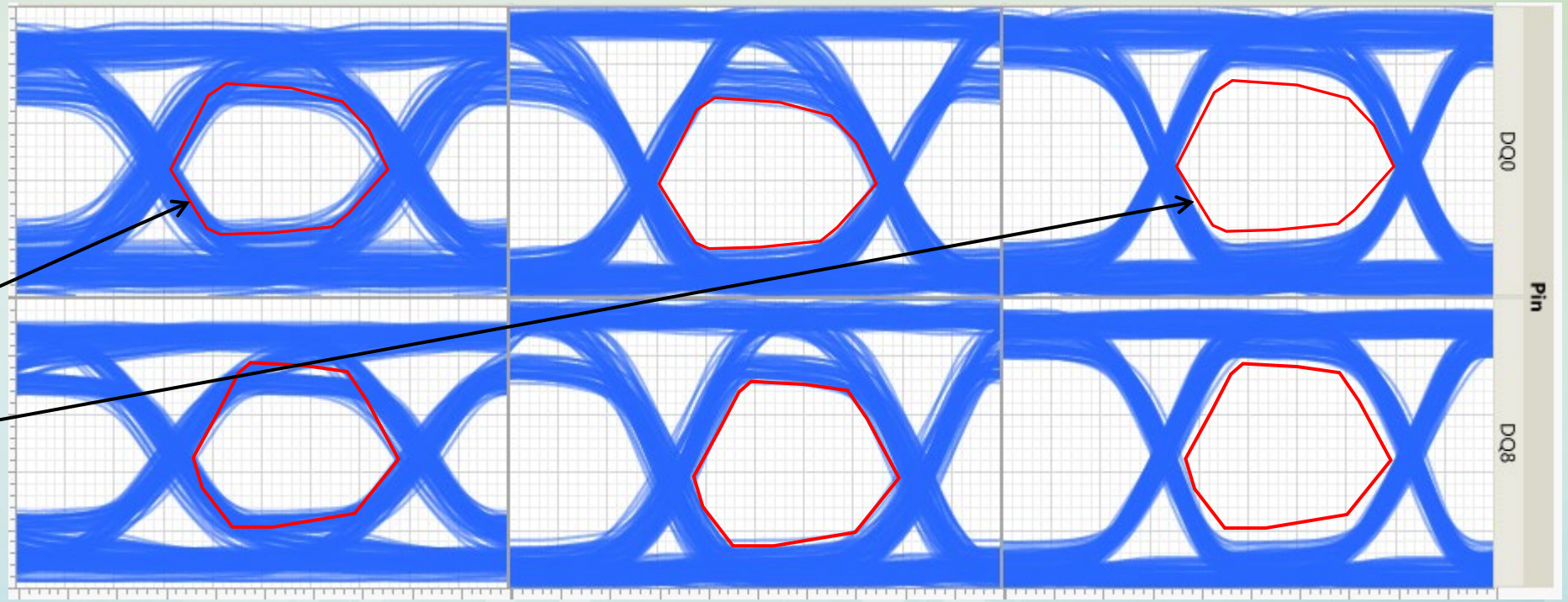
39 probes, 6x1uF caps
117.06 mOhms



Results: Read Data Eye Comparison

Test Conditions:
- 2 DQ's
- Comparable test conditions between wafer and package.

Note:
- Wafer Probe eye collapsed vs. 1-Rank PKG mainly as function of probe CRES and proximity to tester.



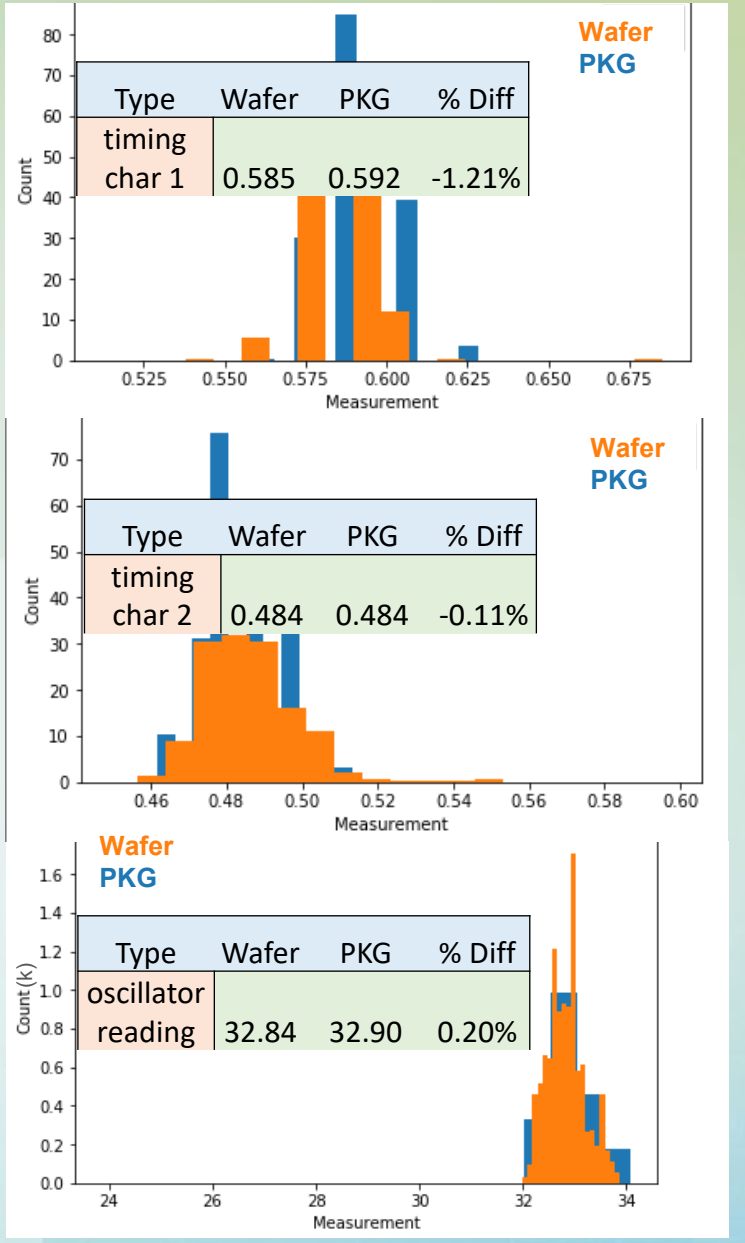
Equivalent width and acceptable height vs. package → qualified

Results: Statistical Comparison

- Several lots probed with High-Speed tester
- 24K passing die packaged and tested
- Speed test correlation: ~99.74%

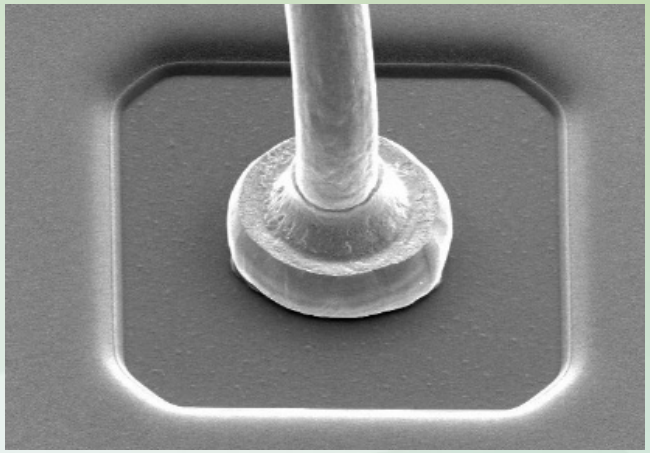
Temperature	Wafer Pass Die	PKG All Fail Die	PKG Speed Fail Die	Overall Correlation	Speed-only Correlation
125C	24705	268	41	98.92%	99.83%
-40C	24713	41	23	99.83%	99.90%

- Only 64 new fails. Induced by assy.?
- Example char mean deltas: -1.21-0.20%



Key Challenge: Pad Size Decreasing

- Pad size decreases as die size decreases and speed increases.
- Calculate parasitic capacitance: $C_p = \frac{(\mathrm{K} \times \epsilon_o \times \mathrm{A})}{d}$
- Where:
  - K = dielectric constant (Si = 11.7)
  - ϵ_o = relative permittivity of free space (8.854×10^{-12} F/m)
  - A = Overlapping surface area of capacitor plates (mm2)
  - d = Distance between plates (mm), assume 5um



- 70x70um pad:

$$\frac{(11.7 \times 8.854 \times 10^{-12}\ F/m \times 0.490mm^2)}{0.005mm} = 10.2pF$$

- 50x50um pad:

$$\frac{(11.7 \times 8.854 \times 10^{-12}\ F/m \times 0.250mm^2)}{0.005mm} = \mathbf{5.18pF}$$

Benefit:

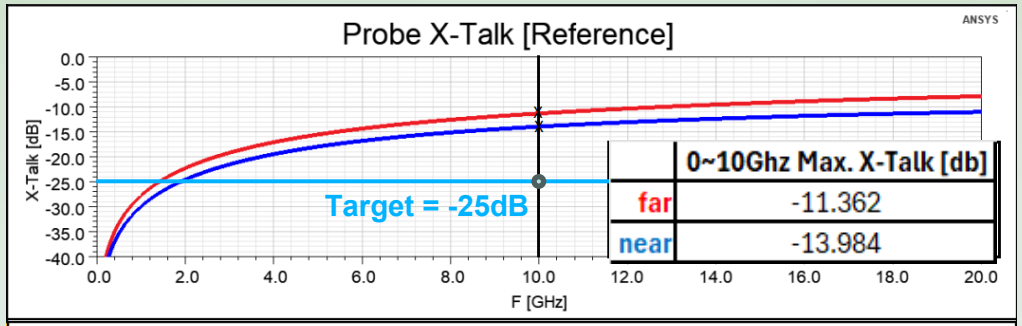
- Smaller bond pad size = less parasitic capacitance!

Challenge:

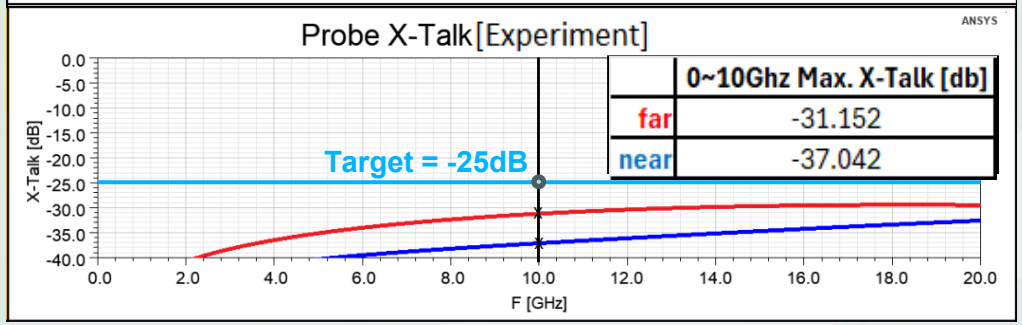
- Smaller pad size = smaller scrub and more accurate probe position required.

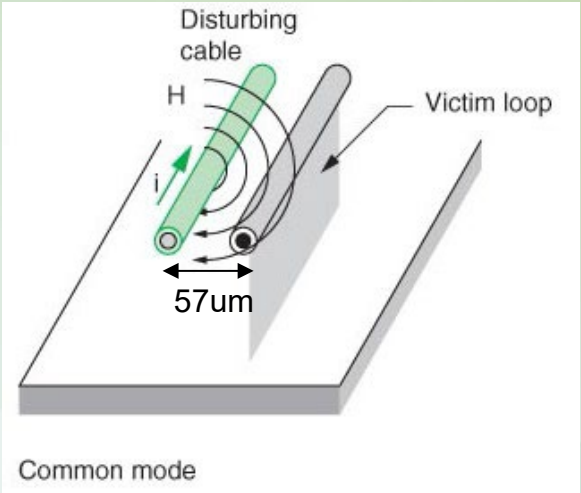
Key Challenge: Pad Pitch Decreasing

Example A:
Ground not fully shielding signal probes



Example B:
Ground more fully shielding signal probes

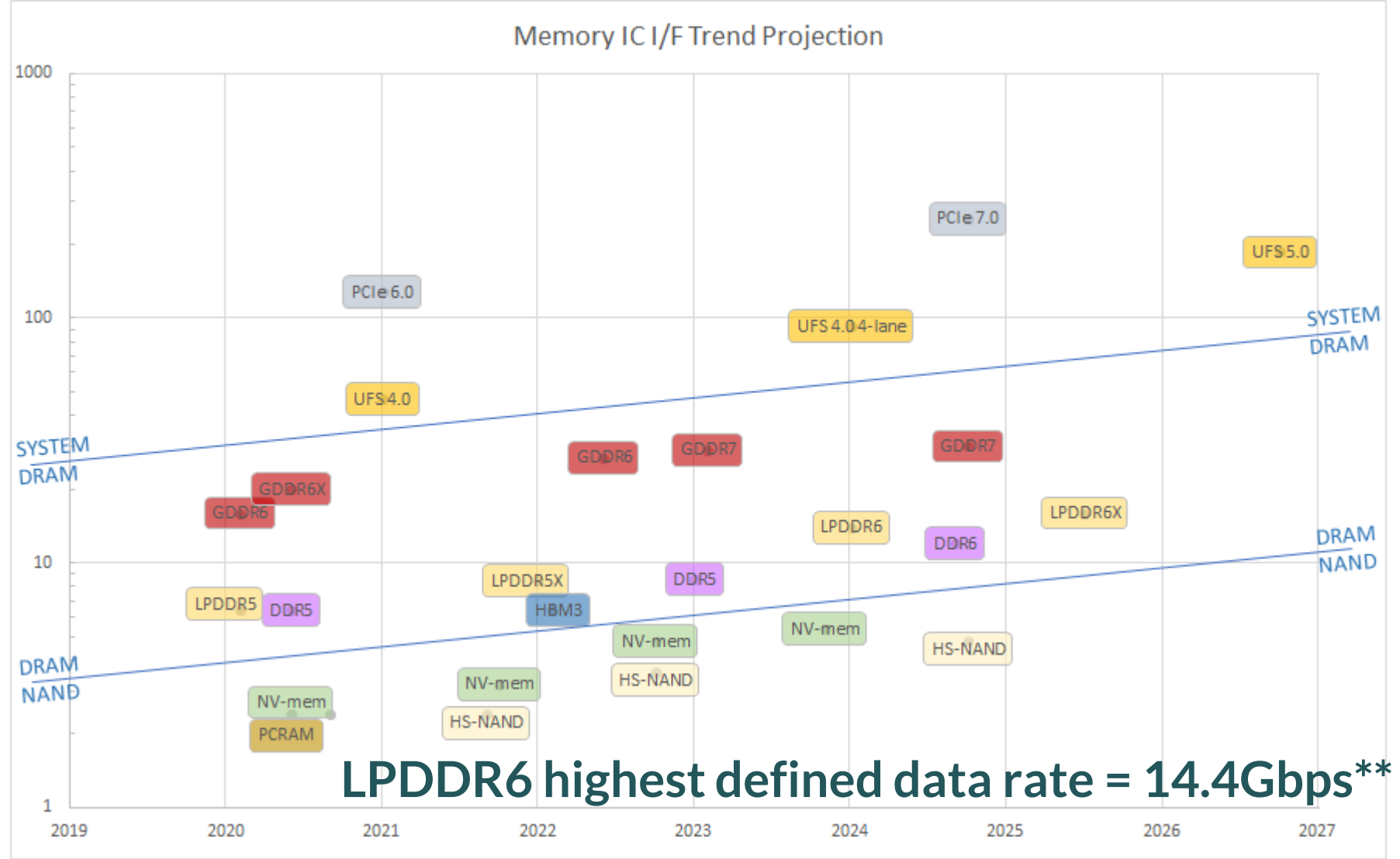




$$L \propto \frac{1}{d} \quad V_{xtalk} = L \cdot \frac{dI}{dt}$$

- Reducing pad pitch as die size shrinks, exacerbates cross-talk.
- Example B ideal case to minimize cross-talk.
- Any lessons from RF/other high-speed applications to apply to Memory probing?

Key Challenge: Speed Increasing*



LPDDR6 highest defined data rate = 14.4Gbps**

*https://eps.ieee.org/images/files/HIR_2024/HIR_2024_ch17_Test_Technology.pdf
**https://www.jedec.org/sites/default/files/Brett%20Murdock_FINAL_Mobile_2024.pdf

Summary / Conclusion

- High-speed wafer testing saves time-to-market for Memory Products.
- Volume monitoring key to accelerating design feedback.
- Continued advancement in probe card technology needed:

Challenge	Criteria / Target
Low PDN target	Component & probe count
Smaller pad size	Parasitic capacitance reduction
Tighter pad pitch	Cross-talk between probes
Higher speed	Device Datasheet Requirement

Questions?

Thank You