SWTEST
PROBE TODAY, FOR TOMORROW
2025 CONFERENCE

HPC & AI Probing Devices Require New Integration Schemes

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SW TEST | INTRODUCTION & MOTIVATION

TECHNOLOGY TRENDS

- 2.5D interposer, 3D stacking, hybrid bonding and CPO suppose increased I/O counts, decreased I/O pitch and I/O density increase at the package level

CHALLENGES

- WARPAGE due to complex heterogeneous integration and chip stacking.
- CTE mismatch: stress can affect the chiplet operation

INCREASING DEMAND

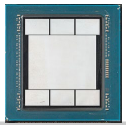
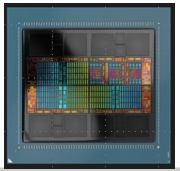
- Test intensity, test complexity and probe card demand increases
- Advanced packaging one of the main drivers for the probe cards market

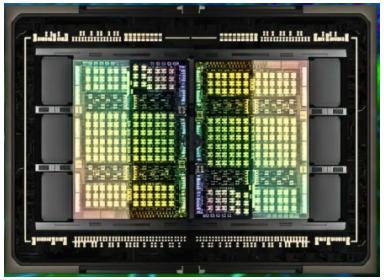
SECURITY & IP PROTECTION

- Highly confidential designs.
- Traceability efforts can be tackled with Die Annotation Feature

**REF: Yole, SWTest2024*

AI Processor Driving Chiplet Technology

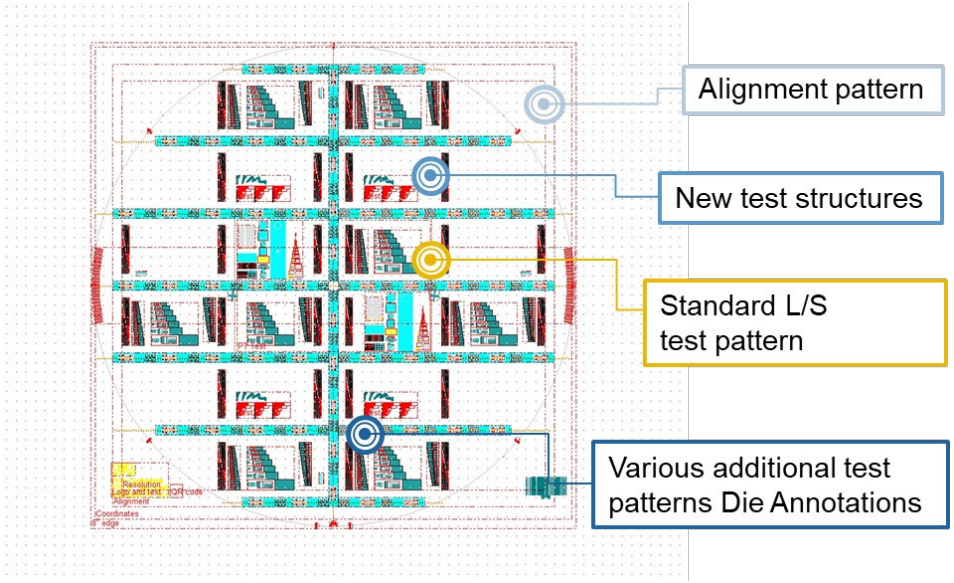


	NVIDIA A100	AMD MI300	AWS Trainium2	NVIDIA Blackwell Ultra
Announcement	2020	2022	2023	2025
Memory	80 GB	80 GB	96 GB	288 GB
Architecture	Monolithic GPU + HBM	4X Chiplet GPU + HBM	4X Chiplet GPU + 12 HBM	4X Chiplet GPU +12 HBM
Packaging	inFO	CoWoS®–S	CoWoS®–R	CoWoS®–L
GPU Die Size	32.3×25.78mm **1X reticle size**	4X 28.7×12.8mm **4.5X reticle size**	4X 32×21mm **5.5X reticle size**	4X 40×28mm **9.5X reticles size**

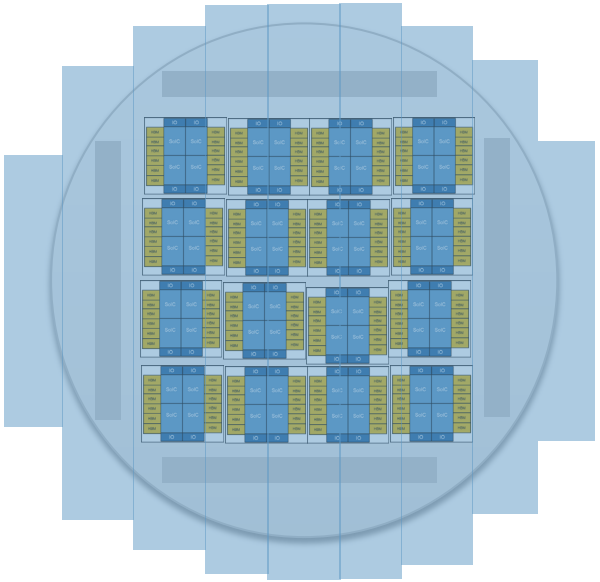
SW TEST | DIGITAL PATTERNING of FINE PITCH RDLs

NO LIMITS for DIGITAL PATTERNING

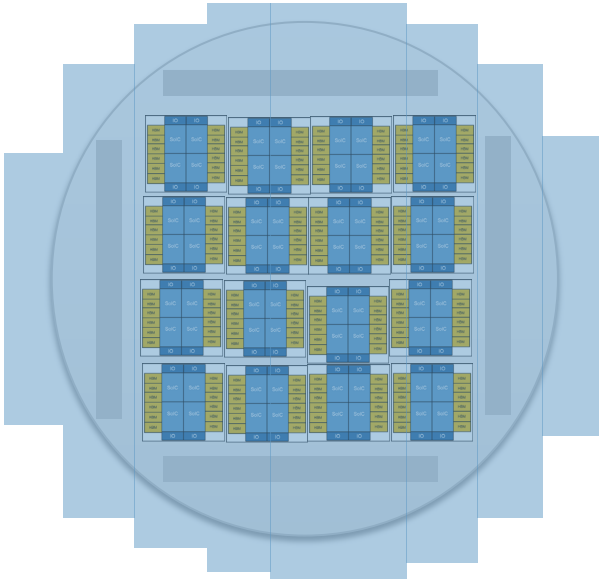
WAFER LEVEL



COMPLEX PACKAGE LEVEL



Comparison BEOL i–Stepper Technology

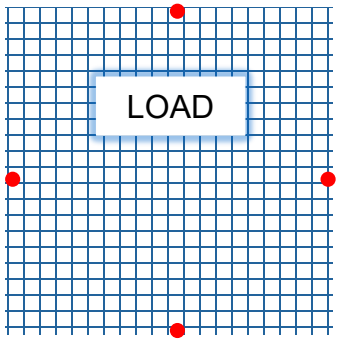


→For patterning of Large Dies: 160 stepper shots.
→Nikon stepper: 76 shots / 300mm wafers (200 wph).
→Throughput significantly decreases vs. nominal stepper throughput.

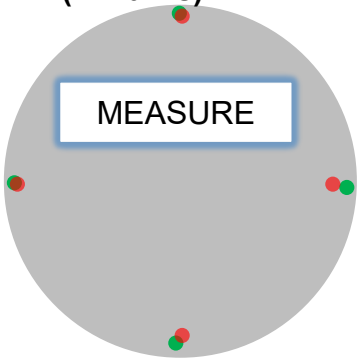
System [wph]	Package 120×150mm 9.5X reticles
i–line Stepper	30 – 100
Maskless exposure Next Generation LITHOSCALE® XT	Constant throughput

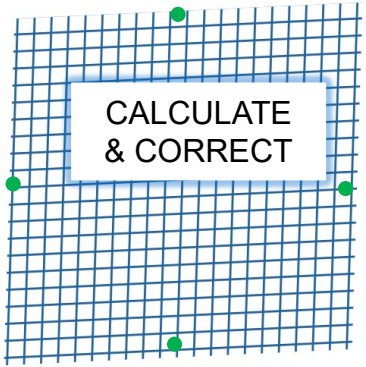
SW TEST | ALIGNMENT – 4 MARKS - STANDARD

Nominal mask file

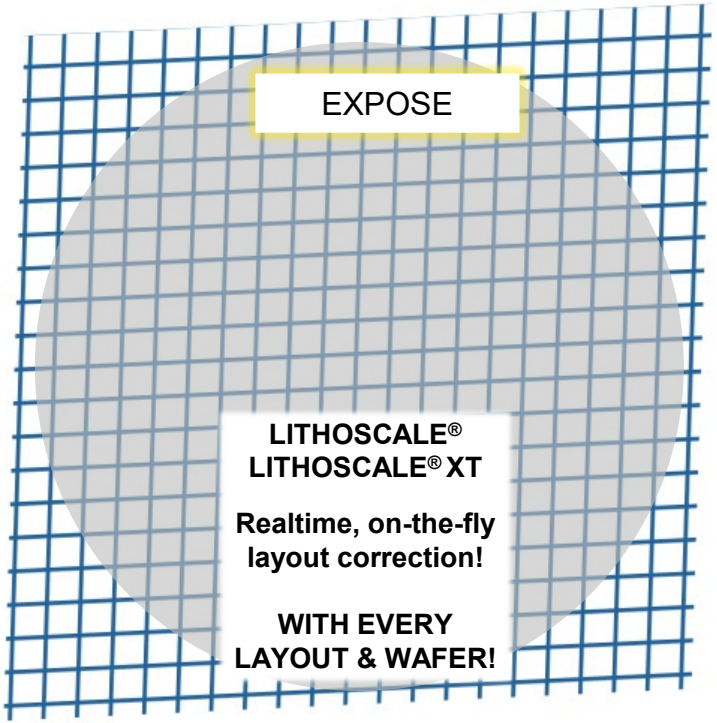


Microscope alignment (4 marks)

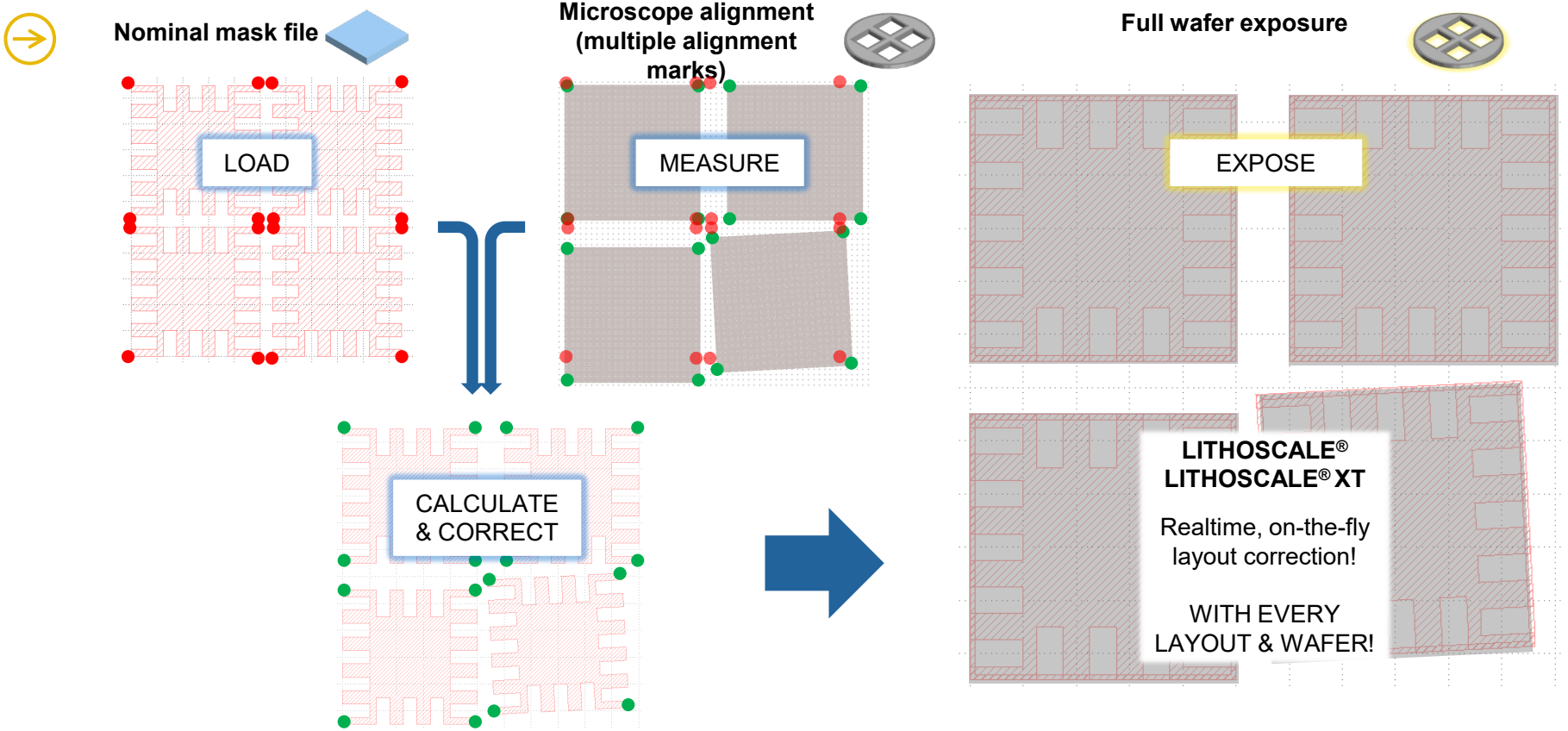




Full wafer exposure

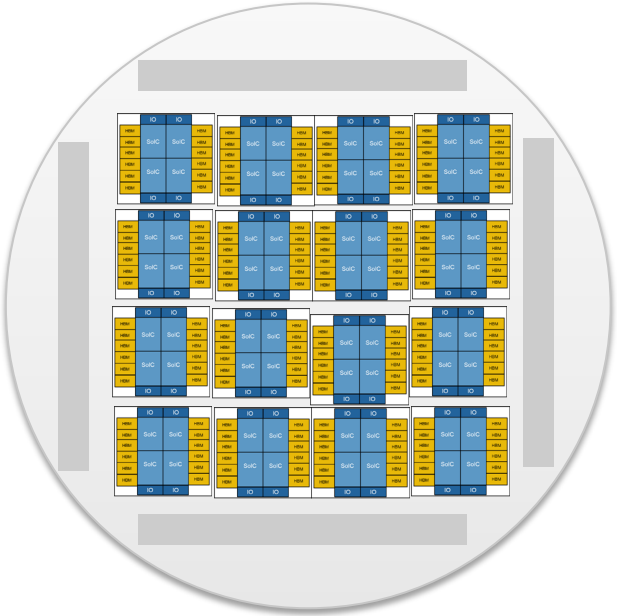


SW TEST | ALIGNMENT – 16 MARKS - DIE SHIFT APPLICATION

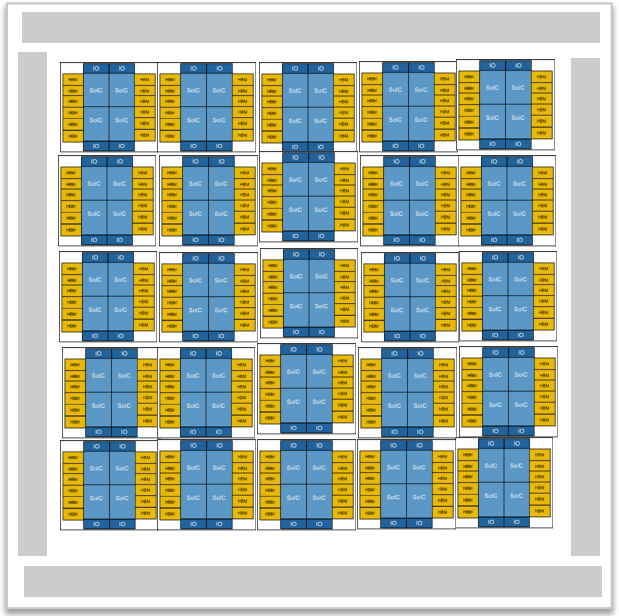


Transition from Round to Square Substrates: Higher Utilization

16 PACKAGES on WAFER
300mm wafer

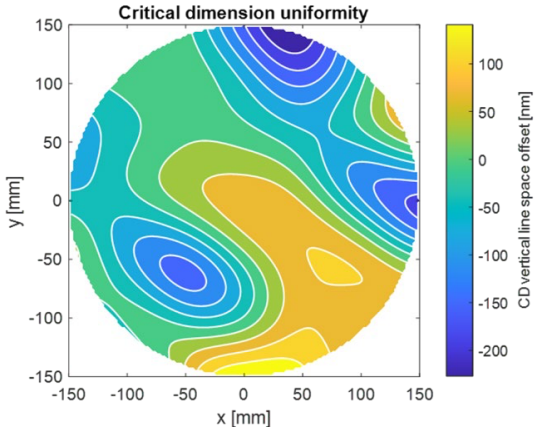


25 PACKAGES ON PANEL
300mm square

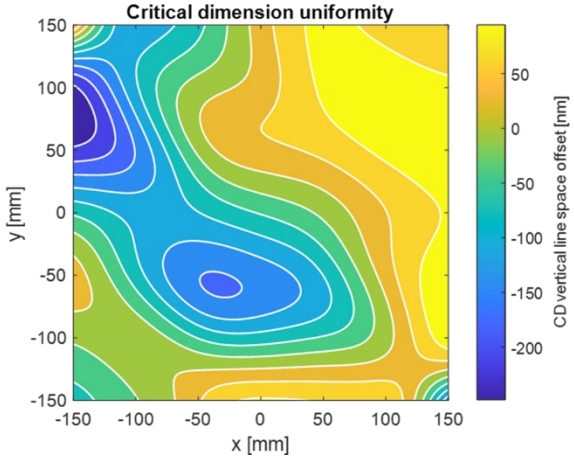


SW TEST | ADVANCED PACKAGING WLP vs. PLP

CD Uniformity at 10 µm L/S

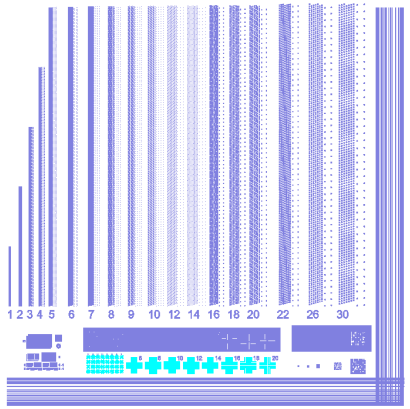


- CDU – contour plot of the critical dimension distribution evaluated as vertical line distance in writing orientation.
- Sampling was performed in a l→r, t→b raster scan fashion. No vertical striping is visible in the scan direction.



- CDU– contour plot of the critical dimension of the **300 by 300 mm² panel** evaluated via as above

PI High Resolution Test Matrix

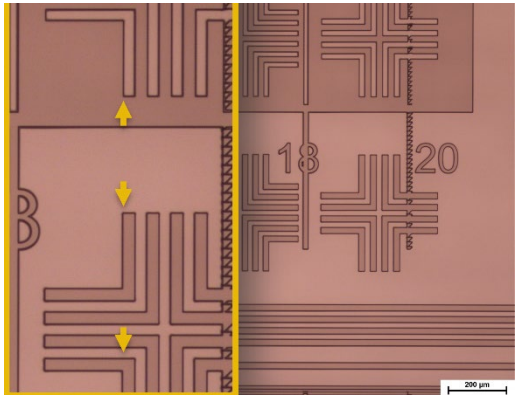


- Design layout is repeated with a period of 11mm in all four directions: dense VIA, isolated VIA, L/S patterns.

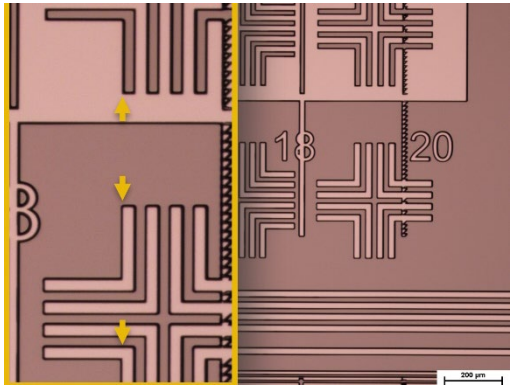
**REF.: ECTC2025*

SW TEST | ZERO STITCH & SIEMENS STARS

- High Resolution PI Patterned with active “**ZERO STITCH**” Software Feature
  - Stitching markers are activated on the left and right of the stitching line (superimposed line and row of triangles).
  - “Stitching line” is demarked by yellow arrows.

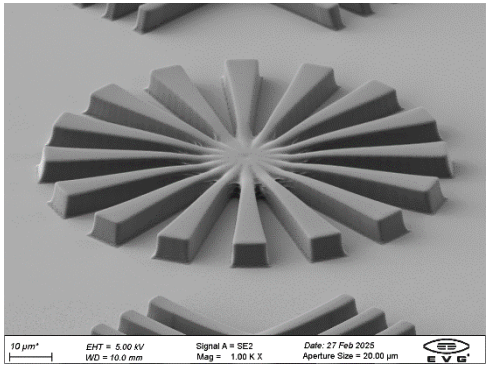


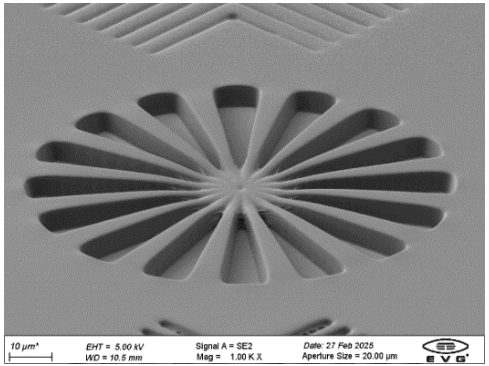
GLASS WAFERS



SILICON WAFERS

- SIEMENS STAR Patterning

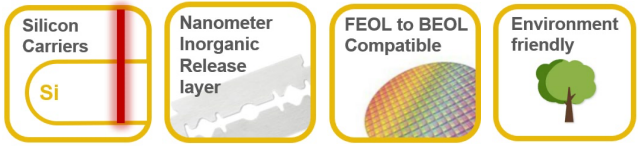




*REF: ECTC2025

SW TEST | 2.5D & 3D INTEGRATION NEW TECHNOLOGY

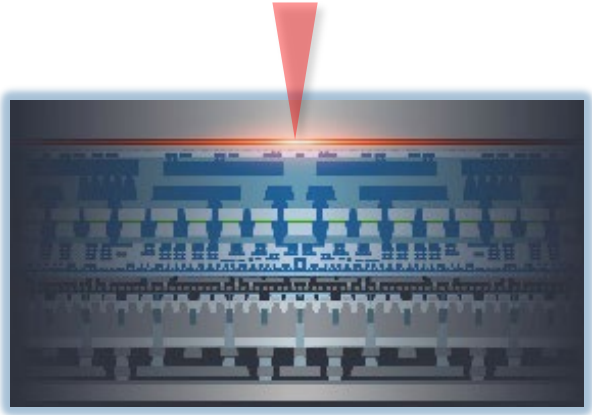
NEW CARRIER SOLUTION



- Enable temporary bonding on Si wafers
- High temperature stability >700 °C
- Precise control of debonding plane with laser energy
- Lower total thickness variation (TTV) then PoR temporary bonding solution.
- Carrier re–usability and cleaning options

REQUIREMENTS SET for LAYERRELEASE™ on Si carrier

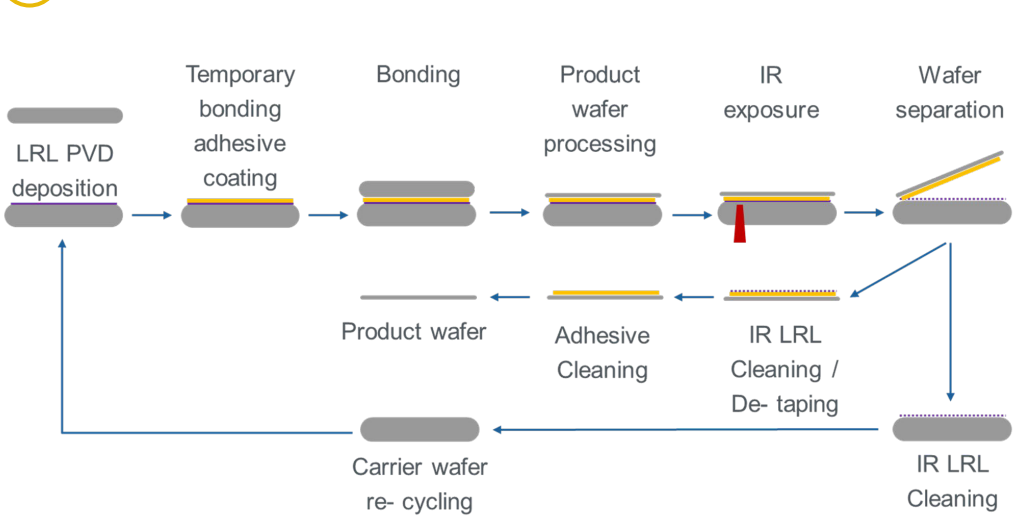
- Low TTV: <100 nm
- High temperature stability 700 °C
- Optimized interaction wit IR Laser: high IR absorption
- Shielding of product wafer

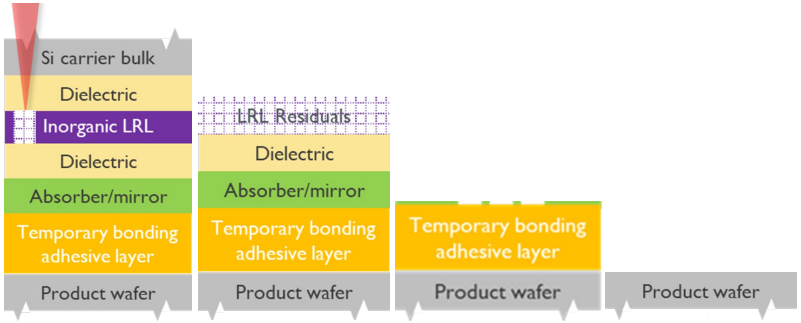


SUSTAINABILITY – eco friendly cleanability of LRL residuals

**REF.: ECTC2024*

PROCESS FLOW





IR exposure of TB bonded stack

Debond interface after lift–off

After APM/ de–tapping

After adhesive solvent cleaning

1) LRL Deposition on Carrier	2) Bonding	3) Backside Processing	4) Layer Release	5) Cleaning
→PVD →CVD	→Fusion →Adhesive bonding	→Thinning →Hybrid bonding →Overmold	→Pre- alignment →Exposure → Lift off	→Wet Clean →CMP →Dry Etching

*REF: ECTC2025

SW TEST | CONCLUSIONS & OUTLOOK

Fine Pitch Probe Cards for HPC / AI Devices

- High pitch, high density RDL processing efficiency.
- Data driven patterning has no limits in large die size patterning.
- Warpage management.

EVG's LITHOSCALE®

- Supports rapid R&D prototyping, faster tape–out and faster response to the customer changes.
- CoO improvement vs. mask based technologies

2.5D/3D integration processes

- RDL First / CHIP LAST approach in probe manufacturing.
- The industry established TB/DB technology can be replaces by novel IR laser layer release processes.

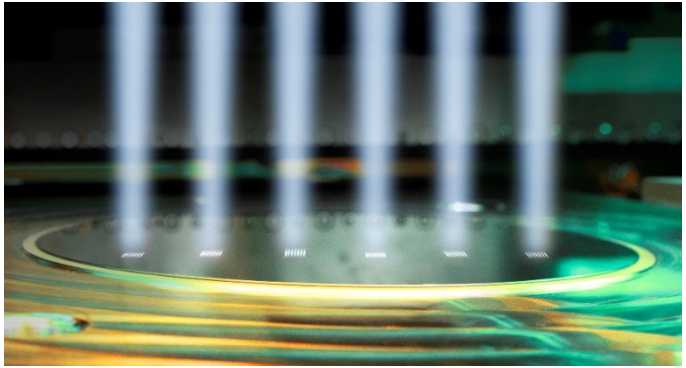
EVG®880 IR Laser LayerRelease™

- Lower TTV, High Temperature processes, Si carrier
- Compatibility with FEOL processes
- Sustainability in the semiconductor supply chain.

SW TEST | LITHOSCALE® XT New Product Launch

High Throughput, High Resolution <2 µm L/S Digital Lithography System

- Wafers up to 300, panels 300×300mm square
- Dual stage concept, six exposure heads
- Parallel data processing and writing.
- Topside, visible light, reflective IR alignment.



GLASS WAFERS
TOP TILTED VIEW
patterned with BLACK RESIST

Thanks for your Attention !

- **Contact the EVG Team with any questions …**

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