SWTEST
PROBE TODAY, FOR TOMORROW
2025 CONFERENCE

Athena PCA

A new generation Probe Card Analyzer for large area and high load devices

Ligi Milazzo [1], FedericoTresoldi [1], Federico Mariani [1], Antonio Rinaldi [1], Gabriel Gedler [2], Davide Appello [1]

(1) TECHNOPROBE

(2) intel

Athena

34th SWTest Conference | Carlsbad, CA, June 2 – 4, 2025

Agenda

1. Motivations to develop a new probe card metrology tool
2. Athena PCA project goals
3. Probe card analysis: Test objectives review
4. Architectural details and results
5. Status and next steps
6. Conclusions

1.1 Probe cards Vs legacy PCA performances

Leading edge performances probe cards

Legacy PCA support space

Memories

DRAM

NVM/other

NON-Memories

HBM

Advanced Logic

MEMS

Power

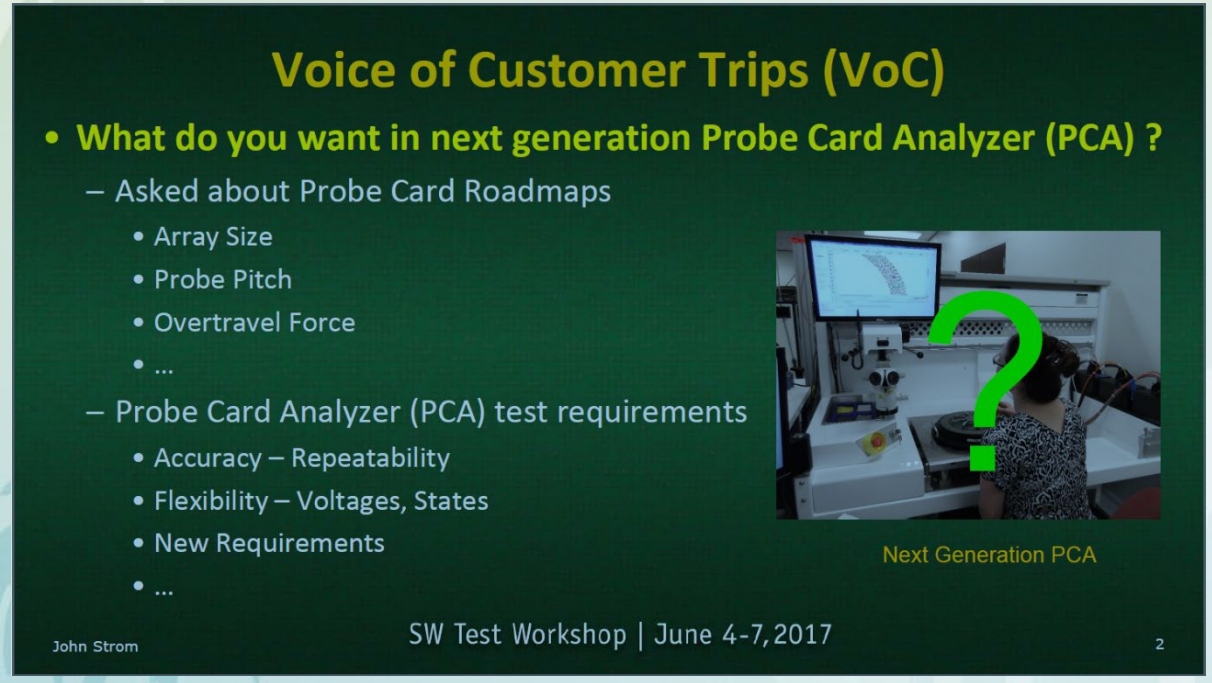
RF

CMOS Image Sensor

Photonics

Accuracy

1.2 What was said at SWT 2017



- Recognised a growing performances gap between existing PCA and new PC certification needs
- Identified key parameters
  - Array size
  - Pitch
  - Force
  - Channel count
- Highlighted higher level requirements
  - Accuracy
  - Repeatability
- Reproducibility has been included among requirements

2.1 Athena PCA project goals

Lack of adequate market offer

Incumbent equipment main suppliers no more developing roadmap: **ensure testing the tester!**

Performances matching

Support high pin count and force, large array size with high position accuracy: **new market needs are here!**

Tool/tool correlation

Ensure results correlation between equipment instances: **essential to support large scale operations**

Multi-domain

Mechanical, Electrical and Optical: **check concurrently the performances**

2.2 Athena PCA project goals

- Designed consider long-term roadmap PC requirements
- Considering multiple usage models
  - Probe card manufacturers
  - IDM and OSATs
- Satisfying
  - High volume / high throughput needs
  - Debugging / engineering
- Enabling re-use of legacy investments on motherboards

3. Test objectives review

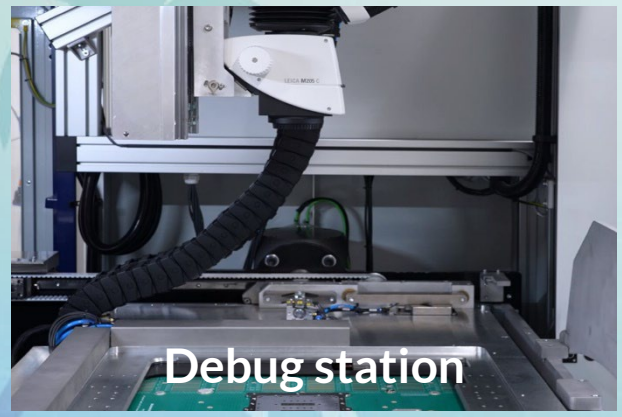
Test	Domain		Unique to ATHENA	manufacturers	End users
PCB test	E	Test		X	-
XY probe position	O	Test		X	X
Z probe position					X
Board components che Cap leakage, passive component					-
Path resistance					X
Array force (vertical)					-
Array force (lateral)					-
Probe lateral movemen					X
Activation, run-in & cle					-
Connection check					X
OverTravel test					X
AOT/POT					X
Loopback through inde					X
3D probe tips analysis	O	Test	X	X	X
Multi-array probe card test	E/M/O	Test		X	X
Probe Head only test	O/M	Test		X	-
Debug	E/M/O	Test		X	X

Capabilities unique to Athena PCA Vs Legacy

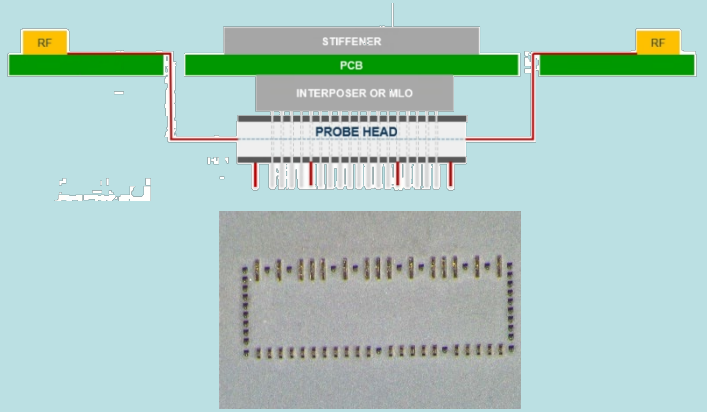
- Z probe position (optical)
- Array force (vertical)
- Array force (lateral)
- AOT/POT
- Loopback through independent flying probes
- 3D probe tips analysis

4. Architectural Details & Results

General Features



PC with embedded RF pins



Motion system based on high planarity granite

4.1 Architectural Details & Results

Experimental Results: Data Sources

Utilization by tool type

Mother boards	Channel count	Number of cards tested
93K	9218	Multiple units
Custom ATE 1	2304	x100
Custom ATE 2	9218	x100
MB from legacy equipment	Up to 9218	Multiple units

Probe cards examples

Probe card	Pin count	Array size	Force
PC-A	51K	51700x47000	144kg
PC-B	160K	43500x65000	280kg
PC-C	40K	FWA 12”	100kg

4.1 Architectural Details & Results

Data from Experimental Results

Tested performances

Test name	Methodology	Range	Repeatability	Accuracy	Run rate	
Optical alignment in XY by 3D inspection	White Light interferometer	300 x300 mm^2	sigma = 0.2um	0.5um/300mm	2.6	sec/mm^2
Optical planarity	White Light interferometer	0.30 mm	sigma = 0.15um	<0.4 um/1mm		
Electrical planarity (loaded):probe height	By loading the array with a conductive plate	300 x300 mm^2	sigma <0.35 um	0.5um/1mm	Up to 1	Sec/Z step
Electrical planarity (loaded):array tilt		300 x300 mm^2	sigma < 10urad	<60urad	As above	
Cres		0-200ohm	sigma=0.15 ohm	< 0.2% Full range	0.026	sec/channel

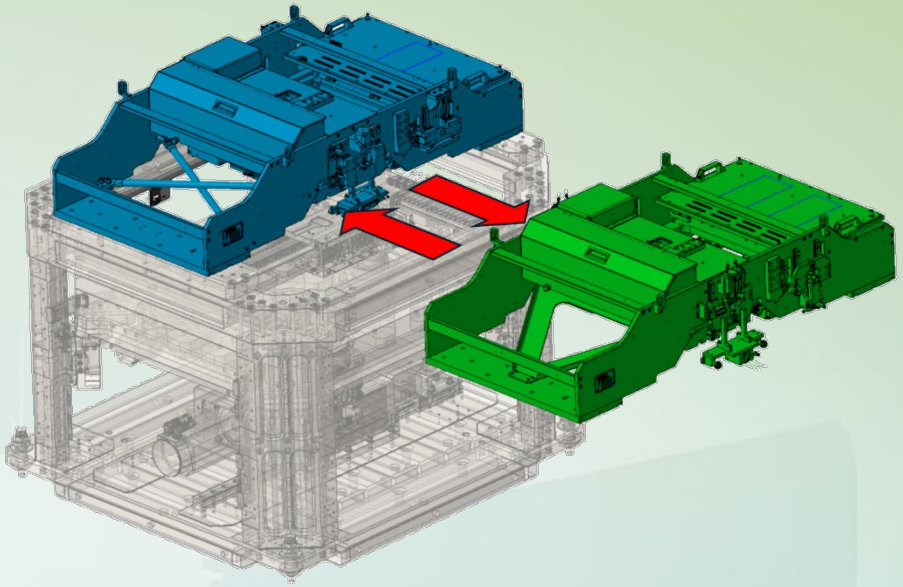
Probe Card PC-A

	Repeatability		Acquisition Time	
Meas ID	**Athena**	**Legacy**	**Athena**	**Legacy**
Optical Alignment @WLI	X sigma = 0.17 um Y sigma = 0.17 um Z sigma = 0.08 um	X s= 0.66 um Y s= 0.32 um Z s= n.a.	90 min	240 min
Loaded Electrical Planarity @Plate	Z sigma = 0.34 um	Z s = 0.827 um	down to 5 min	10 min
Cres @Plate	Cres sigma = 0.1 ohm	Cres s = 0.26	90 sec	n.a.

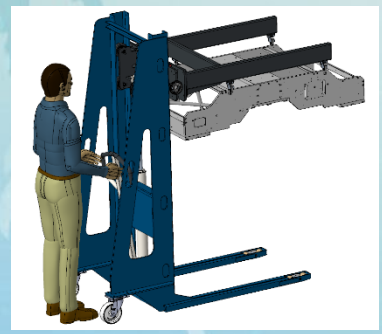
4.2 Architectural Details & Results

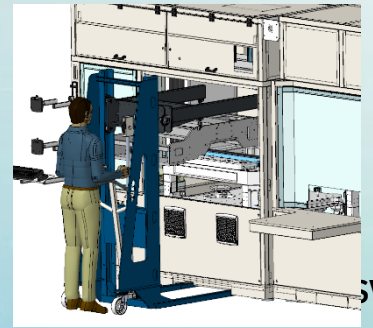
Exchangeable / swappable motherboards and planarity compensation

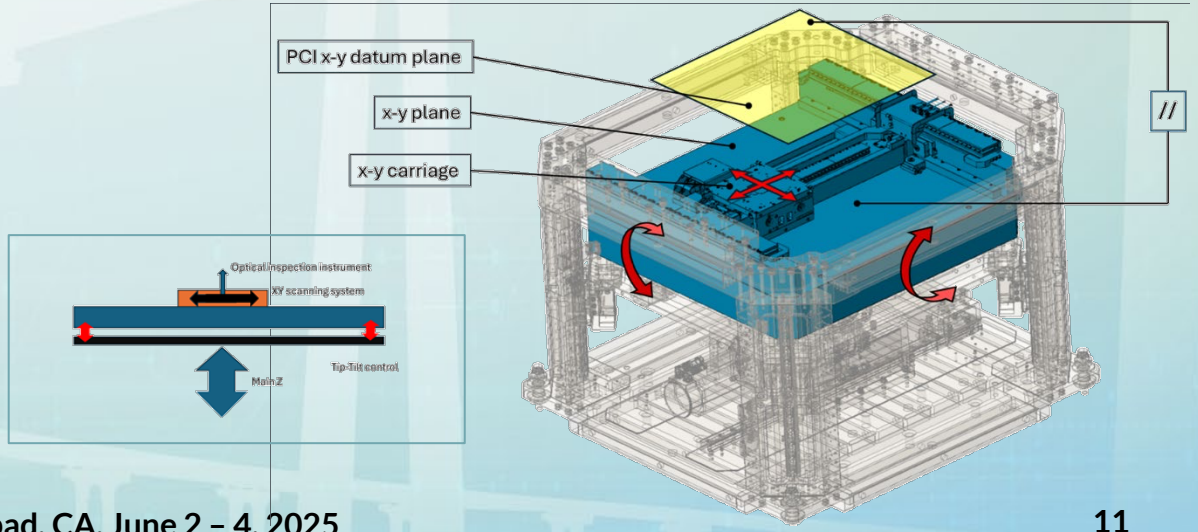
- Motherboards are replaceable
  - Semi-automated tools available



- Motherboard planarity compensation
  - Easy usage of motherboard compensating marginalities
  - Reducing impact of calibration time



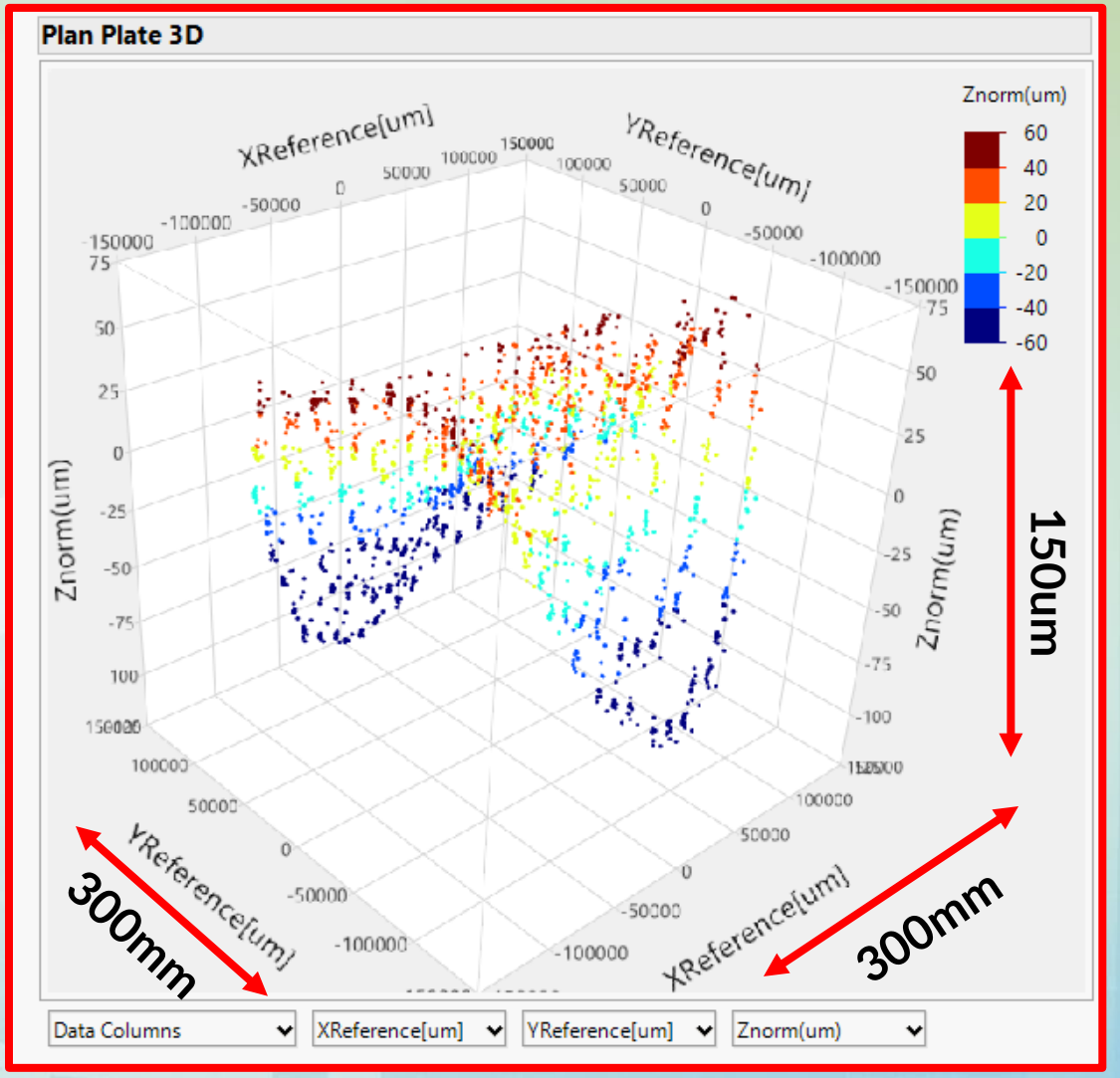




4.3 Architectural Details & Results

3D Morphology analysis with interferometer

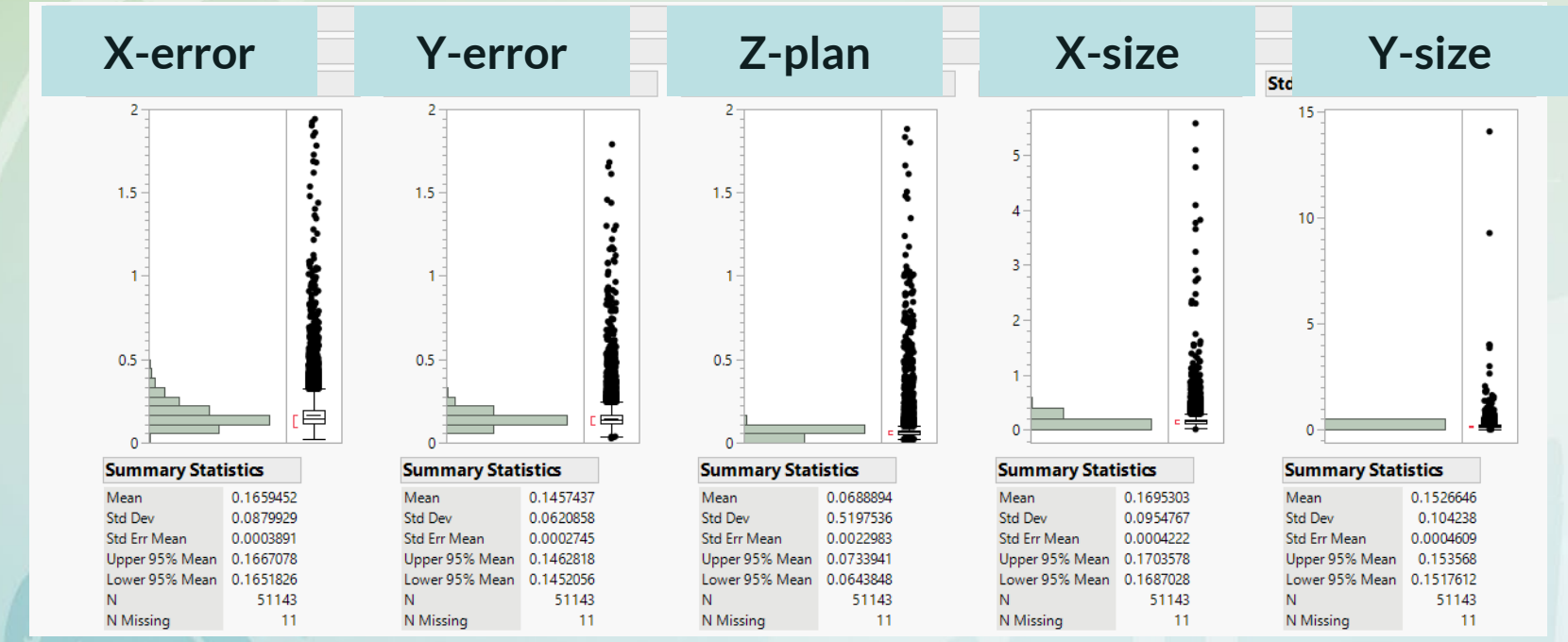
- Higher resolution and accuracy on Z evaluation
  - Up to 40 nm resolution
- Morphology evaluation of probe with features
- Accurate pointed probe diameter measurement
- WLI specifications
  - FOV 890x830 um
    - 1024 X 1102 Pixel
  - 0.81 um lateral resolution
    - max MTF 0.3 lp/pxl

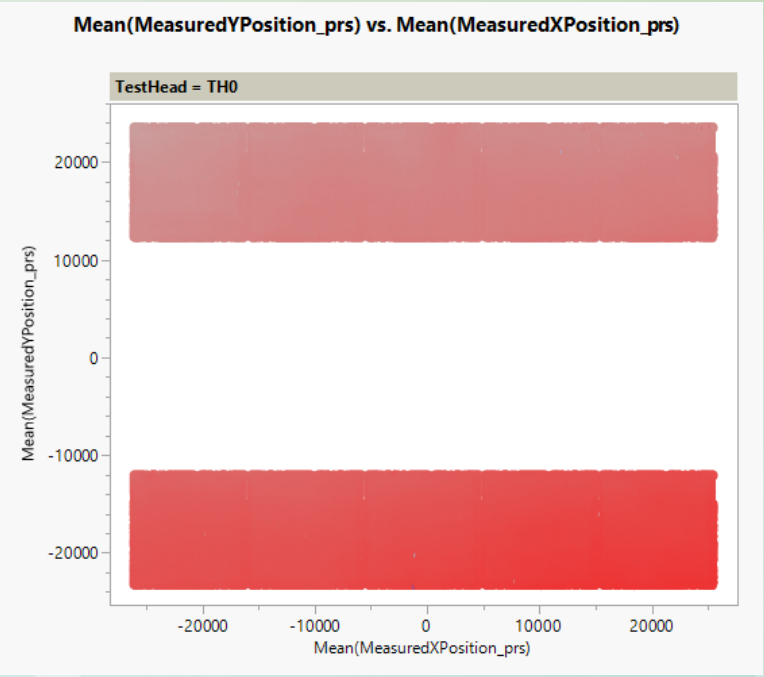


4.3 Architectural Details & Results

High pin count/ density PC: morphology analysis

PC-A – Results from 10 repetitive measurements





Mean Sigma 165,94nm

Mean Sigma 147,4nm

Mean Sigma 68,88nm

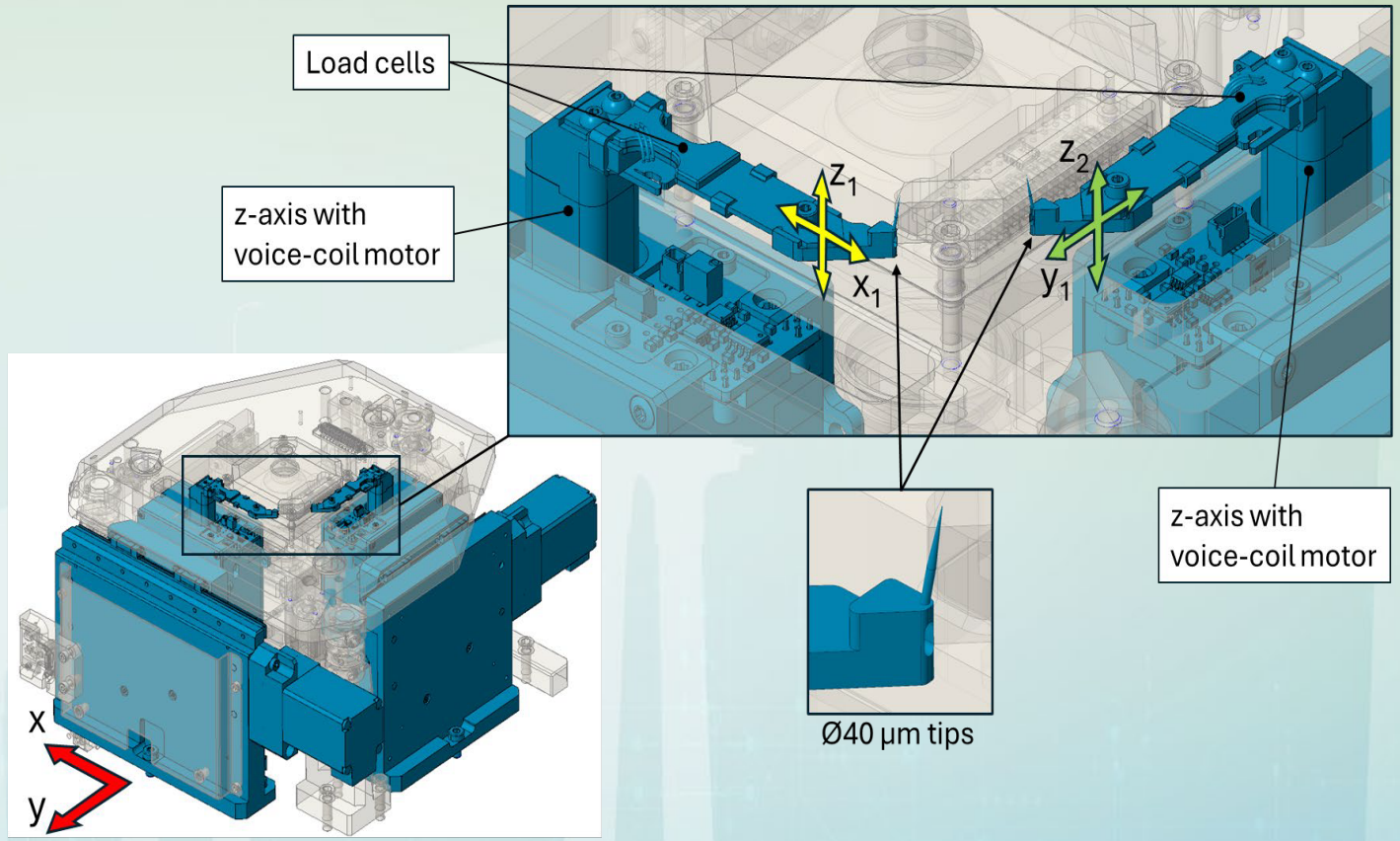
Mean Sigma 169,53nm

Mean Sigma 152,66nm

4.4 Architectural Details & Results

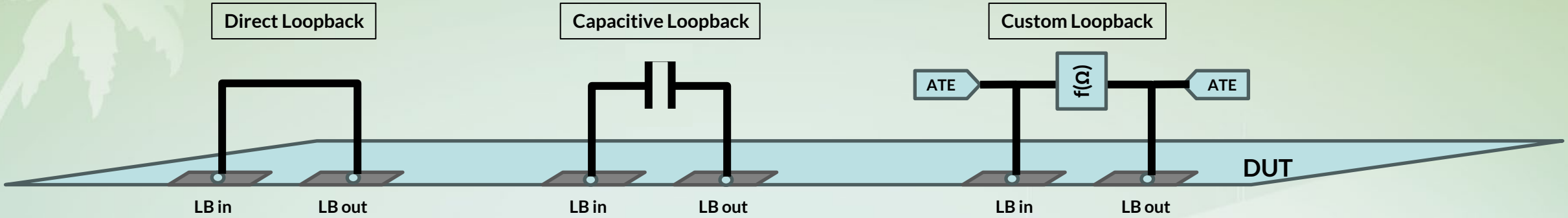
Unloaded Planarity & LB Measurement: high speed/resolution posts

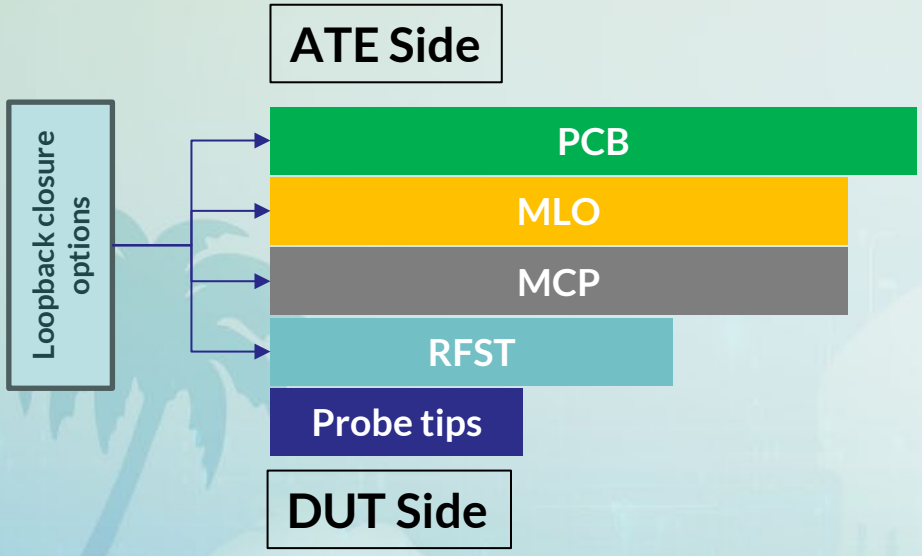
- The archictecture supports two fully independent posts
  - Up to 1um repeatability in Z planarity detection
  - Minimum pitch capability of the tool: 25um
  - Minimum pitch with 40um diameter tips: 50um
- Fast motors
  - Up to 10 probe/sec/post
- A load cell is integrated for spring force evaluation
  - Up to 10gr



4.4 Architectural Details & Results

High speed/resolution posts: loopbacks test

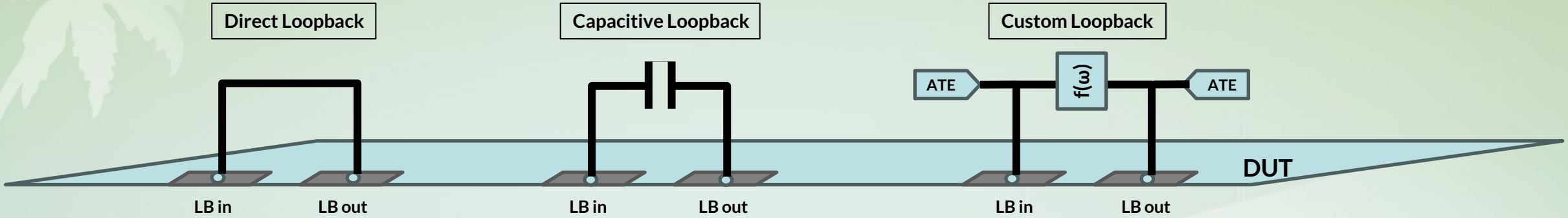


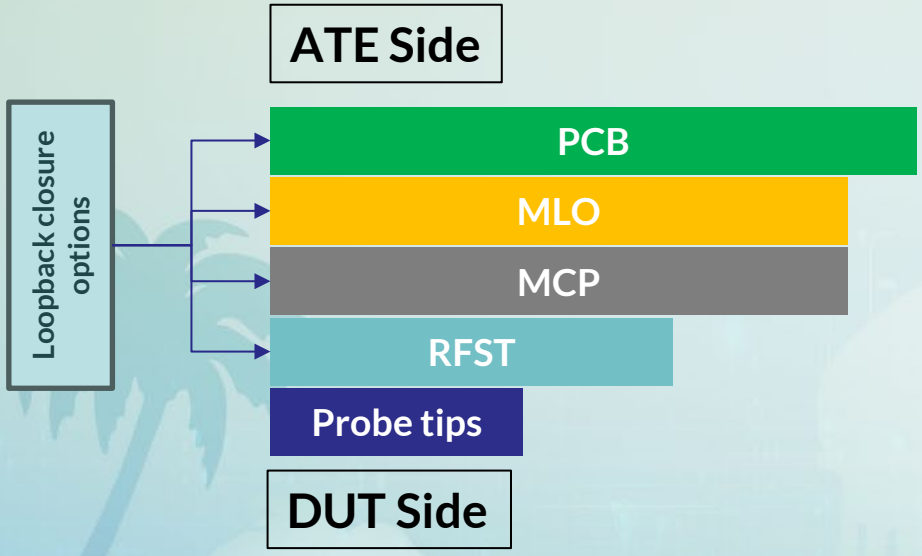


- Multiple loopback variants:
  - Direct, capacitive or with custom circuit (including switches and/or active)
  - Different levels/layers of the probe card where the LB is realized
    - On RFST or MCP on plate (direct and capacitive)
    - On the MLO or PCB for capacitive / custom

4.4 Architectural Details & Results

High speed/resolution posts: loopbacks test





4.5 Architectural Details & Results

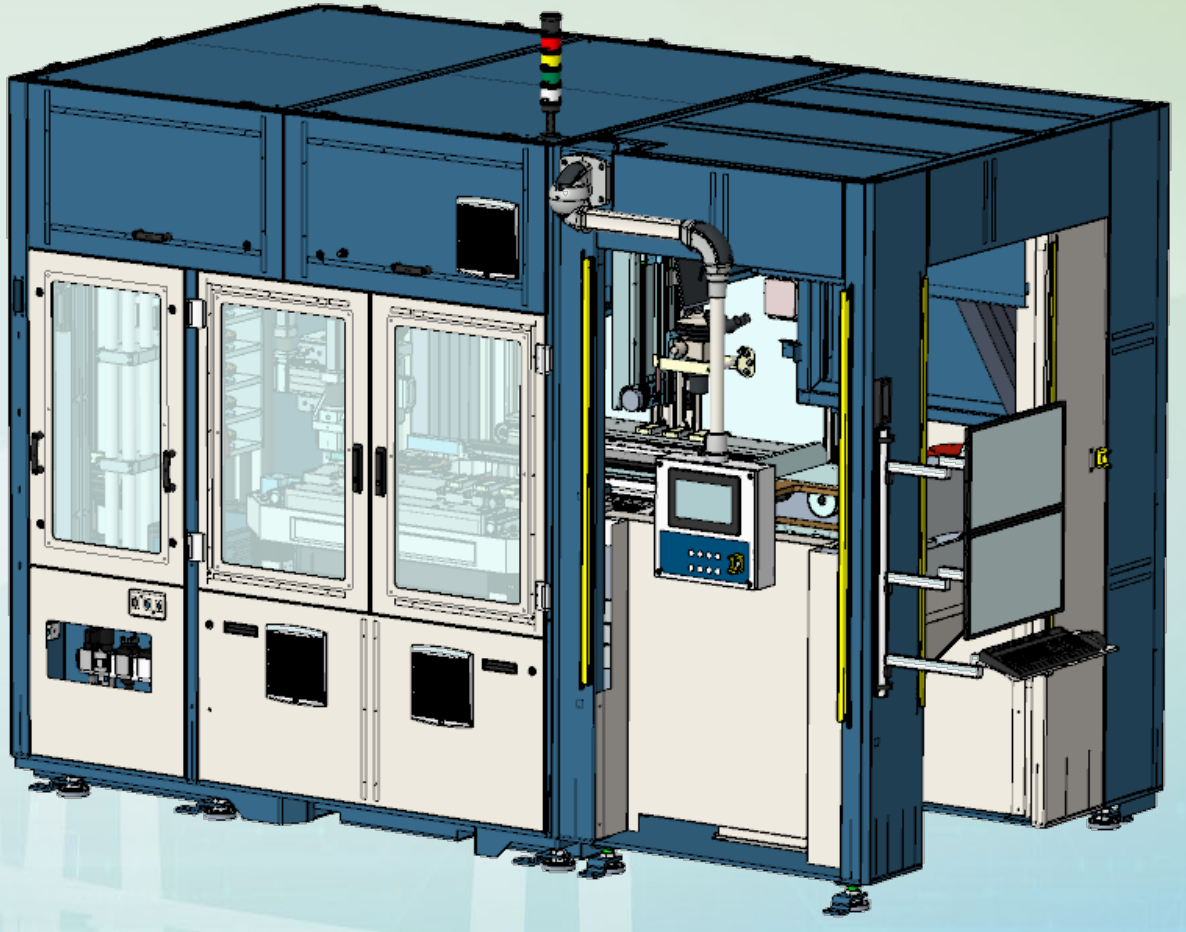
Debugging features

- Re-use of legacy motherboard design
- Automated MB transition from the metrology module to the debug module
- The probe card loads manually while the motherboard is in “live bug” status
- Automation support motherboard rotation to “dead bug” orientation
  - The motorized microscope moves on the array to inspect.

Media plate exchanger module

Base machine: Metrology module

Optional module debug station



4.5 Architectural Details & Results

Debugging features

- Re-use of legacy motherboard design
- Automated MB transition from the metrology module to the debug module
- The probe card loads manually while the motherboard is in “live bug” status
- Automation support motherboard rotation to “dead bug” orientation
    - The motorized microscope moves on the array to inspect.

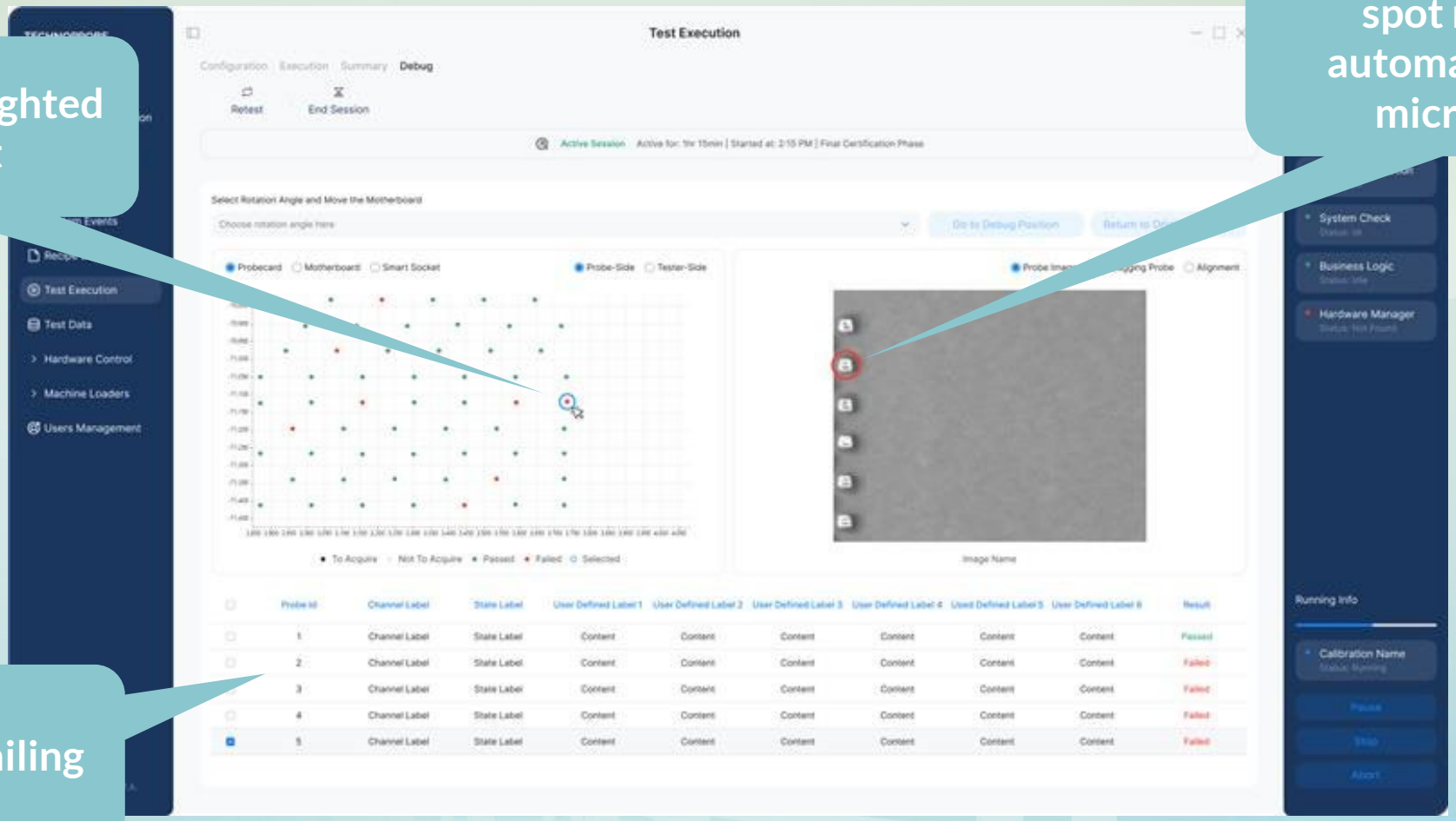
4.5 Architectural Details & Results

Debugging features: navigation automation

Athena BY TECHNOPROBE

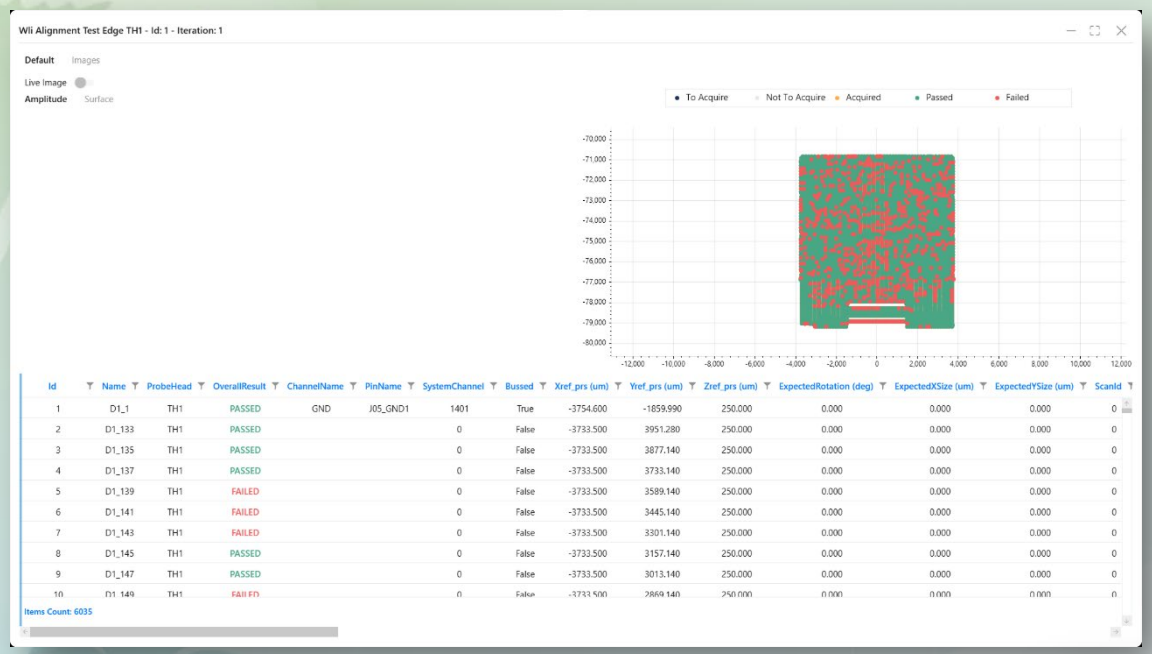
Fail probe highlighted during test

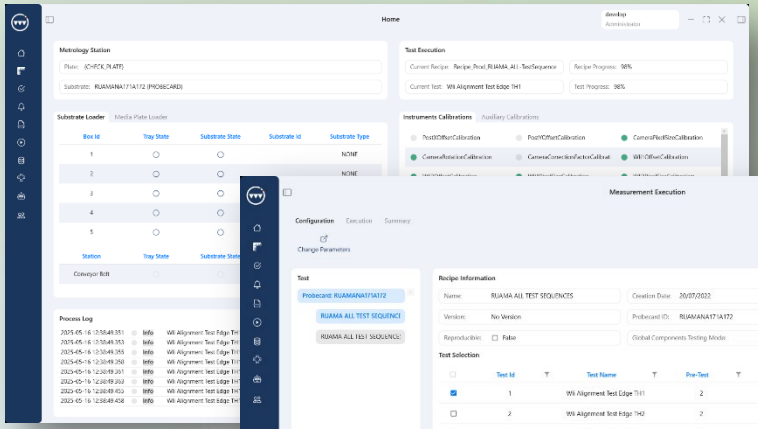
Image of targeted spot reached automatically by microscope

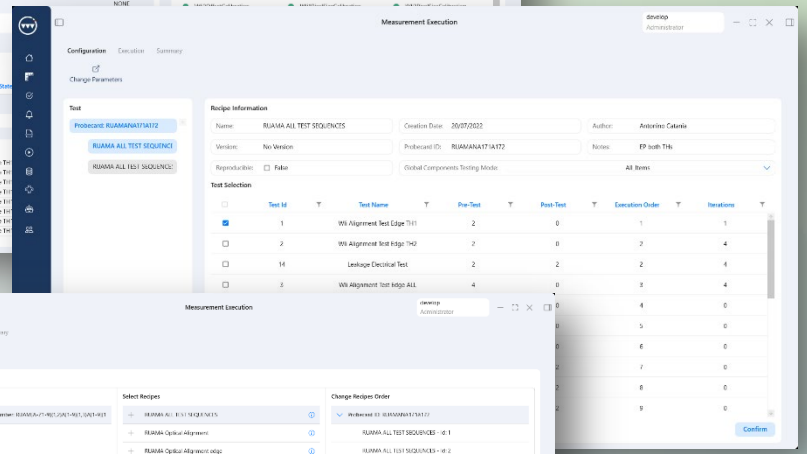


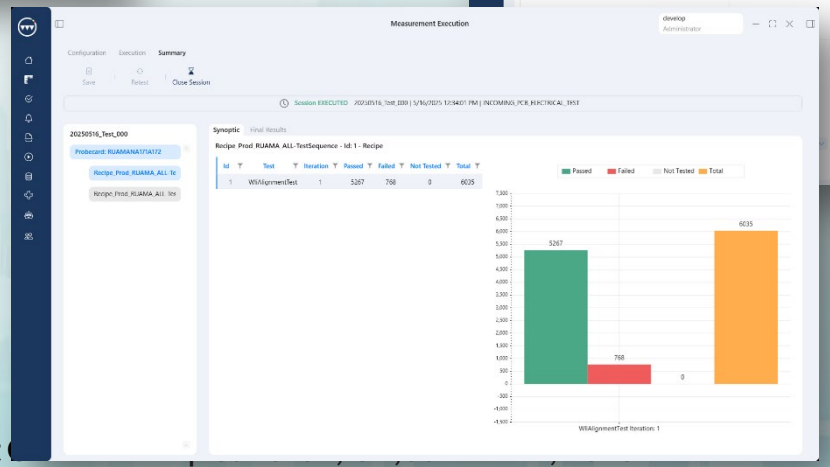
Diagnostic information of failing probe sites

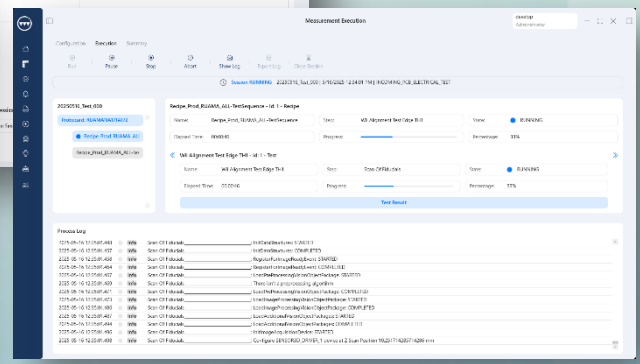
GUI Snapshots











5. Athena PCA Status and Next Steps

- Two versions/options available
  - Autoloader
  - Debug station
- Fully engineered by Technoprobe
- Customization ability
- Install base
  - Five systems deployed at customer sites
  - Five systems in use in the Technoprobe shop floor, planned 20+
  - Three system available for engineering developments
- Lead time and capacity
  - Production CT is currently of 6Mo
  - Scalable operations setup, with short supply chain

- Certifications Received by the Equipment
  - NFPA79
  - Semi S2
  - Semi S8
  - CE
    - Including EMC/EMI specific checks
- Shop floor integration
  - SECS/GEM supported
- Next steps
  - Continously enhancing the engineering features
  - Evaluating customization requests
  - Voice of customers feedback

6. Conclusions

- Advanced logic and memory chip demands
  - Finer pitch interconnect probing
  - Higher pin count
  - Higher loading force
- Since few years, legacy PCA performances are falling behind probe card demand for comprehensive certification
- Athena PCA aims supporting the PC roadmap in the long term
  - Enable complex test objectives, like
    - Force analysis (vertical and lateral), loopbacks test with flying posts, POT/AOT
  - Fit with multiple use model and cost constraints
    - End-of-production line certification
    - High throughput operations for HVM
    - Engineering and debugging
    - Reuse of legacy MB

We are available to demonstrate the tool using your probe card!

SWTEST
PROBE TODAY, FOR TOMORROW
2025 CONFERENCE

Thank You!

TECHNOPROBE

Athena

Athena PCA with Autoloader