SWTEST

PROBE TODAY, FOR TOMORROW

2025 CONFERENCE

Tester on a Probe Card

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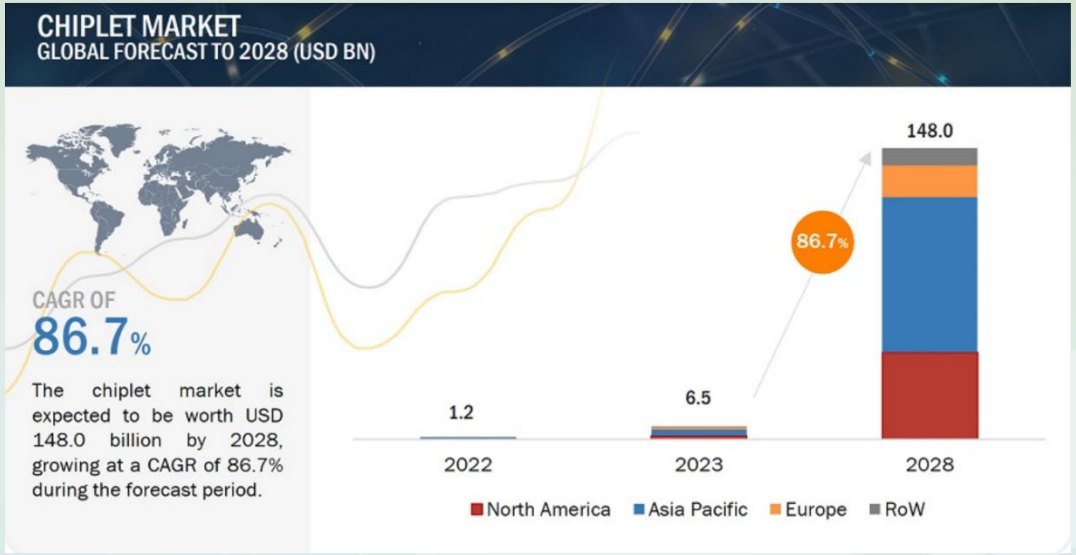
Presentation Overview

1. Forecast for Chiplets and how did we get here
2. Why Chiplets are the way forward
3. Impediments and Challenges – to Chiplet success
4. Tester on a Probe Card: A unique approach to addressing a barrier to Chiplet success
5. Examples and Conclusion

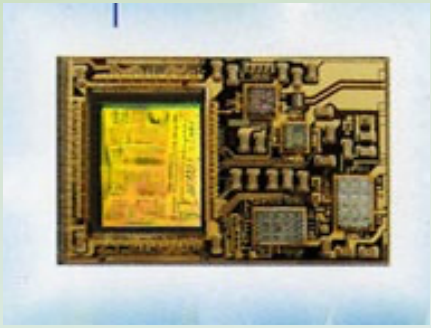
Projected Chiplet Growth

- Projected growth in the Chiplet market varies from positive to very positive



- **BCC Research:** "The global market for Chiplets was valued at $5.3 billion in 2023 and will reach $42.8 billion by 2029, growing at a CAGR of 41.9% from 2024 to 2029
- **InsightACE Analytic:** "The Global Chiplet Market is valued at US$ 5.03 Bn in 2022, and it is expected to reach US$ 633.38 Bn by 2031, with a CAGR of 71.3% during the forecast period of 2023-2031"
- **Tech Insights:** "Revenues for the compute Chiplet market will grow from $43.5 billion in 2024 to $144.9 billion by 2030 at a CAGR of 31% "

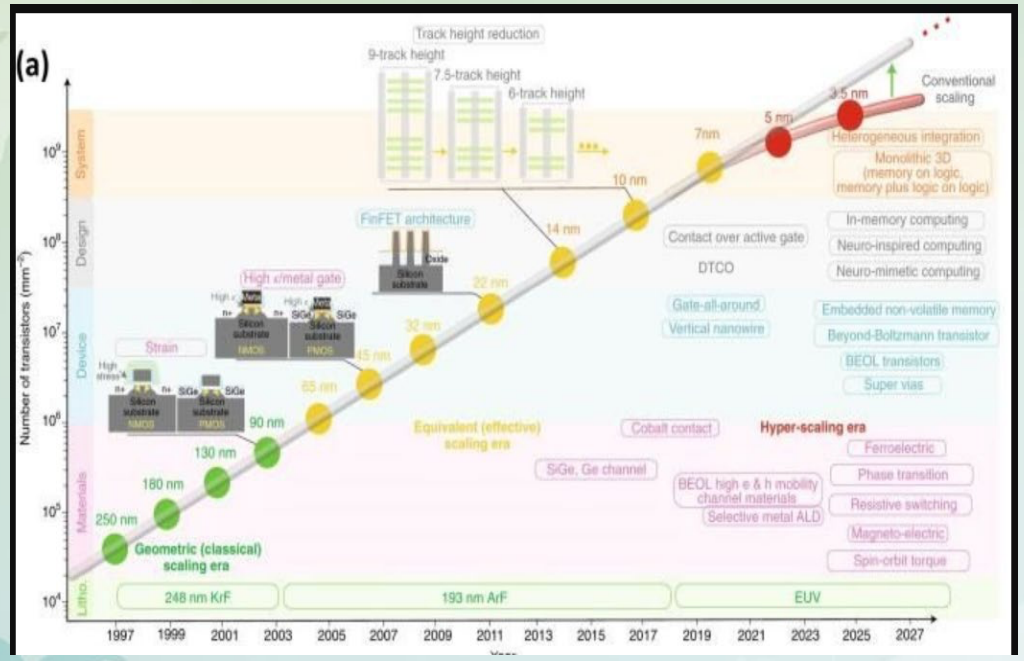
Chiplets are Not New

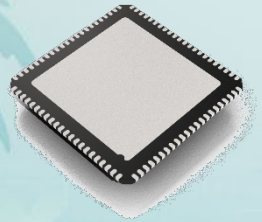


https://www.chiphistory.org/landmarks/hp-93000-soc-series

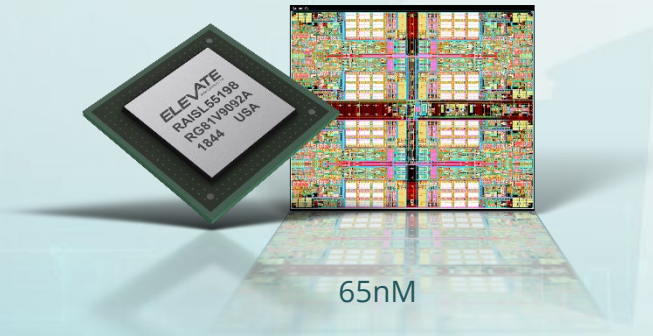
- We presented a paper last year on using Chiplets to leverage IP to create customizable solutions for ATE
- In 1999 - Tester on a chip included:
  - Formatter
  - Error
  - Test Period Generation
  - Timing Generators
  - Level Generation
  - Pin Electronics (1Gbps)
    - Driver comparator load (HV Complementary Bipolar)
  - PPMU – (3uM CMOS)
- MCM packages were expensive to manufacture
- Comprehensive test at probe was difficult
- “Big Iron” testers sold for $1M+ (2-9k per pin) so it was viable

Shift to Monolithic SOC IC





350nM

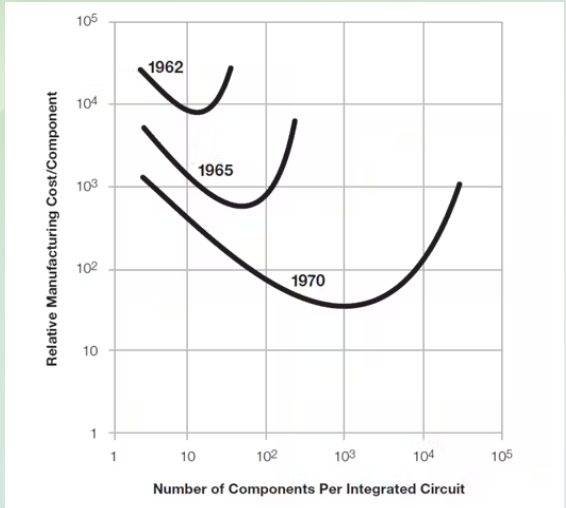


65nM

- **Monolithic SOC Takes off!**
  - CMOS made great strides in device offerings – CMOS, LDMOS, BiCMOS
  - CMOS offered roadmap that allowed companies to pin product roadmaps to process technology roadmap.

  Examples:
    - **Intel**
      - Pentiums (0.8um - 65nM) to
      - Core i7 down to 14nM
    - **Elevate**
      - PE DCL,PPMU, Timing
      - 200Mbps dual to 1.6Gbps Octal

Moore’s Law Stalls



1. Image from “Cramming more components onto integrated circuits,” Gordon Moore, 1965.

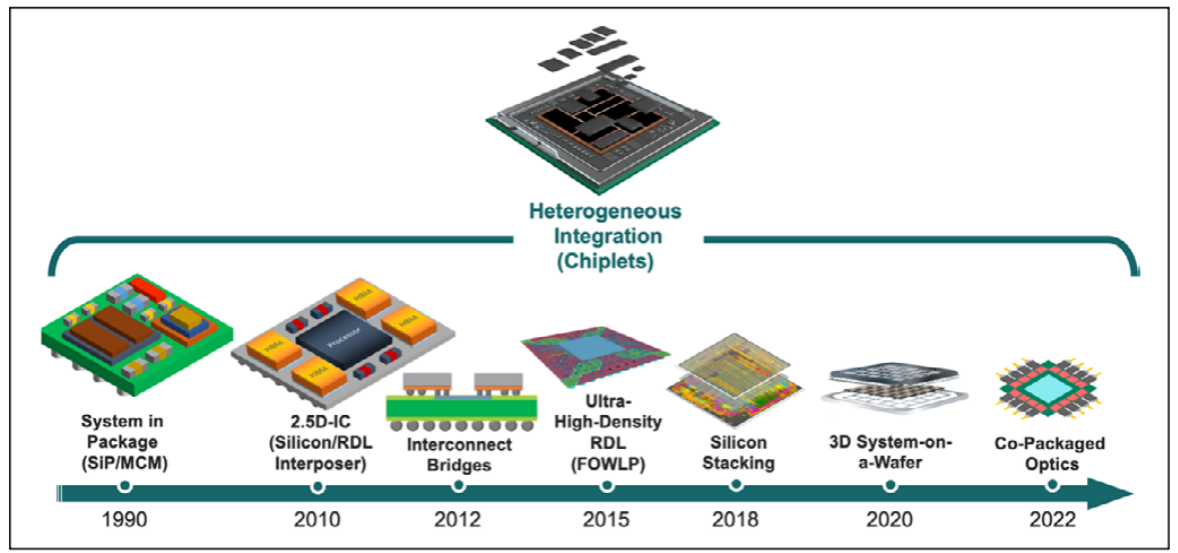
- **Moore’s law:** the number of transistors on a chip would double roughly every two years, with a minimal increase in cost

- **Manufacturing Cost**: Cost of nM manufacturing is increasing rather than decreasing which stresses Moore’s law

- **Development Cost**:
  - SOCs become extremely complex
  - Development teams and tools became prohibitively expensive. 5nM to 3nM developments reported to cost from 1B-20B*

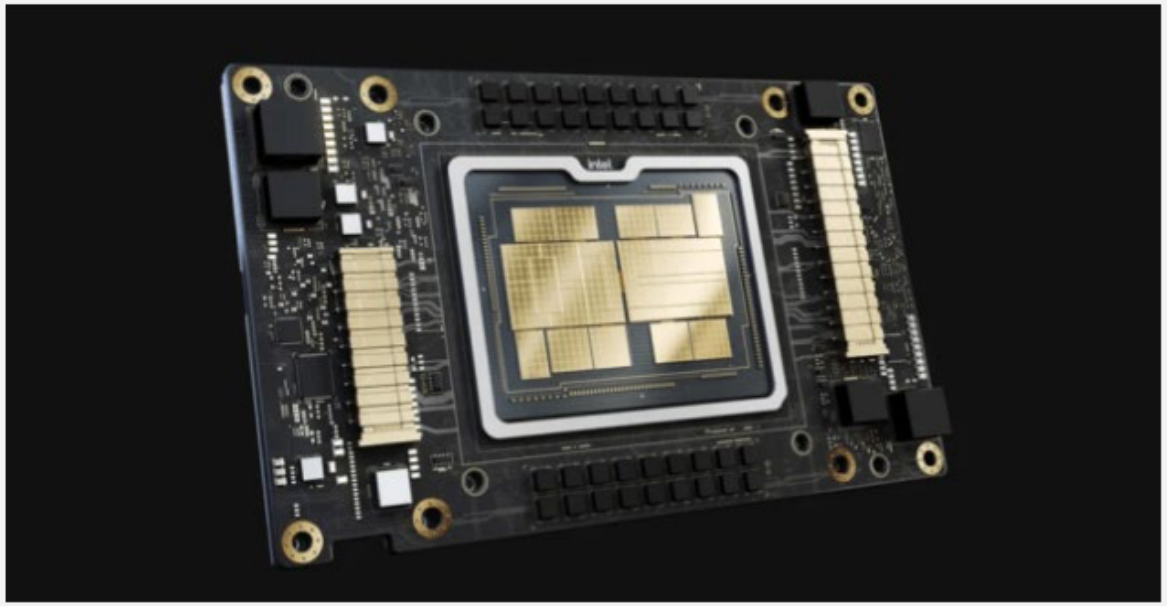
*report by Commercial Times
*NVIDIA annual report.

Chiplet Ecosystem Evolves



- **Cost:** Advanced packaging from 2D to 2.5D to 3D have enabled cost effective ways to integrate Chiplets optimizing interface speed/density per application
- **Interconnect:** Technologies like Chip on Wafer on Substrate (CoWoS) allow low parasitic high speed Chiplet interconnects.
- **Protocols:** Universal Chiplet Interconnect Express (UCIe) provides universal interface protocol between Chiplets creating opportunities to use other manufacturers Chiplets
- **Test Standards:** DFT standards like IEEE Std 1838 make testing at all stages possible

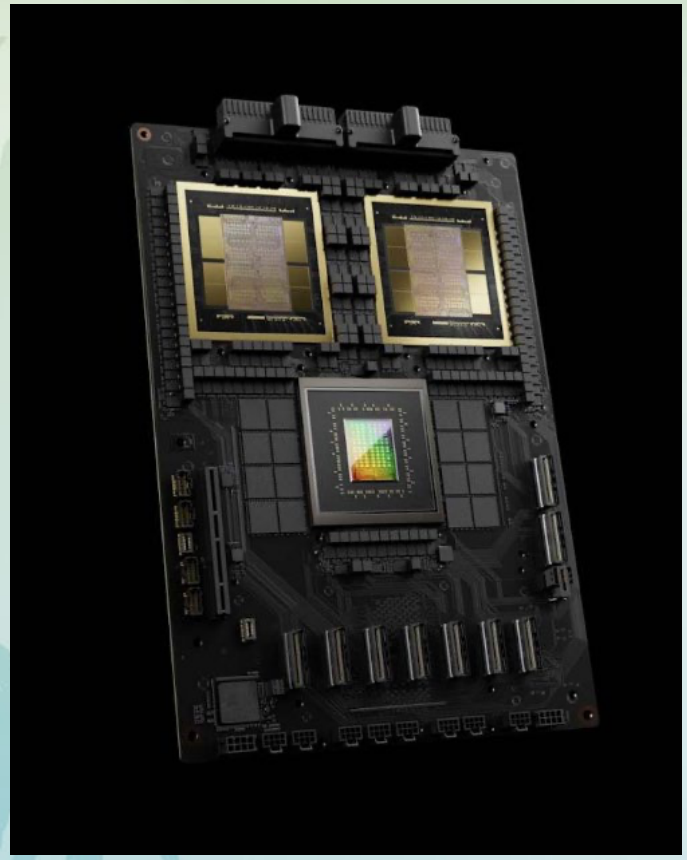
Chiplets in HPC



Source: INTEL

- Intel's Ponte Vecchio has 47 active Chiplets
- **Cost-Effective:** Chiplets solutions can increase overall compute and memory density cost through effective use of technologies thus mimicking Moore's law of cost per density.
  - Optimize device size & Technology to maximize yield
- **Faster Time to Market:** Chiplets can reduce development time and costs by allowing designers to reuse existing components and integrate them into new designs.
- **Technology Flexibility:** Chiplets allow manufacturers to mix and match different technologies, such as high-performance cores and lower-cost I/O components, for better system optimization.

Chiplets in HPC



NVIDIA GB200 Superchip Incl. Two Blackwell GPUs and One Grace CPU
Grace Hopper Superchip and B200 superchip

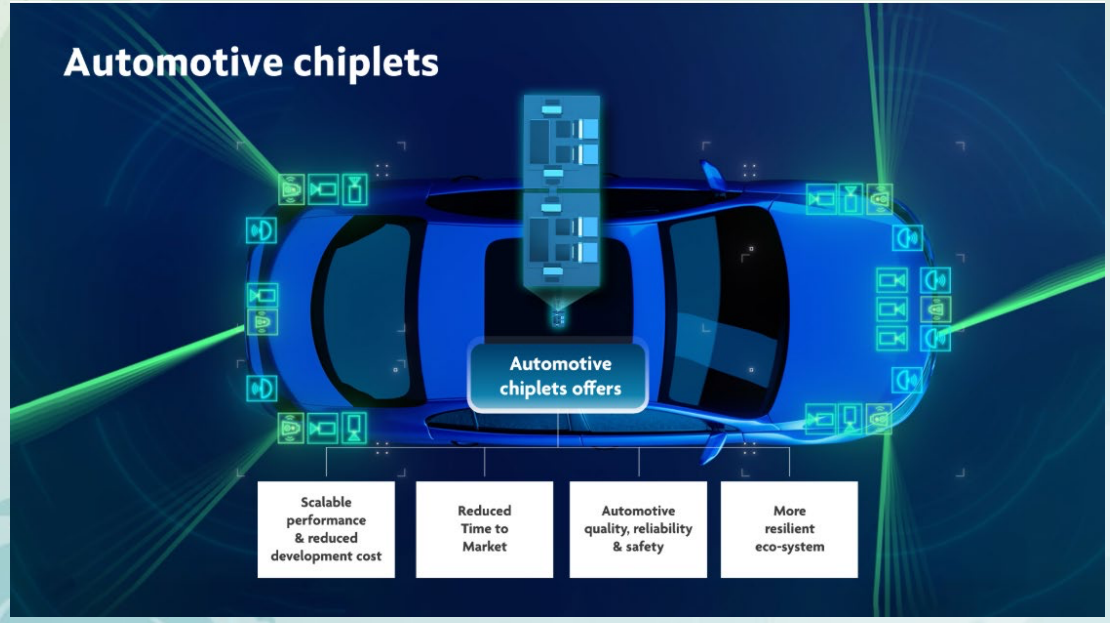
HPC Benefits:

- **Technology Limit -** HPC requires processors that are at the limit of reticle. (Blackwell)
- **Cost -** Using Chiplets to mimic Moore's law as devices hit reticle limits.
- **Scalability -** Enable easier scaling of performance by adding or upgrading individual components without redesigning the entire system. This enhances adaptability to evolving needs and allows for faster innovation.

- ASP of **$30k-$40k/ B200** superchip and $60k-80k for a GB200 (Nvidia)
- Given 4nM wafer estimated to be $20k for 12”
- ~28mmx28mm(Nvidia) ~ 70 die/wafer
- Defect density 0.1/cm^2 = 35 die ~$571/die
- 192GB of HBM ~ $3850 tested
- B200 @75% Margin (Nvidia) Cogs ~ $9k
- Assume FT@80%, package & test would cost>2.5k

Bottom line is TEST/Package cost inhibit high volume production at reasonable cost.

Chiplets in Automotive



- **Cost:** Monolithic ICs are expensive to develop for an automotive product line. Using proven Chiplets reduces development time & cost and allows multiple products to be developed
- **Heterogeneous Integration:** Chiplets allow designers to leverage the best of different technologies and domains, such as logic, memory, analog, RF, and photonics, to create high-performance and power-efficient electronics
- **Quality:** Stringent Quality/Reliability of Automotive market might be easier to achieve using already qualified devices

Limitations on Producing Chiplets

- **EDA Tools:** Design tools focused on Monolithic designs need to manage multiple chip to chip interactions including signal integrity, DFT as well as system design, RTL and Silicon Design
- **Package/Assembly:** Package and interconnect add complexity & cost.
- **Thermal management:** Multiple die with differing thermal and power requirements need to be carefully planned

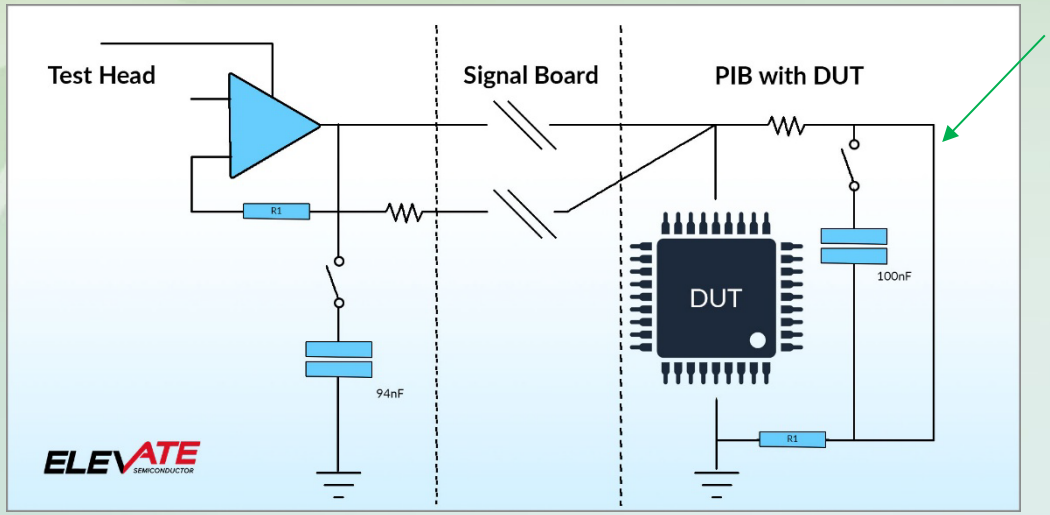
Test

- **Test Complexity:** The added complexity of Chiplet testing increases test time and pushes up manufacturing costs. Having access to scalable, cost-effective methods is therefore essential, if true economic viability is to be realized
- **YIELD: Chiplets require comprehensive testing to establish KGD**
  - 3 die at 50% yield each gives final yield Yield^3 = 50%^3= 12.5%
- **Quantity of Test increased**
  - **Probe –** need KGD
  - **Intermediate test –** Partially build SIPs and test before adding expensive die
  - **Final Test –** Confirm full SIP for interconnect and performance
  - **System test –** Likely takes place outside of ATE environment

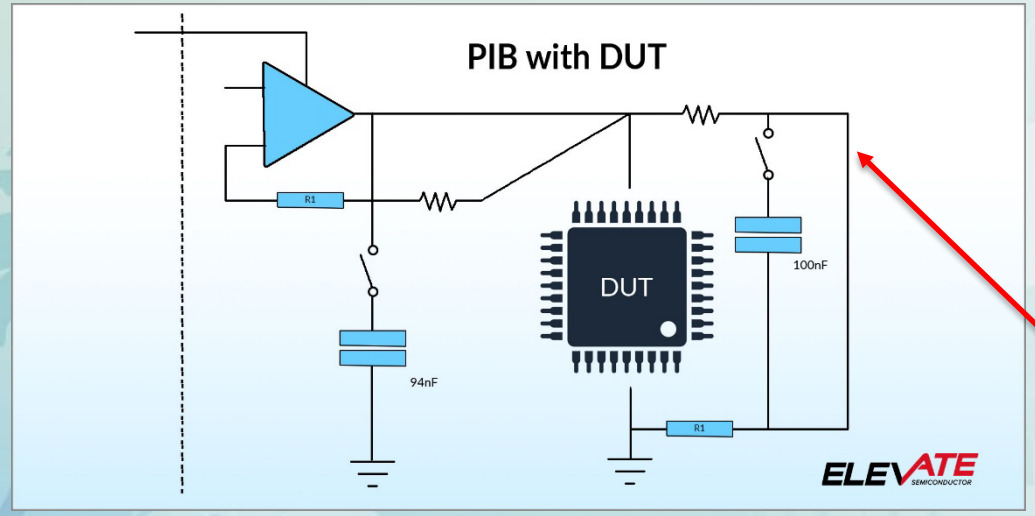
Limitations on Producing Chiplets

- **Inaccessible IO:** 2.5D & 3D configurations often don't allow visibility to internal nodes
- **IEEE STD 1838** means Chiplets test each other
- Debug might be difficult
- **Signal Integrity:** Physical location of instruments requires cabling and connectors that limit signal integrity and power delivery
- **I/O and interconnect** use loopback and PCB test methods but still need parametric test
- Power Delivery
  - **High Currents:** 1000+Amps need to be delivered accurately & efficiently over cabling and connectors
  - **Transient currents:** HPC and AI draw large currents over the same cabling and connectors leading to voltage glitches at the DUT. This can reset or damage parts leading to walking wounded or false rejects

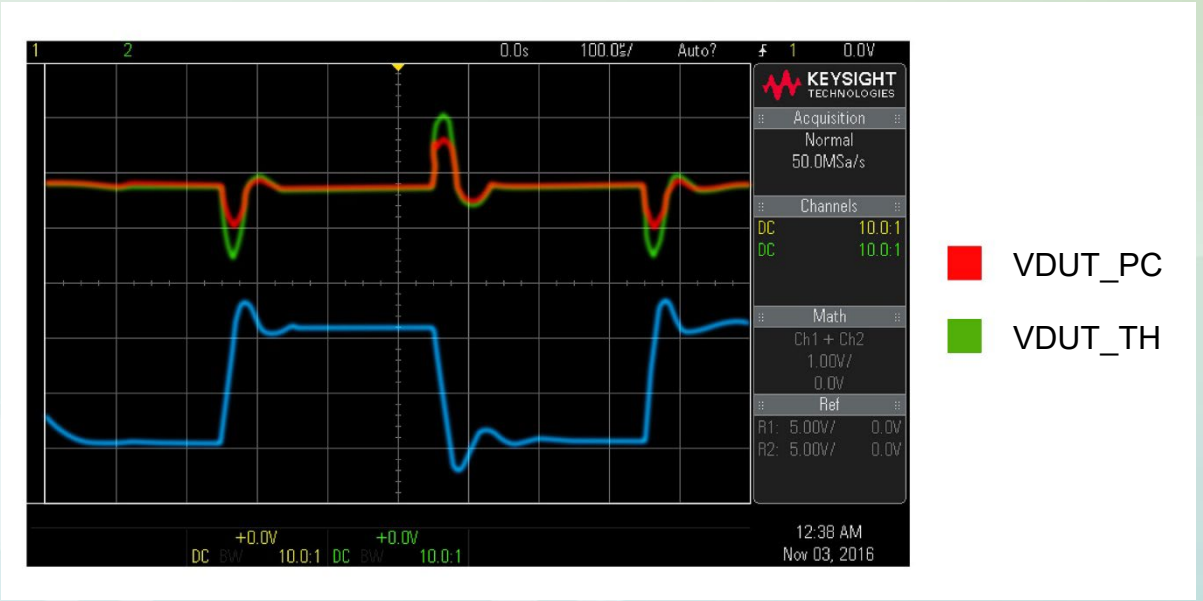
Limitations on Producing Chiplets



VDUT_TH



VDUT_PC



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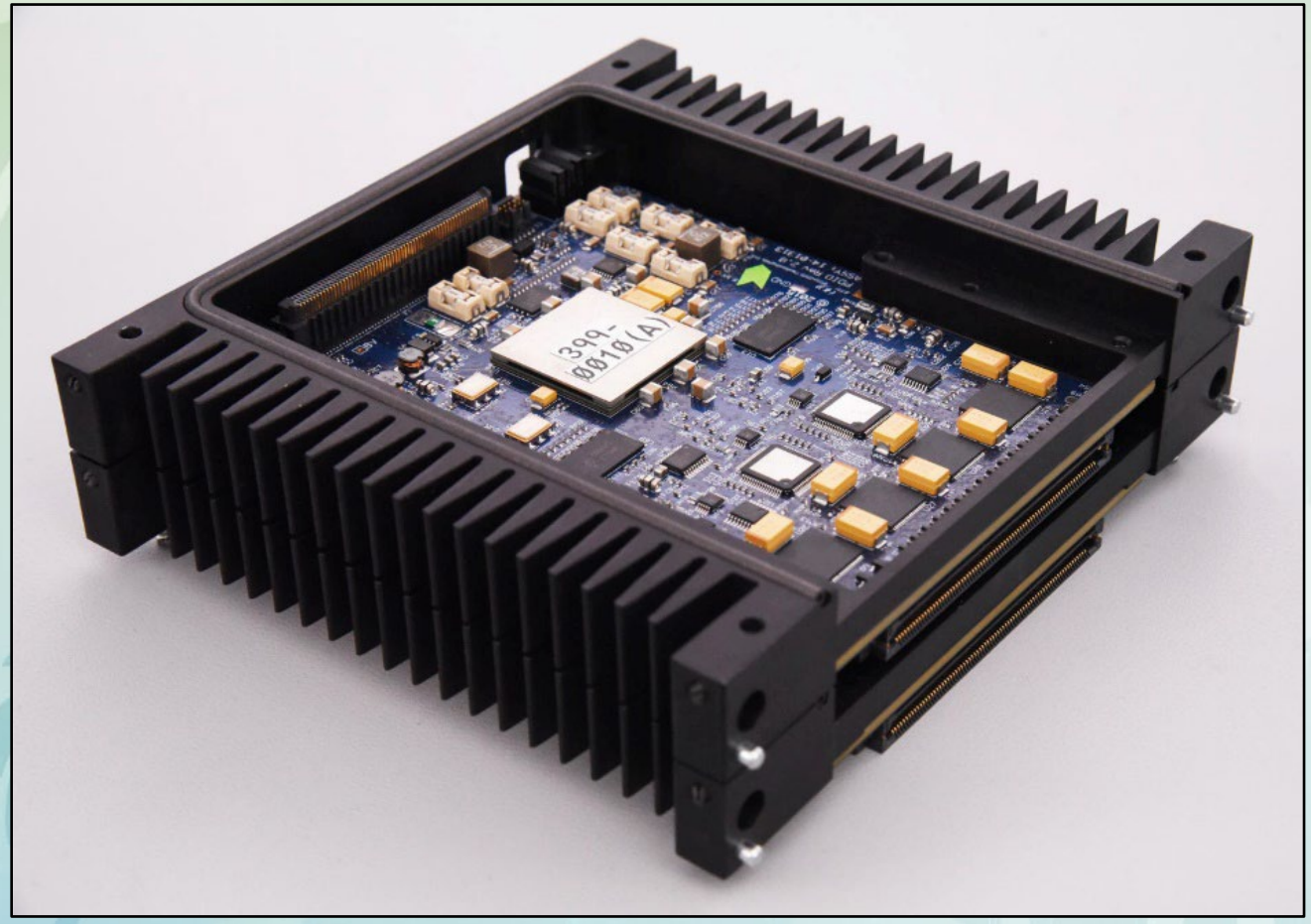
Orion – Tester on a Probe Card

Dan Hicks
President
STAr-Edge Technologies

Orion – Tester on a Probe Card

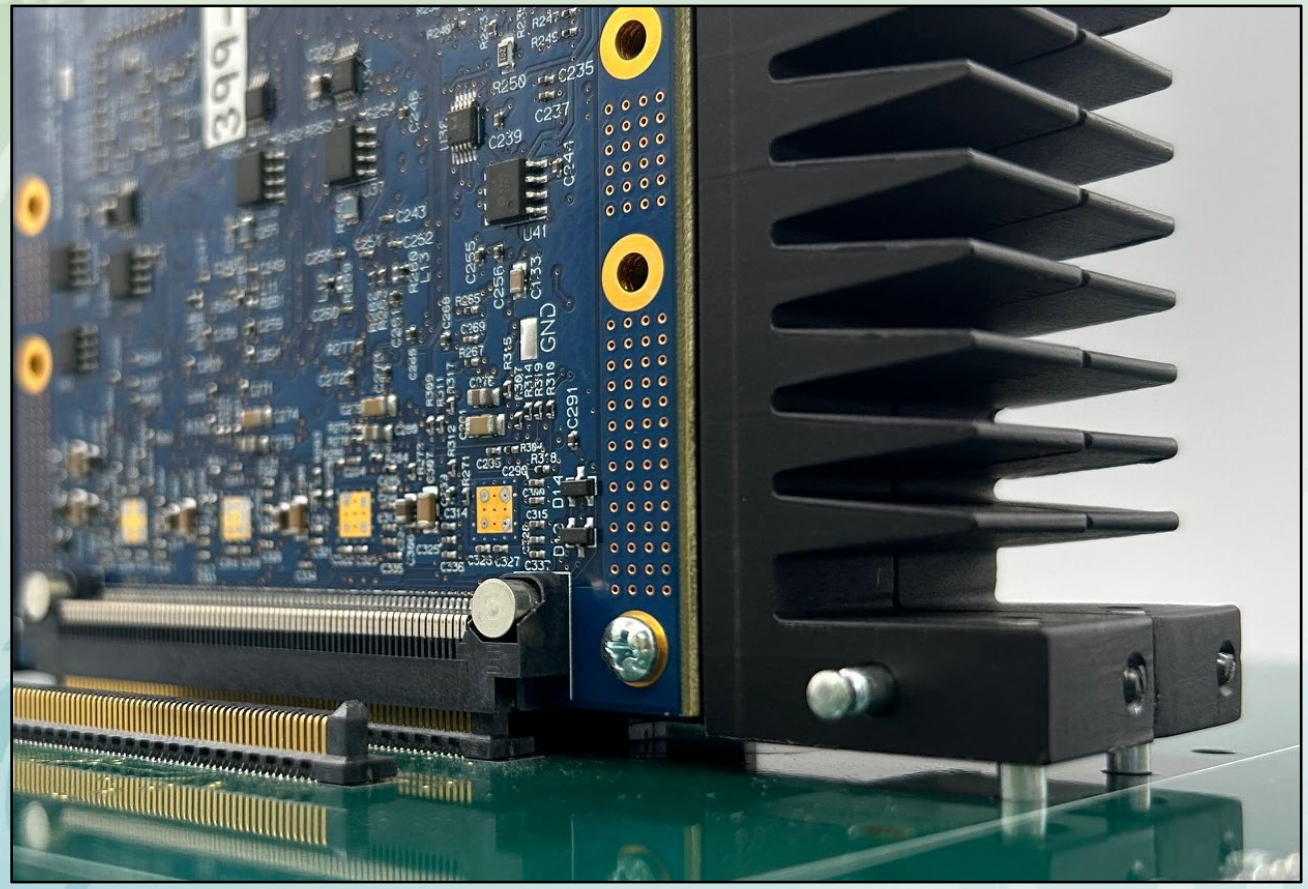
- **Orion** is a small form factor, fully functional ATE tester. Ideal for “Tester on a Probe Card”
- **Slices:** Orion consists of a stack of module ‘slices’ that include instrumentation, power, and communications
- **Flexibility:** Orion is suitable for docking directly to handlers, probe cards, and burn-in systems. It is an ideal platform for labs and test engineers' desks
- **Low Cost of Test:** High density and fully integrated system eliminates costly integration fixtures

Instrument Modules



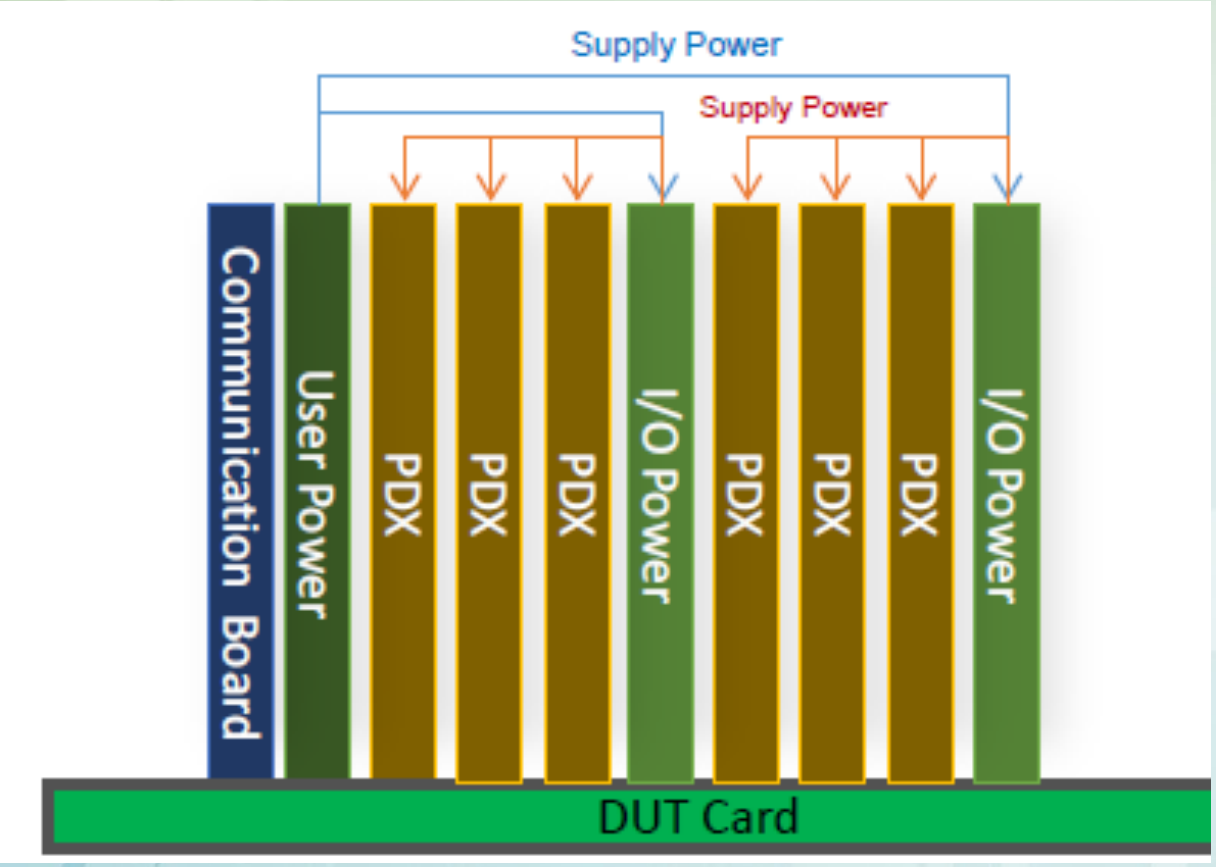
- **PDX36:** 36 Chan – Digital Instrument
- **LPX16:** 16 Chan - VI source
- **QIC:** 4 Chan – Waveform Digitizer
  - 16 Chan – Precision UVM
- **User Power Module:**
  - DUT board power (±15V, 12V, 5V, 3.3V)
  - Relay c-bits: 64 channels

Docking Interface



- Robust High-Speed interface
- Low-cost connectors - Field replaceable
- Per slice alignment – Zero connector stress
- Single operator installation

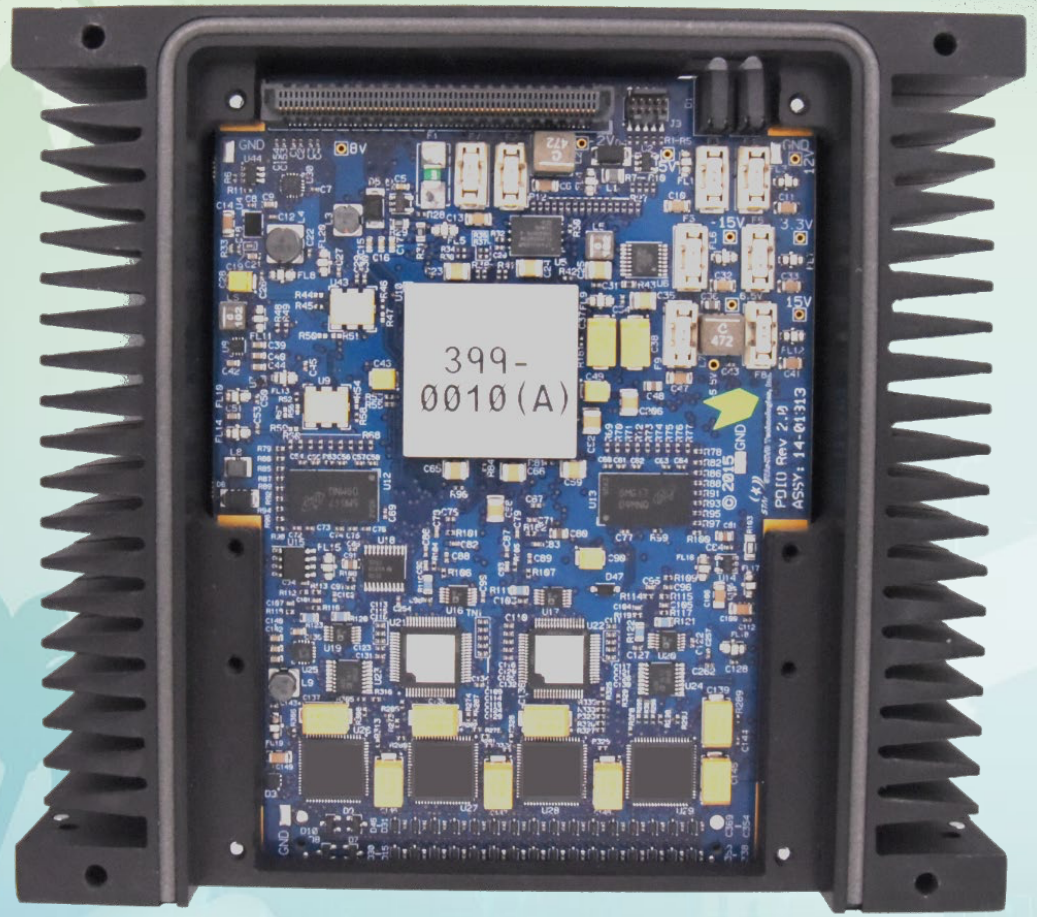
Orion - Architecture



Slices

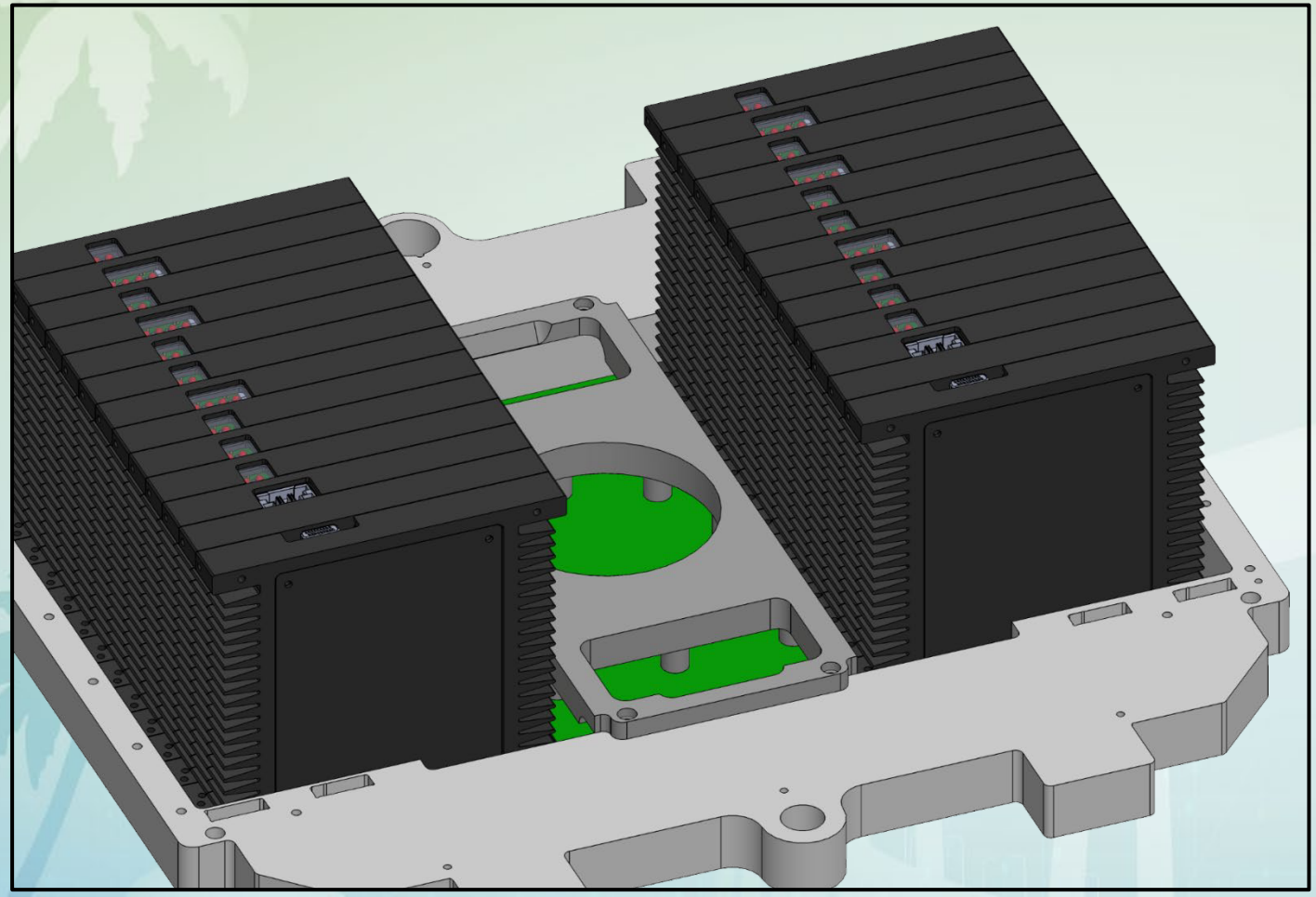
- **Comms:** 5GBPS high-speed bus
- **Power:** Single 48V external supply
- **User Configurable:** Add instruments as needed
- **DUT board power** (±15V, 12V, 5V, 3.3V)
- **Full ATE Software Suite**

PDX36 Overview



- **Digital Channels:**
  - 32 Standard pins 100MHz - 5V
  - 4 High Speed pins 200MHz - 7V
- **Per pin PMU**

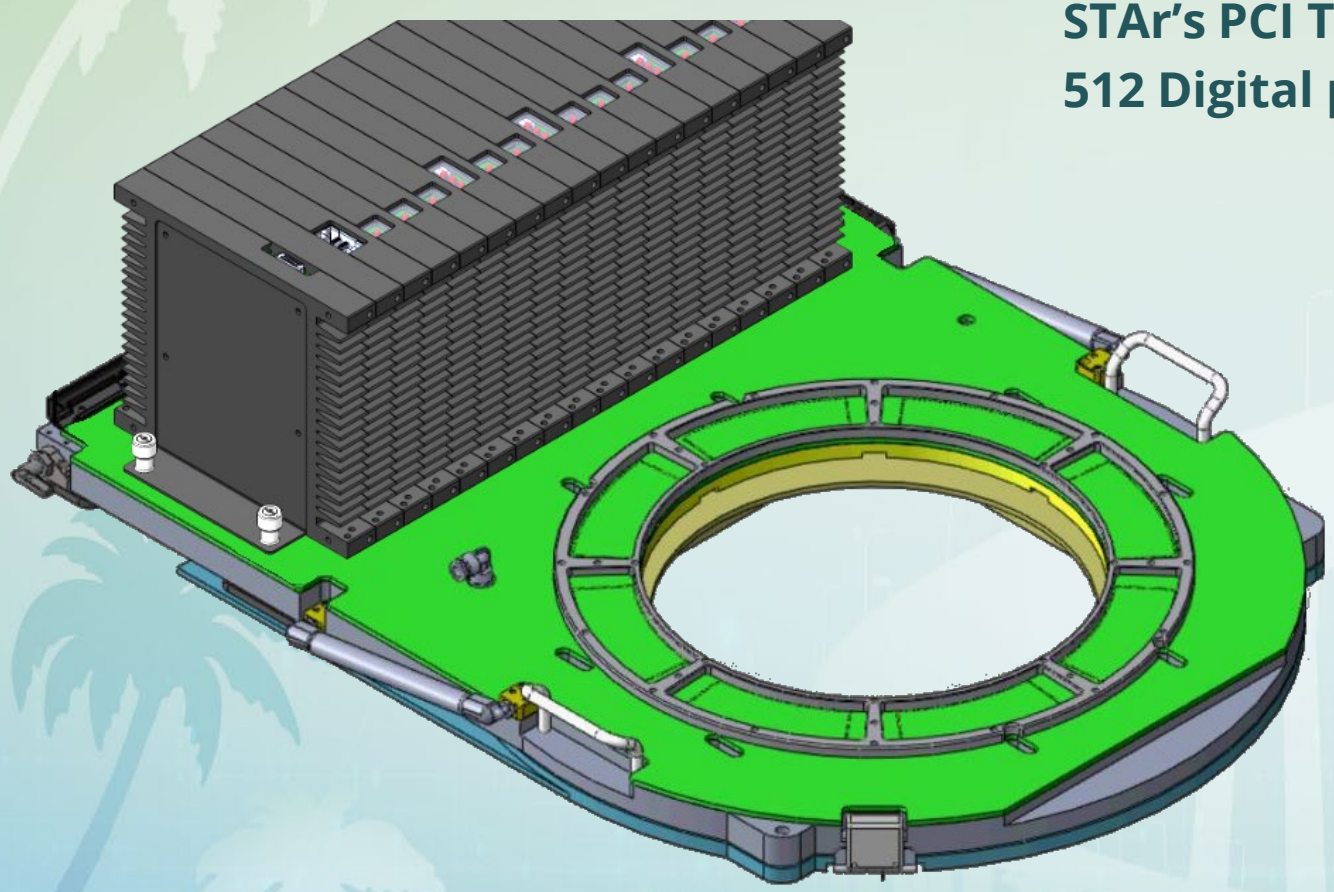
Load Board Tester

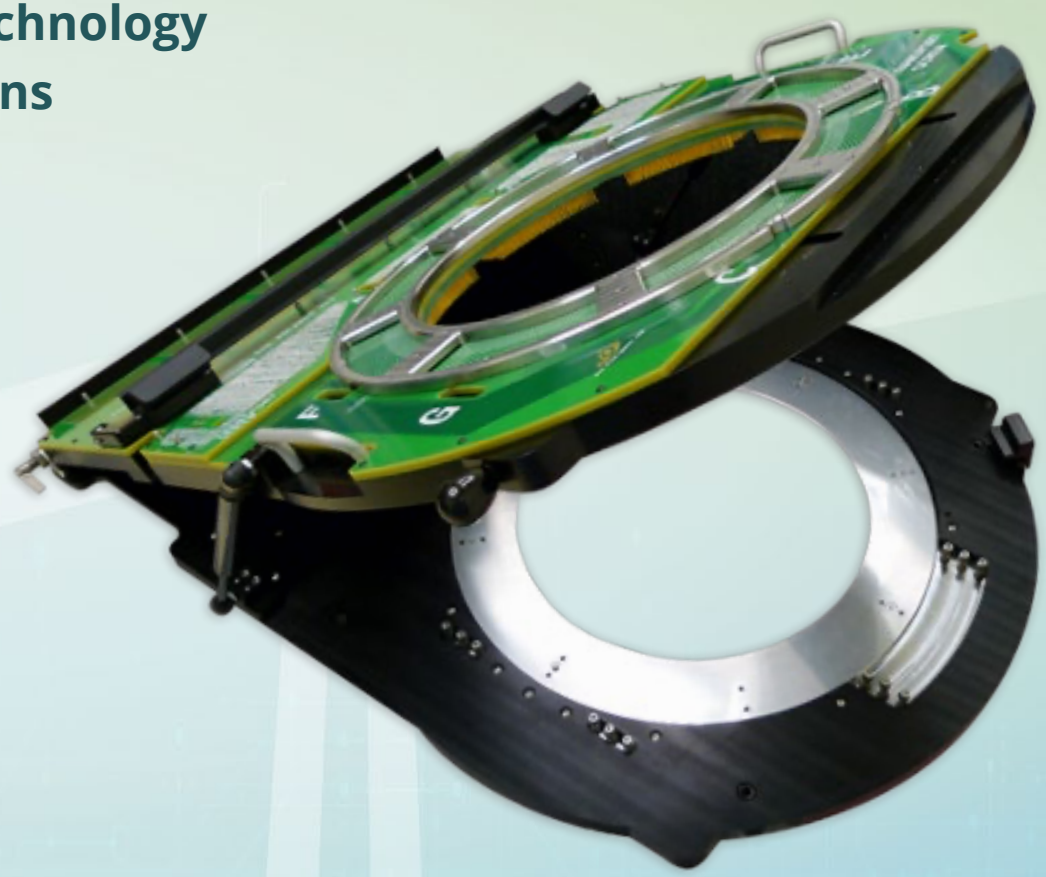


- Direct-Probe
- Short High-speed signal path
- Minimal trace parasitics
- Low-cost mechanical integration
  - No manipulator required
  - No pogo pins
- 512 Digital pins (256 each stack)

Probe Card Interface (PCI)

STAr's PCI Technology
512 Digital pins





Conclusions

1. High Cost of Development and Manufacture for small geometry devices is driving the need for Chiplets
2. Chiplet Ecosystem is being built to support growth
3. Rapid growth in Chiplet use will challenge current ATE manufactures ability to offer solutions that keep COGS reasonable
4. Tester on a Probe Card offers a possible solution to mitigating Chiplet cost