SWTEST
PROBE TODAY, FOR TOMORROW
2025 CONFERENCE

Early Detection of CRES Degradation on High Current Power Planes

ADVANTEST 70th Facing the future together

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Background & Problem Statement

- Probe Needle Degradation can be difficult to detect in its early stages:
- Probe cards and die continue to yield normally

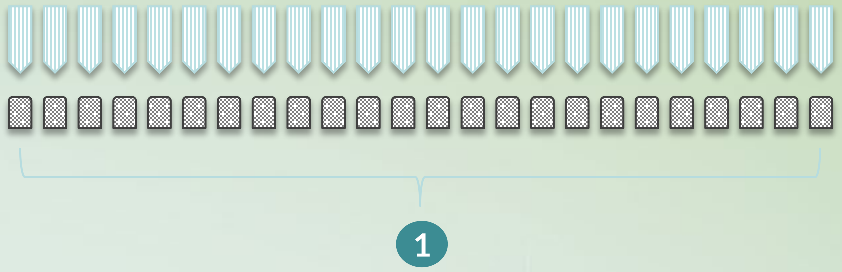
- Traditional Low Current Contact Resistance (C-RES) measurements cannot detect subtle changes isolated within large power planes

- Undetected subtle degradation may precede catastrophic damage, costly repairs

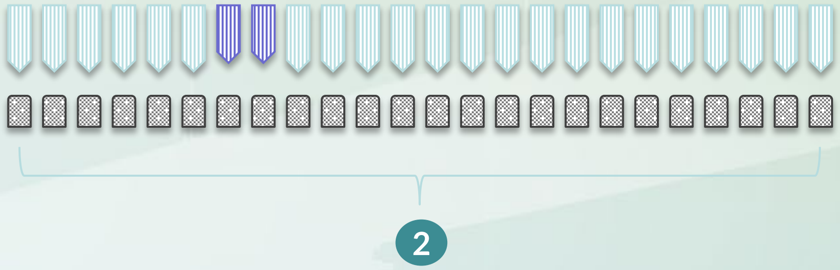
Goal: Detect CRES degradation on High Current Power Planes before yield loss or equipment down-time occurs. Determine various root cause scenarios that damage probe needles.

Uniform vs non-uniform CRES

- (1) Uniform contact resistance measurements across all pins regardless of type …



- (2) Non-uniform contact resistance due to particles, needle warpage, device contact defect or other anomalies …



Uniform CRES changes correlated between IO pins and large VDD power planes.

Non-uniform CRES issues within a large VDD plans are not observable on IO pins unless related IO supply is also impacted

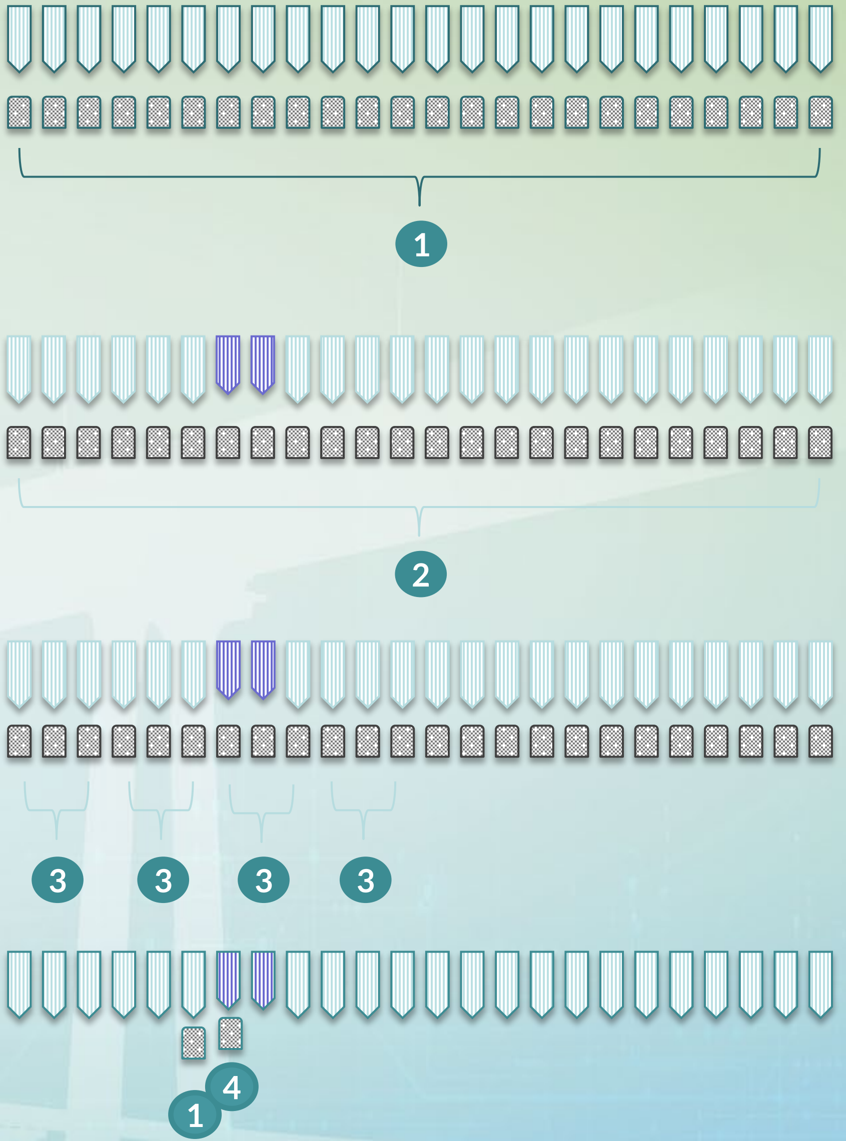
Problem of Probe Warpage & CRES

1. Uniform planarity on clean probe needles expected to produce "normal" CRES measurements

2. Non-planar probe needles are NOT detected by low current CRES measurements within a single power plane. Excess CCC of the power plane can hide poor contact when problems are only present on a small percentage of the contacts. High current CRES measurements & extended vDrop monitoring are expected to detect problems.

3. Sub-gang measurements within a plane are expected to detect CRES variances with adequate measurement resolution

4. OFFLINE CRES measurements with individual needle contact force will detect true contact degradation as planarity problems are compensated



Assessments & Methodologies

CRES degradation on High Current Power Planes

Overview of Considerations & Methodologies

- **Assessments:**
  - **Analysis of established implementation**
  - **Theoretical Assessment of CRES Degradation**
  - **Hypothetical Assessment of Probe Burn Scenarios**

- **Approaches / Methodologies Considered**
  - **vDrop Measure & Monitoring Options: Traditional DPS Measurement, Monitor via Digital IO Channel, ADC based vDrop Monitoring & Extended vDrop capabilities**
  - **Device Considerations: on-silicon measurement capabilities**
  - **DUT Board Design Considerations: Device Core Power Considerations, Power Plane Design, Primary Sense Line Routing & Extended Sense Line Routing**

- **Methodologies Achieving Desired Goals**
  - **Methods NOT requiring additional measurements & Test Time**
  - **Methods leveraging low/no-overhead instrument capabilities**
  - **Methods isolating <u>root cause</u> of subtle probe burns**

Analysis of Established Implementation

- **What data is available?**
- **Can we detect differences from test cell to test cell?**
  - **If not, can we add useful calculations without retesting lots?**
- **Do we have a reliable data signal?**
  - **If not, what is the development time and test time impact of additional methodologies?**
- **What changes are required to enable an ideal solution that *<u>includes root cause isolation?</u>***

- **What are the overall cost / benefit tradeoffs?**
- **Test time, yield improvements, uptime improvements, equipment changes, etc ..**

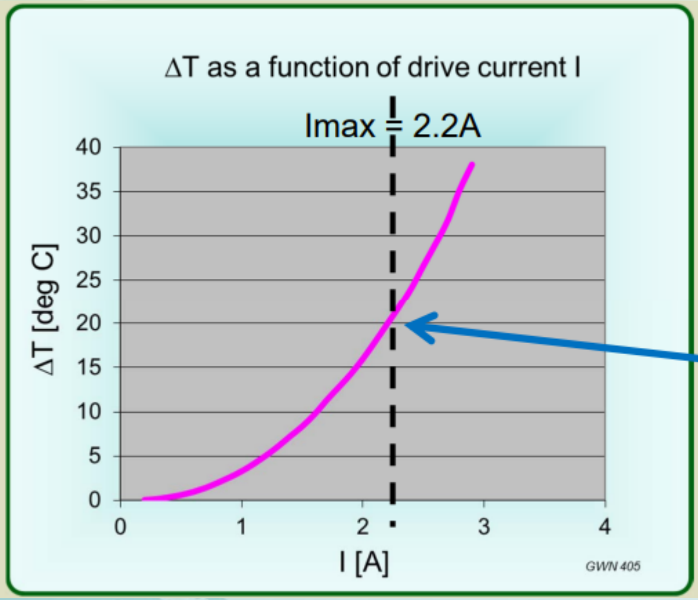
Conditions Leading to Equipment Damage

Category	Scenario	Level of Damage	Confirmation
Device Handling	Device inserted into powered socket	Varies up to catastrophic	Known Hazard
Test Development & Debug	Debug of new test content	Varies up to catastrophic	Known Risk
Characterization	Volume characterization of corner lots	Varies up to catastrophic	Known Risk
Undetected partial opens or CRES degradation **	Increased current thru connected paths is undetected up to yield loss	Loss of planarity / probe needle warpage	Visual Inspection
Production Process Variations	Production stress on high leakage die	Varies up to catastrophic	Speculative
Defective Units *	Die failure during stress or other testing of high leakage defects	Unknown	Speculative
Thermal Runaway	Excessive heating of die or probe head	Varies up to catastrophic	Known Risk
Undetected local/partial shorts/leakage	Undetected internal or external power issues	Unknown	Speculative
Equipment Setup	Improper overdrive or insertion force	Yield loss (mild damage)	Known Impact
Equipment Setup *	Overdrive setup attempted on defective unit	Unknown	Speculative
Device Handling *	Remove DUT while power still applied or Bulk Caps still charged	Unknown	Reasonable Evidence

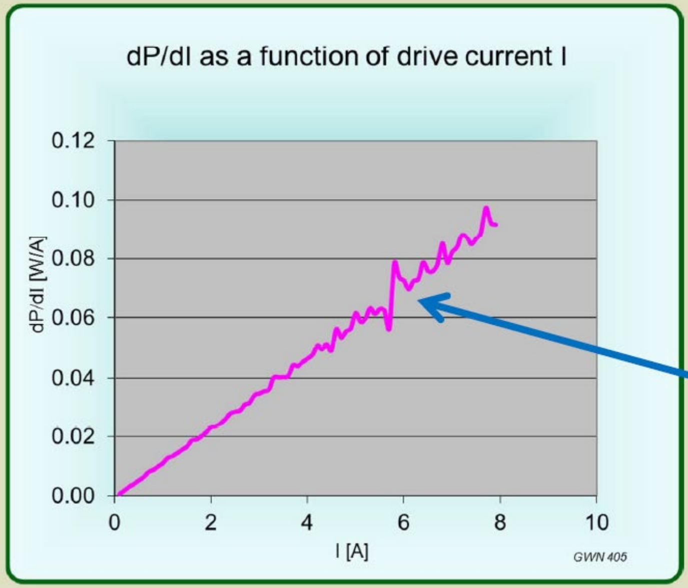
Joule Impact

"Resistance Fluctuations in Contacts Under High Current Loading"

Gert Hohenwarter, GateWave Northern Inc. - TestConX 2021 (Virtual Event)



CCC often defined as current required for a given temperature rise, e.g. 20°C



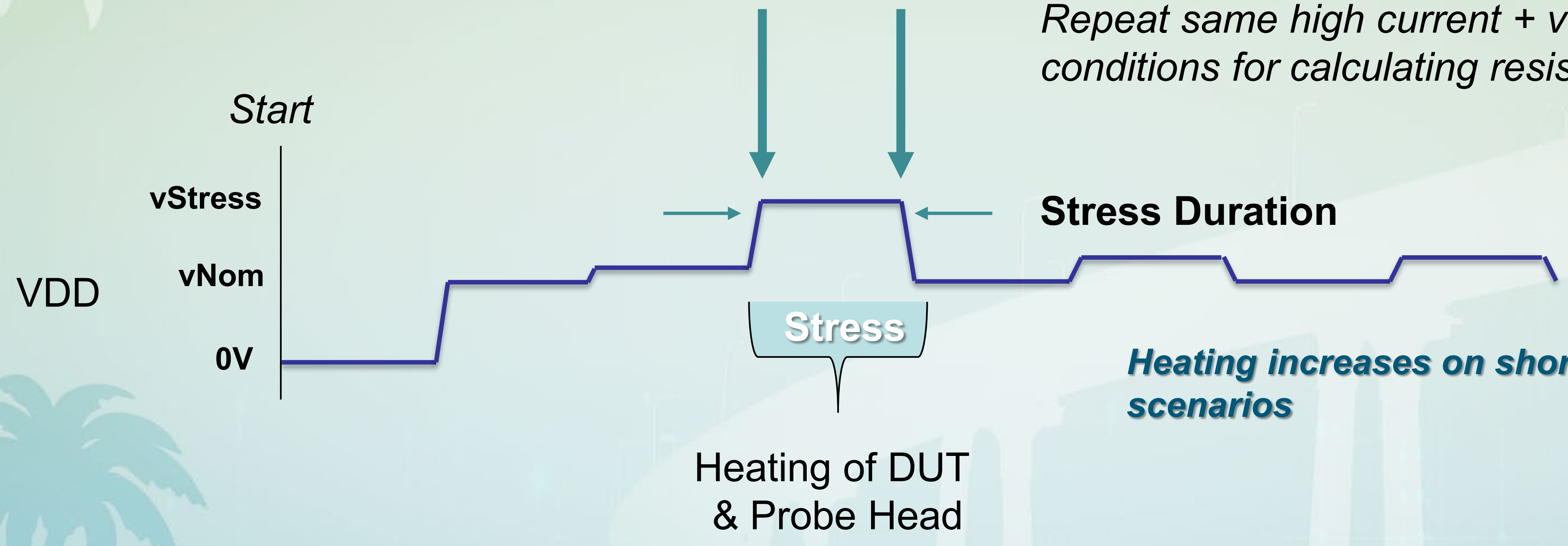
irregularities become visible

Excessive heating of probe needles causes shrinking and loss of elasticity.
Can we detect temporary physical changes vs. permanent damage?
What percentage of needles within a power plane are impacted?
How does test temperature and current flow impact CRES?

Repetition of High Current Measurement

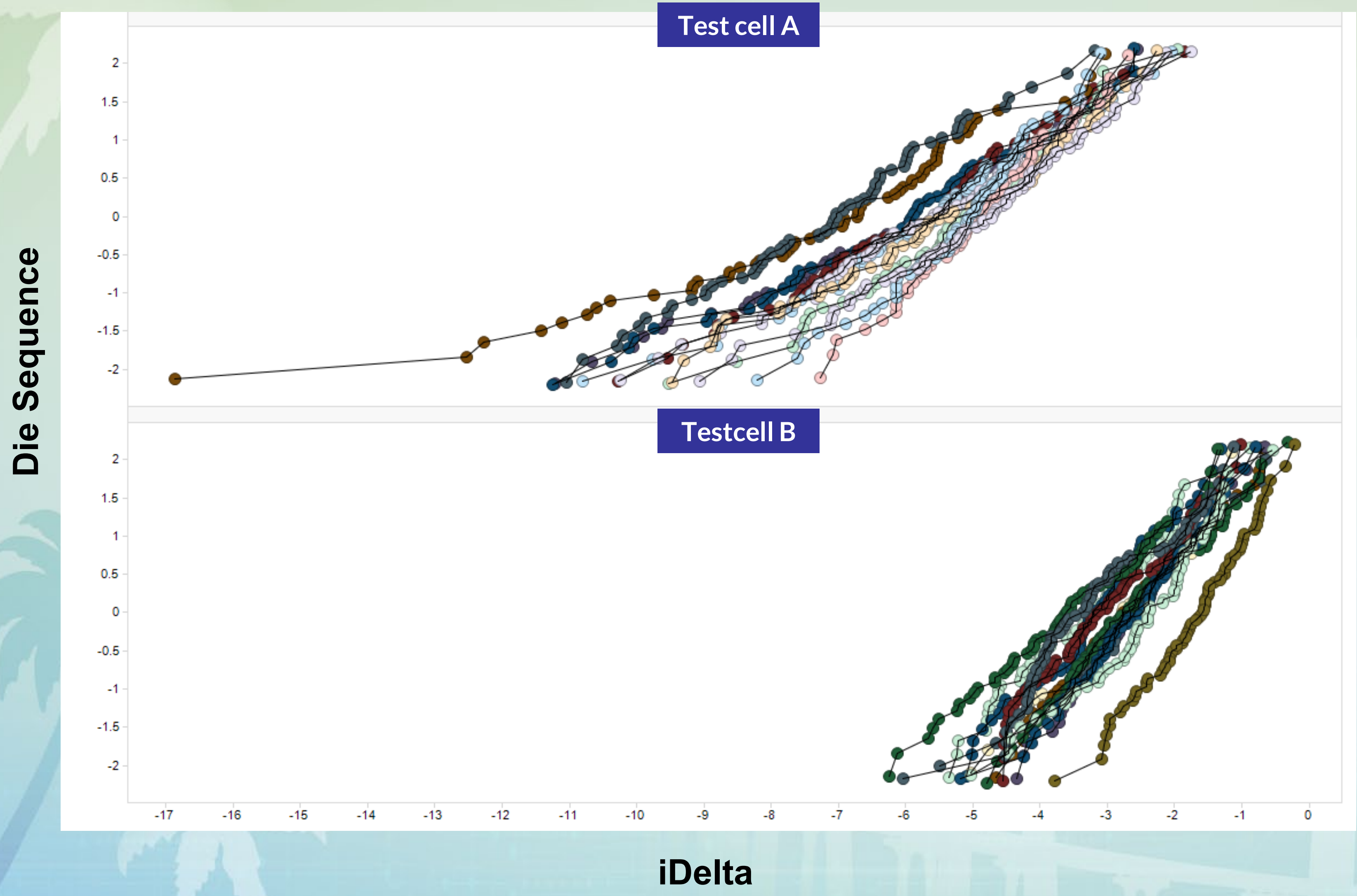
Same iMeas at Beginning and End of High Current Content (Δ iMeas)

Repeat same high current + vDrop measurement conditions for calculating resistance delta,



Heating increases on short Bin Out / Retest scenarios

Current Delta Across High Current Content



One Wafer Lot split across to Test Cells:

- Two testers
- Two probers
- Two load boards, probe cards & probe Heads
- Z-Force expected to be the same
- System cal/diags passing
- Overall yield trend is near identical

Are trends acceptable?

Probe card issue?

Tester issue?

Prober setup issue?

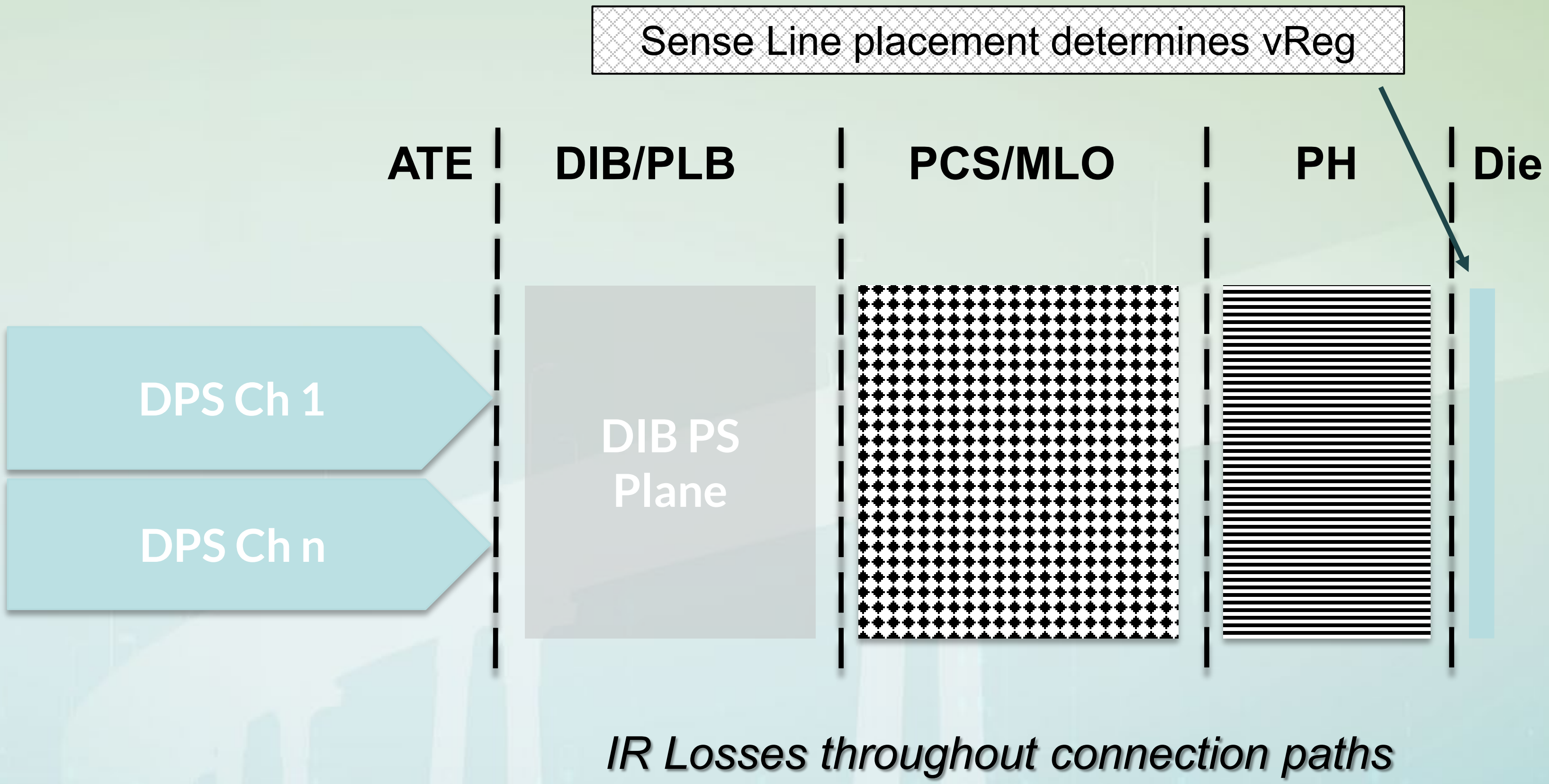
Thermal variance?

Full Path Resistance Factors

- **Die Level:**
- Total rDUT
- On-die vReg
- Pad/Bump contacts

- **Interface Hardware:**
- Probe needles
- Circuit board contacts
- PLB Power Plane

- **ATE:**
- Pogo contacts
- Card/Cable connections

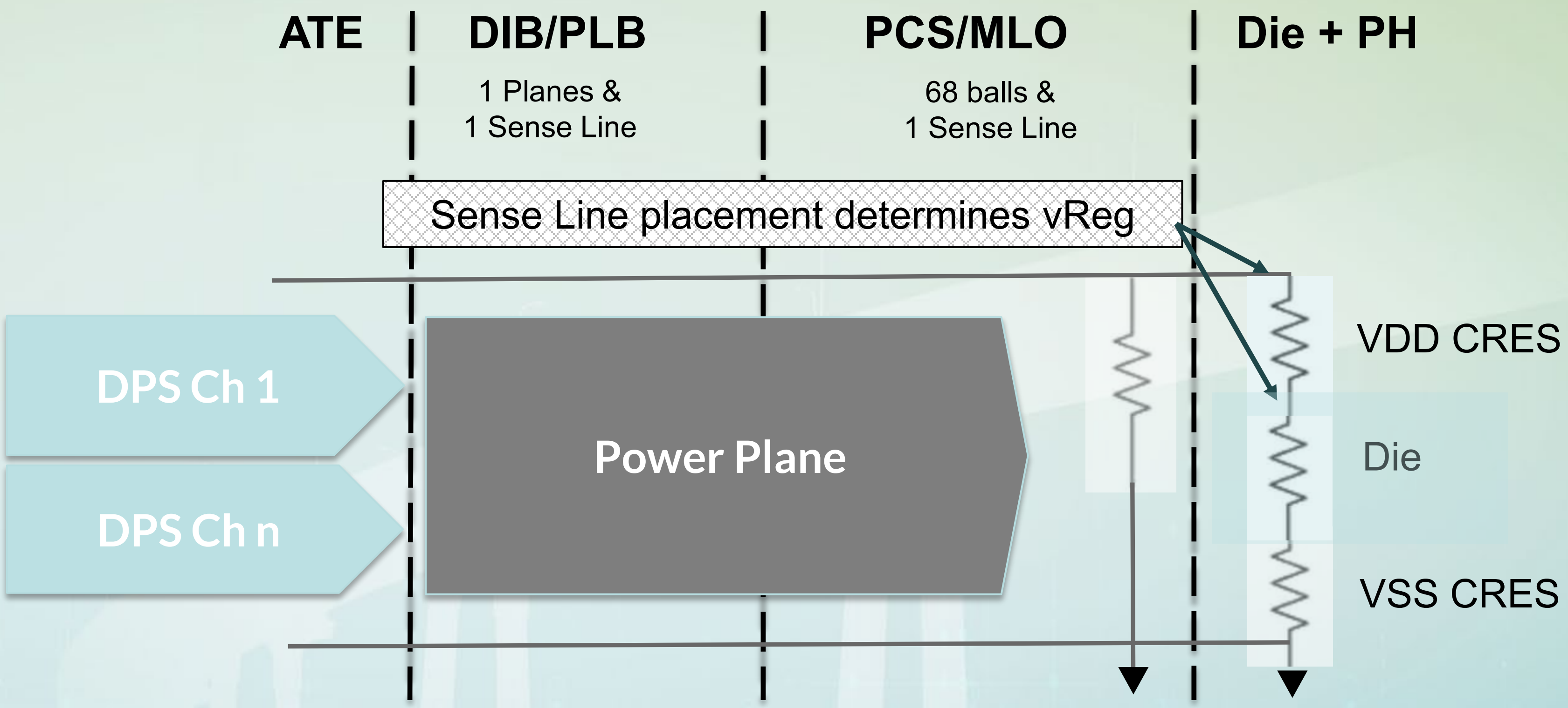


Voltage Drop Consideration

- **Die Level:**
  - Total rDUT
  - On-Die vReg
  - Pad/Bump contacts

- **Interface Hardware:**
  - Probe needles
  - Circuit board contacts
  - PLB Power Plane

- **ATE:**
  - Pogo contacts
  - Card/Cable connections



DPS Sense Line routing determines ATE Compensation

Detecting CRES Degradation

- Detecting CRES Degradation on Large Power Planes ***best*** with High Current measurements
- Melted Probe Needles reduce number of contacts and increases CRES
- High Power content is most likely to cause Probe Burns and exacerbate existing CRES issues
- High-Power current measurement needs to be stable/repeatable for certain methodologies

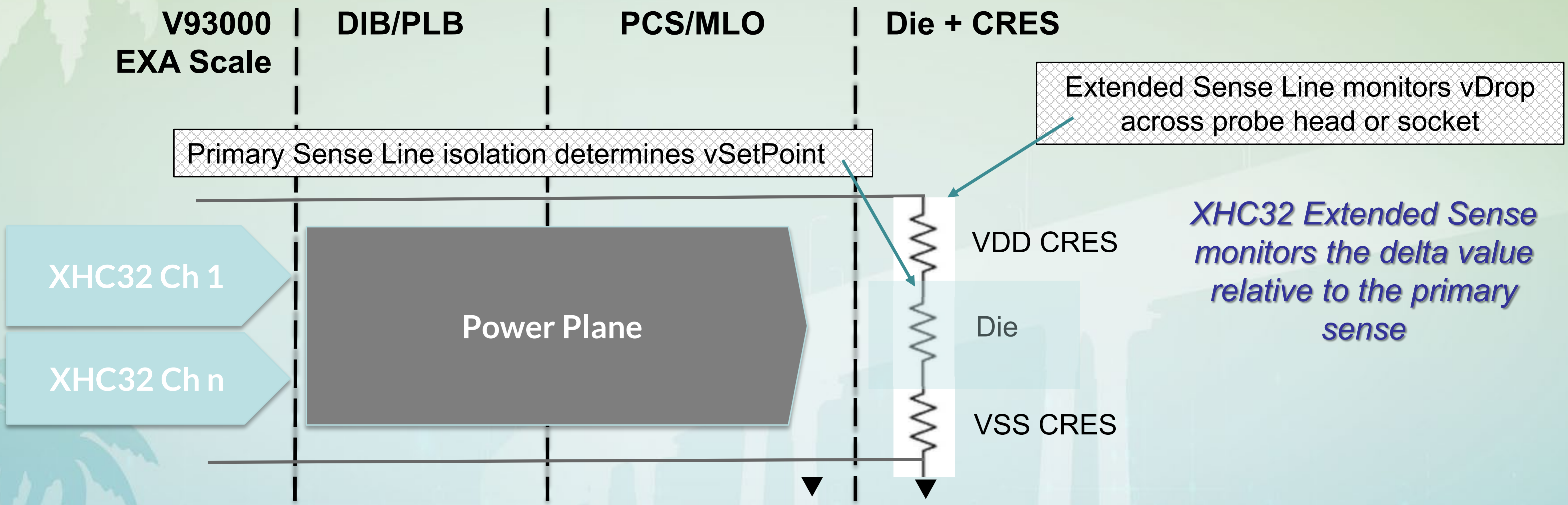
- Hypothesis: Early detection of CRES degradation may be accomplished by:

1. Repeating the same high current measurement at beginning and end of continuous high current content.
2. Sense line routing to the die with the appropriate sense measurement granularity and adequate ATE vDrop measurement accuracy
3. Ideal solution will directly measure vDrop across contacts (socket or probe head)

Implementation & Results

Extended Sense Monitor, Alarms & Measurements

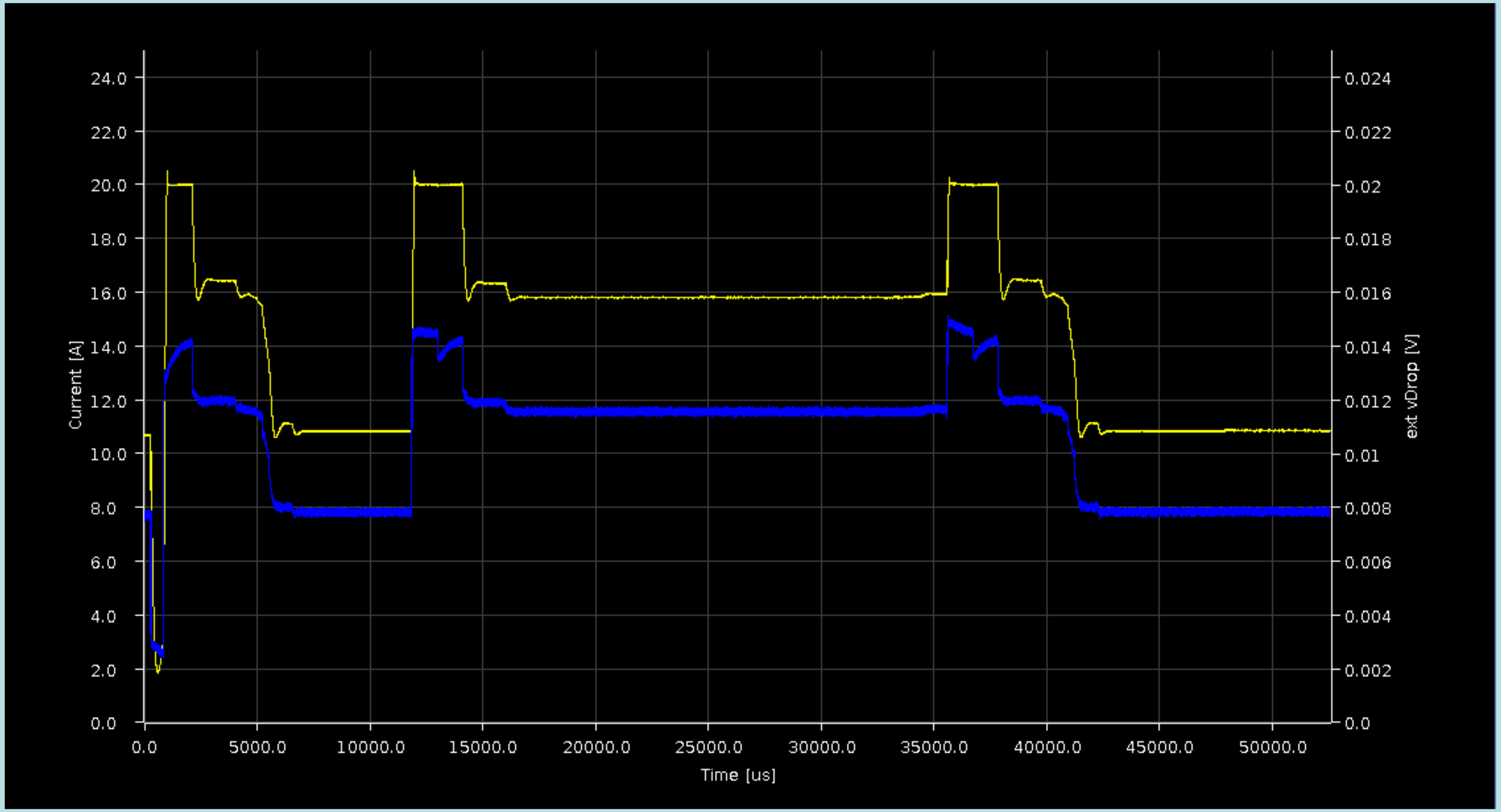
Extended Sense Routing



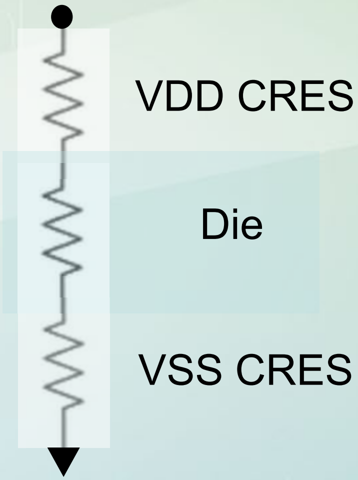
XHC32 Extended Sense monitors the delta value relative to the primary sense

Monitoring and Measurement of vDrop on Opposite Sides of Contactor

Extended vDrop Profile with Current

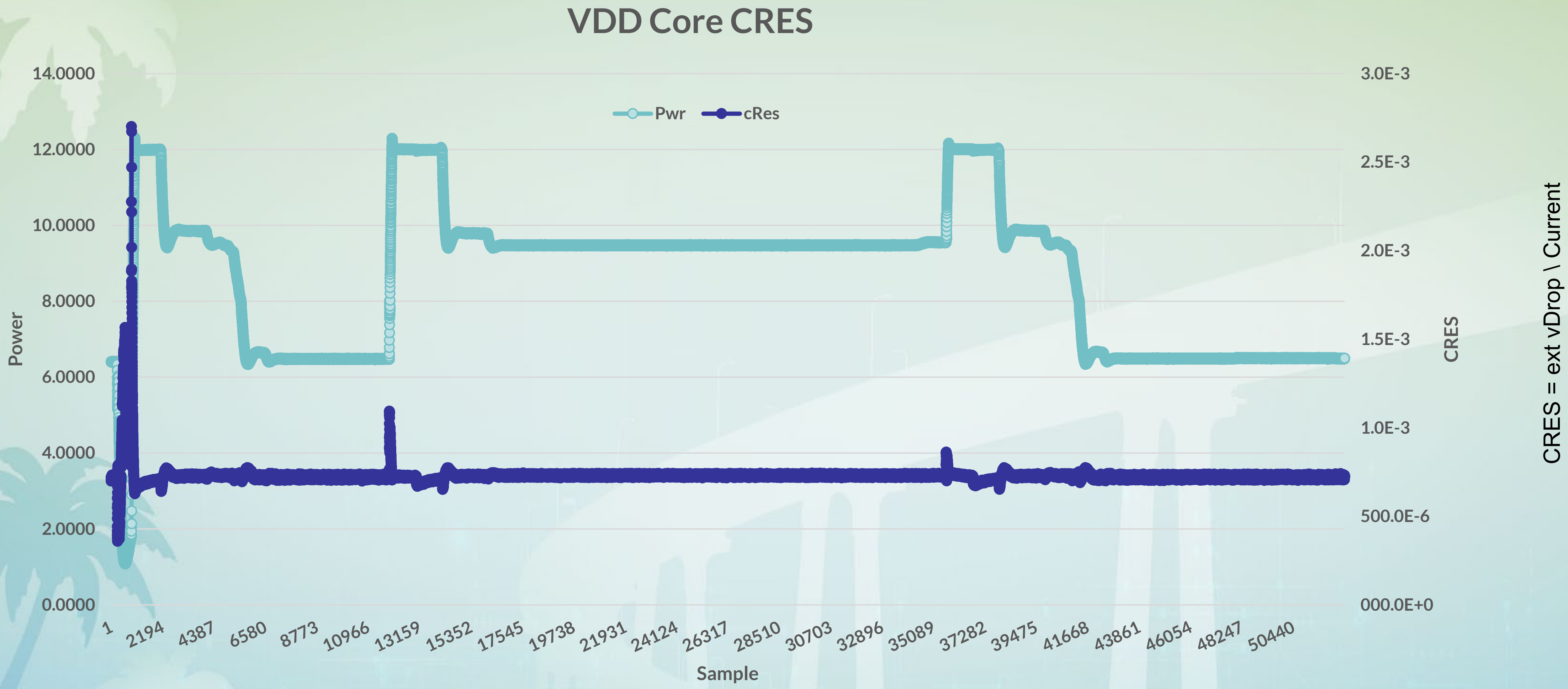


Cap charge / discharge induces transient variations



Extended vDrop scales with current flow
Contact Rating Alarm overcomes expected variances

Current & Extended vDrop converted to CRES

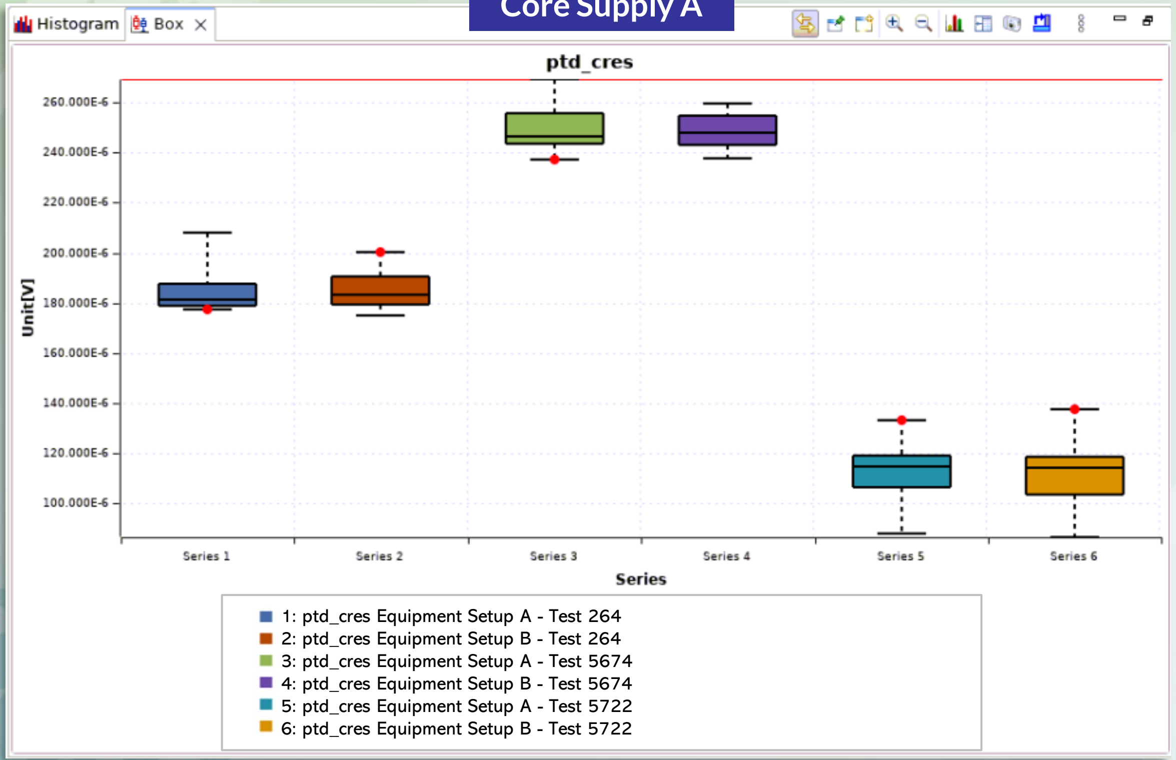


CRES impacted by device/die contacts as wells as probes/socket pins

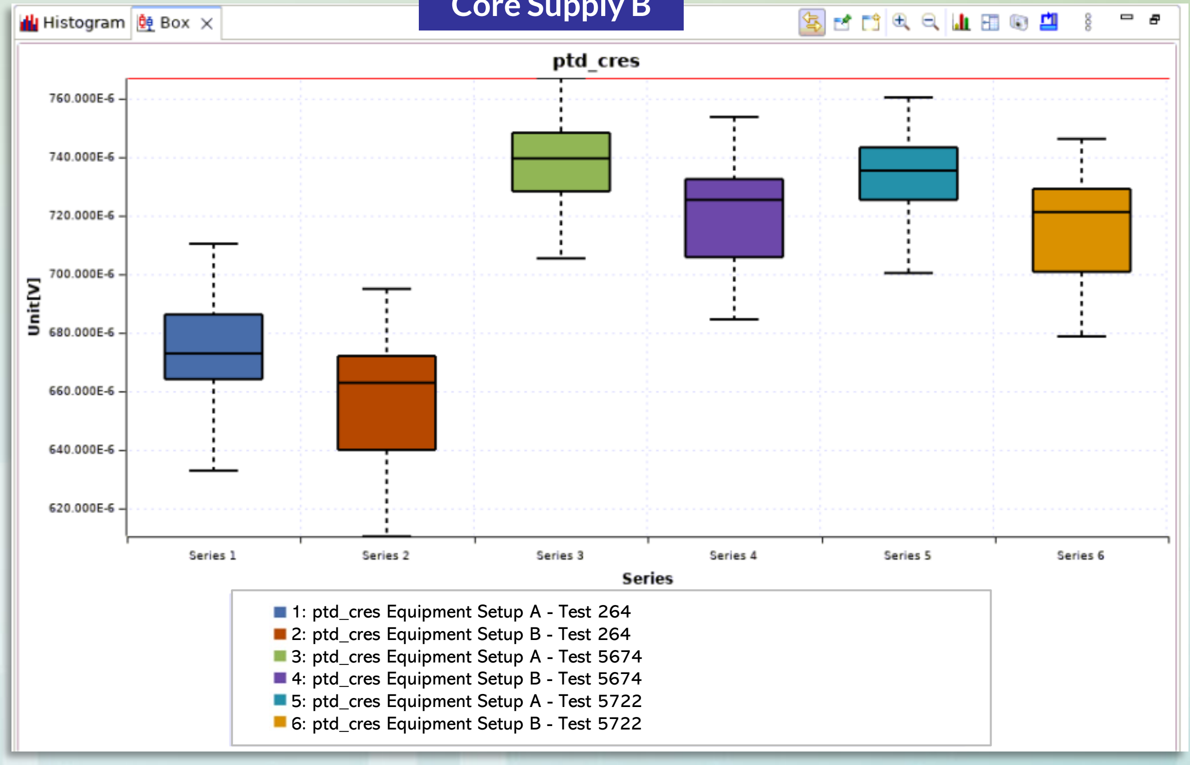
Extended vDrop Measurement Trial Data

Improved Capability When Utilizing Higher Percentage of CCC

Core Supply A



Core Supply B



Induced variation in equipment setup and known variances in DUT contact quality
Simultaneous Current & extended vDrop measurements for three supplies on selected content: Low, Mid & High-Power Scenarios
CRES = ext vDrop \ Current (r = V \ I) plotted for two core supplies

Conclusions & Recommendations

Extended vDrop Monitoring & Per Channel Results can pinpoint problem areas

Success & Key Learnings:

- Extended vDrop measurements can detect test cell variations, but difficult/not practical for root cause isolation of probe burns since they are not continuously running
- Extended vDrop monitoring/alarms can detect exact test suite(s) degrading CRES
- Improper insertion force can produce less-stable measurements
- Heating of contact from current flow changes CRES
- *Don't forget that device contacts can influence CRES measurements*

Recommendations:

- Assess DIB design early & add extended sense capability
  - CRES Monitoring/measurements are not possible without proper sense line routing
  - Retain primary sense in same location; Add extended sense on opposite side of device contacts
  - Route all sub-gang sense lines, when feasible
- Target test conditions that generates vDrop across DUT contacts that is detectable by connected instrument(s)

- Use <u>Contact Rating</u> Alarm:
  - Continuous monitor of extended vDrop & power with Alarms programmed related to CCC & Thermal Constant Ratings

Status & Plans

- Methodology proven in controlled lab environment
- HW & SW are available and deployed
- Volume manufacturing ramp underway
- Seeking additional partners for volume data collection

Thank You

Back-up References Follow

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V93000 Instrument Capabilities

Measuring and/or Monitoring vDrop

Capability	Instruments	Accuracy, Resolution, Sample Rate (BW)
Primary vDrop Profile	XPS256 XHC32 UHC4T	±150µV, 10µV (12 bit), 200ksps (500kHz) ±150µV, 10µV (12 bit), 200ksps (500kHz) ±2mV, 200µV (12 bit), 200ksps (25kHz) – shared ADC
Extended vDrop Profile	XHC32	±150µV, 10µV (18 bit), 2Msps
High Speed Differential Sampler	UHC4T	2mV, 400µV, 10Msps – shared ADC
Digital Comparator	PS5000	±5mV, 1mV, 5GHz
Board ADC	PS5000	±500µV, 10uV (20 bit) 1Msps (130 kHz)

Extend vDrop Measurement Code Examples

Setup & Measurement Samples

```
spec InstrumentViewSampleCode {
    action extVdrop_meas;
    setup dcVI VDDCR_CPU0 {
        disconnectMode = safe;
        connectMode = standard;
        protection.disconnectPulldownState = true;
        result.granularity = perPogo;
        alarm.continueReporting = false;
        action meas extVdrop_meas {
            extendedVdrop.enabled = true;
            extendedVdrop.measType = average;
        }
    }
}

sequence InstrumentViewSampleCode {
    parallel {
        sequential {
            actionCall extVdrop_meas;
        }
    }
}
```

Result Retrieval

```
Map<String, MultiSiteDoubleArray> myMeasResults = myDcVIResults.vmeas()
        .getExtendedVoltageDrop();
    for (String signal : signals) {
        MultiSiteDoubleArray voltages = measResults.get(signal);
    }
```

See TDC Topic of 360994

XHC32 programming – Voltage Drop measurement

vDrop Monitoring vs Measurements

Continuous Monitor vs. Measurements

Digital Comparator

- Mid-Band or H/L Pattern Compare
- High Bandwidth window compare detects small glitches
- Pattern may selectively ignore or compare for known issues

Digital Sampler

- Records numerous measured values at specified interval
- Requires Waveform Analysis
- Results may be processed in the background
- UHC4T requires connect mode change & cannot run ADC simultaneously

vDrop Measure

- Records measured value(s) for a specific point in time or averaged value for multiple samples
- May require additional test time for measurement
- Per pogo results available for some instruments

vDrop Monitor

- Continuous ADC based sampling that triggers an Alarm

Extended vDrop Monitoring

ST8.7.0 XHC32 Setup

DcVi Spec Setup Parameters:

alarm.extendedVoltageDrop (boolean) → enable/disable

protection.maxExtendedVoltageDrop (Voltage) → disconnect voltage threshold
protection.thresholdextendedVoltageDropDisconnect (boolean) → true/false
protection.extendedVoltageDropHoldTime (time) → disconnect & warning time threshold
protection.disconnectwarnExtendedVoltageDrop (Voltage) → warning message voltage threshold

Default protection values may be set in DUT Board file (.dbd)

Fine Granular vs Core Granular Power Plane Design

- **VOICE 2022 – EXA Scale Loadboard Design (Paper ID: 100)**

Power Granularity

Combined Supplies

- Single Net
- Single Sense (*board/remote*)
- Common Bulk

Simple design
Inaccurate per core
Overcurrent risk

Core Granularity

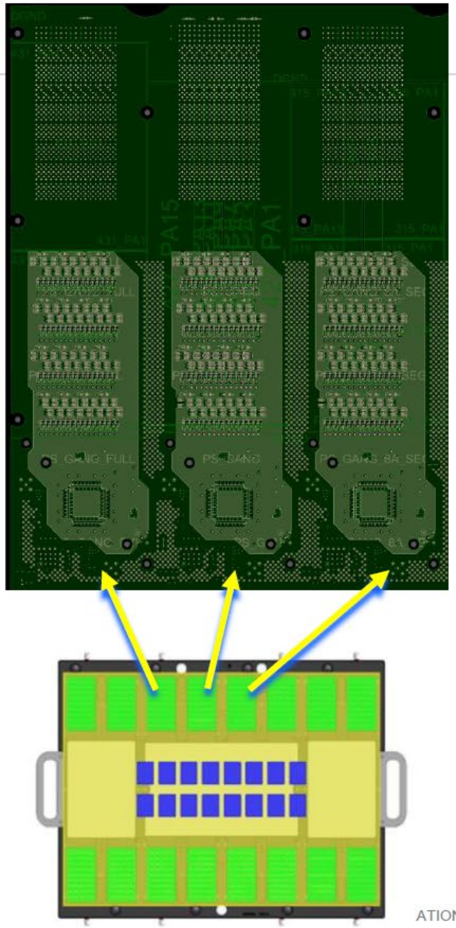
- Power Isolation per Core
- Sense at core (remote)
- Isolated bulk to core requirements

Isolated design
Accuracy to load
Current managed per core

Fine Granularity

- Granularity to XPS256 channel (1A)
- Sense per channel (remote)
- Minimum bulk capacitance

Per-pin power design
Accuracy to load
Ultimate power balance/control



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vDrop & extended vDrop Alarm Example

Console / Report Window Log & Test Result Log

Console | Parameters

System Console

```
WARNING:[TML] [ALARM] S1 alarms on          VDD    : EXTENDED_VOLTAGE_DROP_WARNING VOLTAGE_DROP_WARNING VOLTAGE_DROP EXTENDED_VOLTAGE_DROP VOLTAGE_DROP
WARNING:[TML] [ALARM] S1 alarms on          VDD    : EXTENDED_VOLTAGE_DROP VOLTAGE_DROP VOLTAGE_DROP EXTENDED_VOLTAGE_DROP_WARNING
WARNING:[TML] [ALARM] S1 alarms on           VDD   : VOLTAGE_DROP_WARNING EXTENDED_VOLTAGE_DROP_WARNING VOLTAGE_DROP EXTENDED_VOLTAGE_DROP VOLTAGE_DROP
WARNING:[TML] [ALARM] S1 alarms on               VDD : VOLTAGE_DROP VOLTAGE_DROP EXTENDED_VOLTAGE_DROP_WARNING VOLTAGE_DROP_WARNING EXTENDED_VOLTAGE_DROP

WARNING:[TML] [ALARM] S1 alarms on          VDD    : EXTENDED_VOLTAGE_DROP_WARNING VOLTAGE_DROP_WARNING VOLTAGE_DROP EXTENDED_VOLTAGE_DROP VOLTAGE_DROP
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WARNING:[TML] [ALARM] S1 alarms on               VDD : VOLTAGE_DROP VOLTAGE_DROP EXTENDED_VOLTAGE_DROP_WARNING VOLTAGE_DROP_WARNING EXTENDED_VOLTAGE_DROP
```

Problems | Result | Testflow

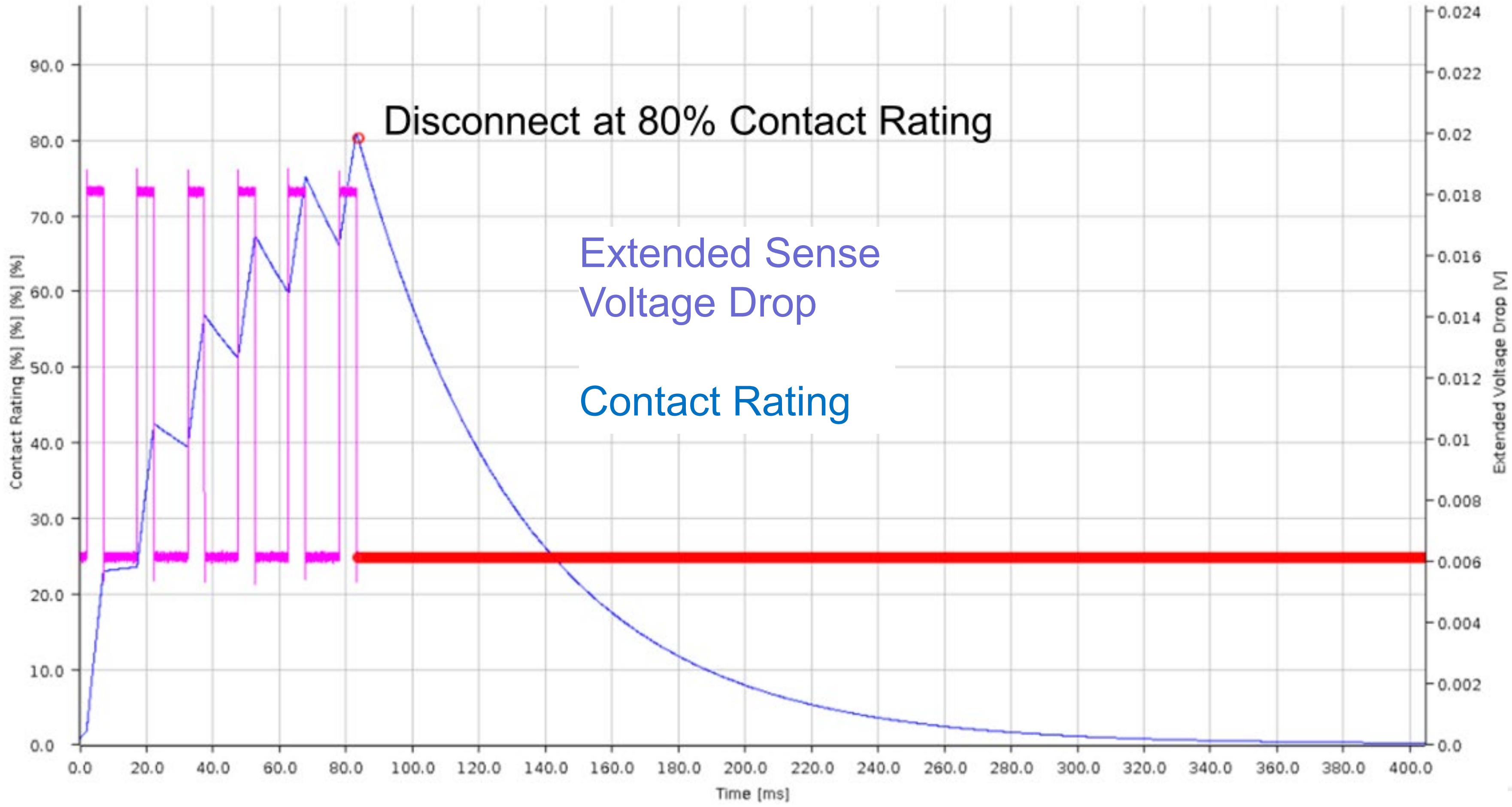
Results for 500 main testflow run(s) are shown

Fully Qualified Name	Site	DUT#	P/F	Alarm
Main.jtag.ClockConnect	1	1	Pass	
Main.jtag.	1	1	Fail	VDD :EXTENDED_VOLTAGE_DROP,VDDCR_CPU0:EXTENDED_VOLTAGE_DROP_WARNING,...
PowerDown.Disconnect	1	1	Fail	VDD :EXTENDED_VOLTAGE_DROP,VDDCR_CPU0:EXTENDED_VOLTAGE_DROP_WARNING,...
PostRun.disableTjControl	1	1	Pass	
PostRun.printSimpleDataStore	1	1	***	
PostRun.endDevice	1	1	Pass	

Test Program | Testflow | Test Suite | Test | Signal

Advanced Contact Protection – Thermal Modelling of Contacts

- Thermal Modelling of Probe Needle(s) with Emergeny Disconnect

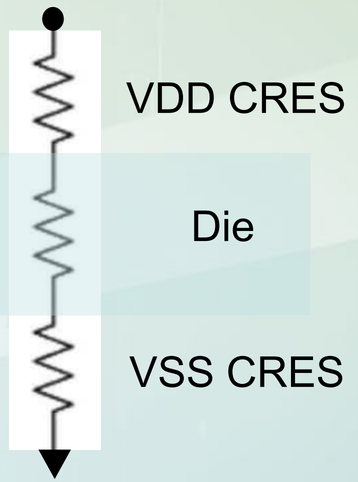



```
setup dcVI VCC_2 {
    level.vforce = 2 V;
    level.vrange = 2V;
    level.irange = 20A;
    level.iclamp = 20A;
    connect = true;
    disconnect = true;
    disconnectMode = lozThenHiz;

    regulation.capacitance = 2mF;
    regulation.loadstepMode = fast;
    regulation.vbandwidth = 30kHz;
    regulation.ibandwidth = 10kHz;

    protection.voltageDropHoldTimeForce = 5ms;

    //Contact Rating Section
    protection.contactRating =true;
    protection.contactNomCurrent = 0.8 A;
    protection.contactNomResistance = 7 mOhm;
    protection.contactThermalTimeConstant = 100 ms;

    protection.maxContactRating = 80;
    protection.warnContactRating = 60;
    protection.contactRatingDisconnect = true;
    protection.contactRatingHoldTime = 1 ms;

    alarm.contactRating = enabled;
    alarm.contactRatingWarning = enabled;

    profiling.voltage.enabled = false;
    profiling.current.enabled = true;
    profiling.extendedVdrop.enabled = true;
    profiling.contactRating.enabled = true;
```

Probe Resistance What-If Scenarios

Hypothetical CRES, Δ iMeas & vDrop Across Probe Head

Description	Ref iMeas	Delta A	Delta B	Delta C	Delta D
vSupply	1.5	1.5	1.5	1.5	1.5
rDUT	14.9E-3	13.6E-3	14.7E-3	5.0E-3	14.7E-3
rContact	71.9E-6	51.7E-6	57.4E-6	51.7E-6	176.0E-6
iMeas	100.00	110.00	101.70	296.93	100.89
Δ iMeas	-	10.00	1.70	196.93	0.89
vDrop Contact	**7.2E-3**	**5.7E-3**	**5.8E-3**	**15.3E-3**	**17.8E-3**
Scenario	Reference	Temp. change	10% open needles	iClamp activation	Low CRES

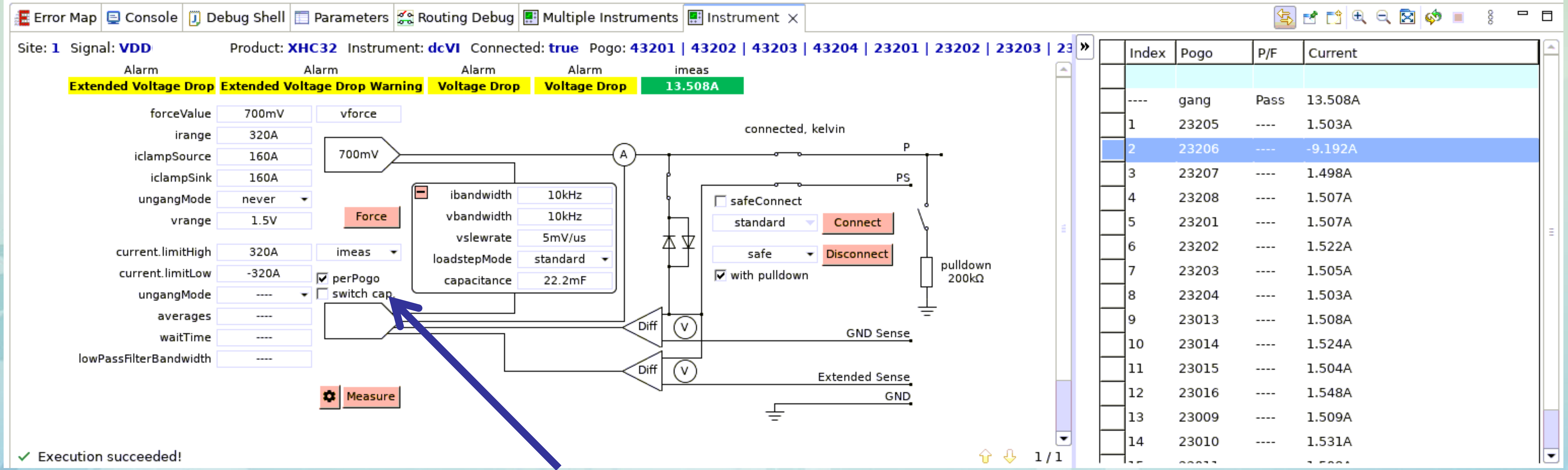


Excellent accuracy required to detect vDrop change across the Probe Head or Socket

Per Channel Result (Ganging Granularity)

- **result.ganging.granularity = perPogo;**

- **dcVi result properties – TDC Topic dcVi_propGroup_result**



Enable perPogo results on Instrument view

Ganged on the Fly: Dynamic Master Channel Switching

Redefining master channel Per Spec

DUT Board File (.dbd) – Global Definition

- ***First channel is master***
- ***Add unique signal name for desired master channel scenarios***

```
signal VDD        {
    site 1 { pogo = 43201|43202|43203|43204|23201|23202|

    defaults.protection.maxVoltageDropForce = 200mV;
    defaults.protection.maxVoltageDropReturn = 200mV;
    defaults.protection.warnVoltageDropForce = 50mV;
    defaults.protection.warnVoltageDropReturn = 50mV;
    defaults.protection.voltageDropHoldTimeForce = 1ms;
    defaults.protection.voltageDropHoldTimeReturn = 1ms;
    defaults.regulation.capacitance =     mF;
}
```

Spec Definition – Uses the desired master channel signal name for selected content

```
setup dcVI VDD        {
    connect = false;
    disconnect = true;
    disconnectMode = safe;
    level.vforce = VDD       ;
    level.vrange = 2.0V;
    level.iclamp = VDD       _iclamp;
    level.irange = VDD       _iclamp;
    level.riseAfter = VDD_11_S3;
    level.riseDelay = RiseDelay_C;
    level.vriseRate = 1V / ( 5.0 * 1ms );
    level.waitTime = 10ms;
    level.postWaitTime = PostWaitTime;
    level.vfallRate = 0.5V / ( 5.0 * 1ms );
    //profiling.operatingMode = local;
    //profiling.recordMode = single;
    //profiling.voltage.enabled = true;
    //profiling.current.enabled = true;
    //profiling.sampleRate = 50kHz;
    //profiling.start = -1s;
}
```

Useful for changing master sense line when IR drop across a power plane varies with test content

vDrop measurement example

TDC Topic 354548

Voltage drop measurement example

Voltage drop measurements are supported by the vdropForce and vdropReturn properties of the dcVI meas action. Measurement filters and Hardware based averaging are also available for voltage drop measurements.

Specification file for a voltage drop measurement on the force line (P#):

```
action meas meas_forceDrop{
    averages                = 16;
    lowPassFilterBandwidth = 100kHz;
    waitTime                = 1 ms;
    vdropForce.enabled      = true;     // Enable forceDrop measurement
    vdropForce.measType     = average; // Option: average, max
}
```

Specification file for a voltage drop measurement on the common return line (GND):

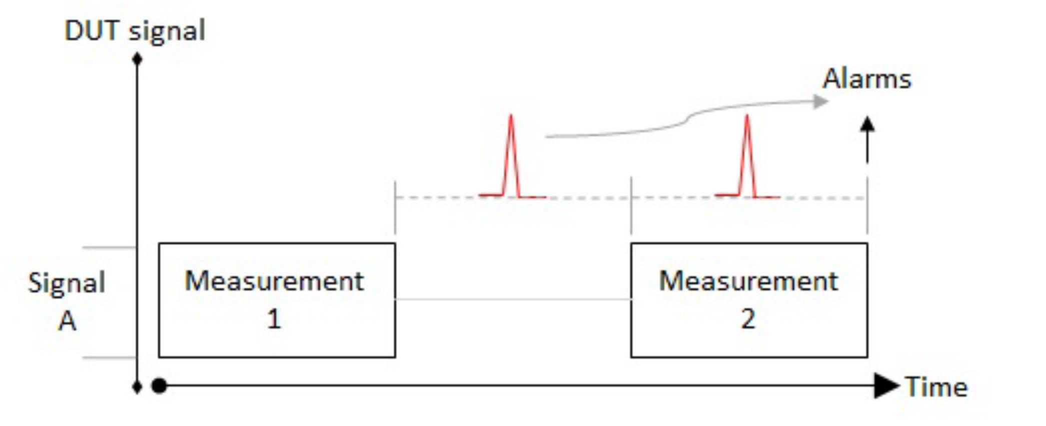
```
action meas meas_returnDrop{
    averages                = 16;
    lowPassFilterBandwidth = 100kHz;
    waitTime                = 1 ms;
    vdropReturn.enabled     = true;     // Enable returnDrop measurement
    vdropReturn.measType    = average; // Option: average, max
}
```

Note: Although the return path "GND" is common for all channels of an XPS256 / XPS128 card, the voltage drop is measured individually for each channel between an internal ground sense reference point and the channel specific "GS#" to "GND" connection at the DUT or on the DUT board.

Surge Tracker - TDC Topic 344312

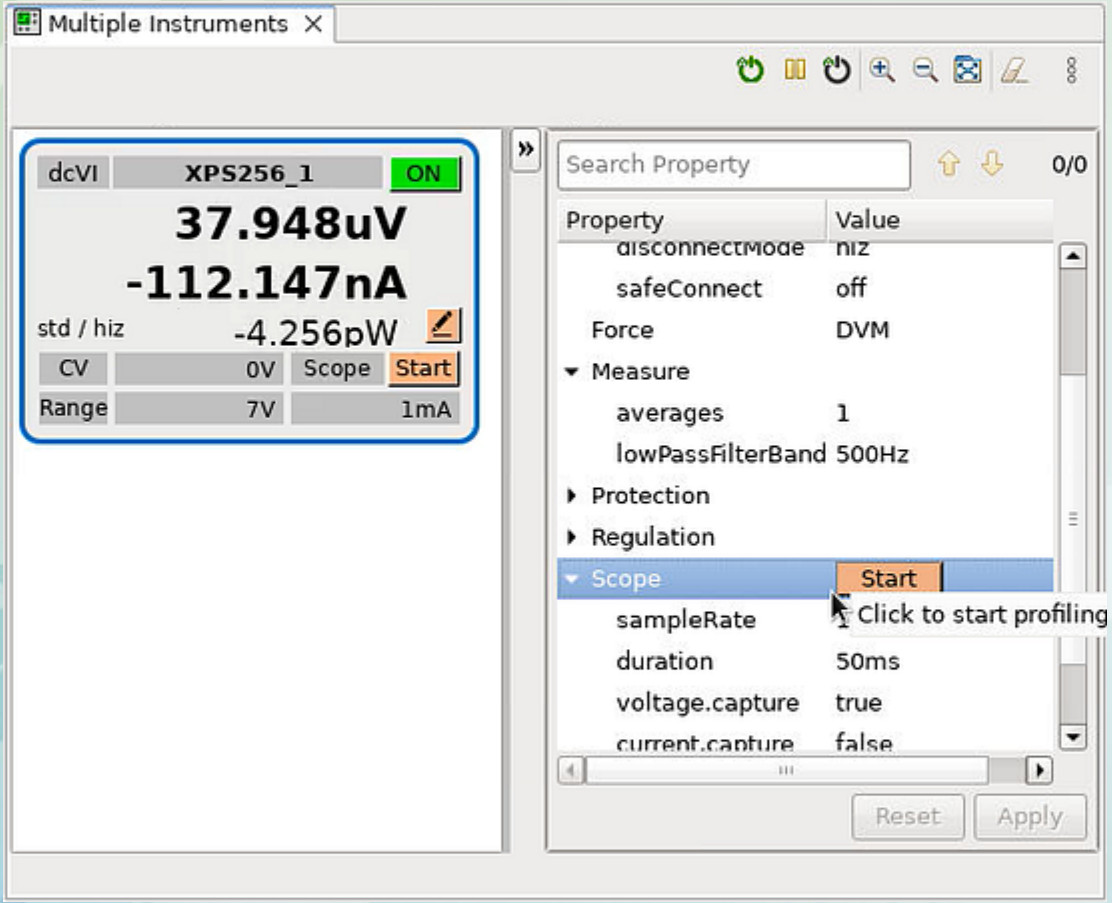
DC VI Instrument Feature

- The surge tracker is an electronic circuit that is part of the dcVI instrument. You can use it to detect any glitches in the current or voltage applied to your DUT during and between measurements.
- Current and voltage glitches-a very fast temporary change in the voltage or current applied to your DUT-can shorten the lifetime of your DUT or even permanently damage it.
- Potential causes of glitches:
  - The instrument is not correctly setup, for example, you forgot to specify the slew rate
  - Your DUT board is defective, for example, due to a broken capacitor on it
  - The test head hardware behind the used instrument is defective
- When the surge tracker detects a current or voltage glitch, SmarTest will **alarm**



Interactive Background Profile Setup

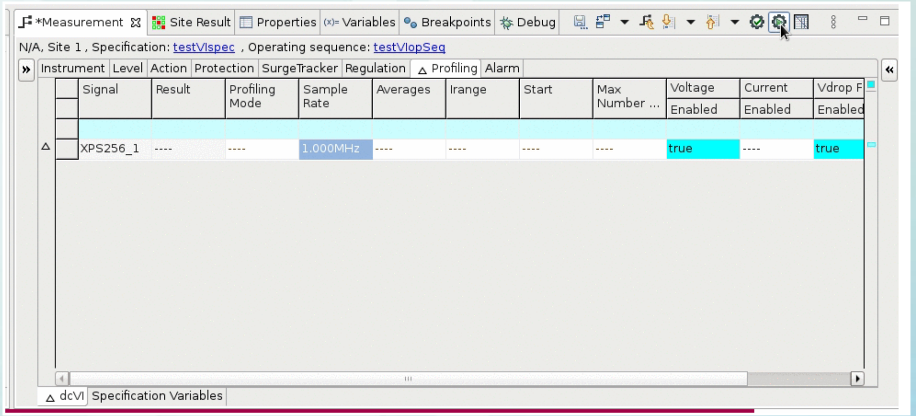
Starting & stopping background profiling – TDC Topic 362097



From the **Multiple Instruments** view, start profiling by clicking the Start button in the diagram or in the Properties pane.

Measurement view supports interactive profiling for an individual test / operating sequence

See **TDC Topic 173505187** - Profiling with XPS256 in Debug from the Measurement View



API Based Profile Setup

Background profiling of test flow or a single test suite / operating sequence

- Background Profiling Start/Stop classes available in dcTML:
  - com.advantest.itee.tml.dctml.DCProfilingOverFlowStart
  - com.advantest.itee.tml.dctml.DCProfilingOverFlowEnd

- Individual OpSeq Profiling:
  - Setup Profling Properties & dcVi action: Profiles a single opSeq run by default
  - ScanTML has built-in profiling support: com.advantest.itee.tml.scan.ScanTestProfiling

- See TDC Topic 344313 - DC profiling the current and voltage waveforms applied to your DUT