SWTEST
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KGD - Ultrafast Dynamic Power Device Probing

T. I. P. S.
Technical Innovation – Physical Solutions

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Intro

- The D.U.T. and (some) tests
- Test setup for ultrafast high power pulses
- Electro-thermal aspects – simulation approach
- "Real world" examples
- Probe cleaning - aggressive + high temp
- Summary

The D.U.T. : Power Devices, bare die

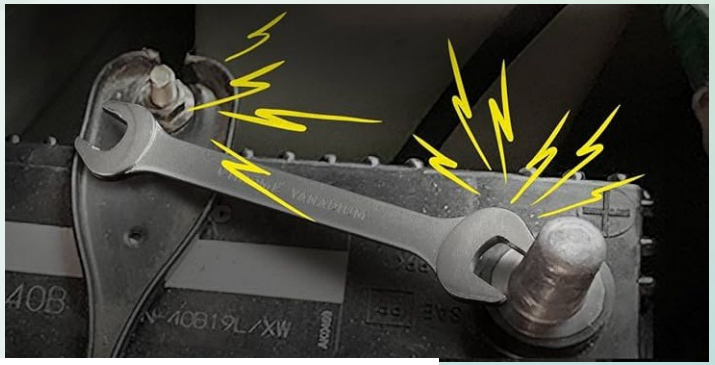
- Power devices in Si, SiC technology, as MOSFETs, JFETs, IGBTs,...
  - For renewable energy , EVs applications (powertrain, charging stations), ...

bare die, SiC and wafer
(photo courtesy: Microchip)

- Reliability and quality of SiC power devices: one of the key topics under high volume manufacturing focus

MOSFET / IGBT overload conditions

- Highly stressful overload conditions - unclamped inductive switching (UIS) and short circuit (SC): extreme heat inside the chip on a short time scale
  - For inverters both for industrial or traction applications, high current overload events like a short circuit on the load may occur for a variety of reasons...
  - Several kinds of protection circuits can be proposed to avoid high-current catastrophic failure (e.g. pyroelectric circuit breakers / battery disconnect devices)

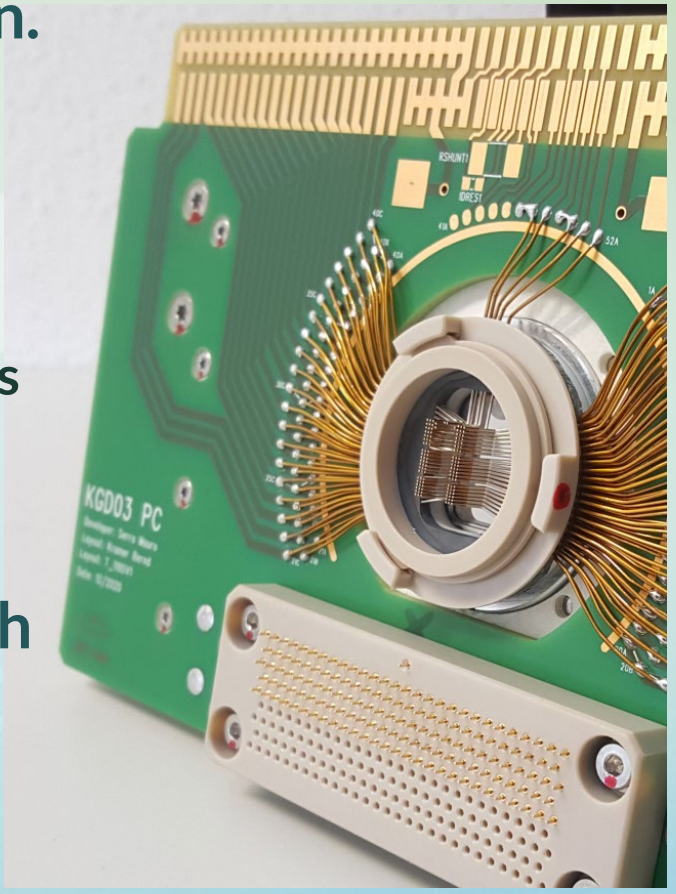


(photo courtesy: KiWAV Motors)

  - However - any power device used in above applications must have a reasonable short-circuit withstand time and energy dissipation capability before the protection circuitry kicks in.

Ultra-Fast Dynamic Power Test

- Test aimed to fully characterize the dynamic behavior and robustness of the power devices in similar conditions as in the final application.
  - SCT and UIS implemented on singulated die for sorting out "hidden" defects that are revealed only at very high enery levels and might not be detectable in "static DC" tests as R_{on} and HV_{leak}
  - Sorting out bad die before assembly into packages or power modules (-> need for "Known Good Die")

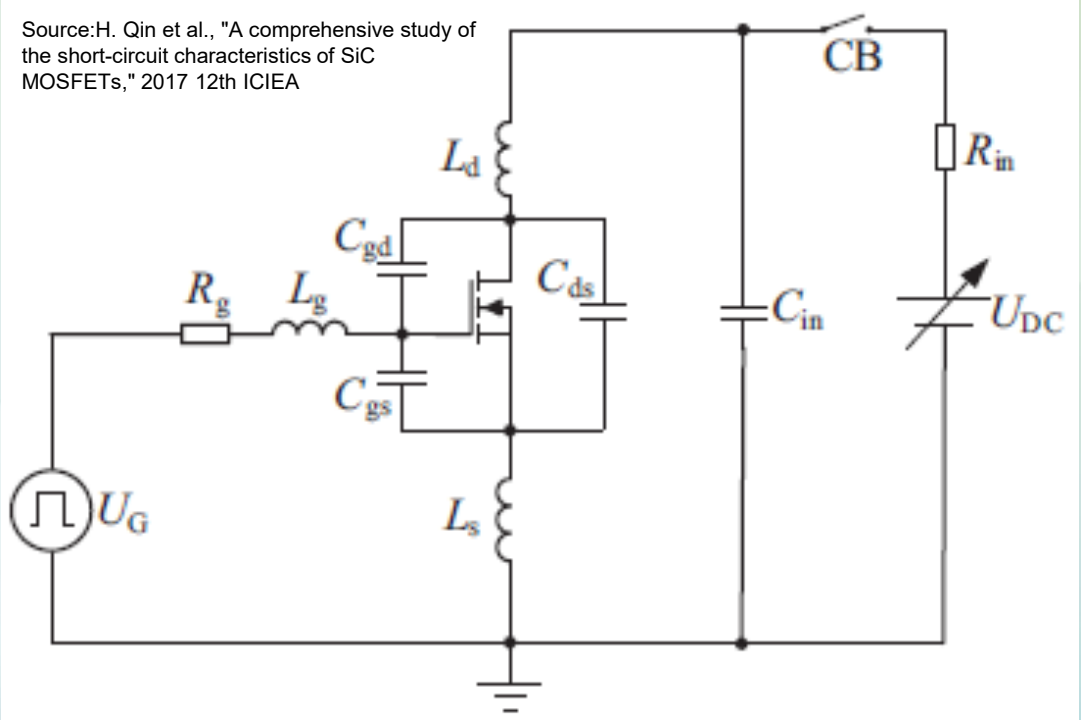


- From a technical point of view singulated die test (KGD) with its intrinsic potential to minimize parasitic inductance is the key for enabling ultra-fast switching test.

Short-Circuit Test (SCT)

- Pulses of Megawatts during Microseconds – MW@µs

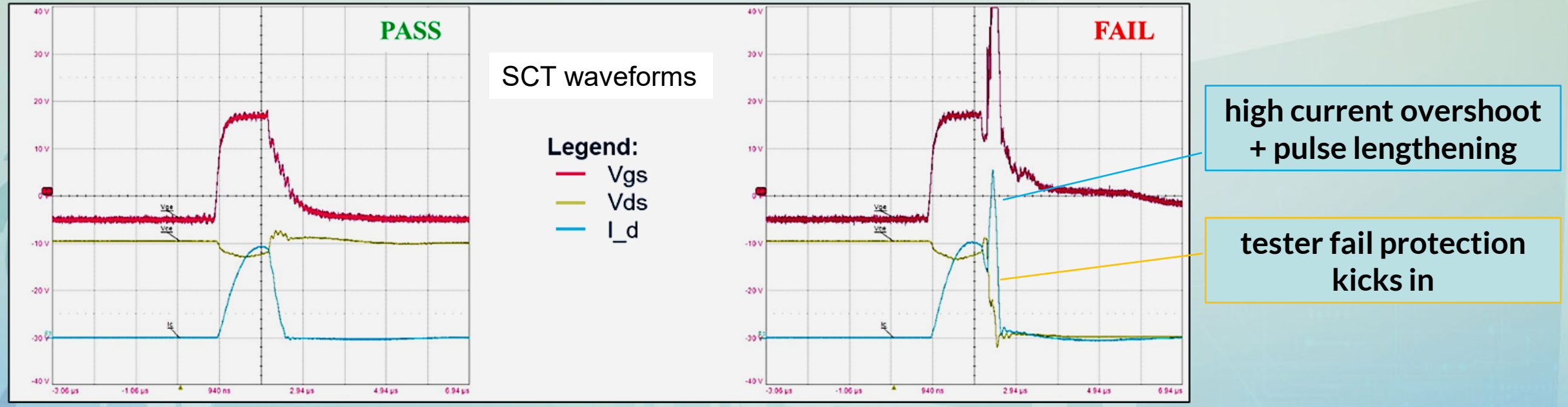
- Test sequence:
  - at t0: CB is closed with the MOSFET switched-off with U_G<0V
  - the device is switched on (UG>>VTh), dissipating energy for a nominal SCT withstanding time, then switched off (UG<0V)



Typical SCT electrical schematics, including device parasitics and key features of the test circuitry. These parameters strongly influence high current waveform and test behavior.

"Dynamic" tests - what happens within µs?

- "Dynamic" power test is 1000 times faster than "static" test: µs <-> ms!
  - pulse duration / time domain becomes essential for probe contact temperature
  - other significant factors:
    - contact resistance (Cres) and contact area -> probe tip cleaning!



Short-Circuit Test - Pass and Fail

- SCT catastrophic failure mechanism
  - "Hot Spot" formation: high power density concentrated to a localized small area on the chip
  - A localized thermal runaway process in the chip occurs leading to an uncontrollable increase in the MOSFET drain current
  - Catastrophic event occurs: locally molten pad metallization + sublomation (metal splash), thermo-mechanical strain in chip material leading to breakage /cracking of chip, cause adverse effects on contactors (probe card / micro chuck)

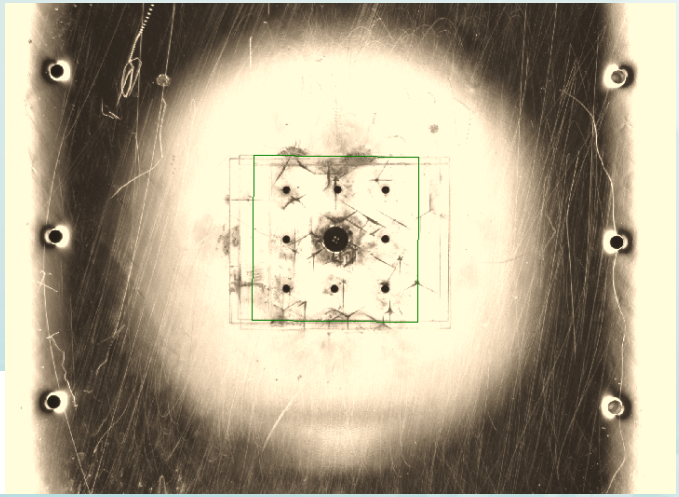
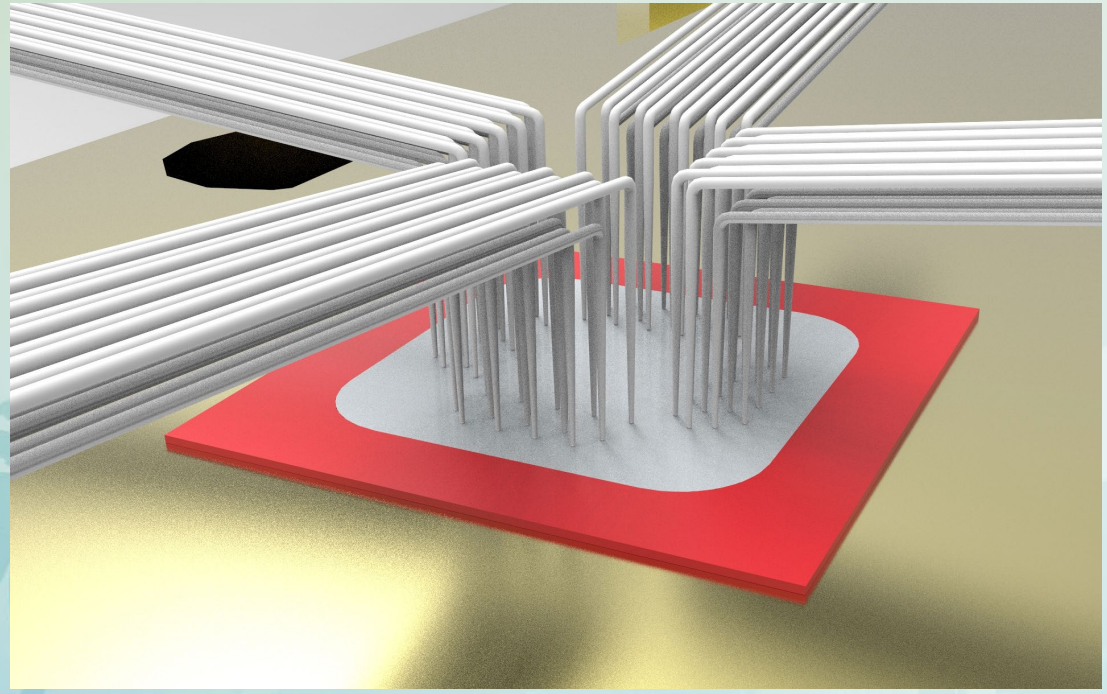


Fig. 3: chuck damage from broken chips

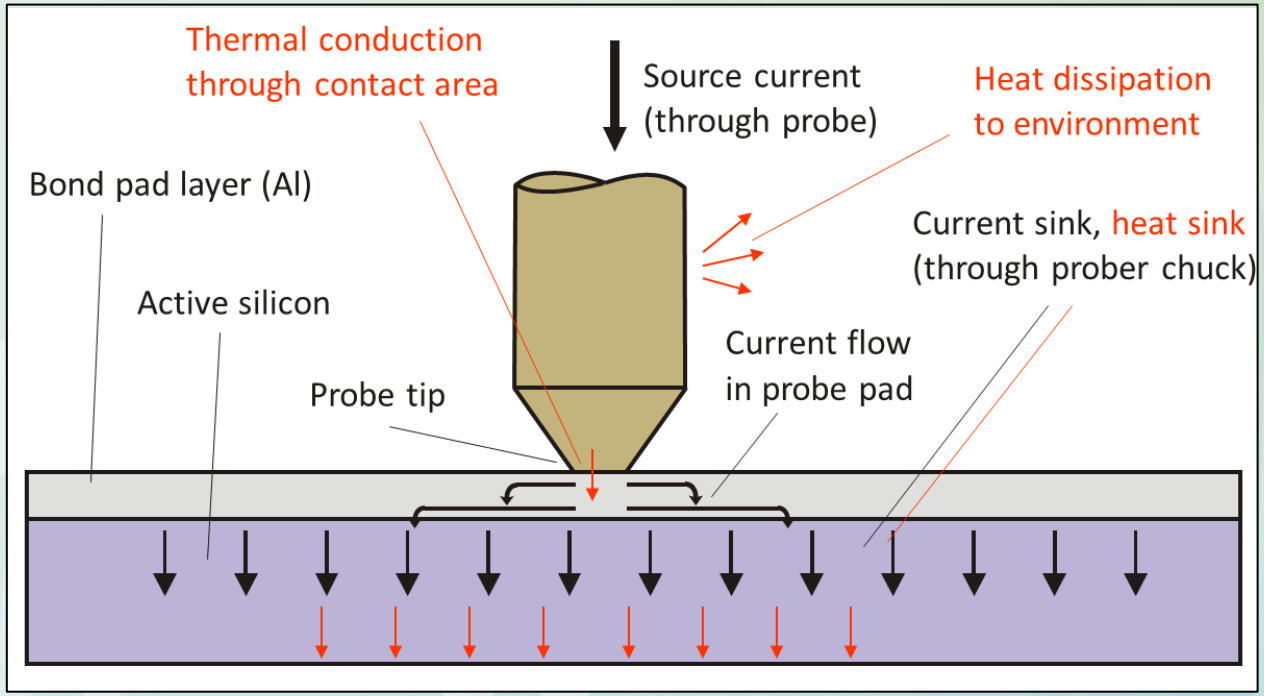
Fig. 4: "hot spot" damage on chip pad metal

Making Contact: Electro-Thermal Aspects

- Contact case study – electro-thermal simulation: high current cantilever probes
  - Current density level: 17 A per probe during SCT pass, surging up to 48 A per probe during SCT fail



Cantilever probes contacting power device

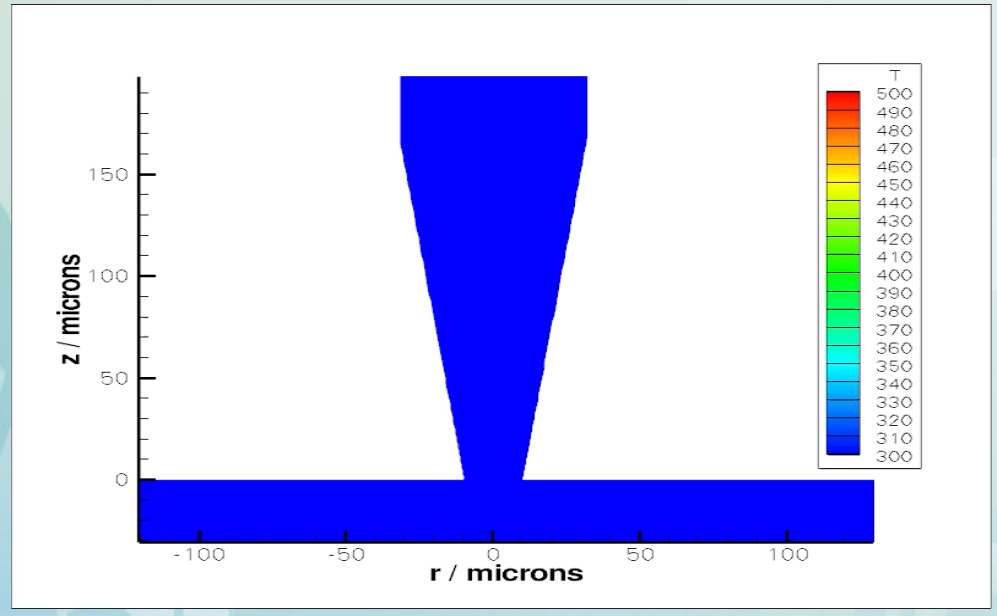


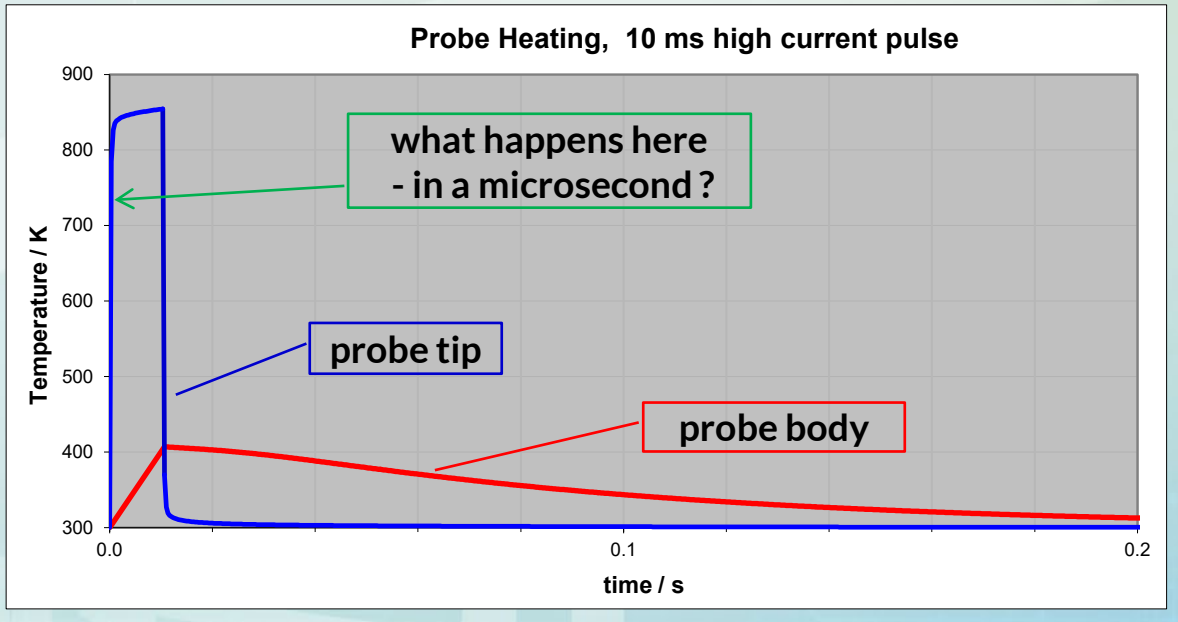
geometrical model of chip – probe contact used for electro-thermal simulation [1)]

1) Aspects of High Power Probing, SWTW 2011

Electro-Thermal Simulation

- "Finite Volumina" method for numerical solution of the "Instationary Thermal Equation"
  - 2011 work: "classic" high current test considered [1)]
  - typical pulse length for "static" high power tests: **milli-second** (ms) range, "dynamic" tests: **micro-seconds** (µs)
  - probe tip heating is predominant
  - mainly depends on current amplitude and Cres
  - "**static**" power tests: **pulse length is not a factor for probe tip heating** (for pulses in the milli-second range)!



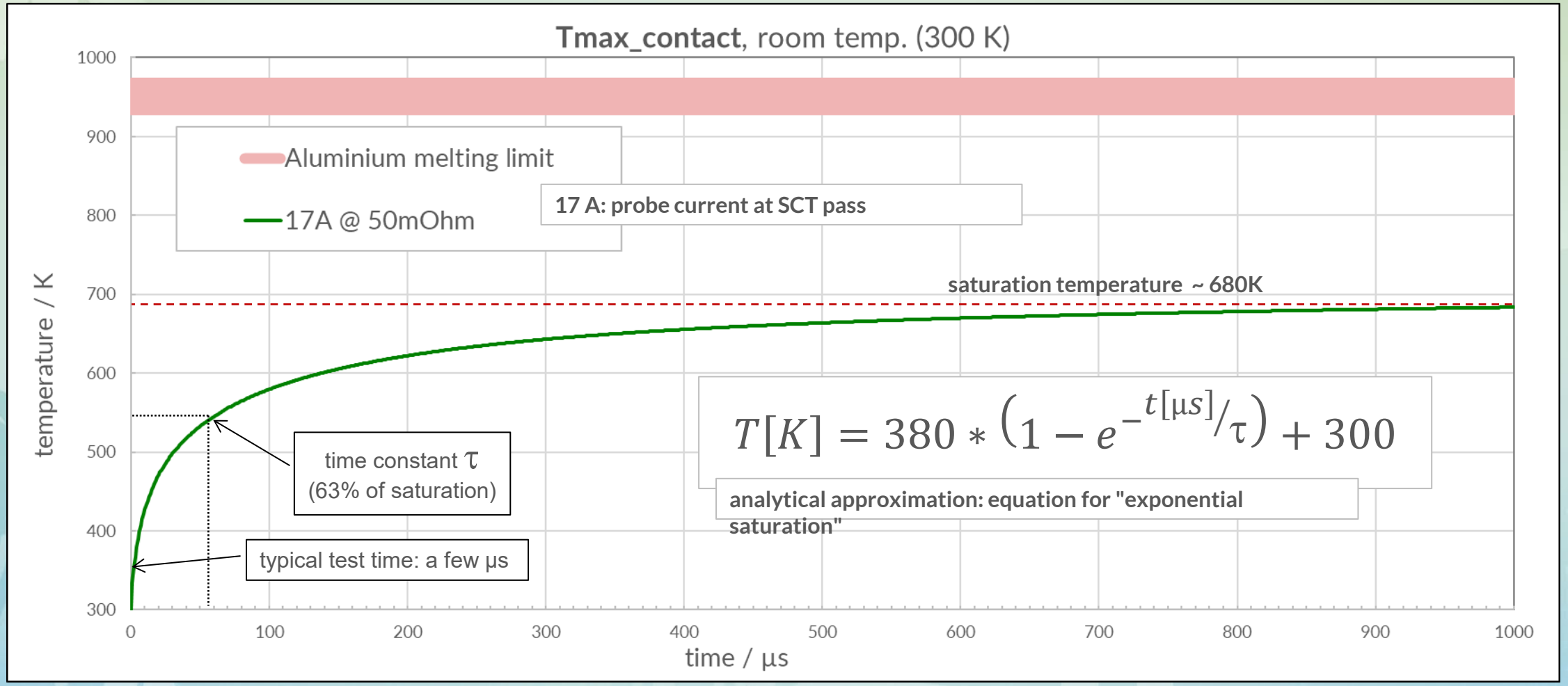


1) Aspects of High Power Probing, SWTW 2011

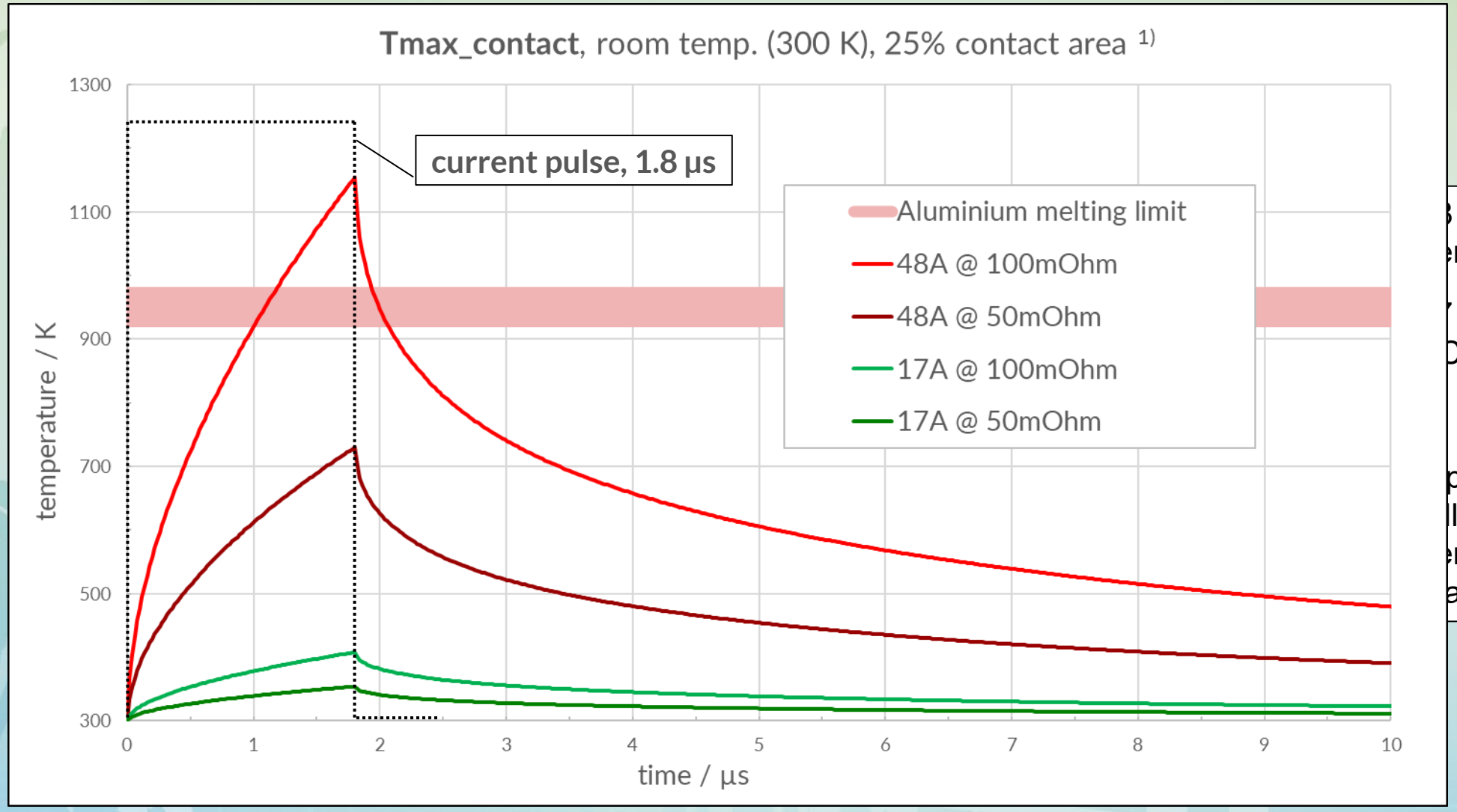
Simulation Results – Points of Interest

- fast dynamics at the probe/chip contact - µs time domain!
  (find out time constants for probe tip/contact heating)
- current density influence
- contact resistance variation
- contact area change (e.g. due to probe tip shape change)
- 3-dimensional effects (-> thermally induced mechanical stress)

Contact Heating – Time Domain Dynamics



Contact Heating – Current Density / Cres



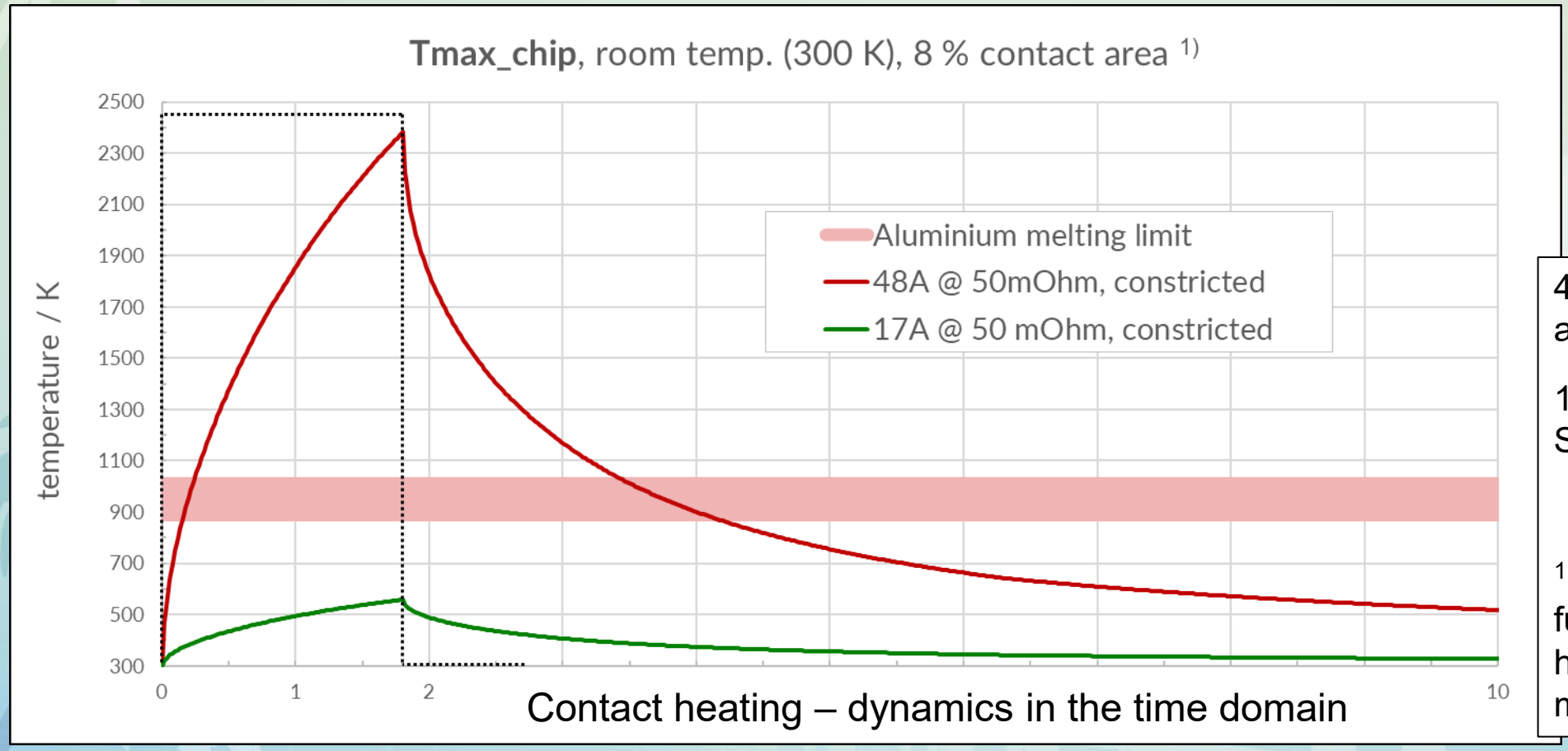
A: max. probe current
nsity at SCT fail

A: current density at
T pass

percentage of
l probe tip area
re: 50% of tip diameter
aking contact

Contact Heating – Contact Area Constriction

- reduction of contact area due to fusing of chip material to probe tip

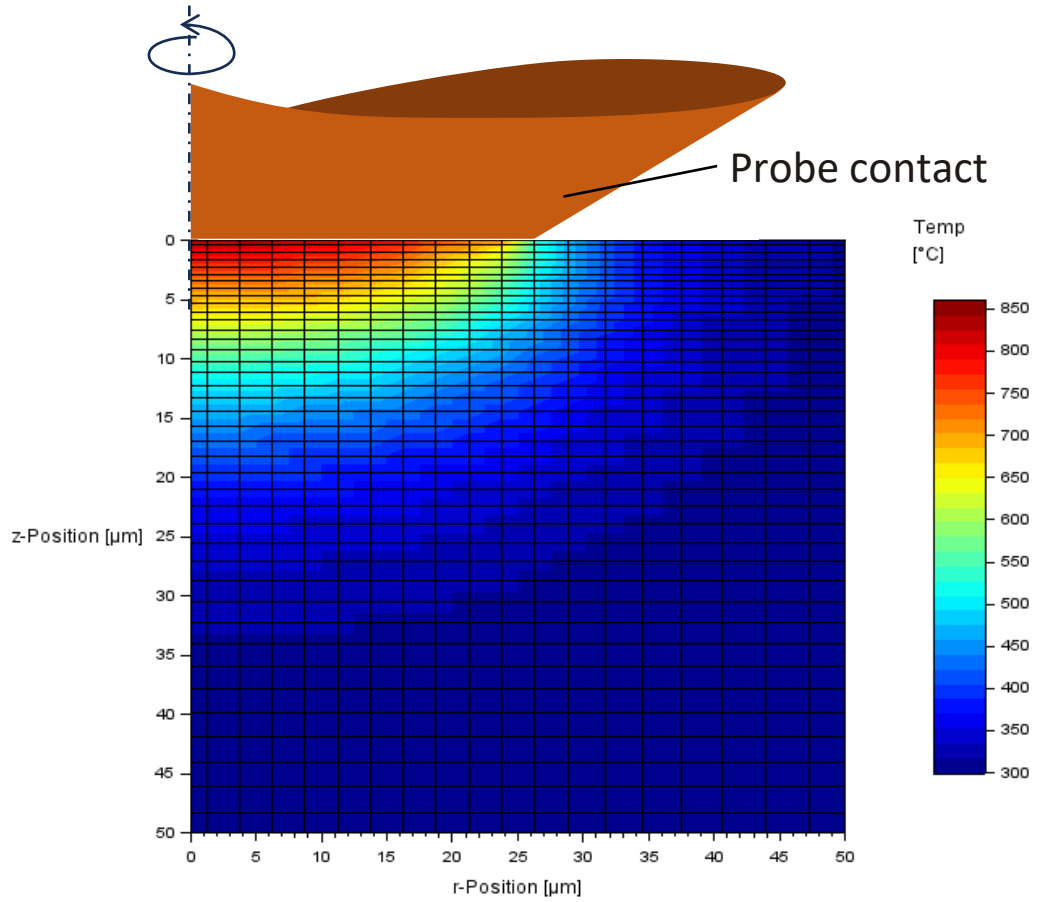


48 A: max. probe current at SCT fail

17 A: nominal current at SCT pass

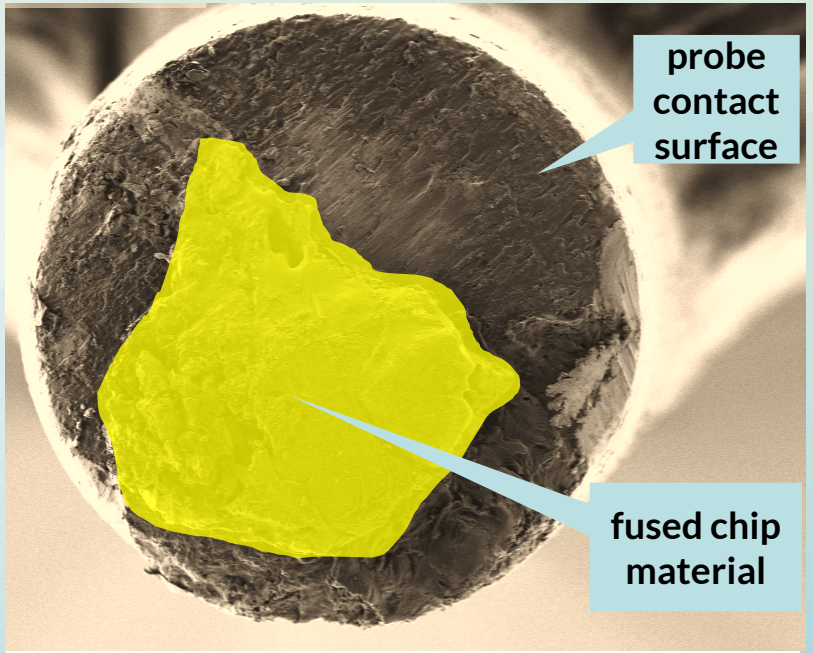
1) percentage of full probe tip area here: 20% of tip diameter making contact

Contact Heating – 3D Profile



Temperature distribution inside chip after current pulse (constricted contact)

- steep thermal gradient inside chip volume + associated thermo-mechanical stress
- might be an explanation for these:
  - chip cracking
  - fusing of chip surface fragments to probe tip...



SEM image of probe tip showing fusing of chip surface material

Probe Tip Cleaning

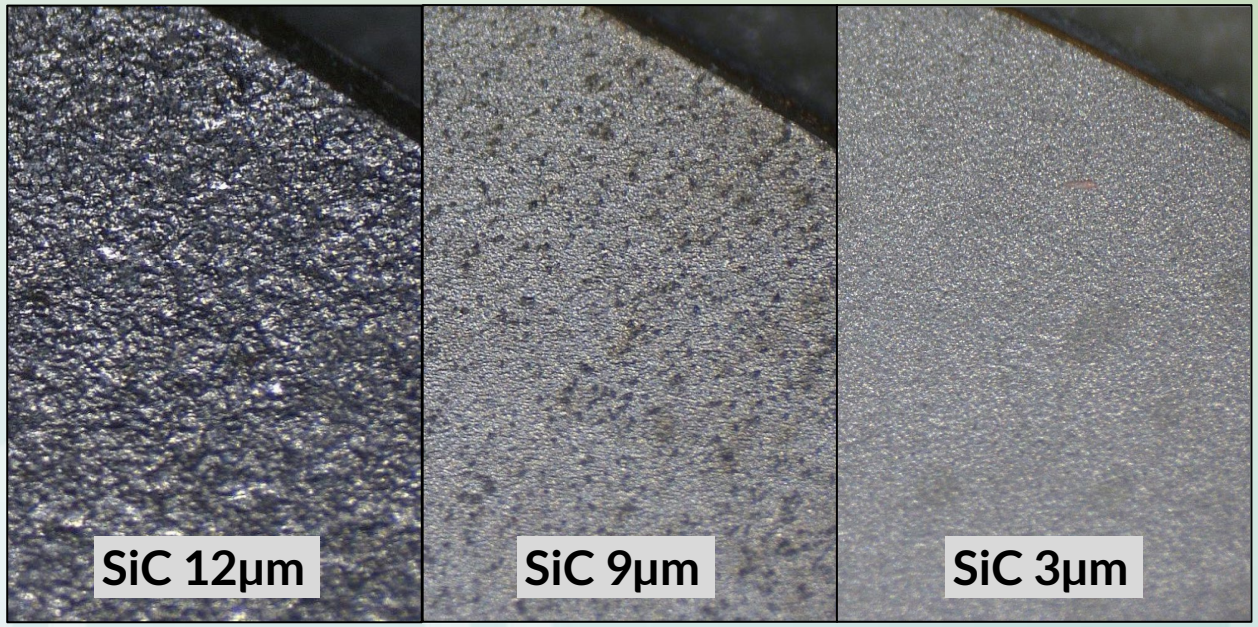
- Probe tip condition has a major influence on contact behaviour
  - chip material fused to original probe tip may form a small diameter "secondary tip" -> constriction heating + high Cres
  - hard sticking fused contamination
- Traditional online cleaning "too soft"
  - too many cleaning strokes required will affect test throughput
  - fine grain lapping films ineffective in "breaking loose" chip-borne contaminants
  - non useable on high temperature micro chuck (polyester film will blister...)
  - short lifetime (Epoxy-based binder for abrasive grain)

➢ A radically new approach to online cleaning media is needed...!

High-Performance Probe Lapping (1)

- metal bonded abrasive grain

"Court Alchimist" Dr. Salbrechter in action

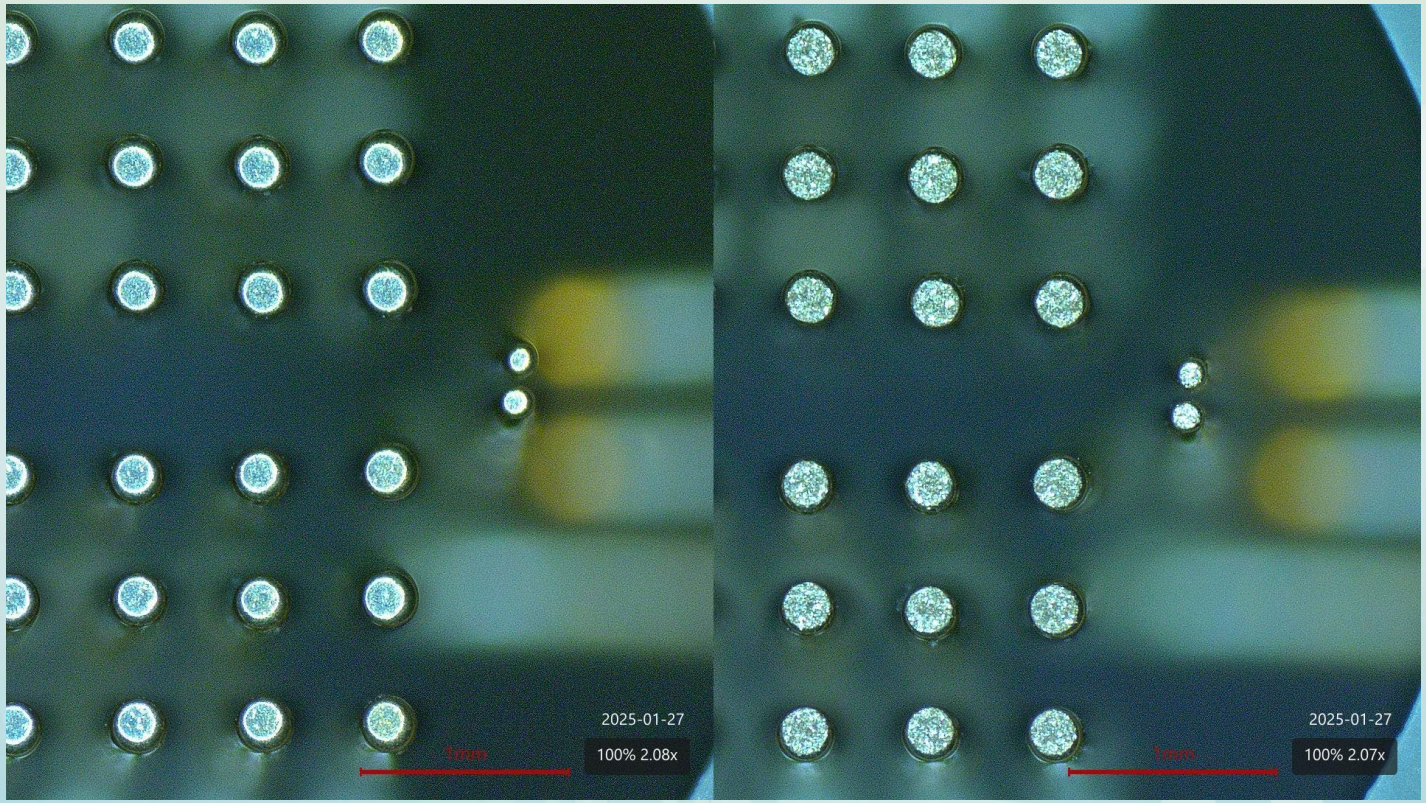


Lapping discs with different grit sizes

- coarse-grit lapping plate to break out chip-borne contamination and establish a contact surface with defined roughness -> consistent Cres stability
- high temperature tolerance (hot chuck application, 200 °C)

High-Performance Probe Lapping (2)

- First qualification trials on KGD handler look very promising, news coming soon...



Conclusion

- Ab-initio simulations can give deep insights into dynamics of the thermal behavior of the probe – chip contact for fast high current pulses.
- These lead to much better insights in failure modes at extreme high power device testing, as short circuit test
- Methods both from the probe design approach ("pulsed – CCC model") and from operational aspects ("hard and heavy" online cleaning) are established to enable a smooth testing process together with an acceptable probe card lifetime.

Thanks to the people and teams contributing to this work...

...and THANK YOU for your attention!

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