SWTEST
PROBE TODAY, FOR TOMORROW
2025 CONFERENCE

# Advanced Localized Thermal Management for Wafer Probing in High Power AI and GPU Applications Under Dynamic Thermal Conditions


Klemens Reitinger
ERS
CTO

Klaudiusz Holeczek
watttron
The benchmark of efficiency
Head of R&D and BDM

# Agenda

1. Motivation
2. …in the News
3. Test Strategies for Semiconductor Makers
   a. "Shift left"
   b. Full content test
4. Technical Challenges
   a. Thermal behavior during test
   b. Thermal resistance
5. ERS concept of section controlled fast thermal responding chuck
   a. SLC -> enables ATC at wafer probing prior to dicing
6. Results and outlook

# Motivation

## Traditional Test flow:

Wafer Finish → Wafer test (probing) $ → Dicing → Optical bare die test $ → Packaging → Final Test $$$

## HPC Chiplet Test flow:

Wafer Finish → Limited wafer test (no thermal control) $ → Dicing → Full content bare die test $$$ → Packaging → Final Test $$$

## Ideal HPC Test flow:

Wafer Finish → Wafer test (full content die = ATC) $ → Dicing → Optical bare die test $ → Packaging → Final Test $$$

# ...in the News

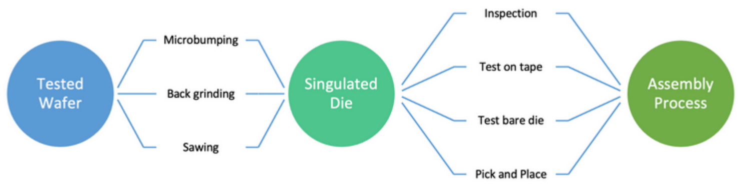



Fig. 1: Manufacturing process steps from tested wafer to assembly process. Source: A. Meixner/Semiconductor Engineering

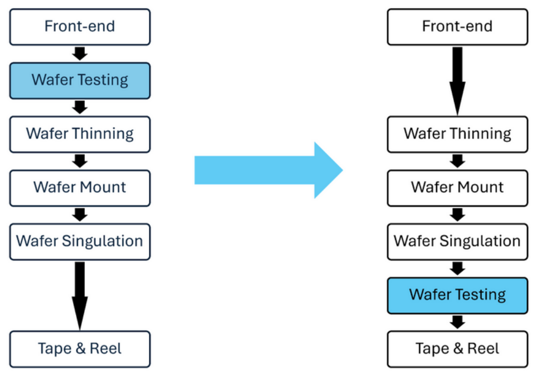



Fig. 3: Wafer level packaging process flow showing shift right of wafer testing. Source: A. Meixner/Semiconductor Engineering (after Ref. 9).

**Key Message:**
**HPC Wafer test**
**"shift right"**

## ATC = Active Thermal Control

"ATC capability can enable additional stress testing and test conditions more closely resembling package testing for higher voltage and frequency corner testing," said Intel's Gardner. "This can boost good die into packaging, which in turn can improve package test yields. Singulated die testing's ability to run higher frequency testing can also enable binning and performance segregation before packaging. This, in turn, can enable better die pairing of chiplets during the assembly process, which can be an additional benefit to advanced packaging products."

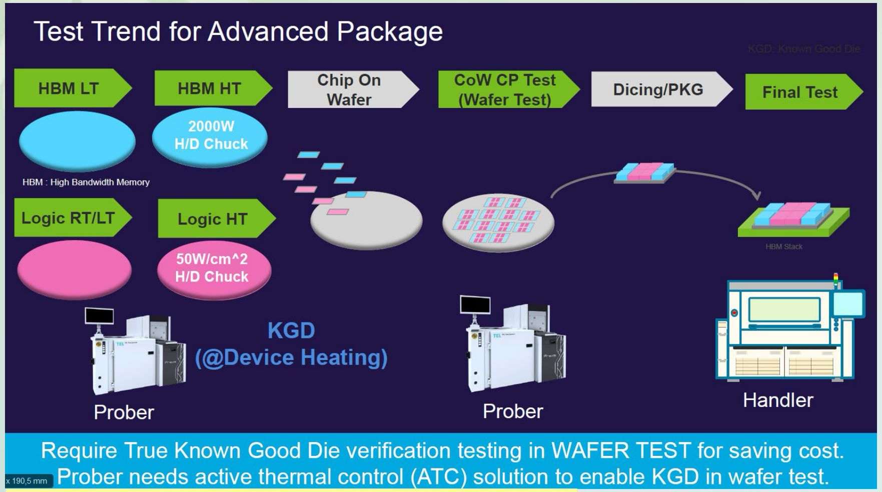
And active temperature control, once only possible at final test, now can be implemented prior to assembly to improve yield and reliability earlier in the manufacturing process.

**Key message:**
**Wafer test is not enough, only singulated die test can solve thermal issues.**
**But it is at high cost**

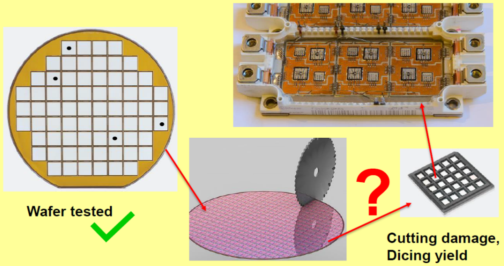
Source: https://semiengineering.com/quest-for-kgd-drives-singulated-die-screening/

# Test Strategies for Semiconductor Makers

## KGD for HBM and CPU/GPU




**Modules Yield...it's all about statistics**




| dicing process yield | single chip yield | 12x module combined yield | 32x module combined yield |
|---|---|---|---|
| 99% | 99% | 89% | 72% |
| 98% | 98% | 78% | 52% |
| 90% | 90% | 28% | 3% |

Yield 3%(!) in a 12-chip module

Source: T.I.P.S. GmbH ISTW 2019

## KGD for any Chiplet


Only way to solve this is to bring stress and full class content to sort. So-called, **Known Good Die.**

**Only way to solve this is to bring stress and full class content to sort. So-called, Known Good Die.**

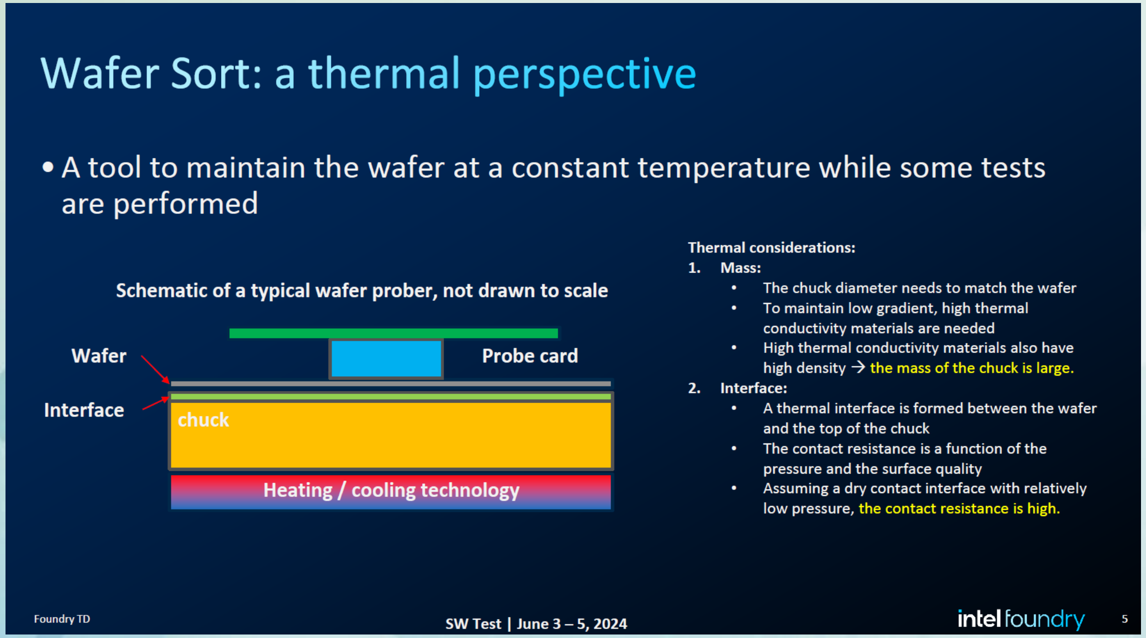
Source: Intel SWTW 2024 Carlsbad

**Key Message: No Wafertest / No bare die test = poor Yield**

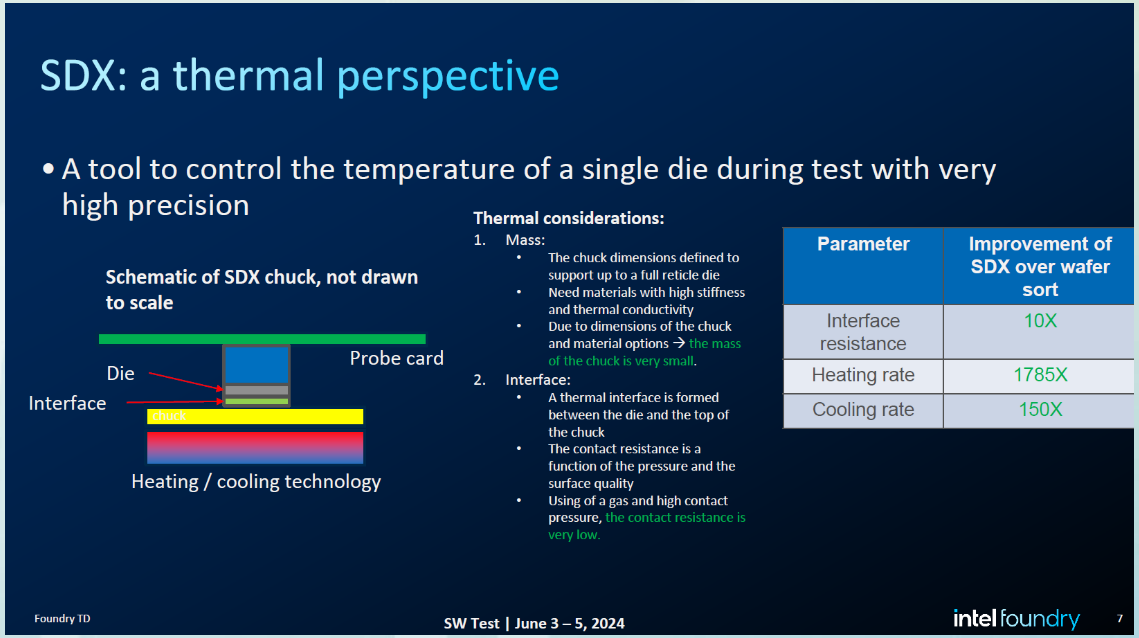
# Challenge: Thermal Behavior During Test

**Key Message:**
**The mass of the chuck is too large to have fast thermal change as it can be done with low mass in single die / final test**

## Wafer Test



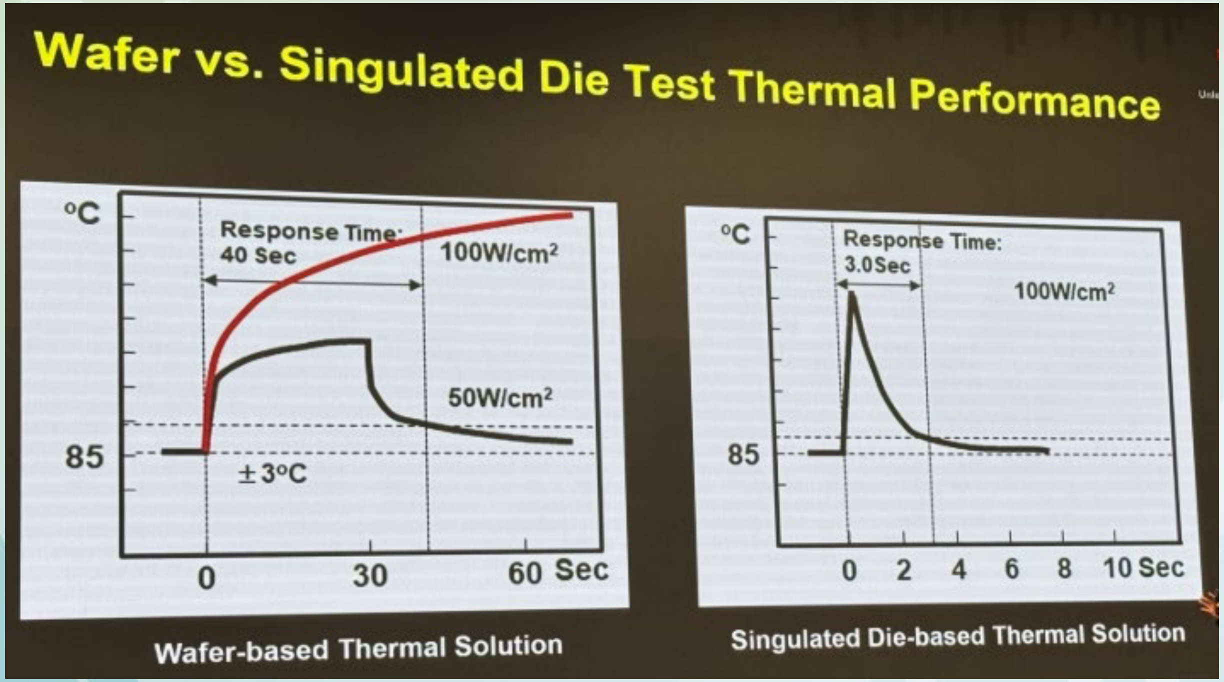

## Final Test




| Parameter | Improvement of SDX over wafer sort |
|---|---|
| Interface resistance | 10X |
| Heating rate | 1785X |
| Cooling rate | 150X |

Source: Intel SWTW 2024 Carlsbad

# The Fundamental Issue in HPC Wafer Test

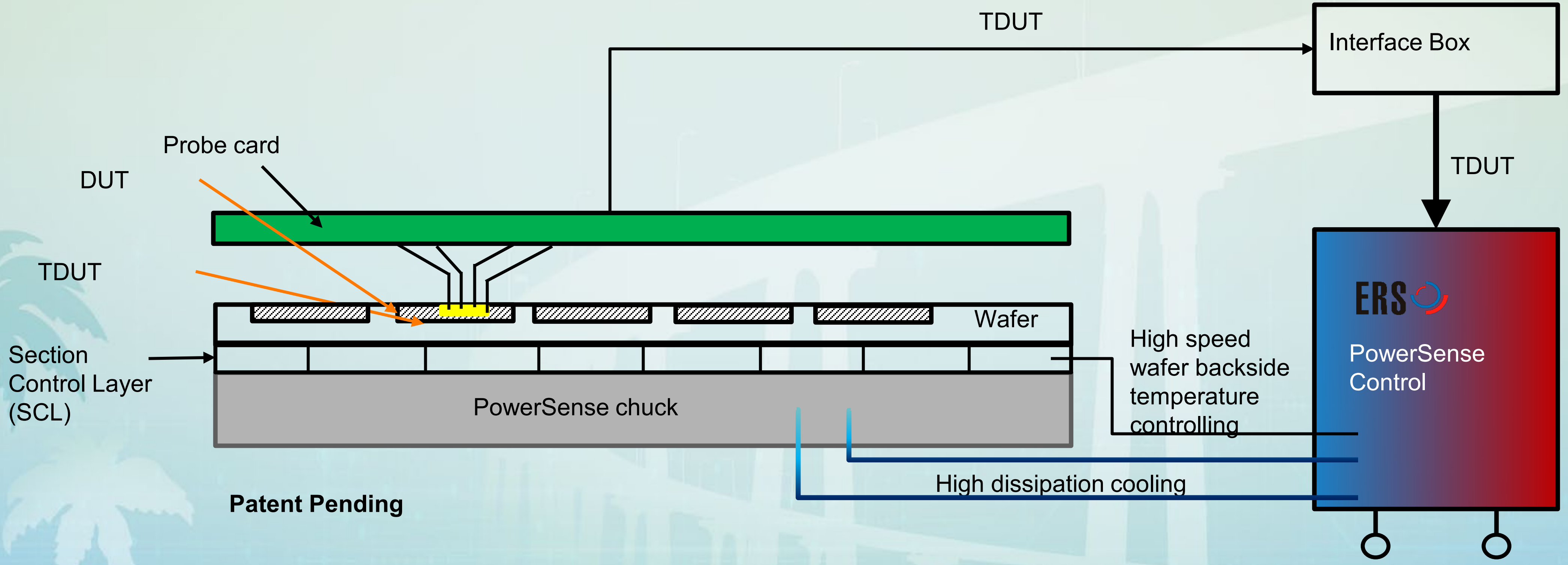



Source: TSMC I.S.E.S. Taiwan 2025

- **As a result of the thermal mass of the chuck, response time to power applicated locally is not fast enough.**
- **It is not enough to keep the top side of the chuck temperature constant, very fast lowering of the top side of the chuck locally is needed to keep DUT temperature constant**

# SCL Concept for HPC Wafer Test

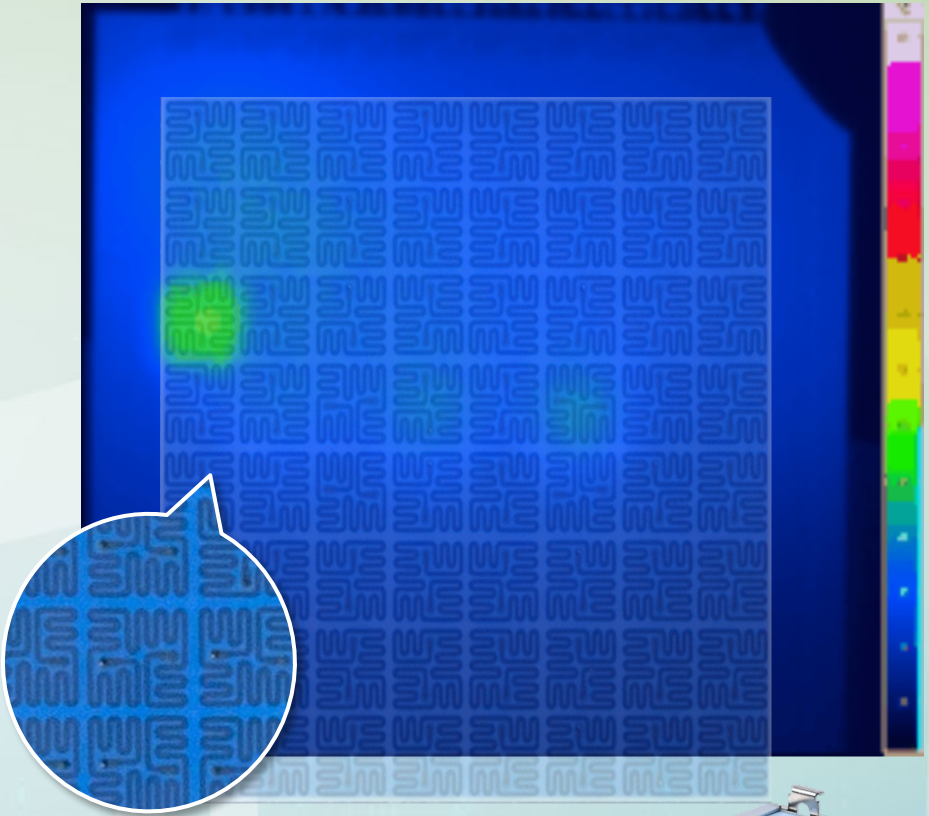
- Use ERS PowerSense Chuck System
- Use SCL (section layer) concept
- Use watttron Matrix Heater as section layer
- Use internal sensor for each section
- Use interface box to readout DUT temperature during test
- User DUT temperature for section control




**Patent Pending**

# Matrix Heater core technology (1/2)

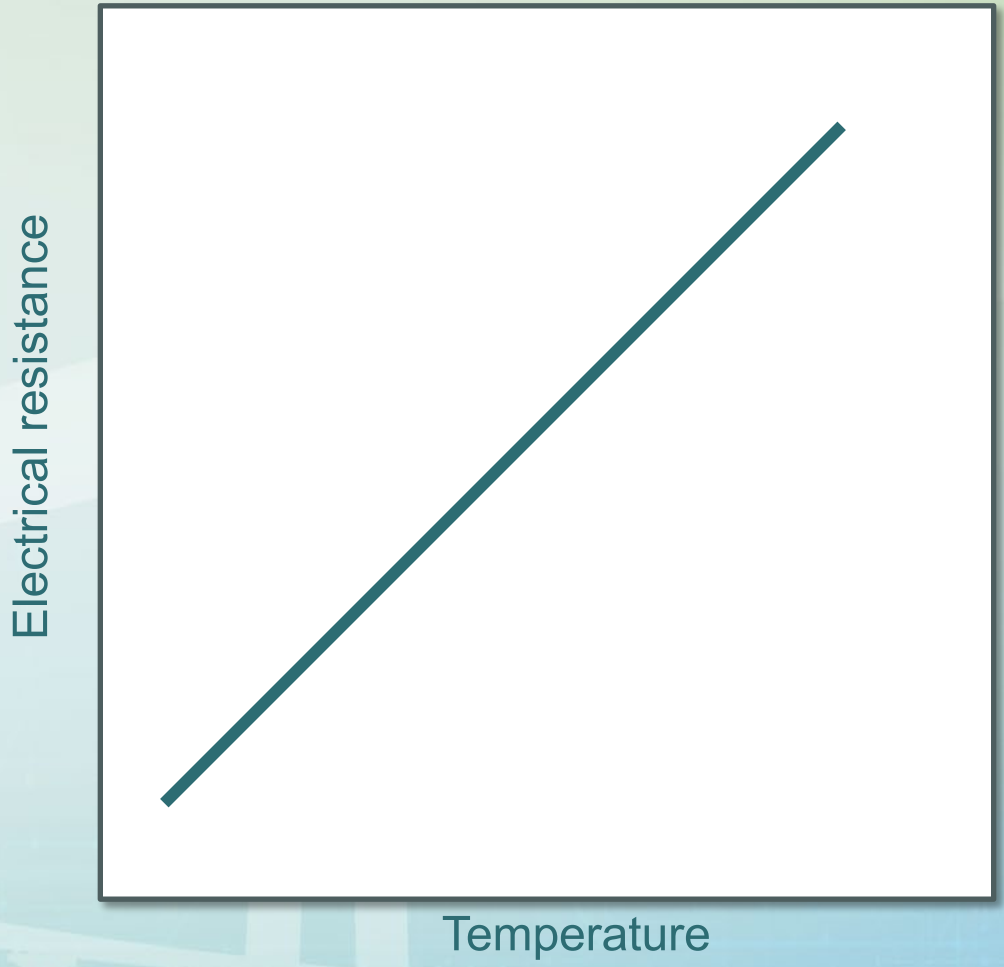
- 1000s of printed heating pixels for perfect temperature control
- Pixelwise temperature control allows either defined heterogeneous or perfectly homogeneous temperature distribution – that´s digital!
- Low thermal mass → Ultra-fast heating (up to 7000 K/s)
- ±0.5 K accuracy per pixel—even during ramp-up
- Broad operating range From ~35 °C (or below with cooling) up to 600 °C
- Can sustain a 100 K difference across just 5 mm



# Matrix Heater core technology (1/2)

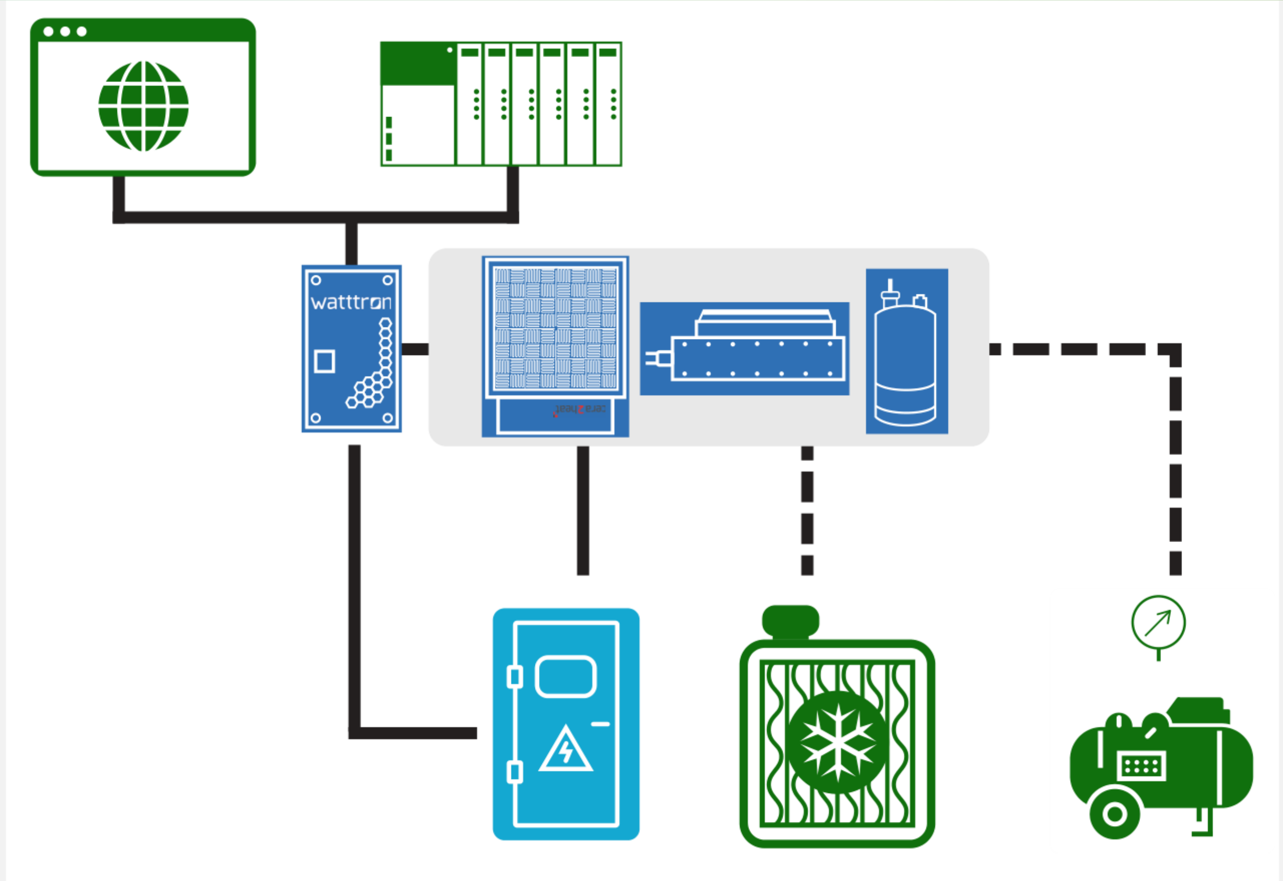
- Tripple functionality
  - Heating: Each pixel acts as a Joule heater when current passes through its resistive trace
  - Sensing: The pixel’s resistance change with temperature provides real-time feedback, enabling closed-loop control
  - Cooling: By attaching the heating pixels to a cooling block

Fast, spatially resolved, temperature-driven heater/cooler system



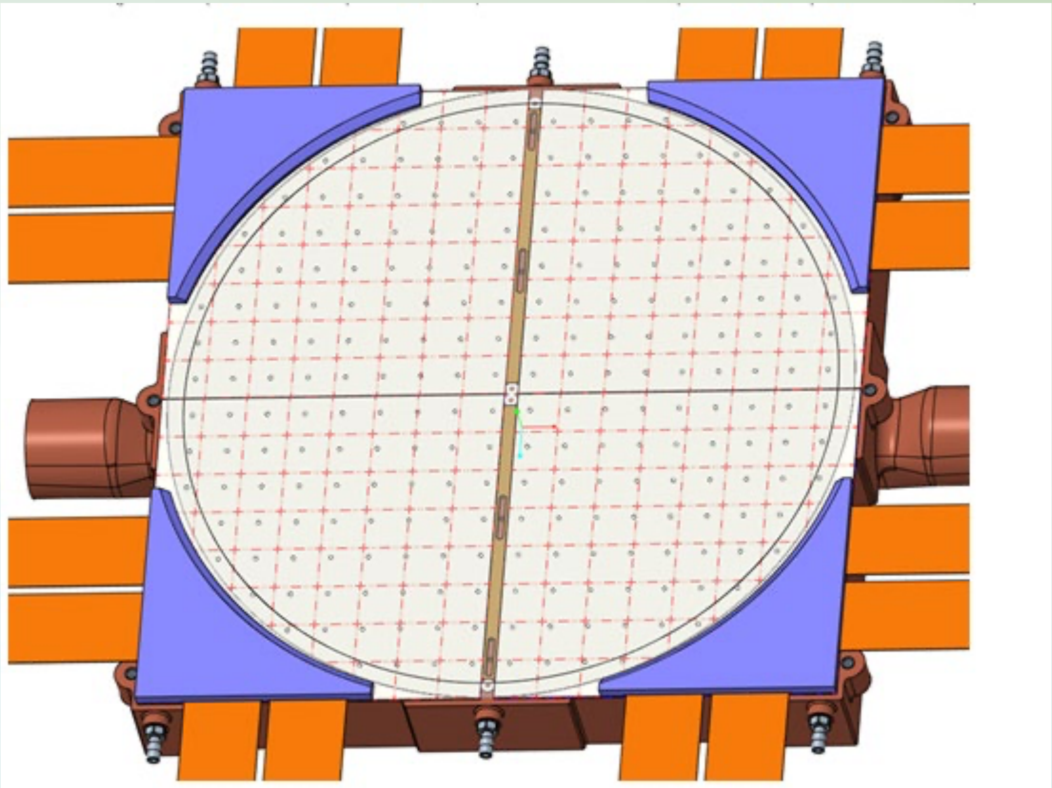
# Matrix Heater Key Features

- Up to 100 K/s cooling with water cooling
- Heats up to 850 K/s with sub. 1 K precision
- Wide Temperature Range: 35 °C to 600 °C
- Temperature Gradients: 100 K difference over 5 mm
- Power Density: Up to 180 W/cm$^2$
- Inert Materials
- Smart Control: Detects process deviations via temperature monitoring
- Scalable Design: Modular heaters fit various equipment sizes



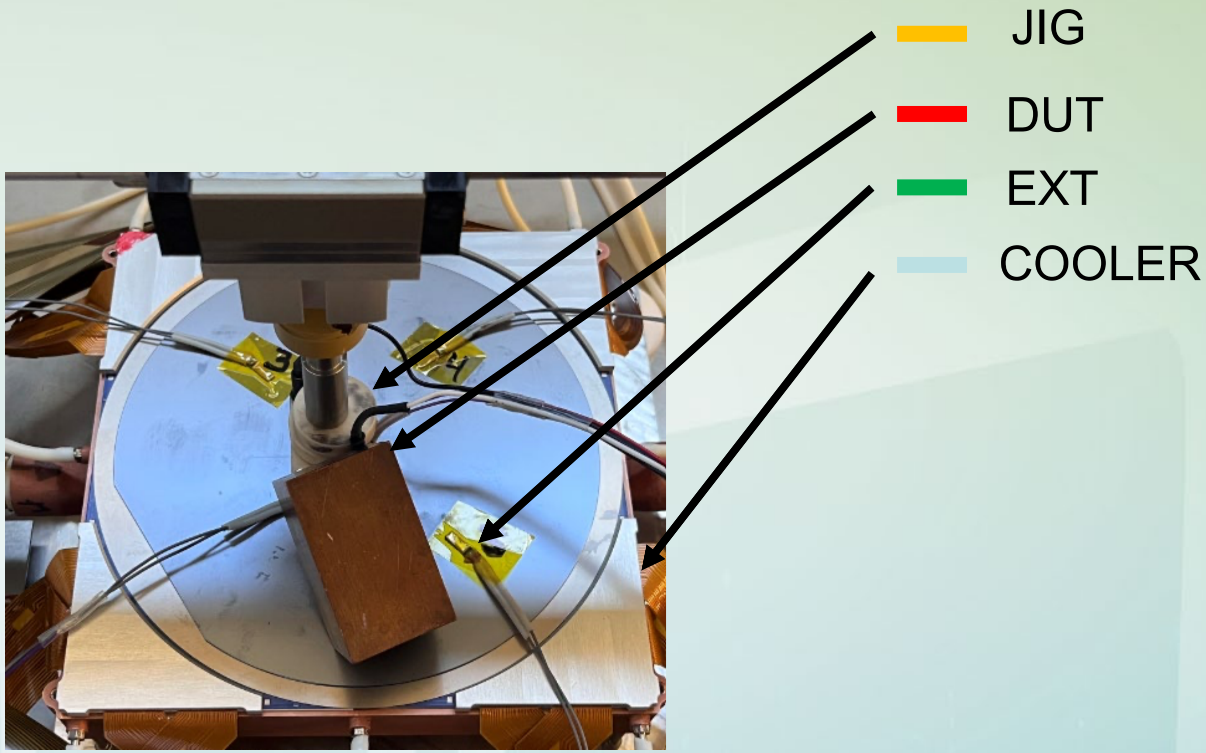
# HPC Wafer Chuck DUT Test Vehicle

- 150mm thermal chuck with 256 independent sensing and controlling zones
- Total dissipation power > 5kW
- Thermal change speed per section > 50°C / sec
- Dissipation density > $50W/cm^2$



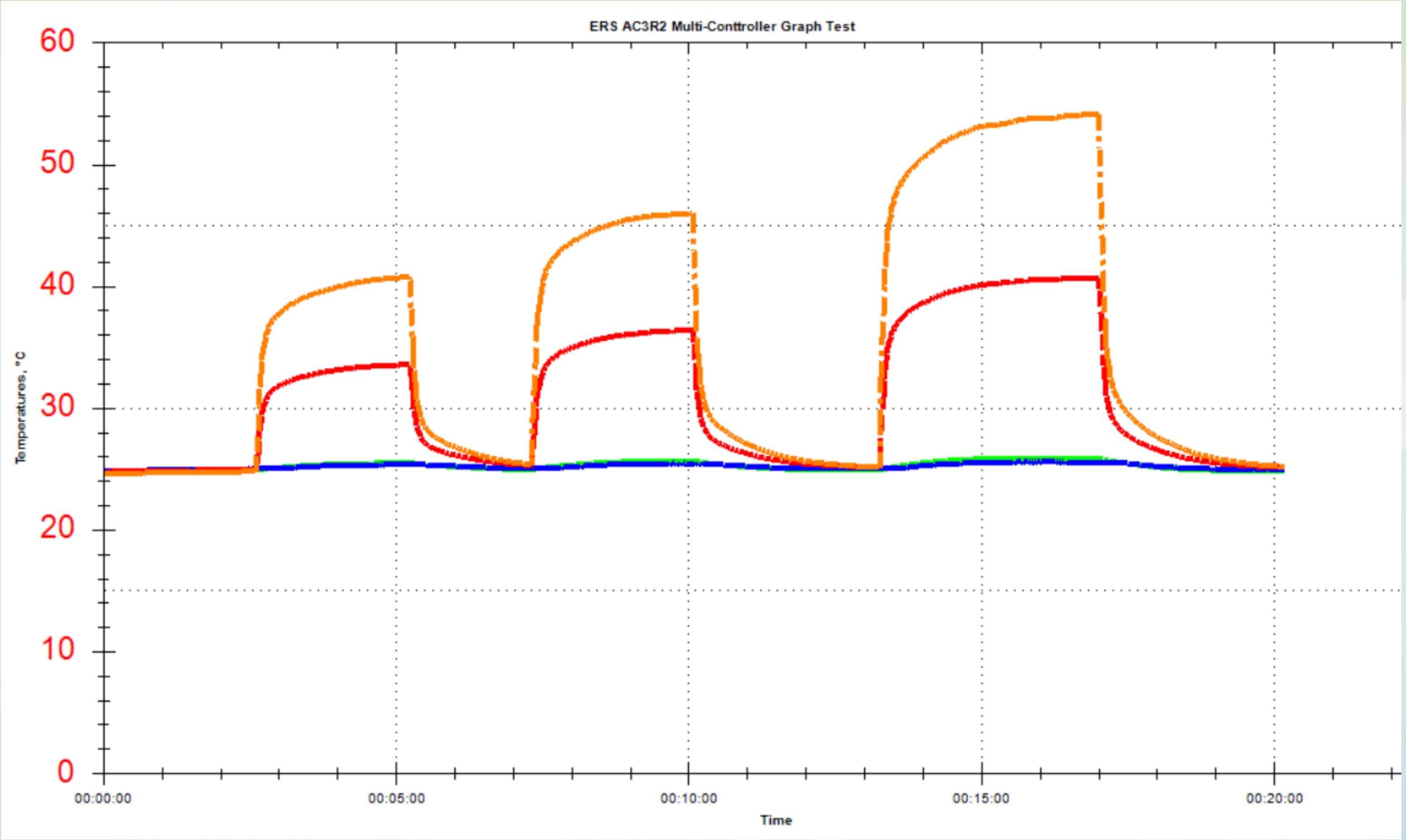
# Test Plan

- Set up a JIG representing the DUT, in our case 25mm x 35mm size
- Qualify Temperature raise with regular cold chuck
- Compare to SCL controlled chuck



# Result Cooler Only (80/100/150W)

JIG
DUT
EXT
COOLER




Set Temperature:
+25°C

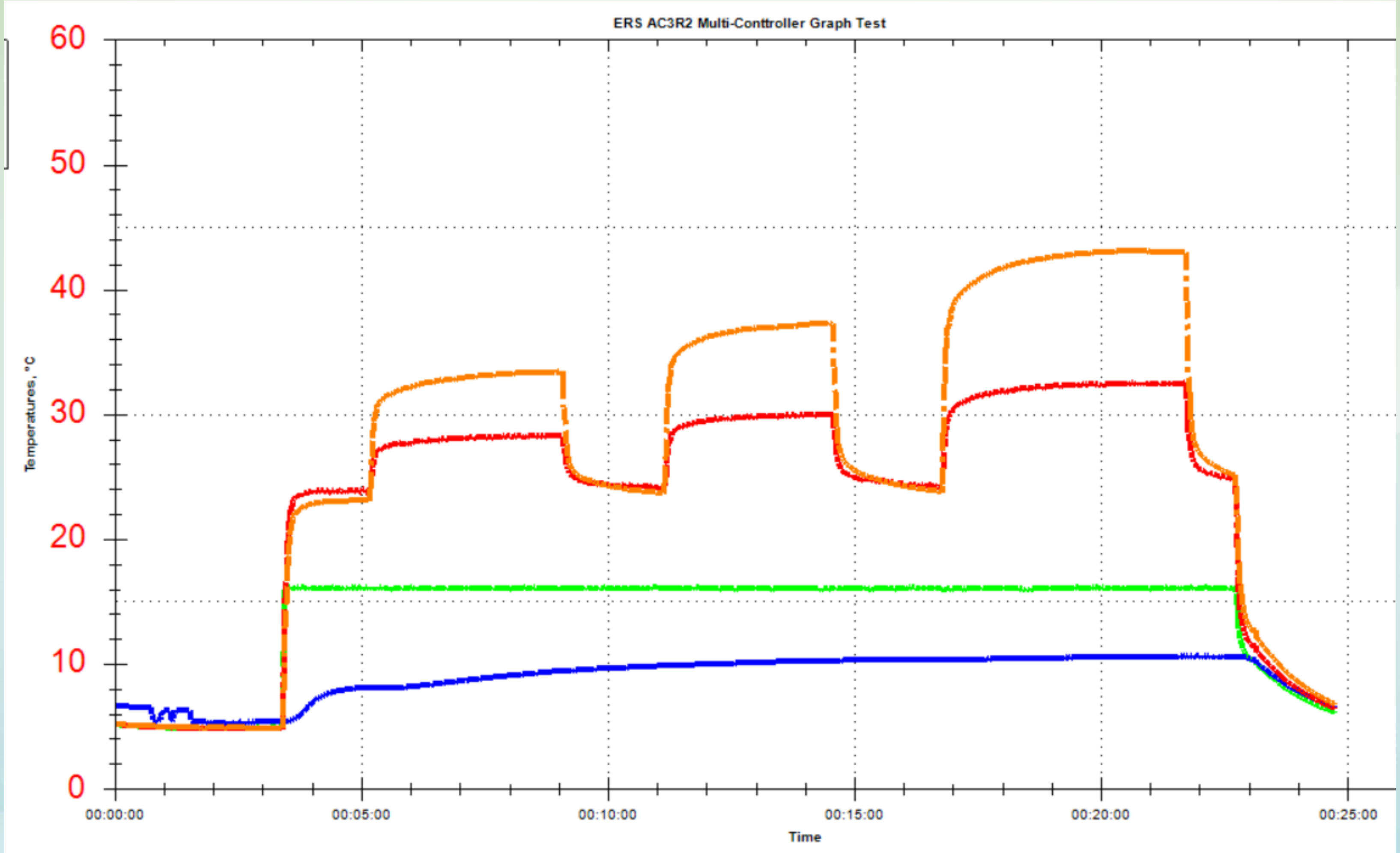
DUT
Temperature:
+33°C
+36°C
+41°C

DUT Temperature
Rise:
+ 8°C
+11°C
+16°C

**<u>"baseline"</u>**

# Result SCL static (80/100/150W)

- JIG
- DUT
- EXT
- COOLER



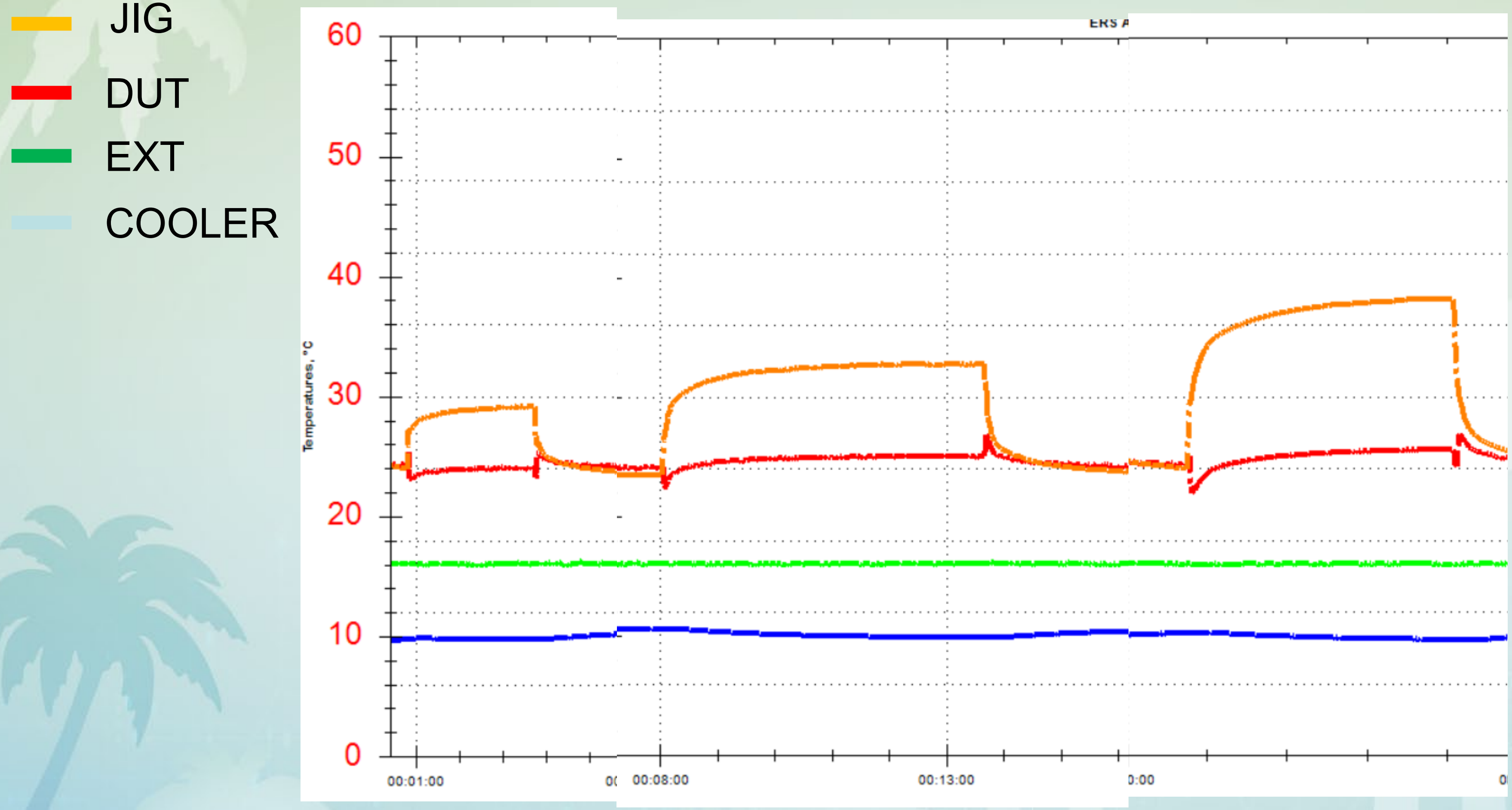

Set Temperature:
+25°C

DUT Temperature:
+28°C
+29°C
+32°C

DUT Temperature Rise:
+ 3°C
+ 4°C
+ 7°C

**<u>5°C…9°C improvement</u>**

# Result SCL dynamic (80/100/150W)




Set Temperature:
+25°C

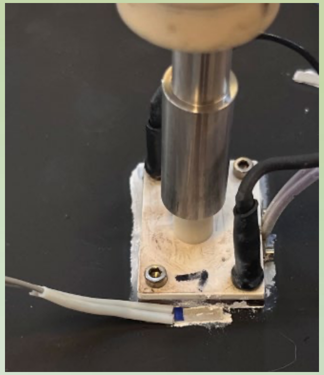
DUT Temperature:
+24°C
+25°C
+25,5°C

DUT Temperature Rise:
- 1°C
+ 0°C
+ 0,5°C

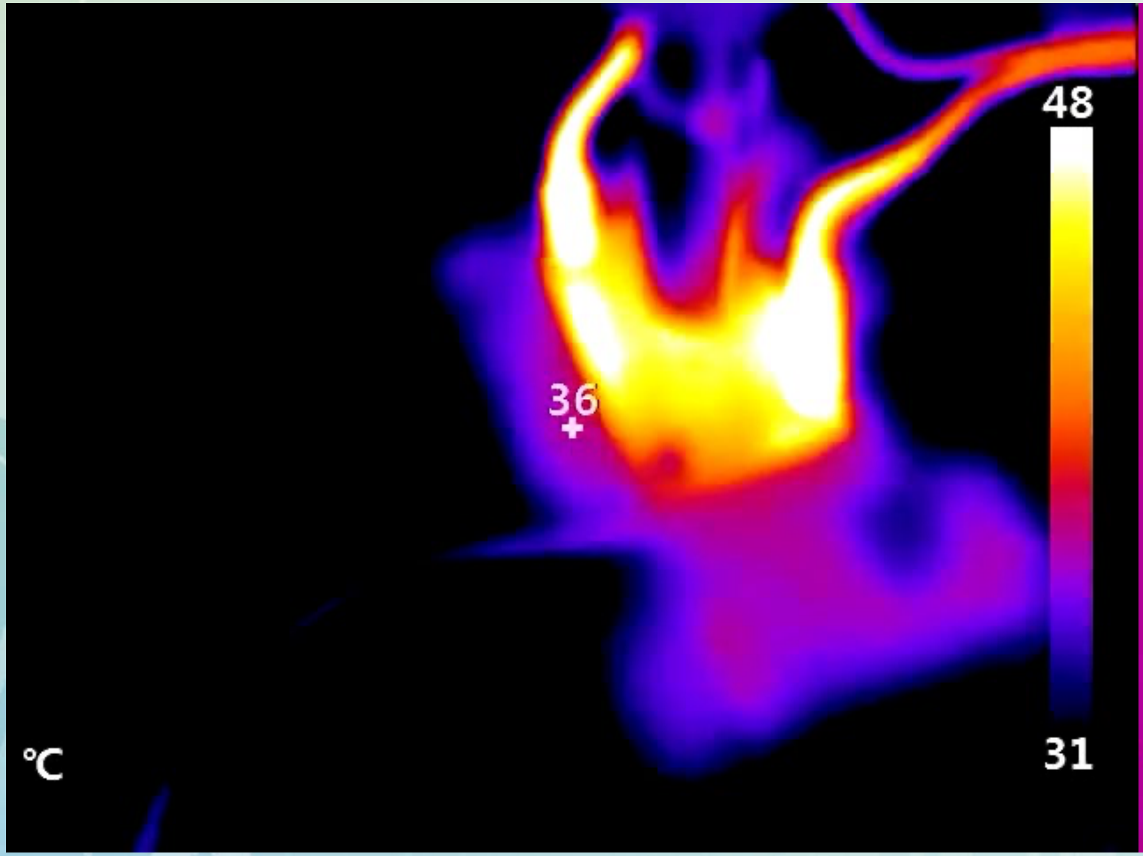
**<u>8°C…16°C improvement, DUT temperature locally constant better than +/-1°C</u>**

# Side-by-Side Comparison

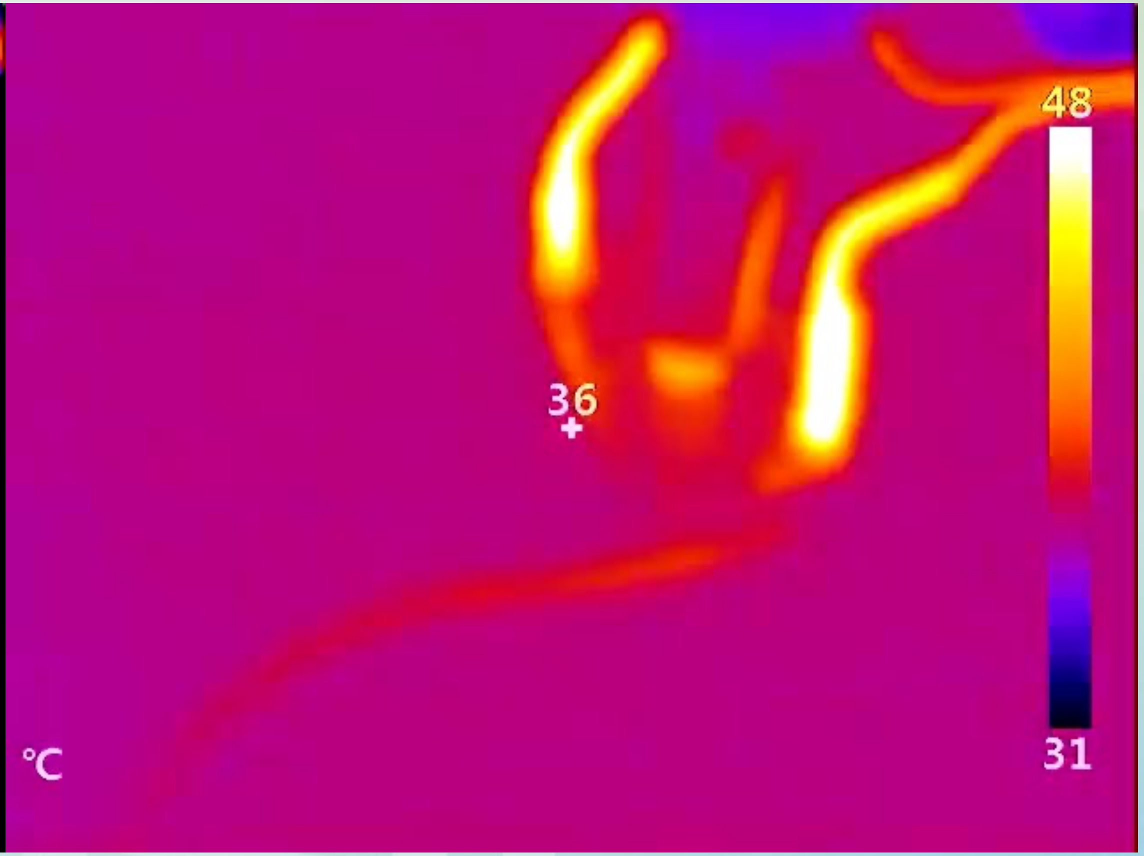
## Temperature reaction of DUT when power is applied



### With SCL

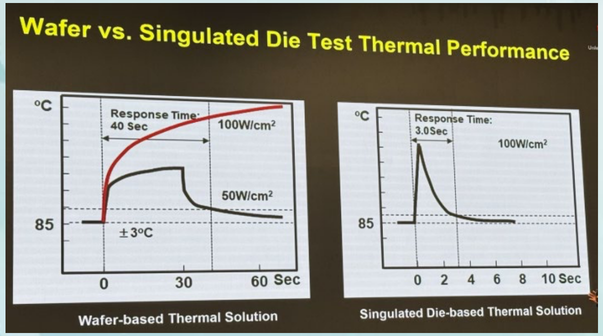



### Without SCL



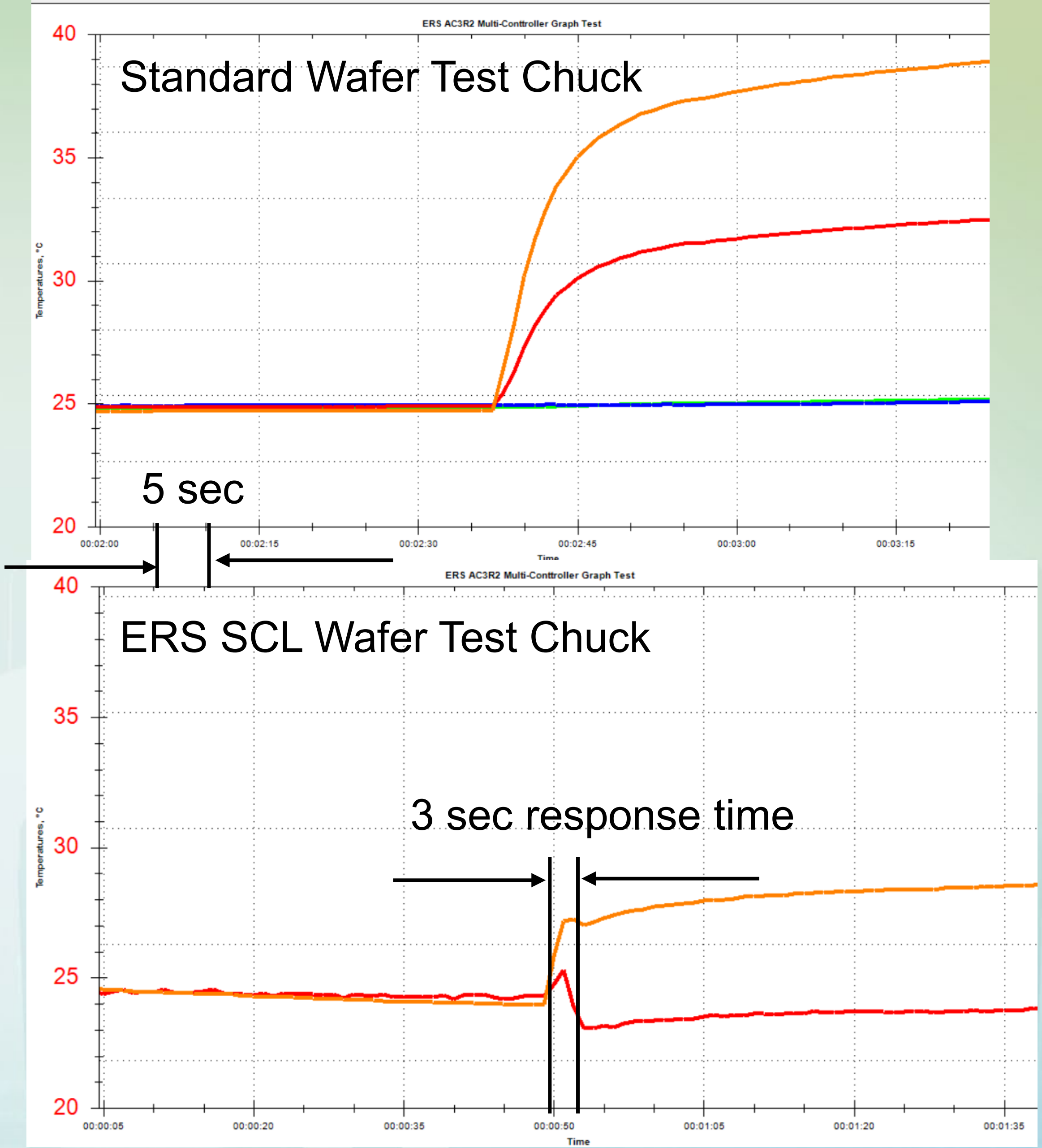
# Conclusion

- Section Layer Control enables local fast thermal response to the DUT temperature
- Same performance as singulated die test
- Key is extra fast lowering of the temperature of the backside of the DUT
- This is a fundamental difference to all existing thermal chucks



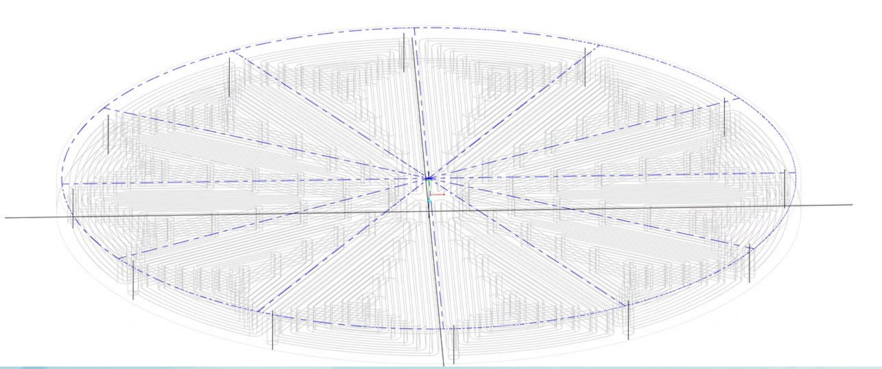

Source: TSMC I.S.E.S. Taiwan 2025

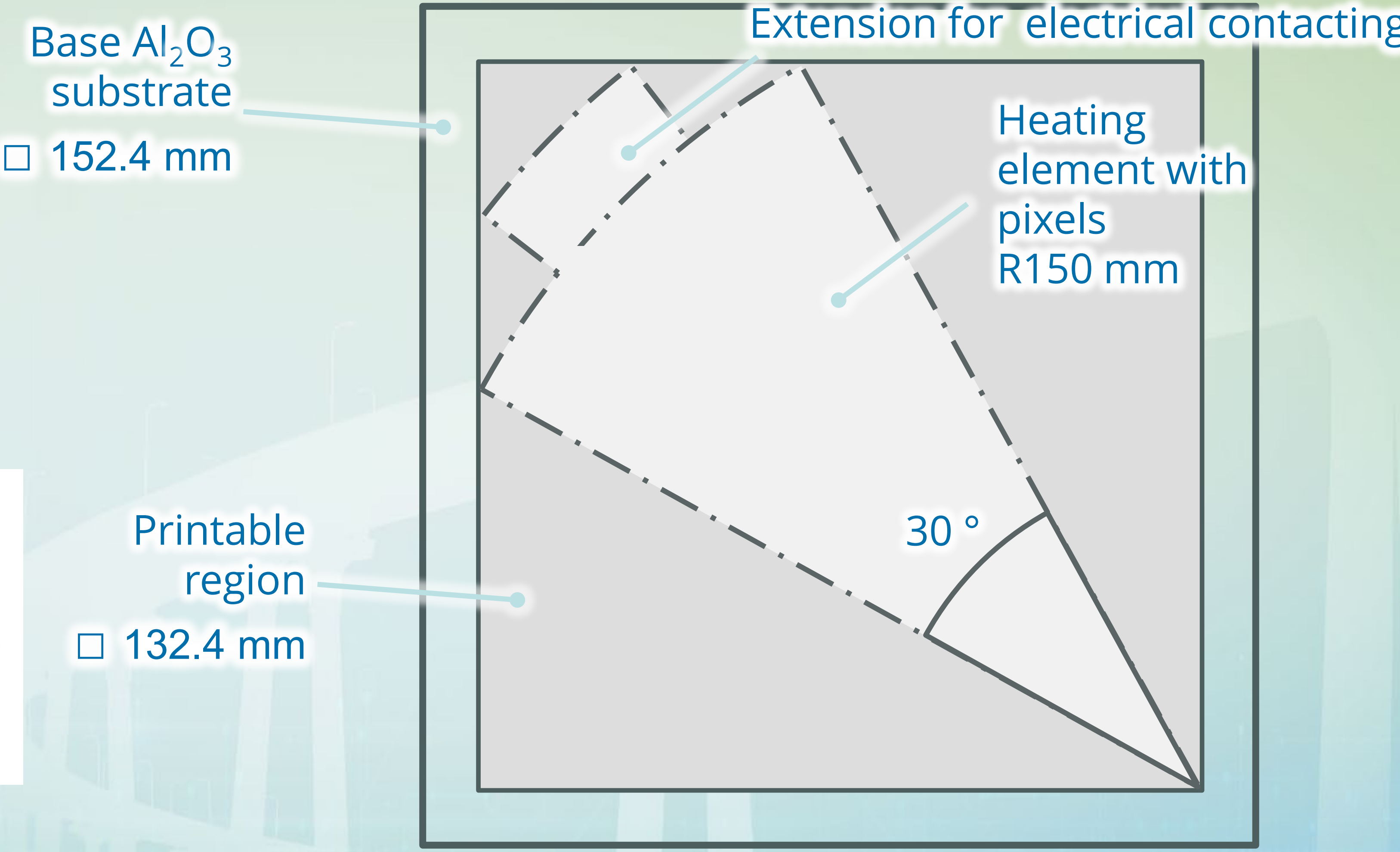
Solution



# Future Work (1/2)

- **Extension of the heating system to 300 mm**
- **Backside is fully accessible to attach a cooler**
- **Modular design**





# Future Work (2/2)

- Present Capability: 50 $W/cm^2$ dynamical control
- Next Chuck will have 120 $W/cm^2$ capability
- Making 300mm Chuck for existing automatic wafer prober
- Providing the interface box to read out DUT temperature from existing probecard
- Reduction heating pixels size --> Increase of area heating power by factor 4
- Metallization of the heating pixel surface

# Thank You!
# Any Questions?

For more information, contact kreitinger@ers-gmbh.de