SWTEST 2026 CONFERENCE

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Opto-electronic wafer-level probe card with optical fiber array and RF interface

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Developing, Delighting

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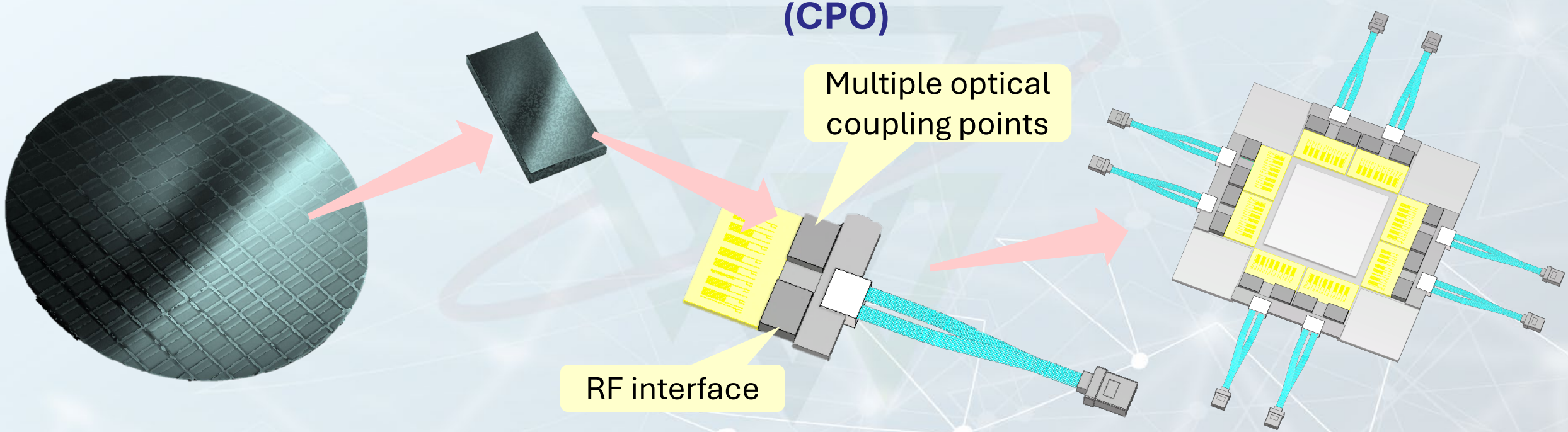
Outline

- Background
  - Test Requirements (Electrical and Optical)
- Fiber Array Alignment Challenges
  - Optical I/O-Dependent Alignment Tolerance
  - Rotational Misalignment
- DC Demonstration Using an MZ Modulator
- RF Interface Design Using Bumps and Flexible Interconnects
- Summary

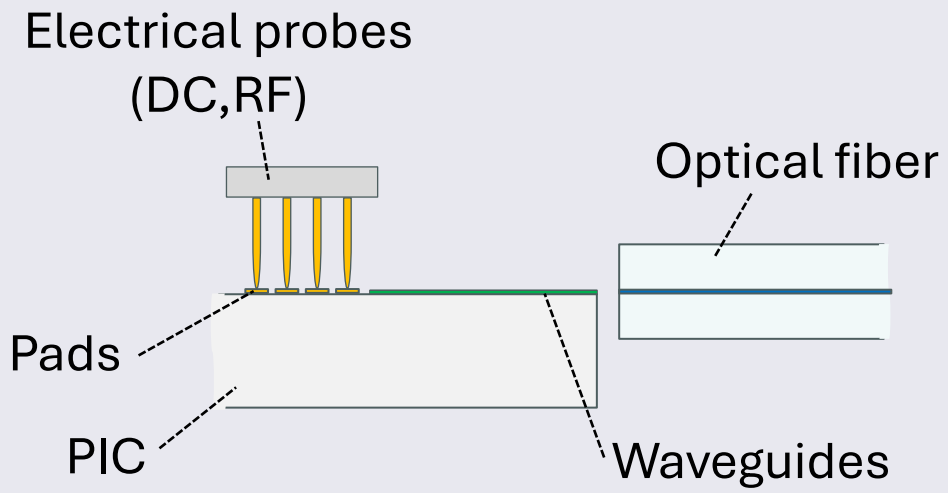
Importance of Wafer-Level Testing



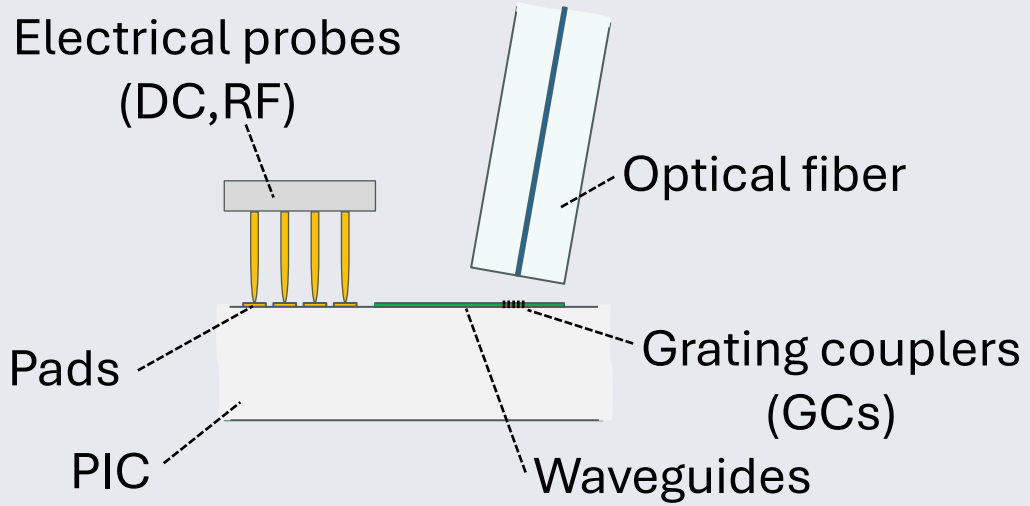
- To improve yield and reduce manufacturing cost in HPC modules, Known Good Die (KGD) must be selected at the early wafer-level test stage.
- Wafer-level testing must support both multiple optical I/O and RF interfaces.

Opto-Electronic Probing for PIC

Edge coupling



Surface coupling

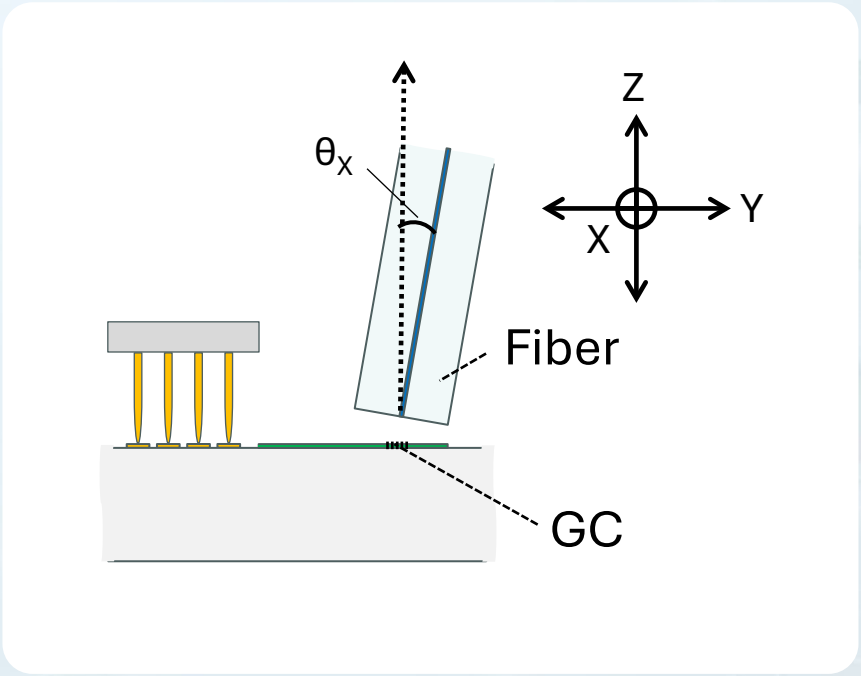


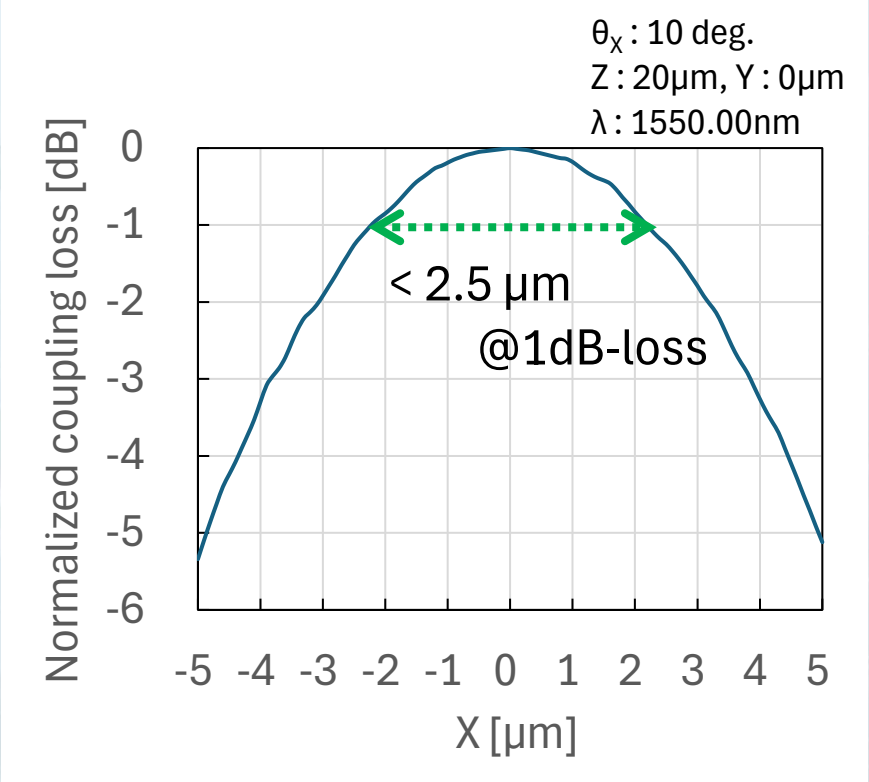
- Wafer-level testing must simultaneously satisfy both electrical contact and optical coupling requirements.
- In this presentation, we discuss opto-electrical probing based on surface coupling.

Probing Requirements

	Electrical contact		Optical coupling
	DC	RF	
Ideal	Zero contact resistance	Impedance matching	Zero excess coupling loss
		Multiple contact +	Multiple coupling
Realistic goal	To simultaneously achieve near-ideal electrical and optical performance while supporting multiple electrical contacts and optical couplings.		

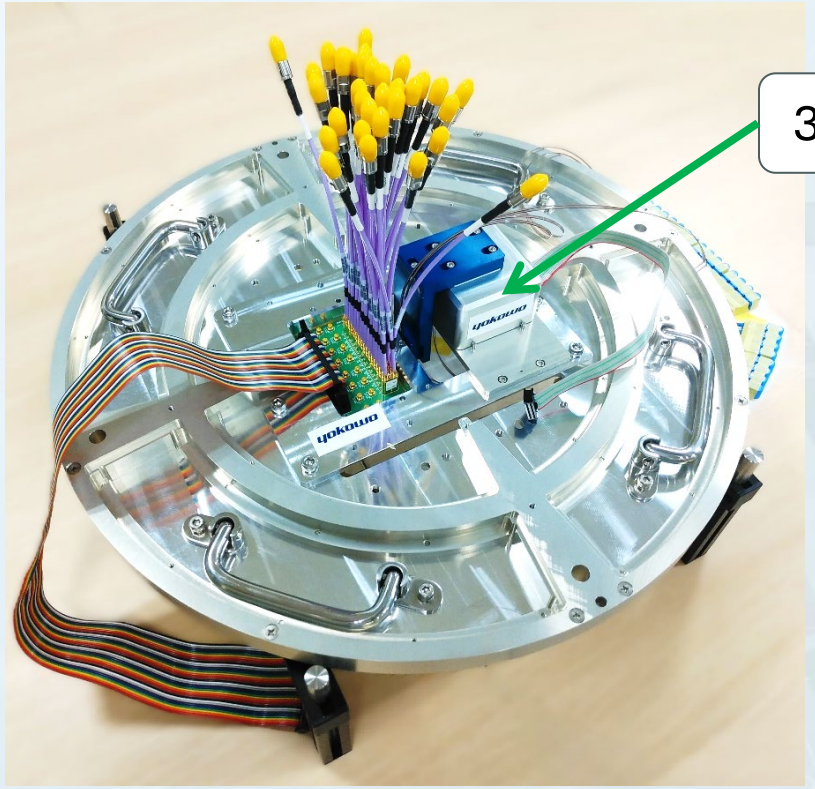
Alignment Accuracy Requirements

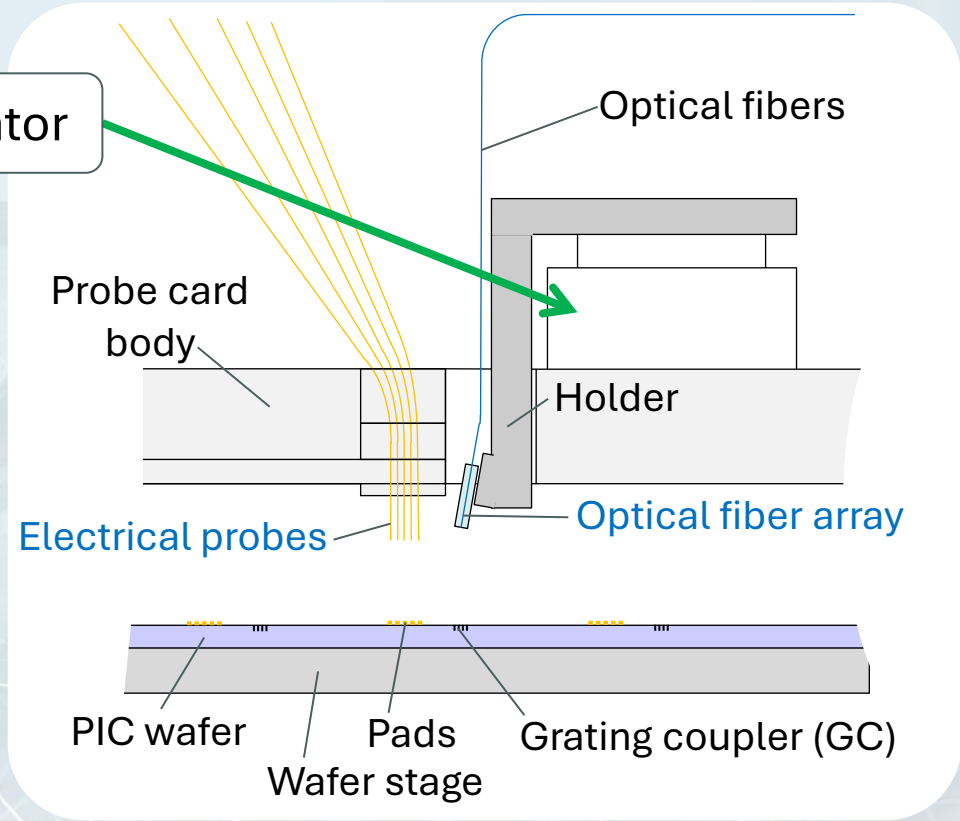




- Optical coupling requires sub-micron-level alignment, which is significantly tighter than electrical requirements.

Probe Card with a Micro-Actuator





- Electrical contact leverages the accuracy of a conventional prober.
- Final optical alignment is achieved using a 3-axis micro-actuator to enable sub-micron alignment.
- The electrical probe tip is positioned to extend beyond the optical fiber tip to account for probe overdrive.

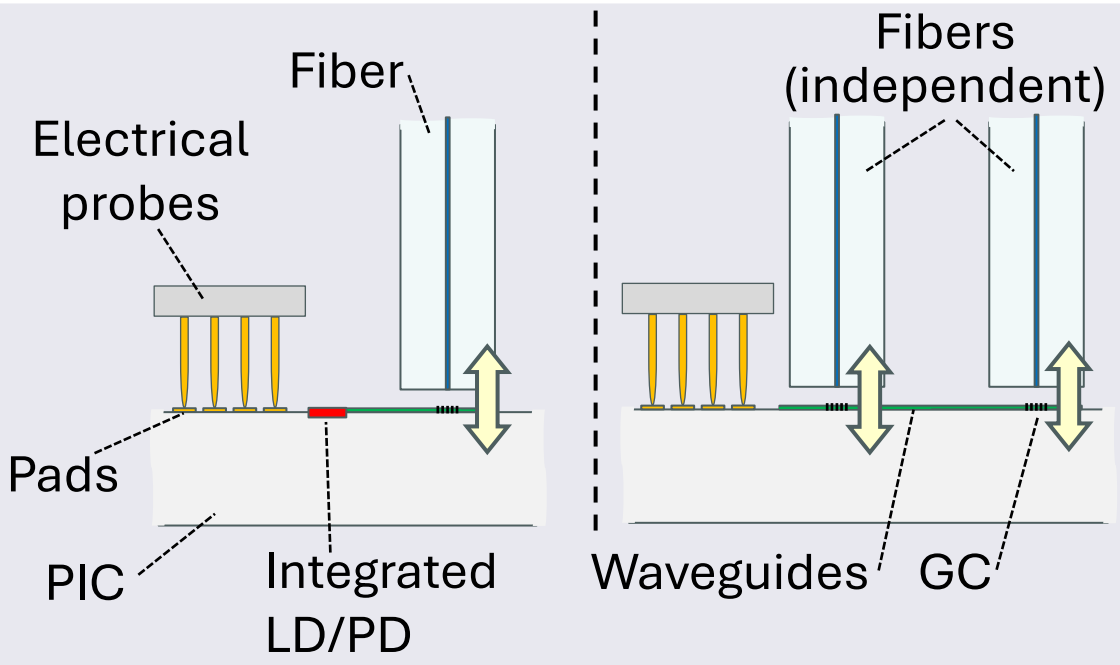
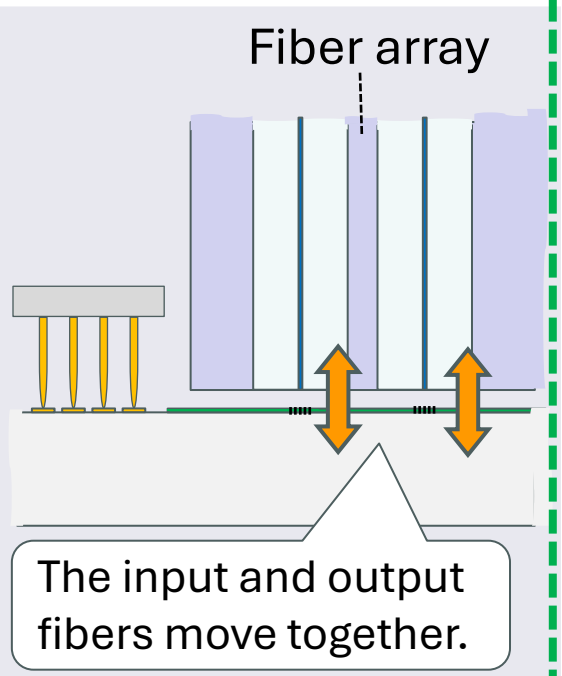
I/O Types

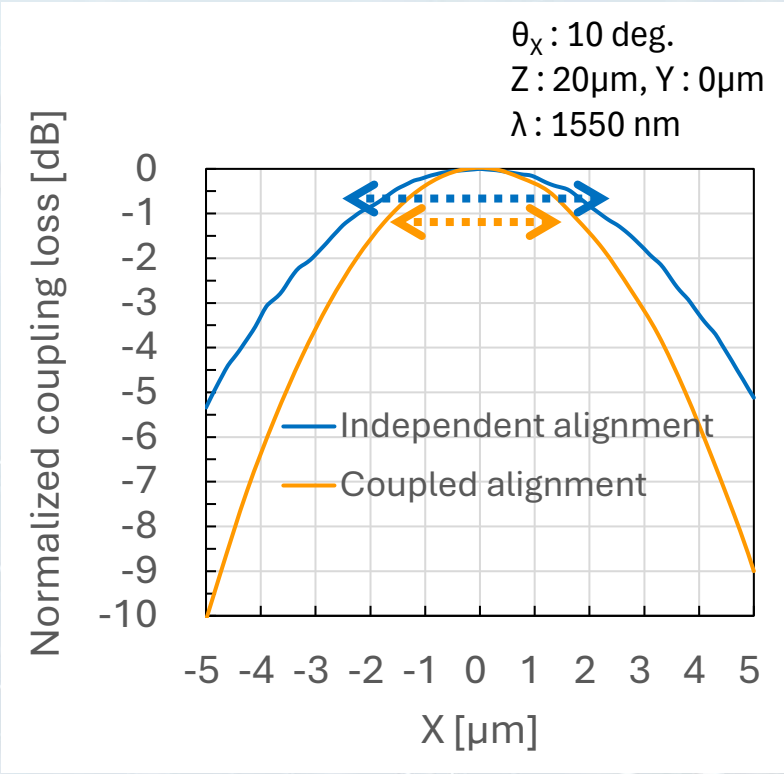
I/O type	Circuit example	Number of optical coupling ports per circuit
E → E	Basic (DC-bias, RF-signal)	-
Items added to PIC inspection		
E → O	Light source (LD)	1 port (optical output)
O → E	Photo detector (PD)	1 port (optical input)
O → O	Passive component (Splitter/Coupler, AWG, etc.)	2 ports (each side of the optical input/output)
O → O ↑ E	Active component (Optical switch, Modulator (MZI,RR), SOA, etc.)	2 ports (each side of the optical input/output)

- This presentation introduces a DC evaluation example using an MZ modulator.

LD : Laser diode
PD : Photo diode
AWG : Arrayed-waveguide grating
MZI : Mach–Zehnder interferometer
RR : Ring resonator
SOA : Semiconductor optical amplifier

Independent vs. Coupled Optical Alignment

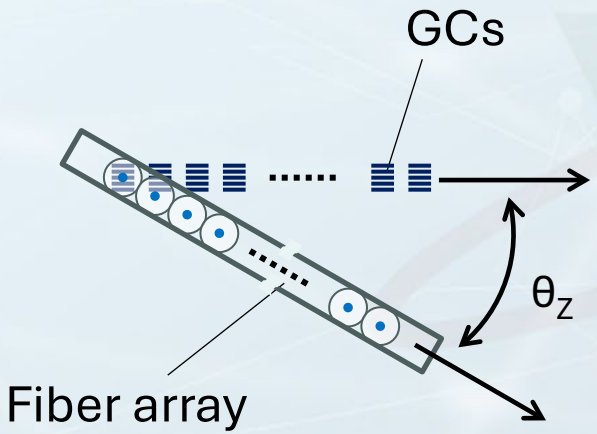
Independent optical alignment	Coupled optical alignment
	
1dB-Loss tolerance	< ± 2.5 μm	< ± 1.5μm

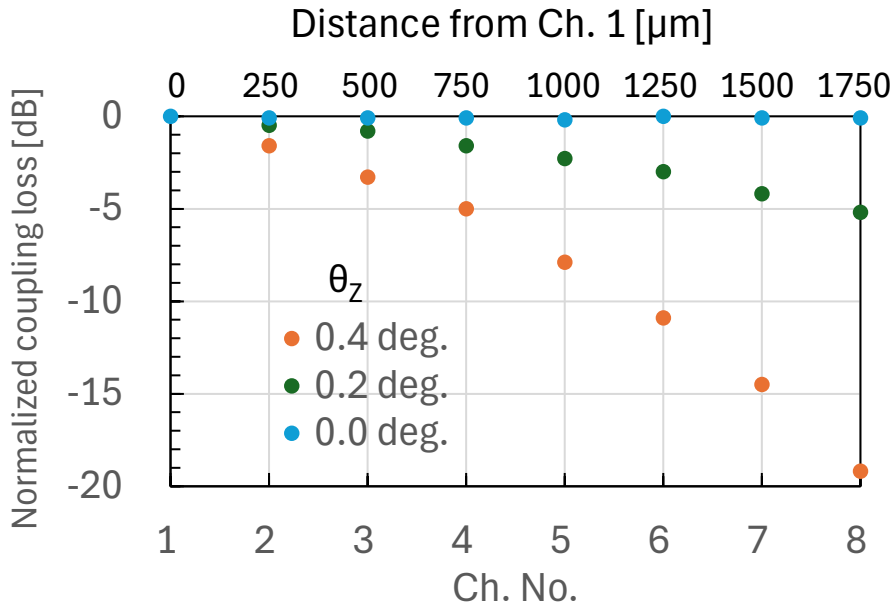


- Coupled optical alignment requires tighter alignment tolerance because input and output are constrained by the fiber array.

In-plane Rotational Misalignment

- When using a fiber array, the input and output ports cannot be aligned independently, which leads to coupling loss caused by in-plane rotational misalignment.





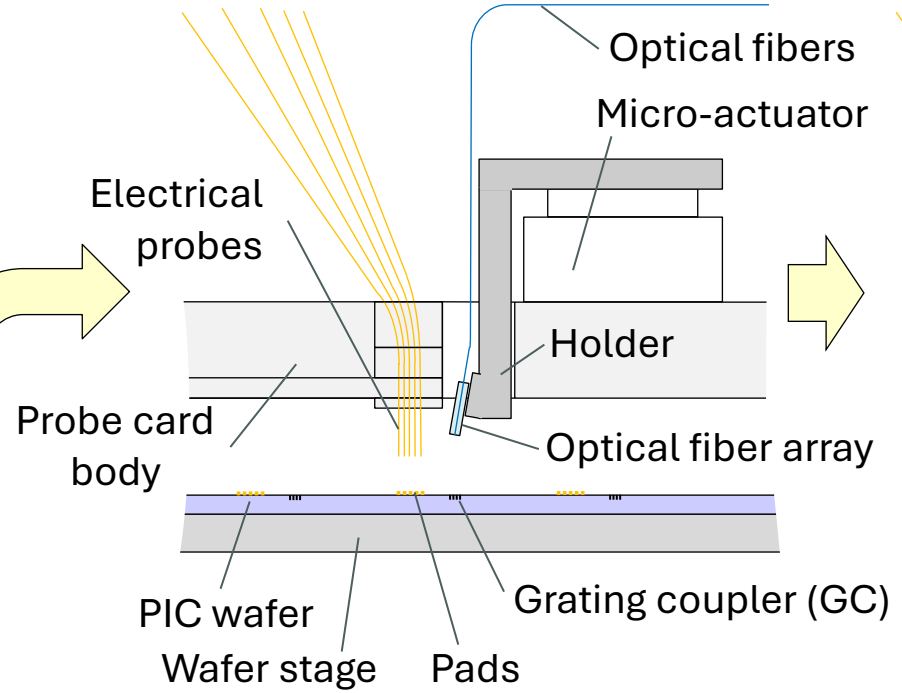
- Fortunately, global wafer rotation can be corrected immediately after wafer loading using the inherent functionality of a prober.

Probe Card Operation

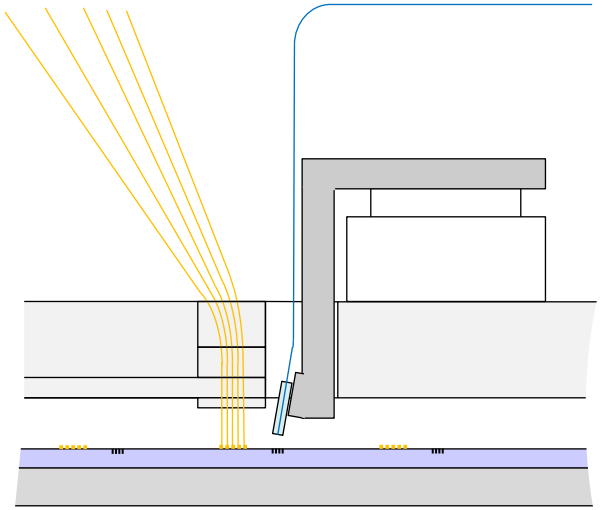
Wafer loading
and Calibration (Rotation, Height, etc.)

Wafer unloading

Initial state

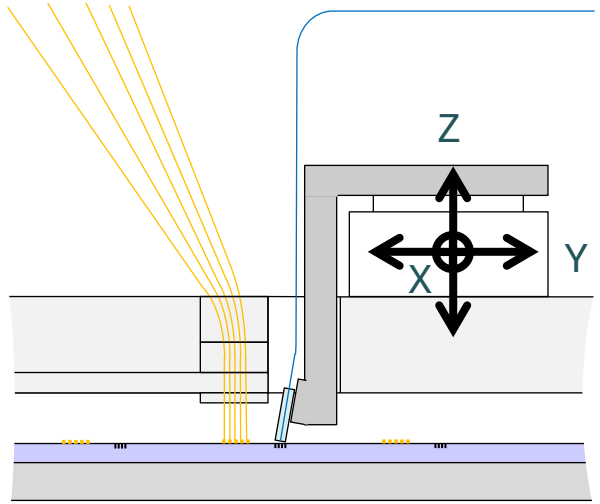


Electrical contact



Wafer lift-up
and
Electrical probe contact

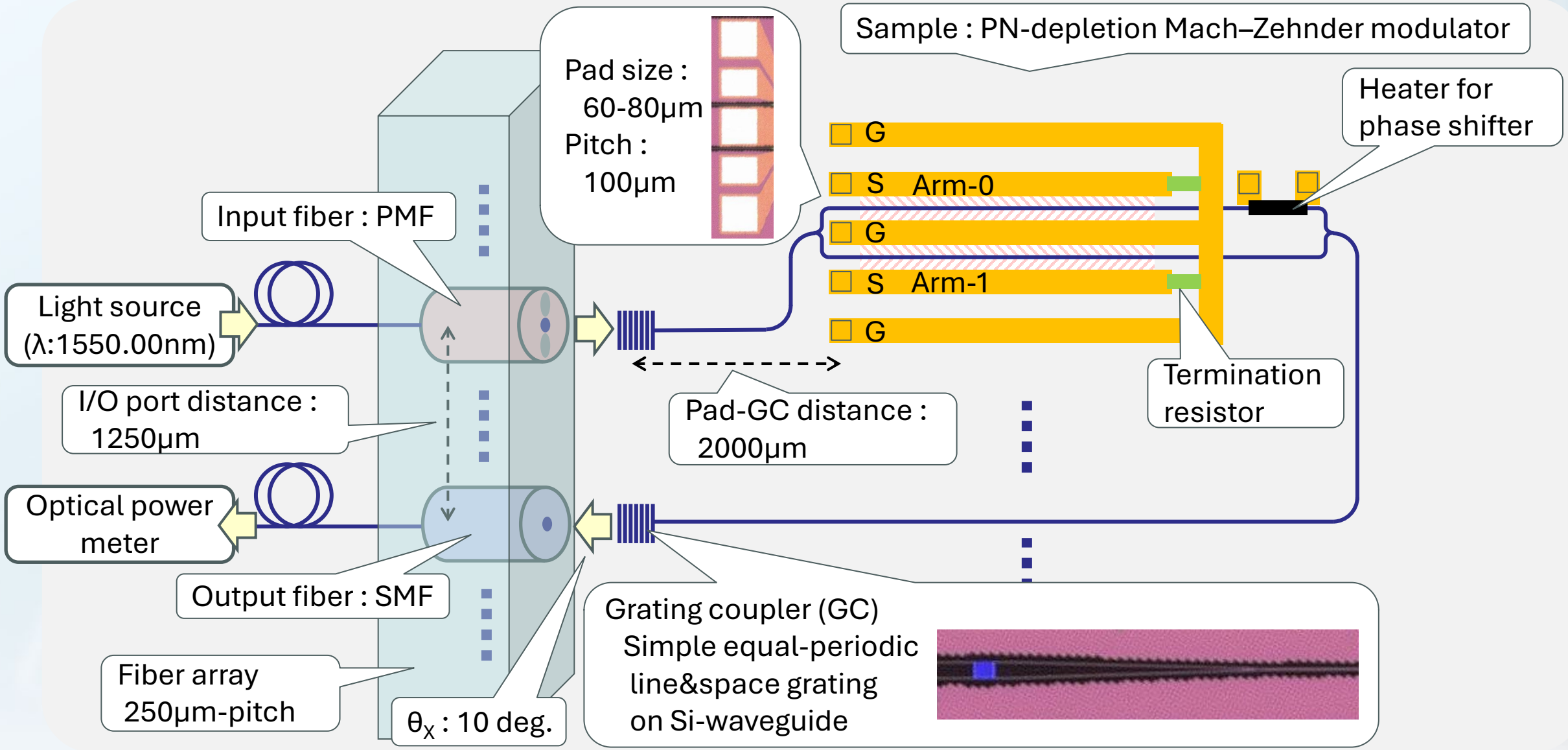
Optical alignment



Fine optical alignment by micro-actuator
and
Chip testing

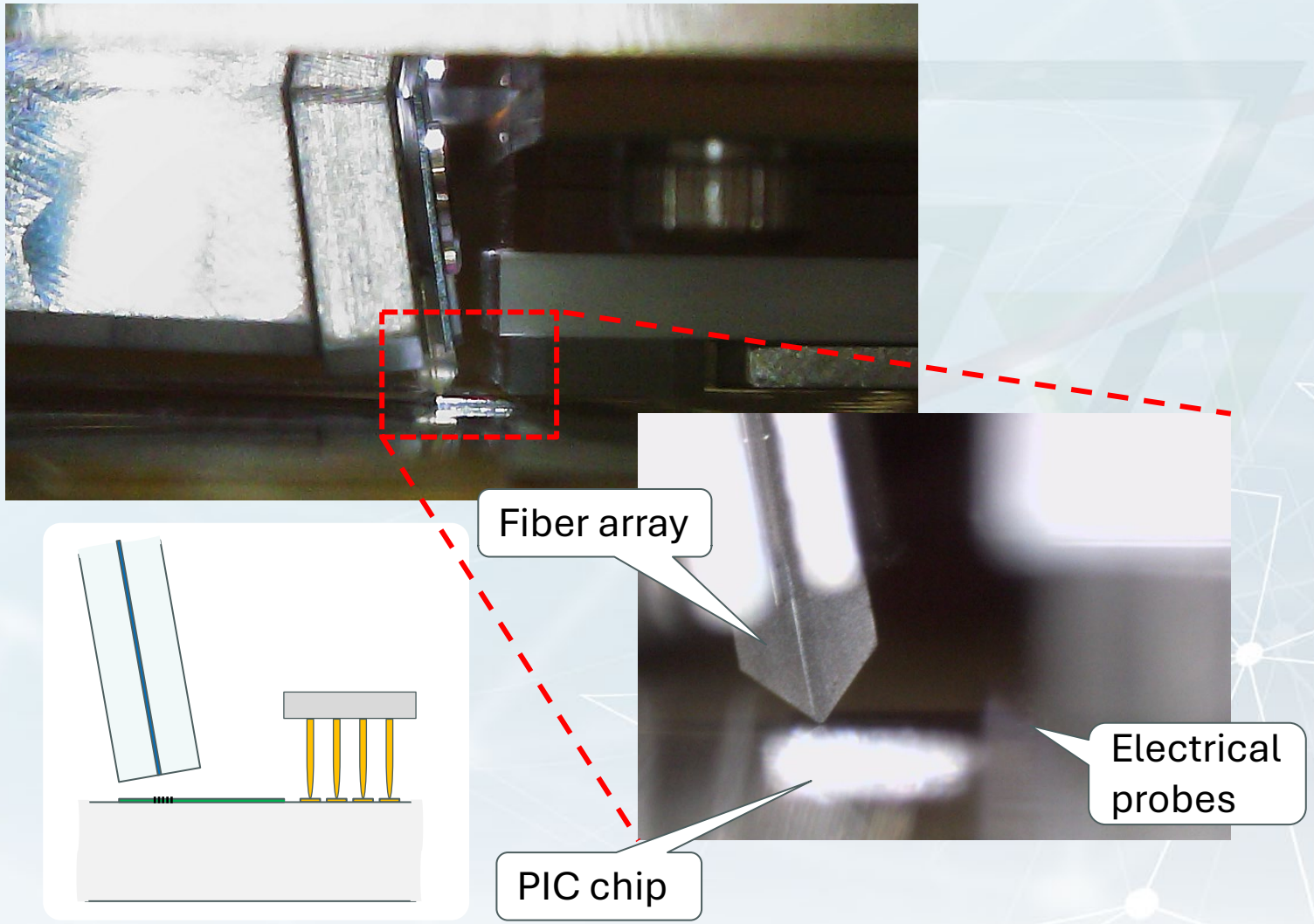
Chip-by-chip testing (Repeated)

Evaluation System

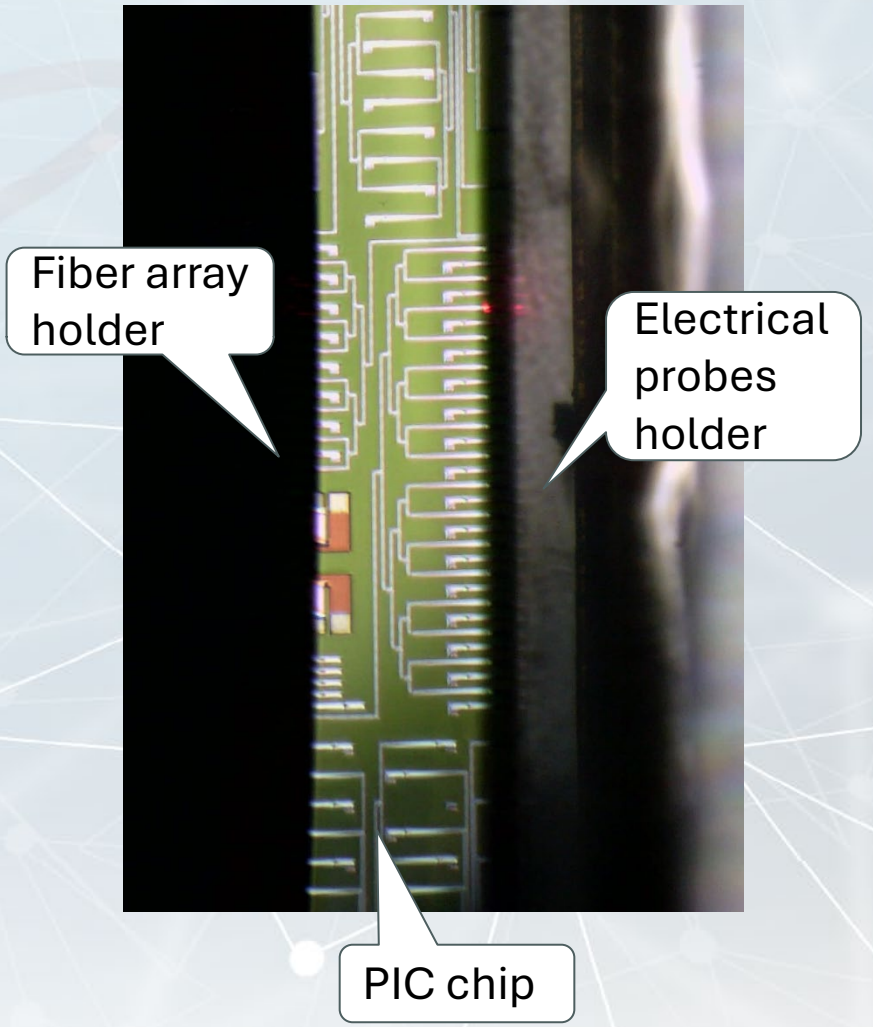


Measurement Setup Images

View from side

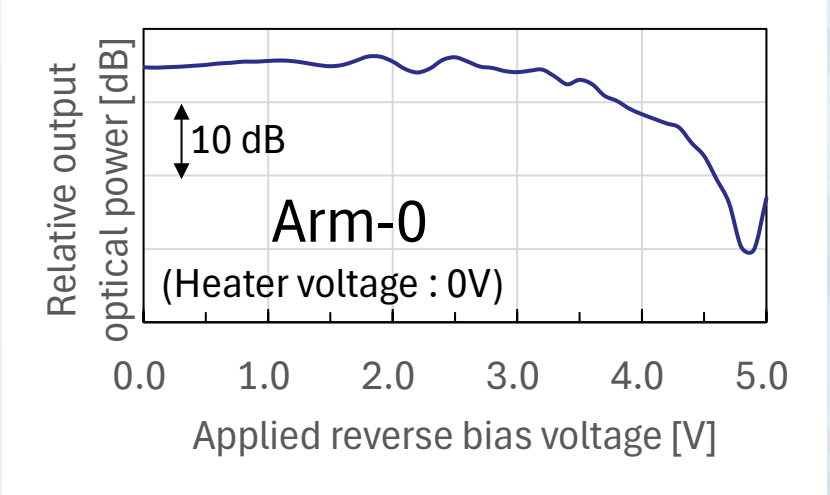


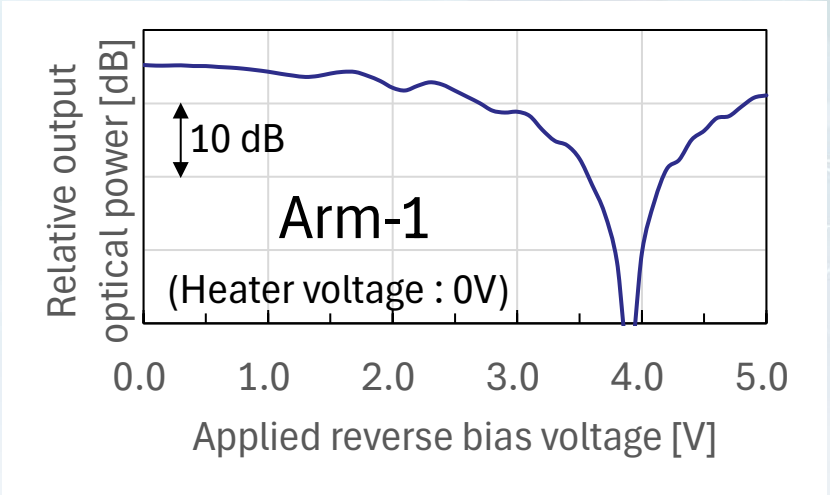
View from above

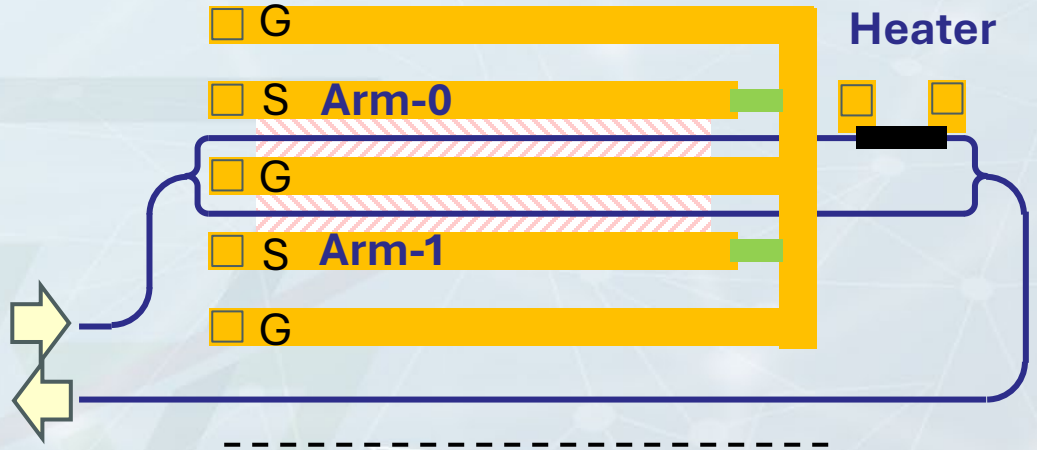


DC Extinction Measurement Results

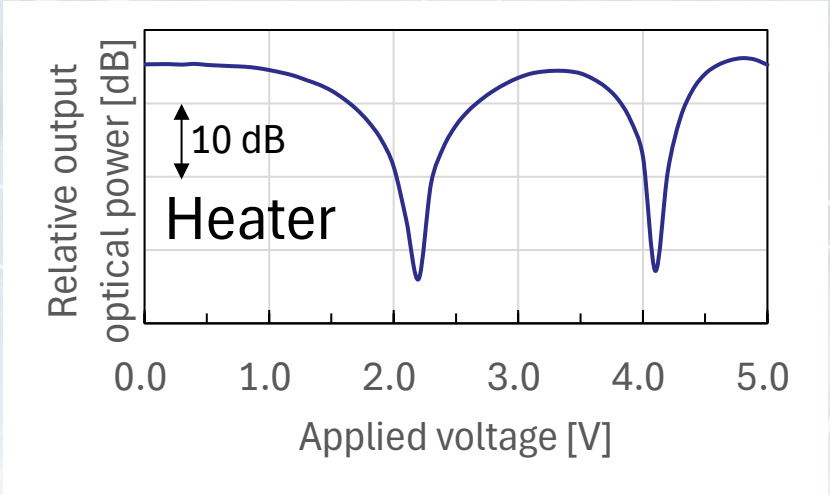
By carrier plasma dispersion effect





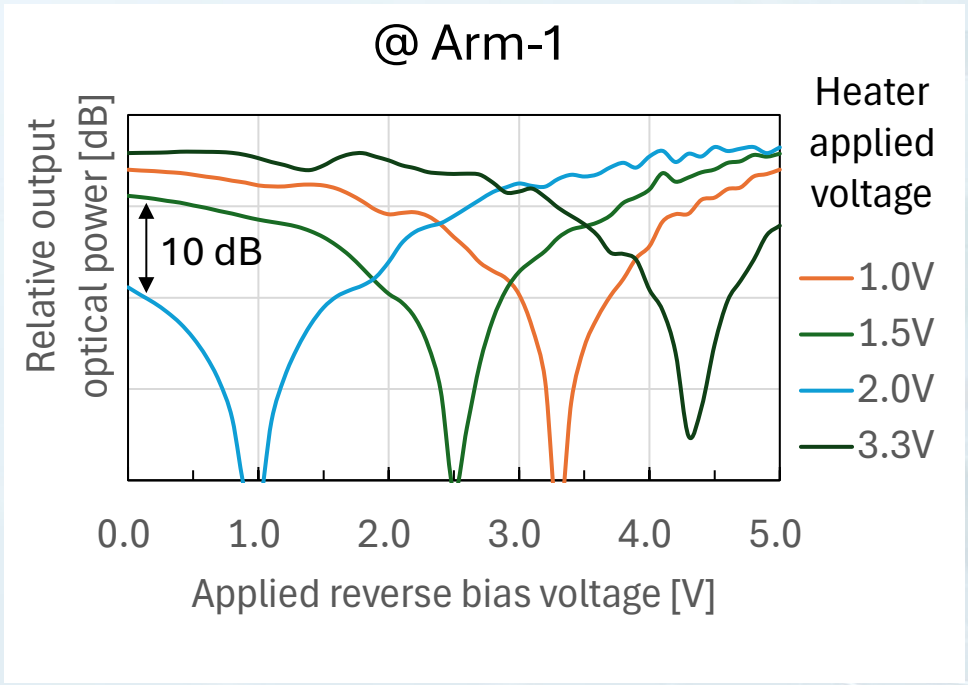


By thermo-optic effect

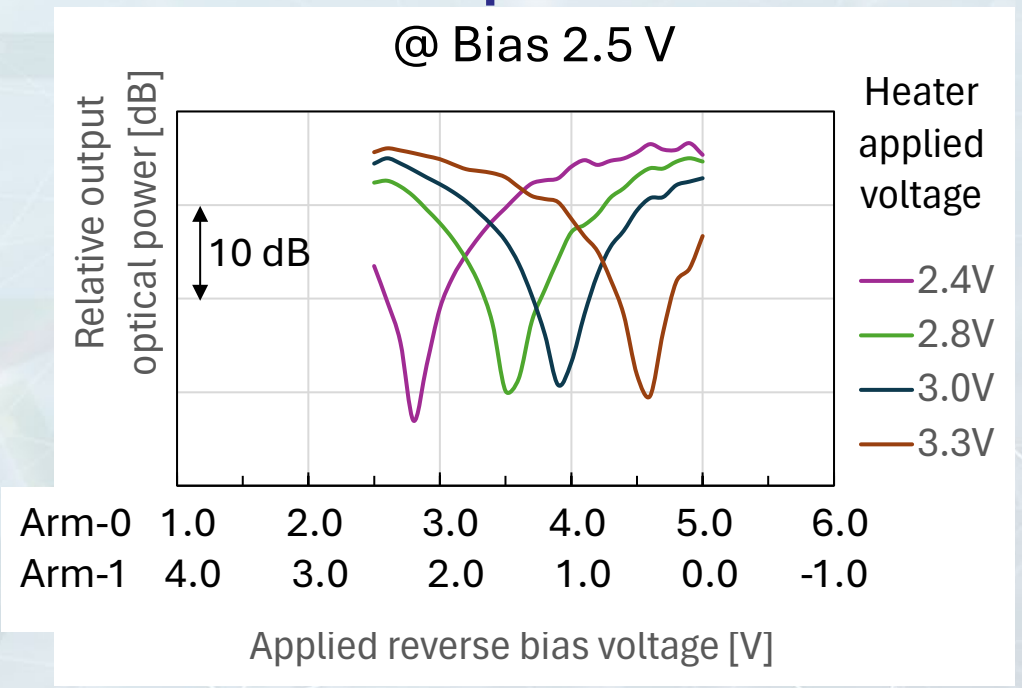


DC Bias Condition Search

Single-arm drive



Push-pull drive



- We confirmed that our probe card supports multi-channel optical I/O and enables the measurement of opto-electrical interaction at the DC level.

Need for RF Testing Beyond DC-Level Validation

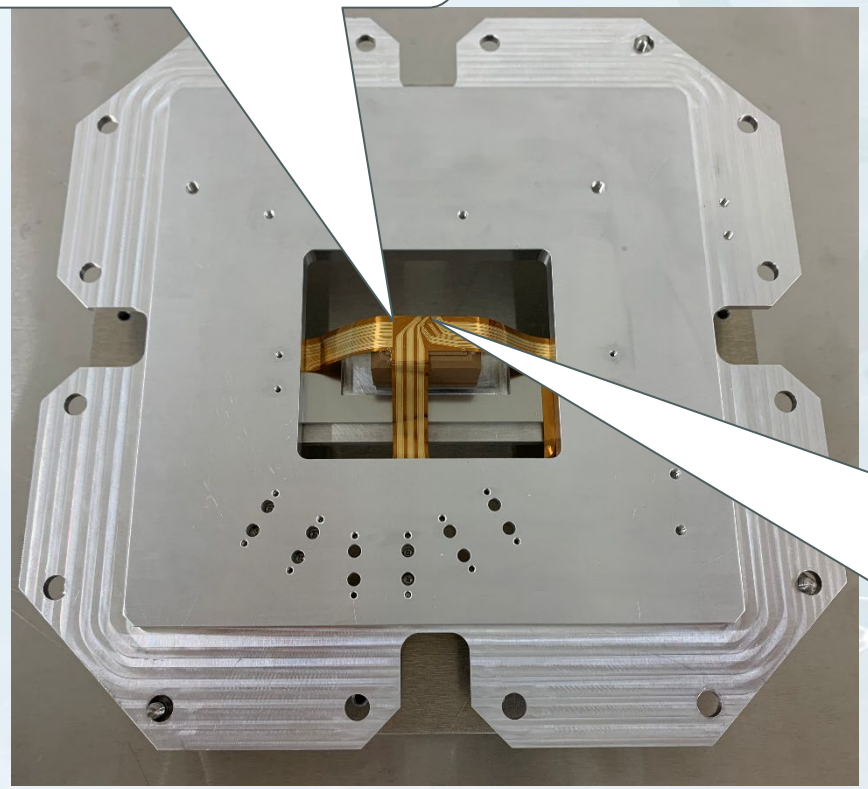
- DC-level testing alone is insufficient to ensure high-speed signal integrity (e.g., PAM4).
- Accurate KGD screening at the wafer level requires RF characterization.

DC Characterization	RF Characterization
• Continuity • Resistance	• Insertion/Return Loss • Impedance • Phase / Group Delay

- Therefore, we investigated RF test capability in our probe card.

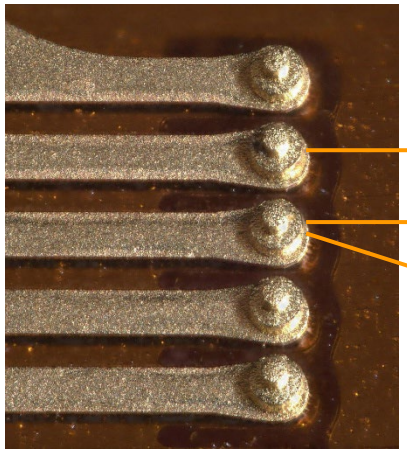
RF Interconnect Structure Using Bumps and FPC

Flexible Printed Circuit (FPC)



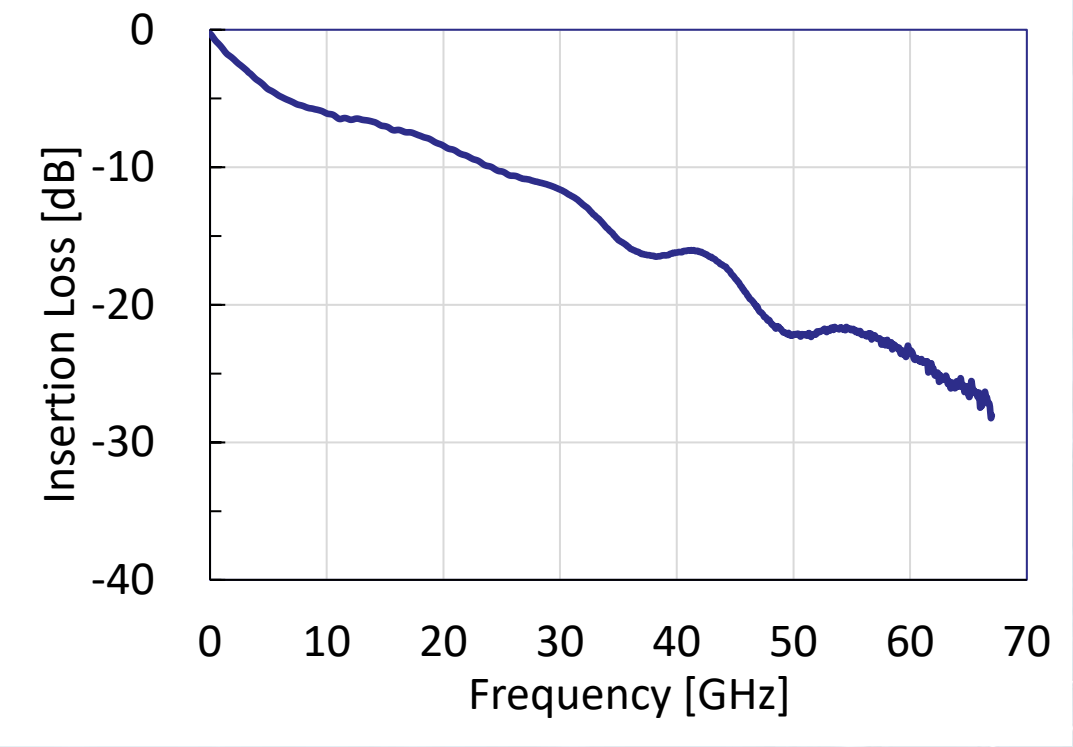
Features

- Fine-pitch RF routing
- Reduced reflections/resonances
- Low parasitic inductance by low-profile bumps
- Flexible structure for stable contact

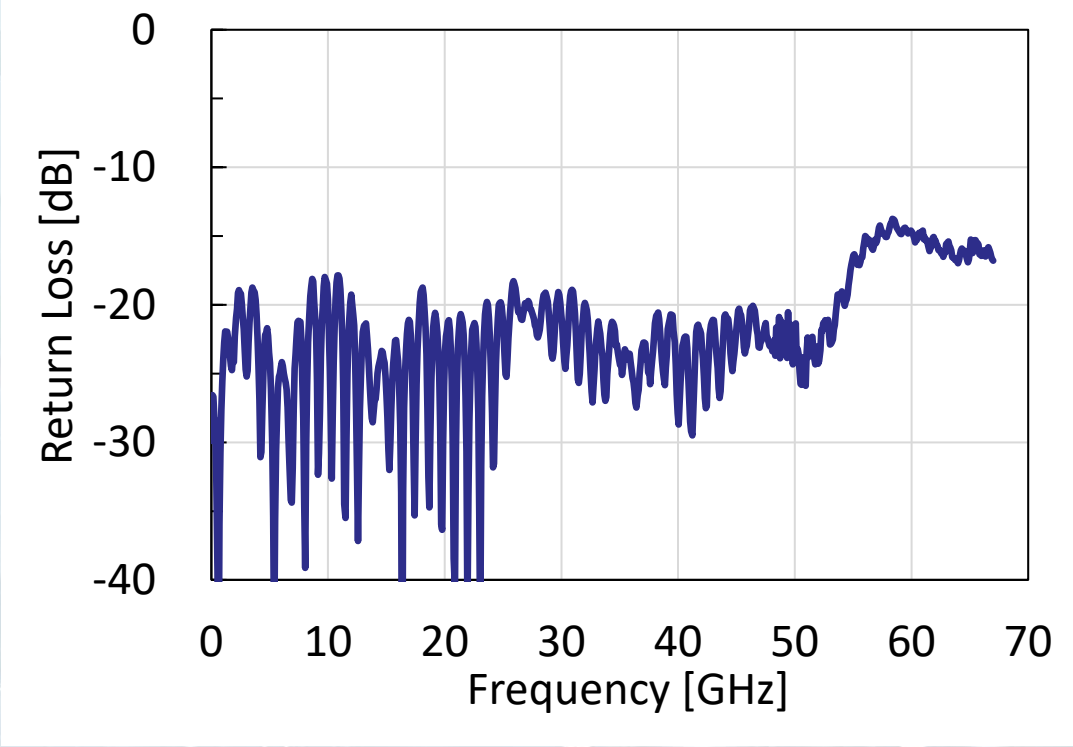


RF Measurement Results

Insertion Loss



Return Loss



- Insertion and return loss were successfully measured up to 67 GHz without major issues
- Further optimization is underway, including layout and interface improvements

Summary

In a probe card configuration integrating a fiber array with a micro-actuator,

- Fiber array alignment challenges (I/O-dependent tolerance and rotational misalignment) were investigated and characterized.
- DC-level opto-electrical interaction was demonstrated using an MZ modulator.
- RF interface using bumps and FPC interconnects was investigated.

Outlook

- Demonstration of RF testing capability
- Development and demonstration of integration with standard prober and tester
- Extension to edge-coupling interfaces