SWTEST 2026 CONFERENCE

35th ANNIVERSARY

Micro-bump Probing For Advanced System-on-Chip Testing: A Preview Into Native-Pitch Solutions And Their Challenges

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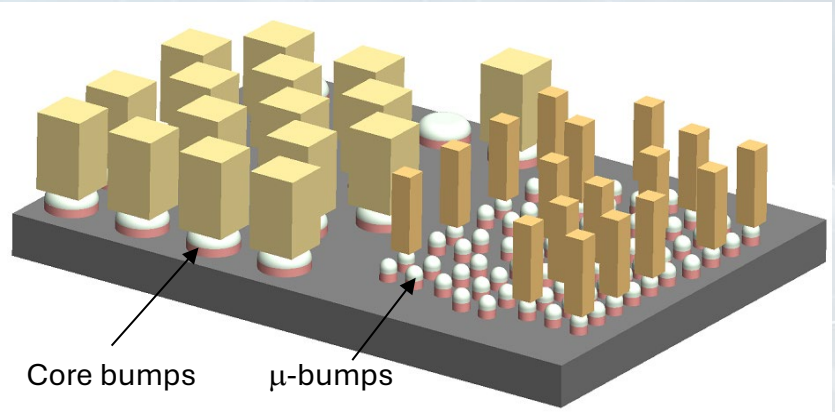
Introduction: Core + μ-bump Mixed Probing

- Compute die in advanced multi-chip packages have both
  - Large (~ 75.0 μm CD) core bumps
  - Small (< 30.0 μm CD) μ-bumps
    - ➢ that connect to adjacent die through the EMIB or EMIB-T die embedded in the substrate.

Intel EMIB 2.5D

- High die count package yield improvement need
  - Drives shift-left strategy for test
  - Need for probing on both core and μ-bumps
    - ➢ Even at **native pitches** (< 50.0 μm) in the μ-bump areas.



Schematic of a die under test (DUT) with mixed probes

Conventional Vs. Native Pitch Mixed Probing At Intel

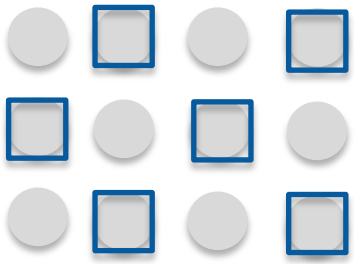
- Intel's Foveros-S assembly technology-based products such as MeteorLake are being probed with mixed (two types) probes, albeit at non-native pitches (**> 90.0 µm**) → **H68 / F36 Tech**
  - One probe type for power and ground bumps
  - One probe type for signal bumps

- A new solution where the µ-bumps are probed at **45.0 µm** native pitch → **K Tech**
  - **Enabled by Technoprobe!**

- Note: Material in this presentation correspond to probing on solder bumps.

µBump Probing Configurations

Standard Probing Strategy



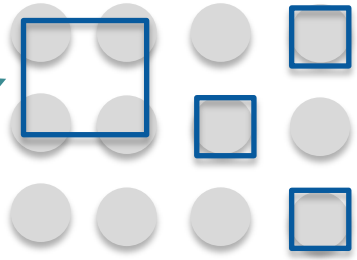
- Single needle probing for µ-bumps only array
- Non-native pitch

✓ Low force probes to avoid bump damage

✓ Very high pin count

Intel Patent # 12,163,982

µBump Cluster Probing Strategy

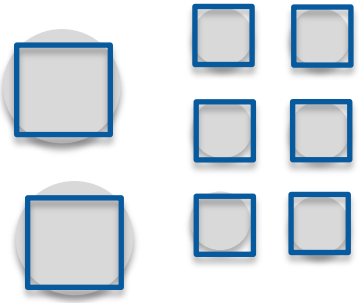


- Mixed probing for µ-bumps only array
- Non-native pitch

✓ Maximized coverage with 4 µ-bumps cluster probing

✓ **Ex: Foveros**

Native Pitch Mixed Probing Strategy



- Mixed probing for Core & µ-bumps array
- Native pitch

✓ **New capability**

➢ Native pitch µ-bump probe characteristics: **Low force | Tighter probe alignment | High Speed**

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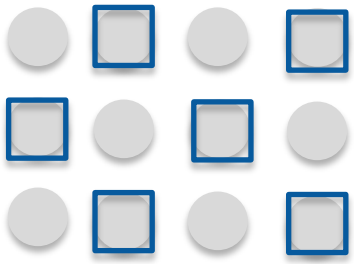

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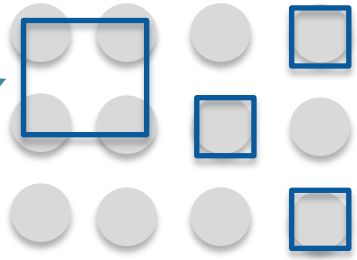

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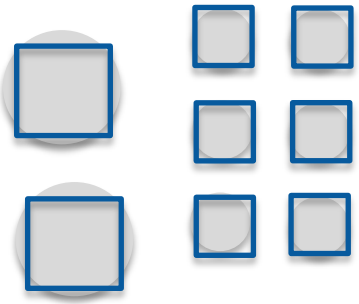

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- Native pitch

✓ **New capability**

Today's Focus!

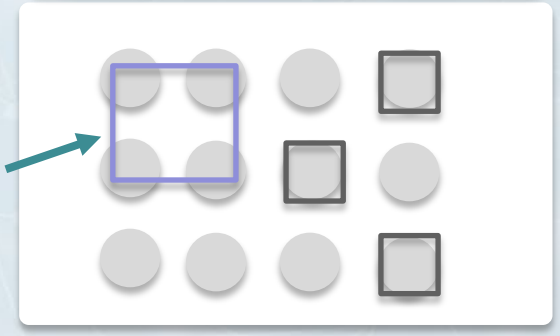
➢ Native pitch µ-bump probe characteristics: **Low force | Tighter probe alignment | High Speed**

µBump Cluster Probing Tech (Foveros)

DoW Tech: H68 (I/O probes) + AH68 (GND/PWR probes)

- Long, vertical probing needle technology
- Multiple GPs Probe Head template
- TPEG™ manufacturing (+ ARIANNA™ tech for AH68)
- LCR2™-based core material
- Zero Lateral Force configuration
- **Probe vertical spring force**
  - 1.2g (H68)
  - 3.5g (AH68)
- **Probe Current Carrying Capability (CCC)**
  - 500mA (H68)
  - 850mA (AH68)

µBump Cluster Probing Strategy



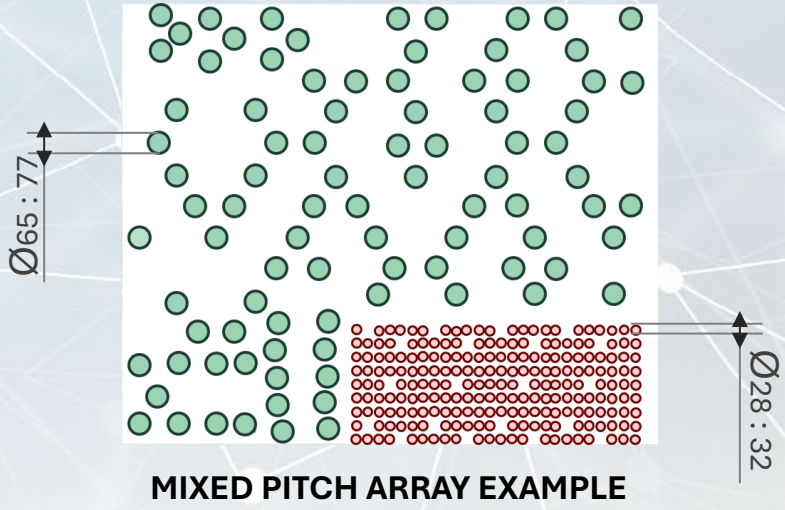
Second Generation DoW Tech:

- Improved GND/PWR probe → F36
- LCR4™-based core material
- Reduced probe force
  - **2.5g** (F36)
- Increased Probe CCC
  - **1050mA** (F36)

Native pitch µ-Probing

- **Native Pitch Probing of µ-bumps** (28µm to 32µm CD)
  - Rectangular pattern configuration
  - Min µ-bump pitch = 45µm
  - Min probing pitch = 45µm

- **Probing single core bumps** (65µm to 77µm CD)
  - Any Angle configuration
  - Min bump pitch = 100µm
  - Min probing pitch = 100µm

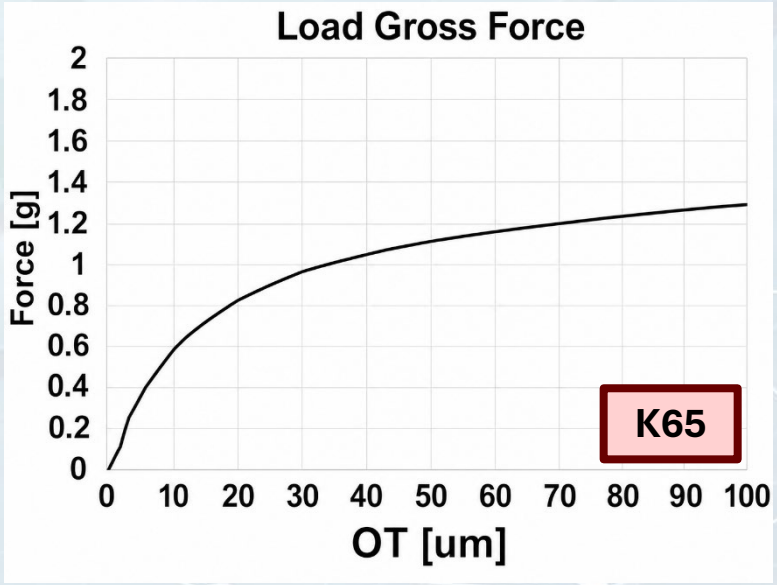


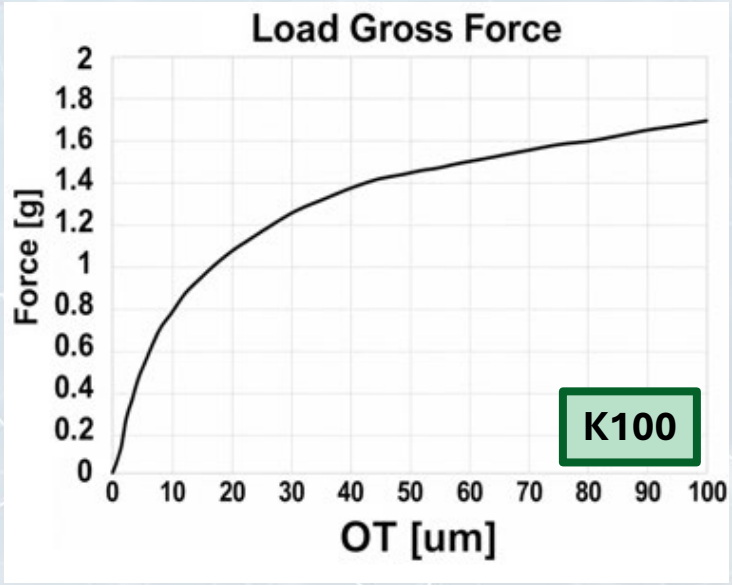
MIXED PITCH ARRAY EXAMPLE

Native pitch µ-Probing: K tech

K65 & K100 Tech

- Shorter needle length for High Speed performance improvement
- SA2™-based core material
- Zero Lateral Force configuration
- Probe vertical spring force
  - 1.2g (µ-bump **K65**)
  - 1.6g (Core bump **K100**)

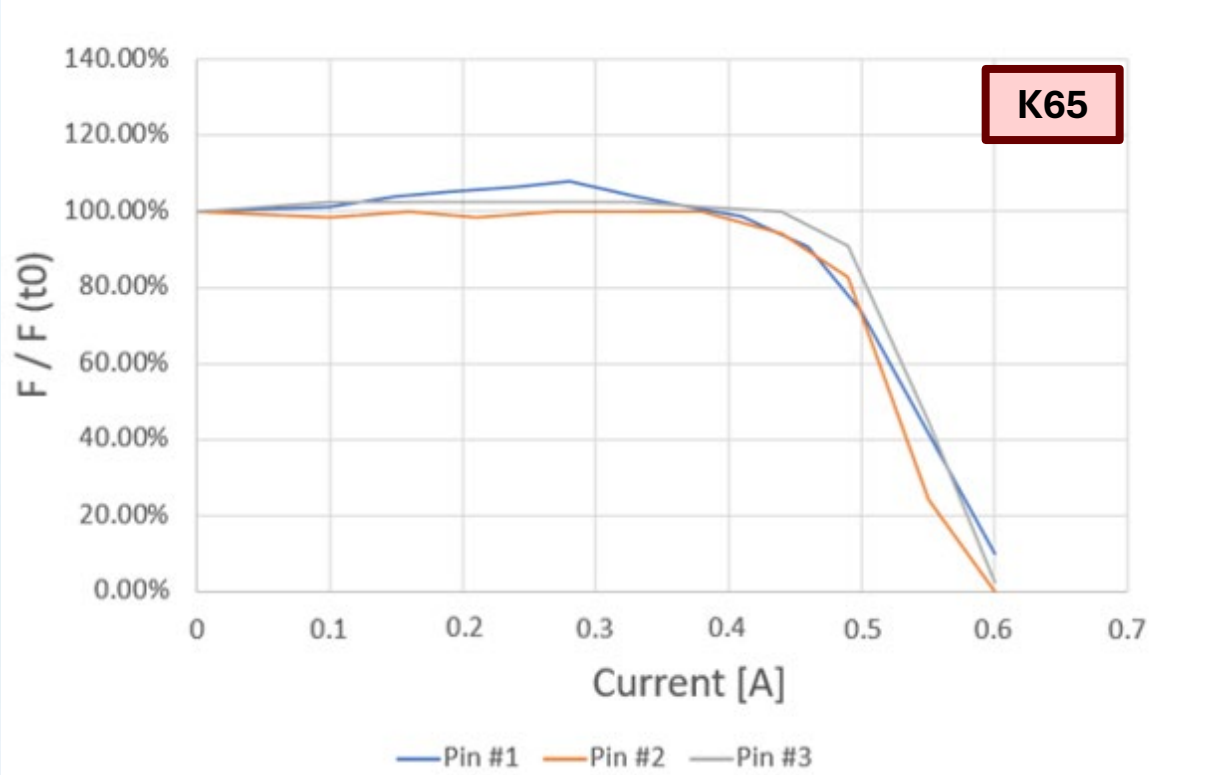


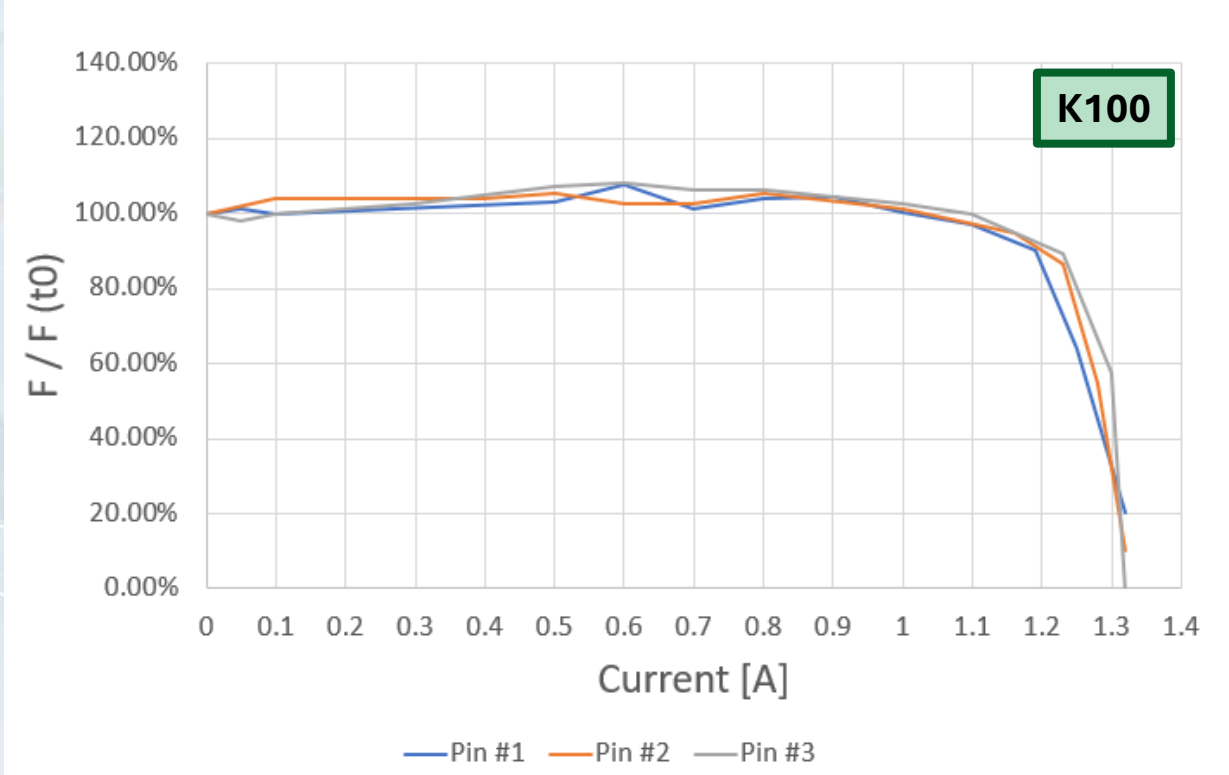


Native pitch µ-Probing: K tech

Probe Current Carrying Capability (CCC)

- 480mA (µBump **K65**)
- 1200mA (Core Bump **K100**)





Native pitch µ-Probing: K tech

K Tech mechanical reliability

µBump probe design optimization via **FEM mechanical simulation**

- Fine tuning of probe geometrical features

Mech Fatigue Test on high pin count prototype PHs

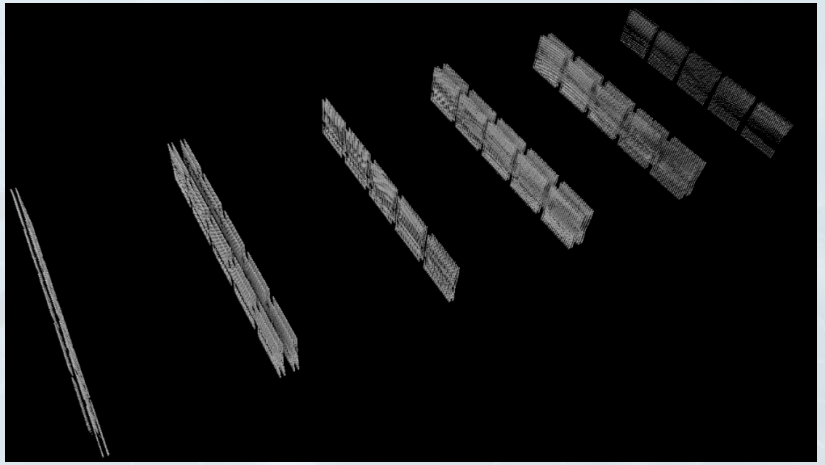
- Hybrid stress recipe
- Vertical TDs + CTDs (X scrub)
- Multiple OT on same prototype

Progressive checkpoints with **XRM analyses**

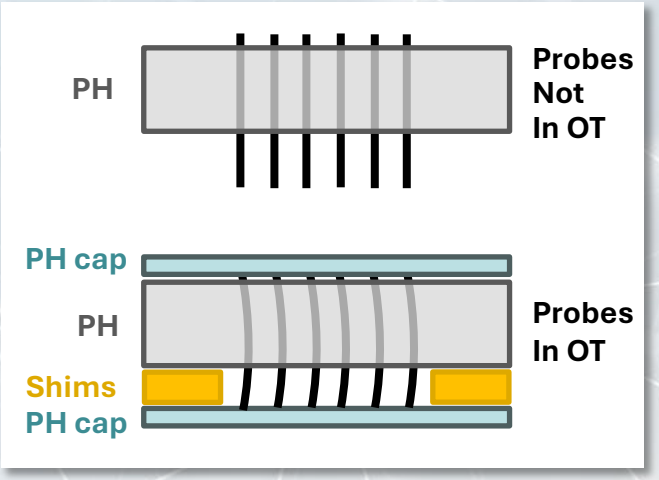
- Detail at single probe level
- With probes in OT (**caps** + **shims**)

Result

K tech probes meet 500K TD mech reliability expectations



XRM 3D reconstruction of probes within prototype PH

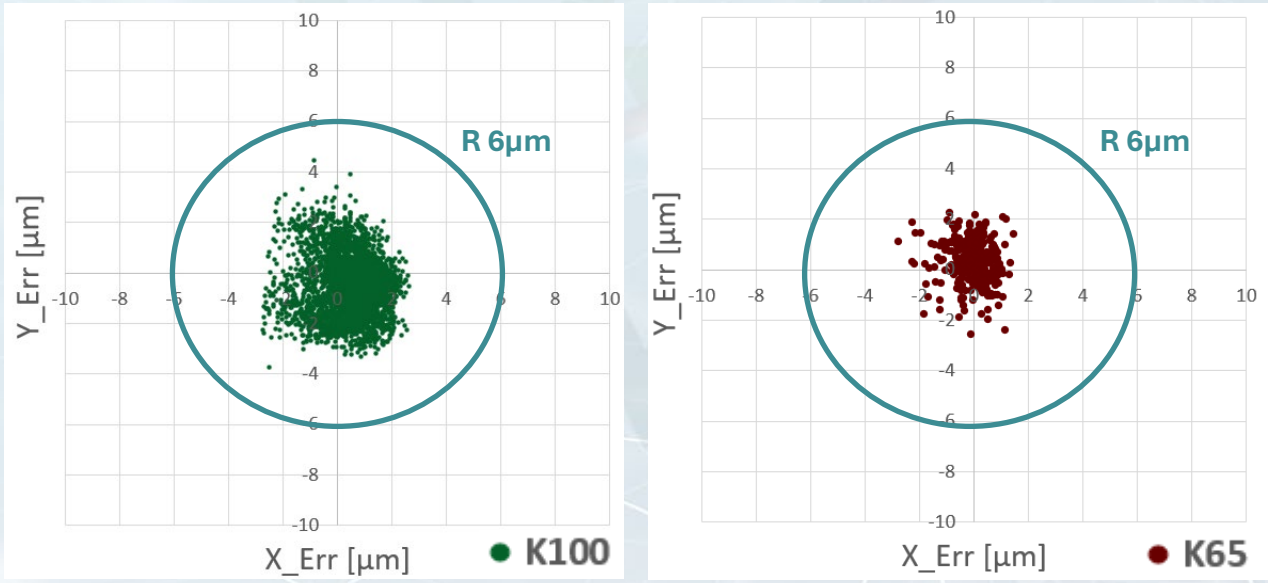


Prototype PH setup for XRM with probes in OT

Native pitch µ-Probing: K tech

Probe tip radial alignment < 6µm

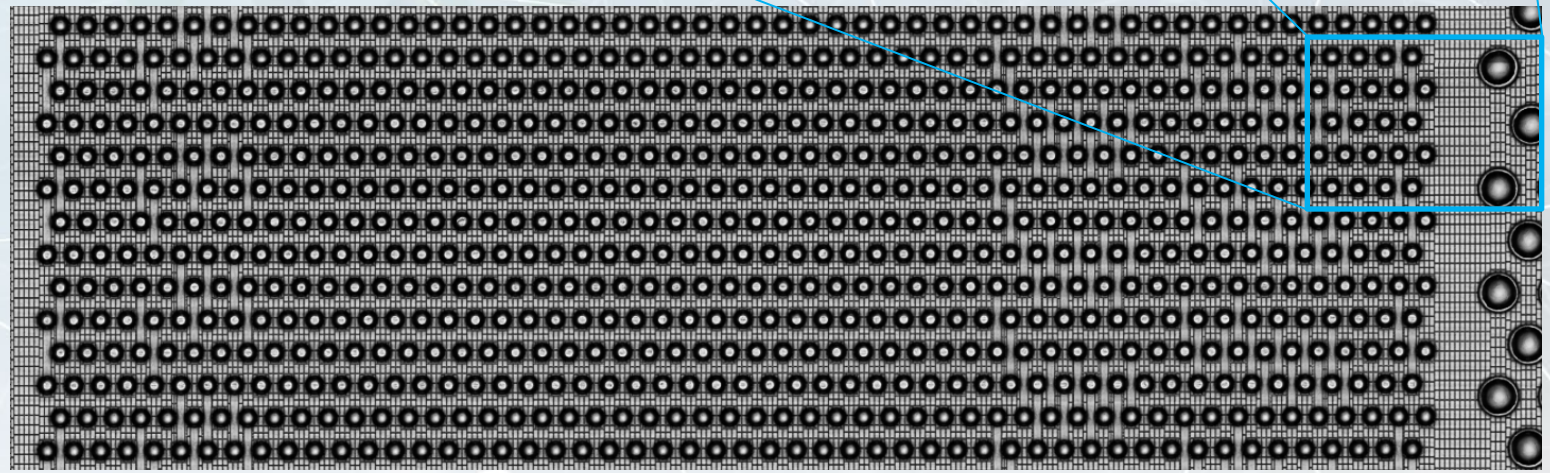
- The design features of the PH are tuned to ensure a tight tip needle position tolerances.
- If needed, a post-assembly correction on specific layers of the PH is possible to re-center the distributions.



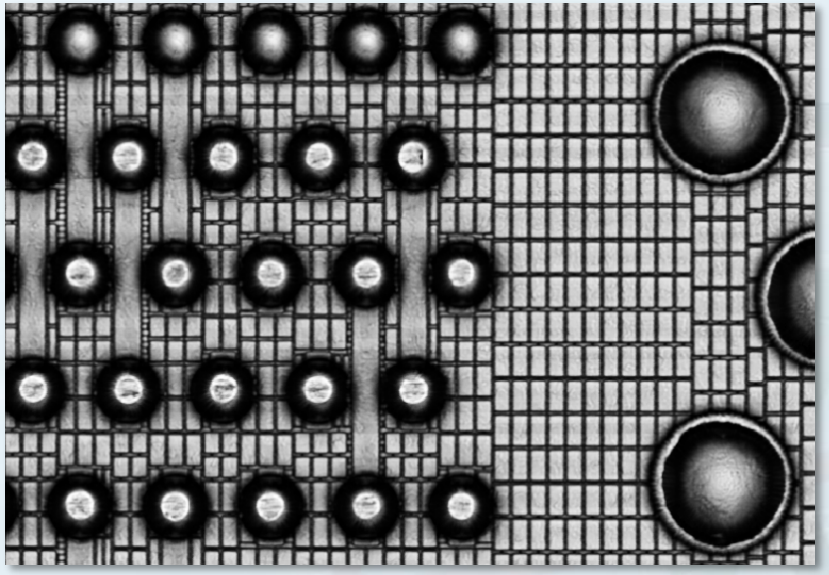
3.5k total pin count (3k **K100** + 500 **K65**)

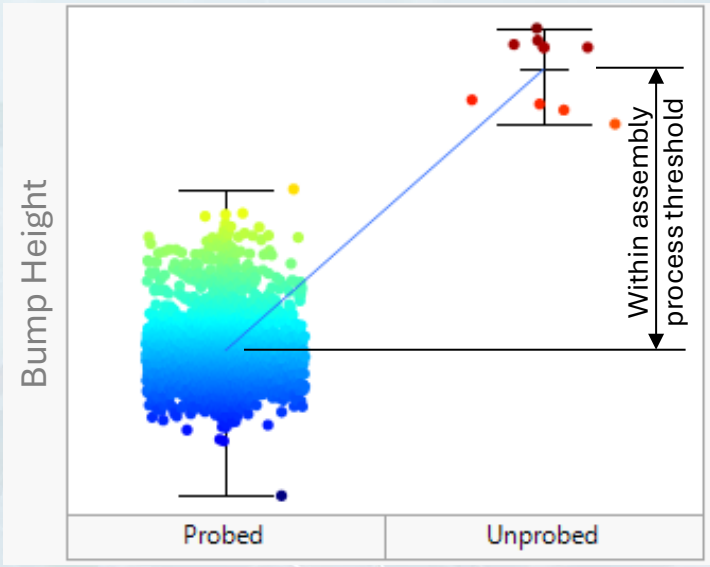
μ-bump Probing – Shorting Risk

- Test vehicle has ~ 3000 μ-bump probes.
- No evidence of shorting over several die TD.
- Some μ-bumps show partial contact.
  - Due to probe radial offset variability.



µ-bump Probing – Bump Deformation

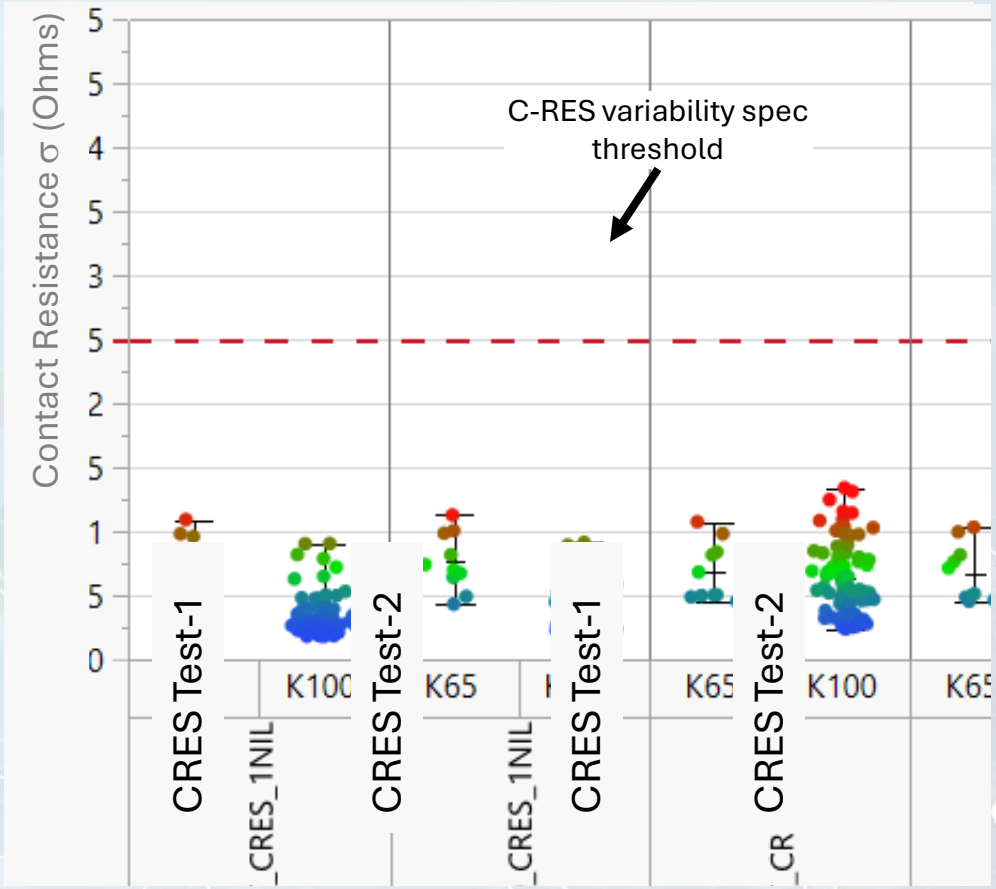




- µ-bump height deformations are well controlled.
- Unprobed to probed bumps height difference is within assembly process threshold.

µ-bump Probing – C-RES Stability

- Repeatability studies show that both core-bump and µ-bump probes' CRES are very well controlled with sufficient margin.



Summary

- Intel & Technoprobe collaboratively developed a mixed probing solution at **native µ-bump** pitch for advanced package compute die high stress testing.
- Multiple parameters were optimized for the **new probe Tech development**:
  - Reduced length (-55% w/r to **AH68**/**F36**) → improved High Speed properties
  - CCC increase (for **K100**, +40% w/r to **AH68**, +15% w/r to **F36**)
    - an extra +15% could be added applying HiP Tech on K Tech PHs
- **Probe performance** and **bump deformation metrics** are on track to pass criteria for high volume sort.
  - Metrics include:
    - C-RES stability
    - No shorting
    - Bump deformation

Message To Our Customers

- Intel and Technoprobe have a **time-tested collaborative methodology** for test interface TD and HVM ramp that has **delivered every time**.
- Intel is rapidly adopting **industry standard test platforms**.
- We invite customers to **engage with us early in the product definition cycle** to define test strategies for HPC and AI products.

Thank you!

Acknowledgement

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