



SWTEST
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The Ever-Increasing Challenge of Probe Card Power Delivery

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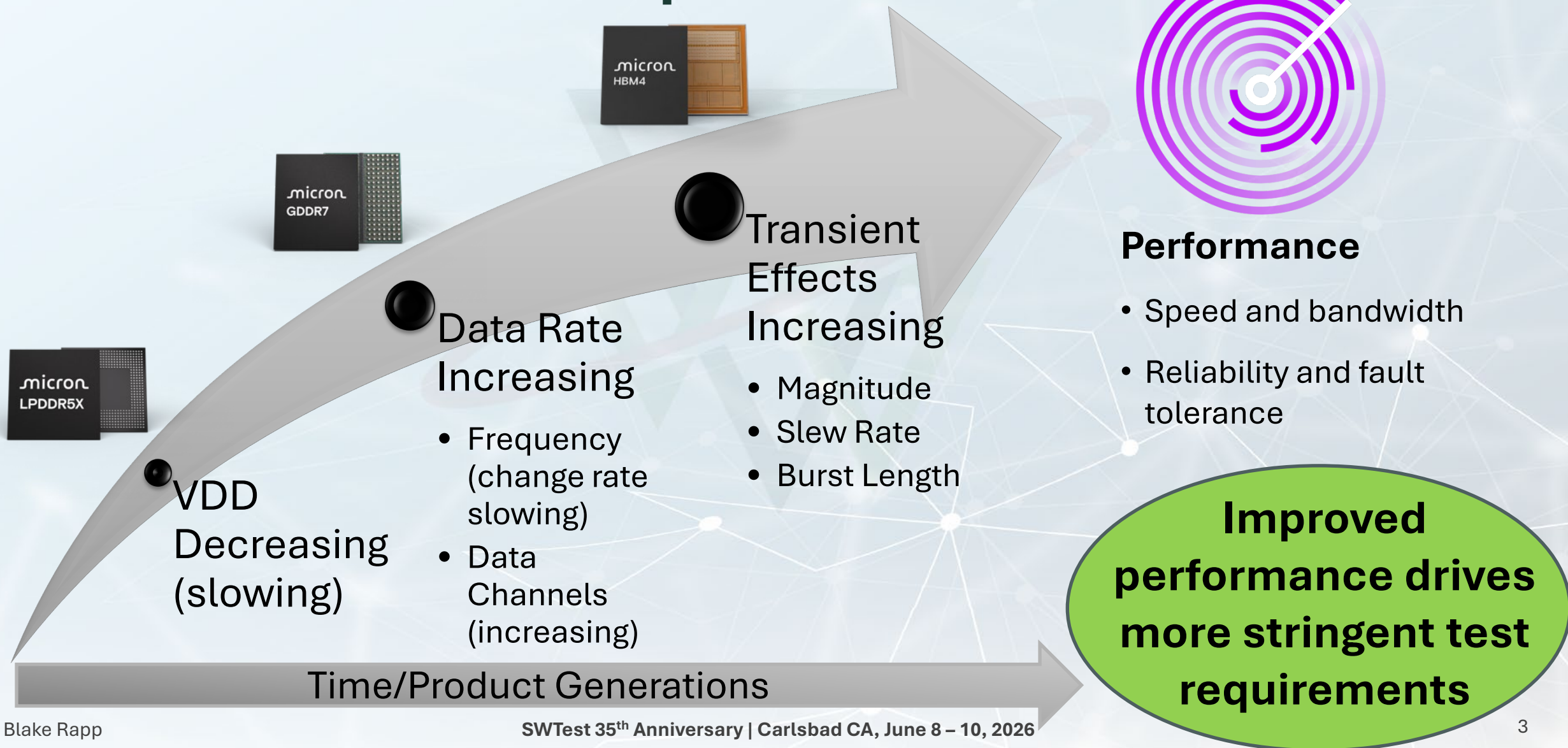
Blake Rapp
Micron Technology, Inc.

Outline

- **Changes in requirements**
- **Key factors and impacts on PDN**
 - Higher signal densities
 - Probe contact resistance
 - Lower voltage droop tolerance
 - Power supply path length
 - Test temperatures
- **Conclusion**



Trends in Memory Device Requirements



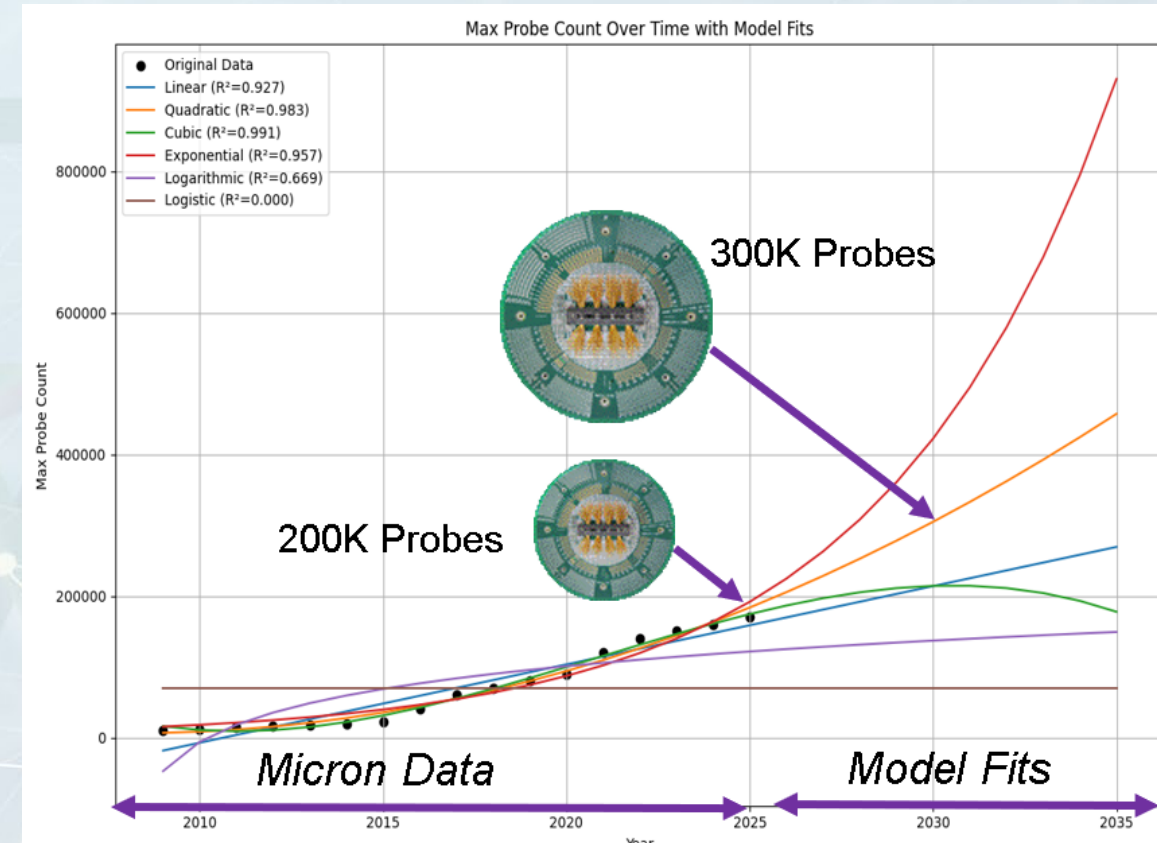
Key Factor: Higher Signal Density

- **Contributors:**

- Die size shrink (NVM, DDR, LPDDR)
- Probes per die increase (HBM)

- **Implications:**

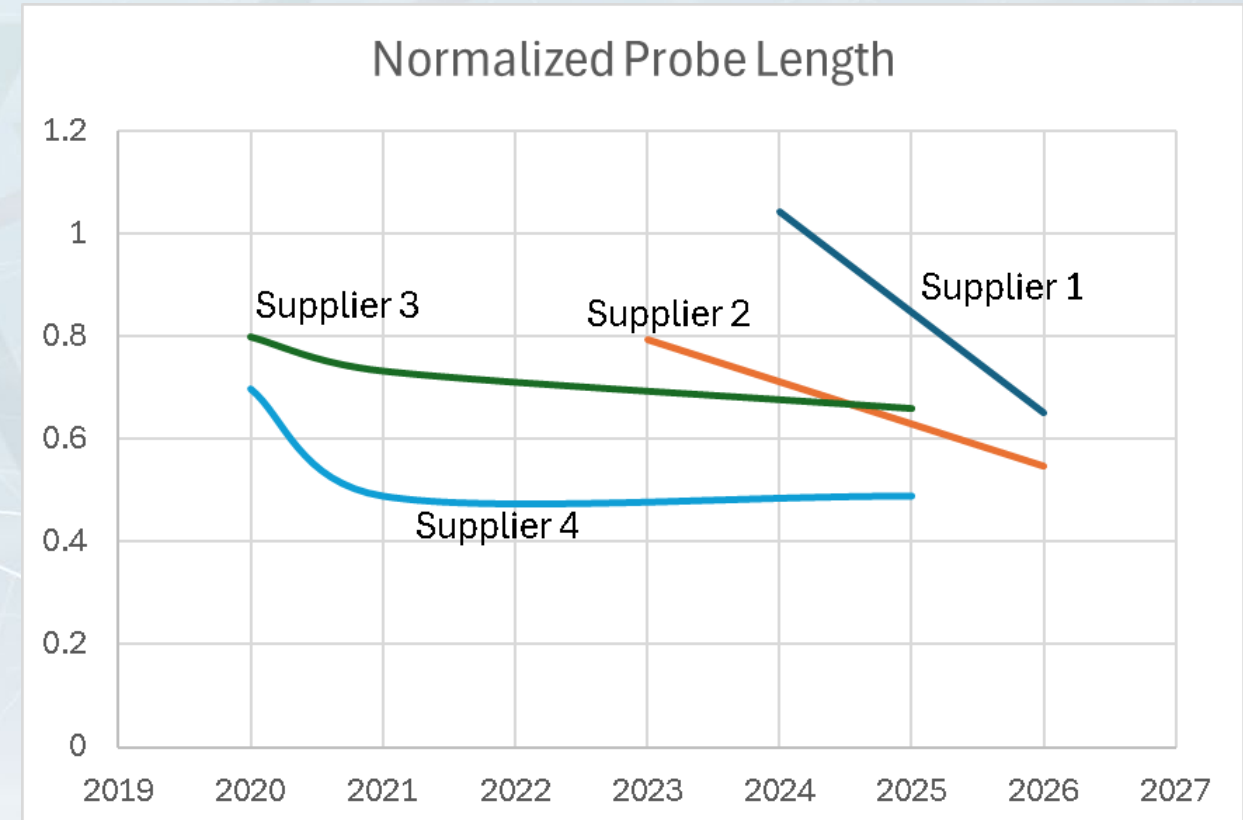
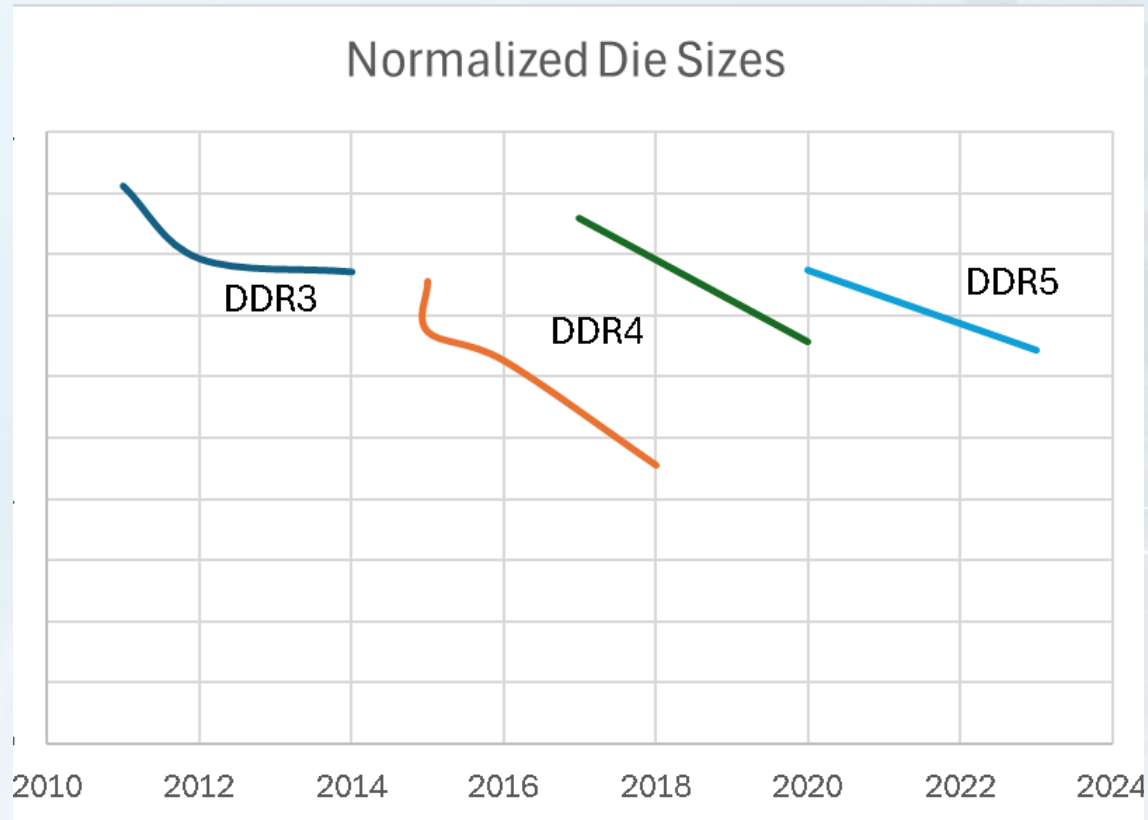
- Less room for decoupling capacitors
- Can impose constraints on probes per die depending on layout
- Leads to smaller pad sizes that drive smaller probe tip size



Reference: Alistair Laing, Micron 2025 SW
Test Asia Fukuoka

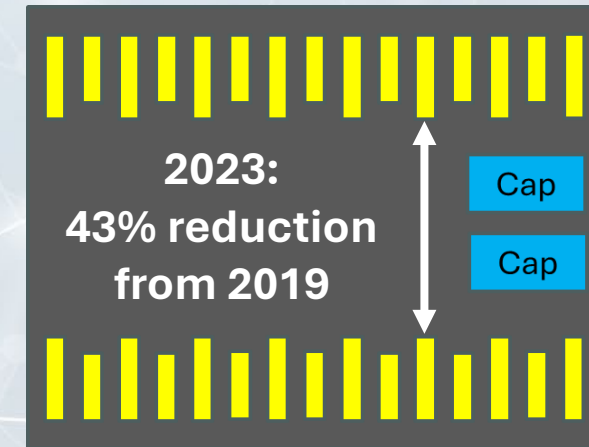
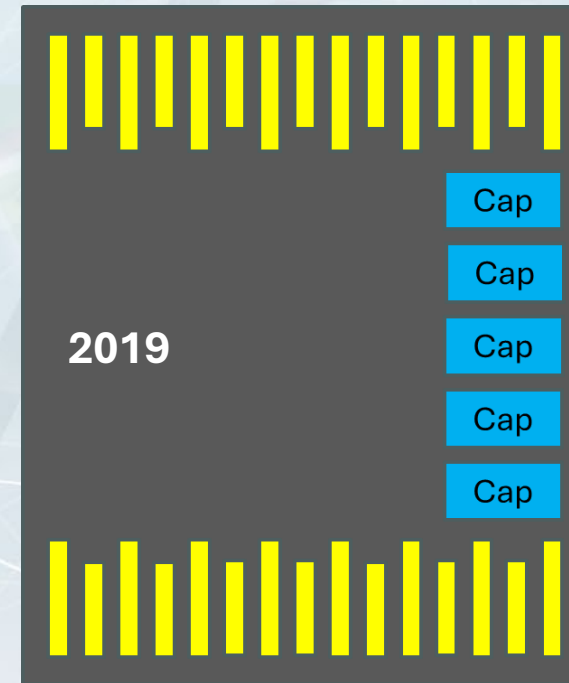
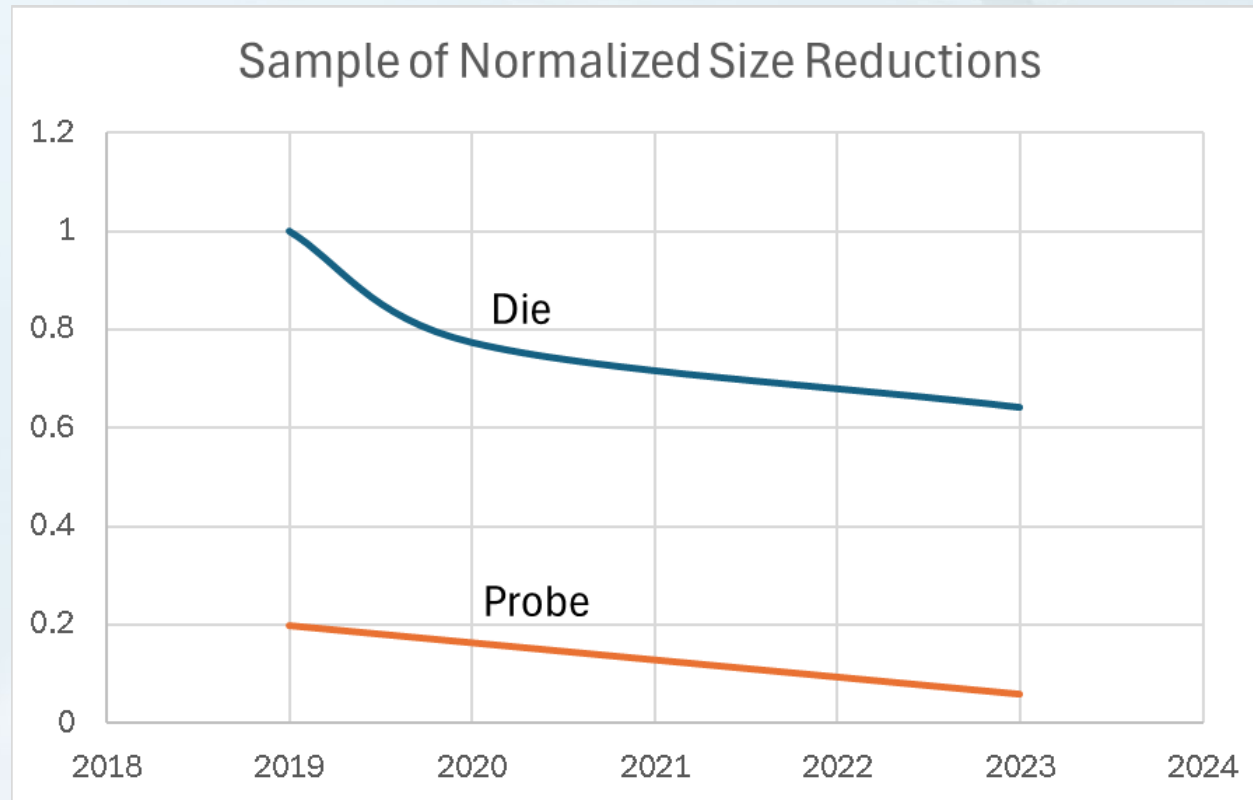
Probe Length Reduction

- Probe length and die size reduction rates are similar
- The scale of change is an order of magnitude different



What Did That Mean?

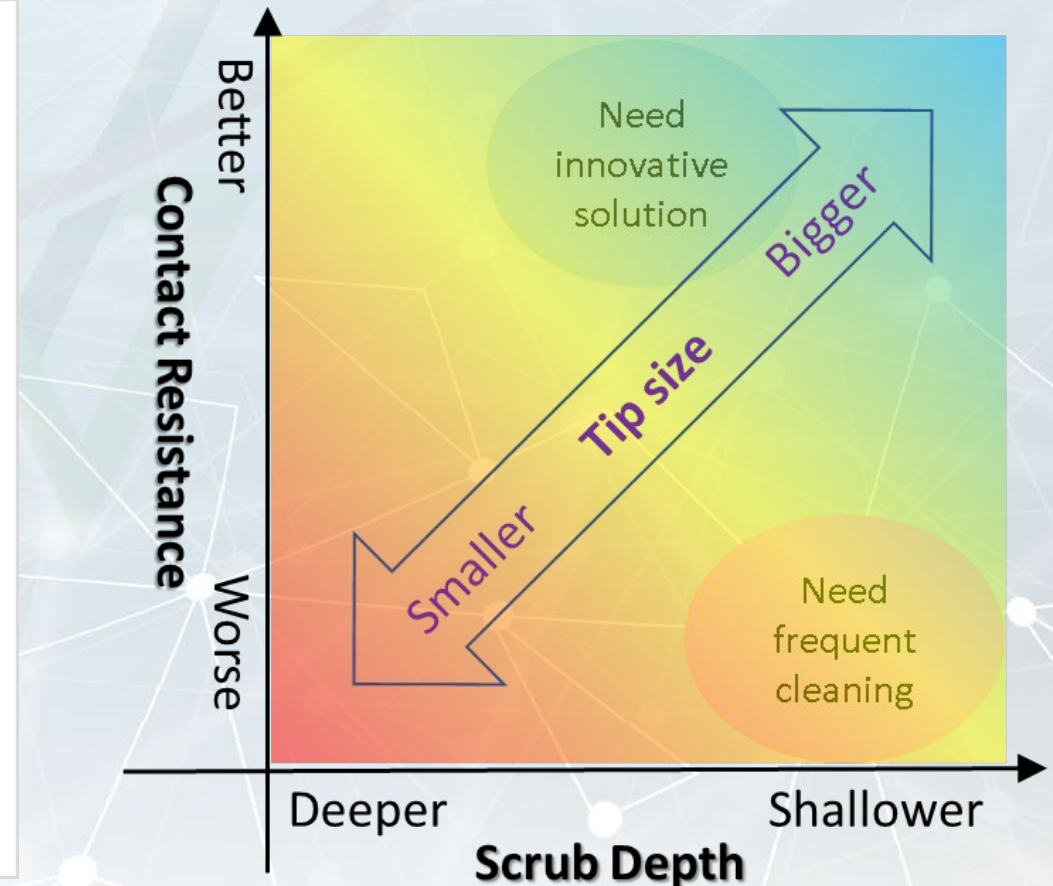
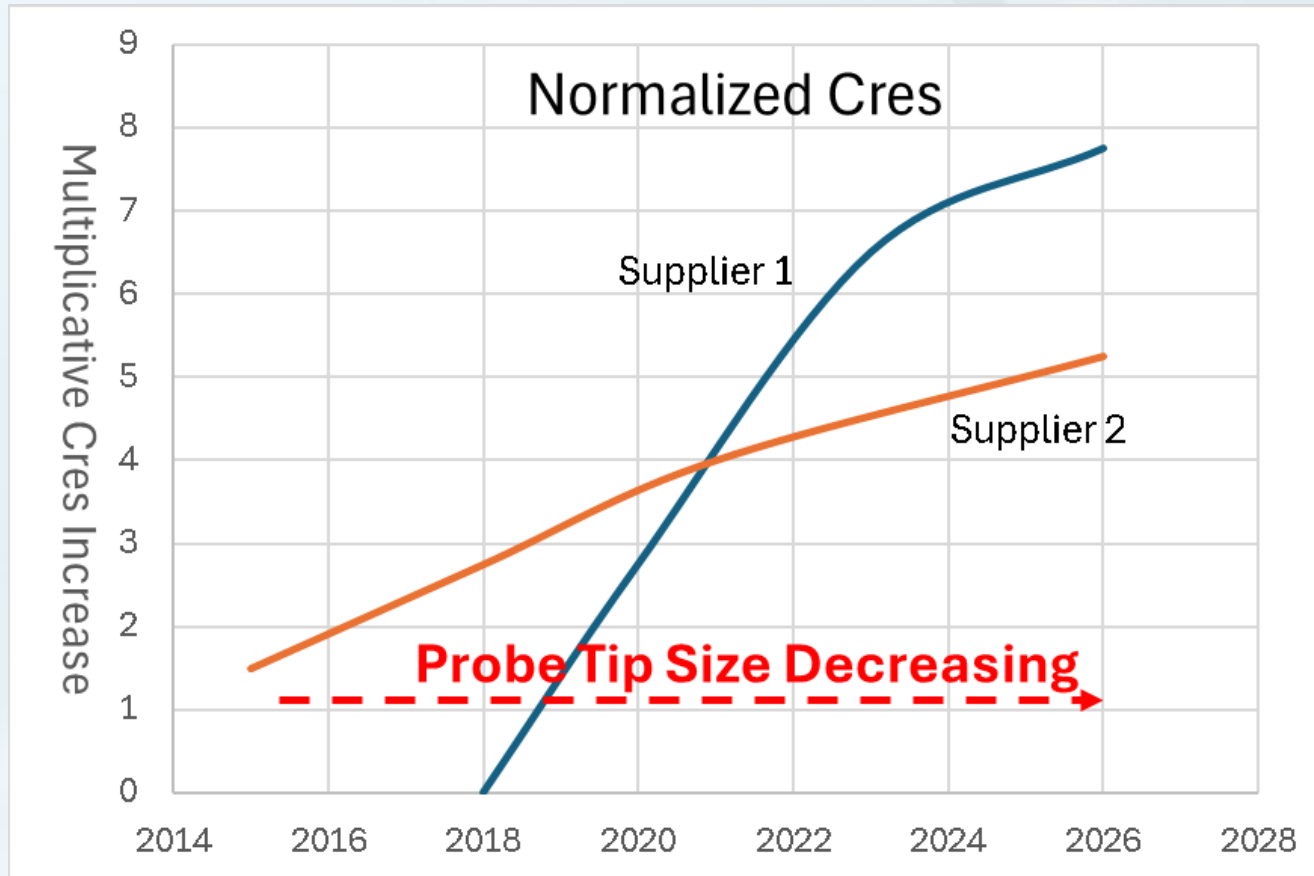
- **Die size decrease is a magnitude $>$ probe length reduction**
- **Limits area for passive components**



Key Factor: Probe Contact Resistance

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- **Contributors:** probe to pad interface, pad oxide layer, probe tip size
- **Implications:** voltage droop requiring compensation at DUT



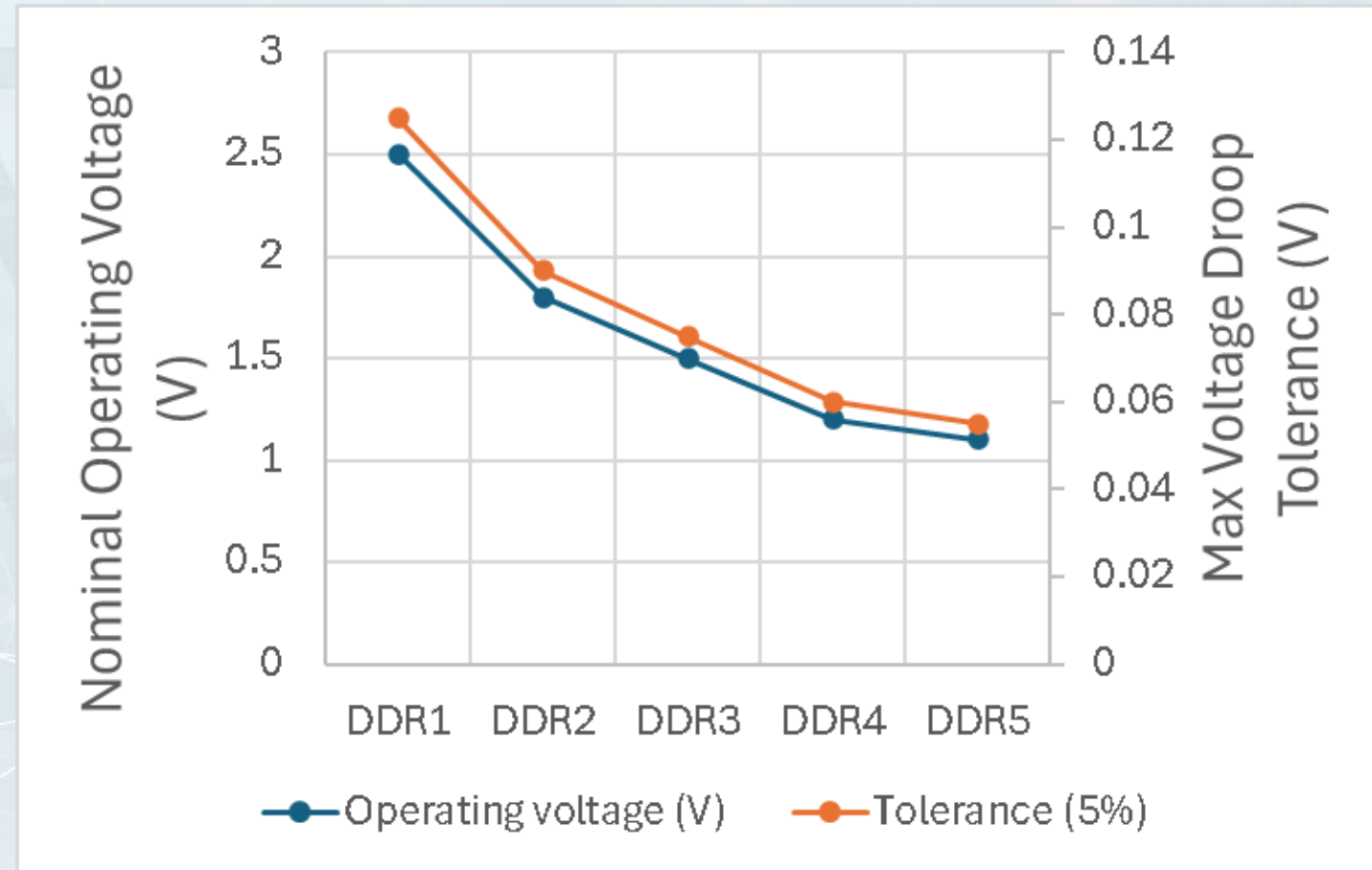
Key Factor: Lower Voltage Droop Tolerance

- **Contributors:**

- Decreasing VDD
- Selectable voltage settings allowing low-power modes for LPDDR6 and HBM
- Increased data rates and/or number of data path sub-channels

- **Implications:**

- Smaller voltage droop margin against lower VDD
- Higher current transients during higher data rate operations



Summary of JEDEC guidance

Key Factor: Power Supply Path Length

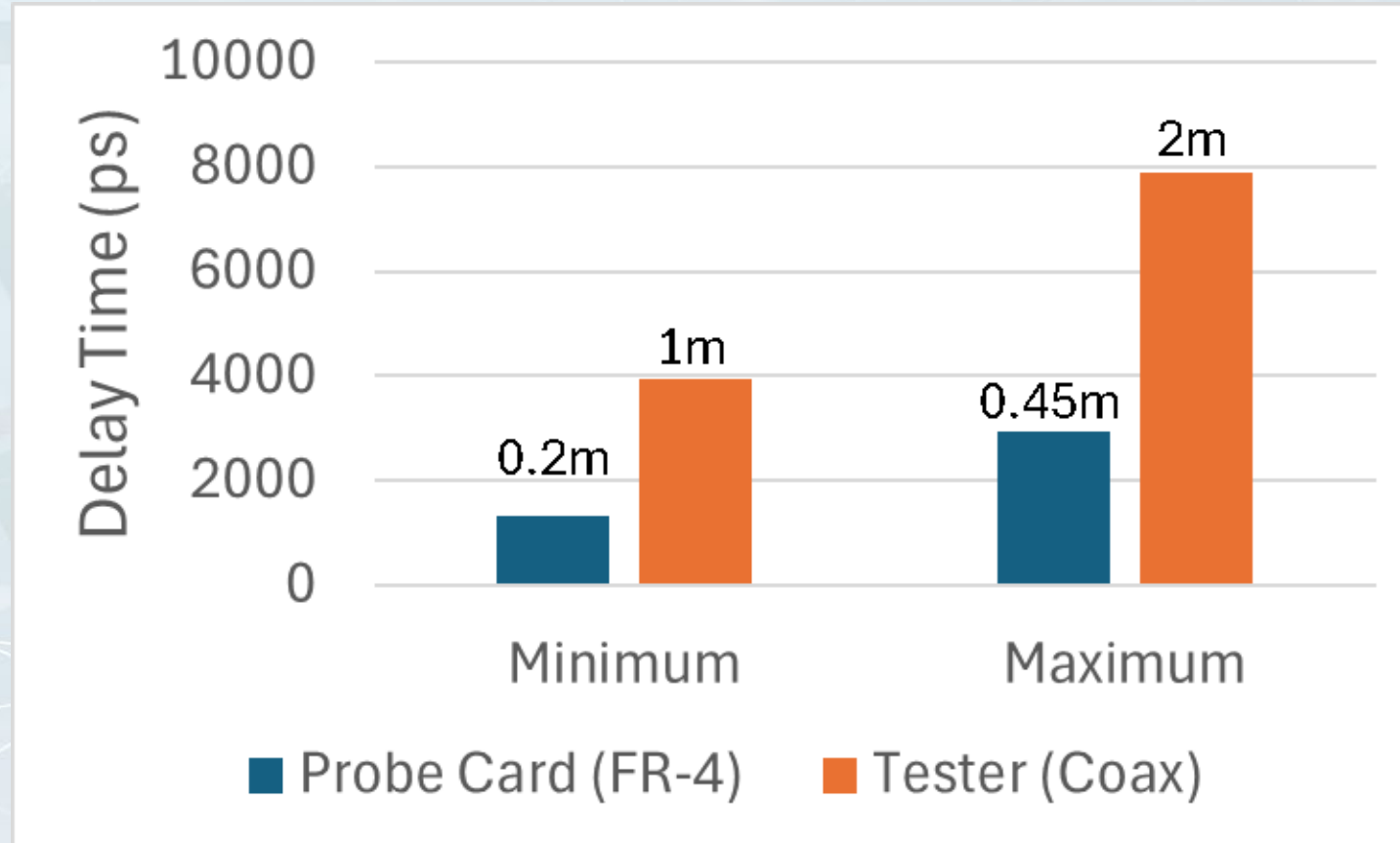
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- **Contributors:**

- Power supply and feedback paths remain unchanged as data rates/transient durations change
- Inductive losses delay perceived power supply response
- Resistive losses dilute power supply output

- **Implications:**

- Die power demand delayed
- PDN design issues can look like contact or SI problems in test results
- Total path length round trip: 10 – 20 ns



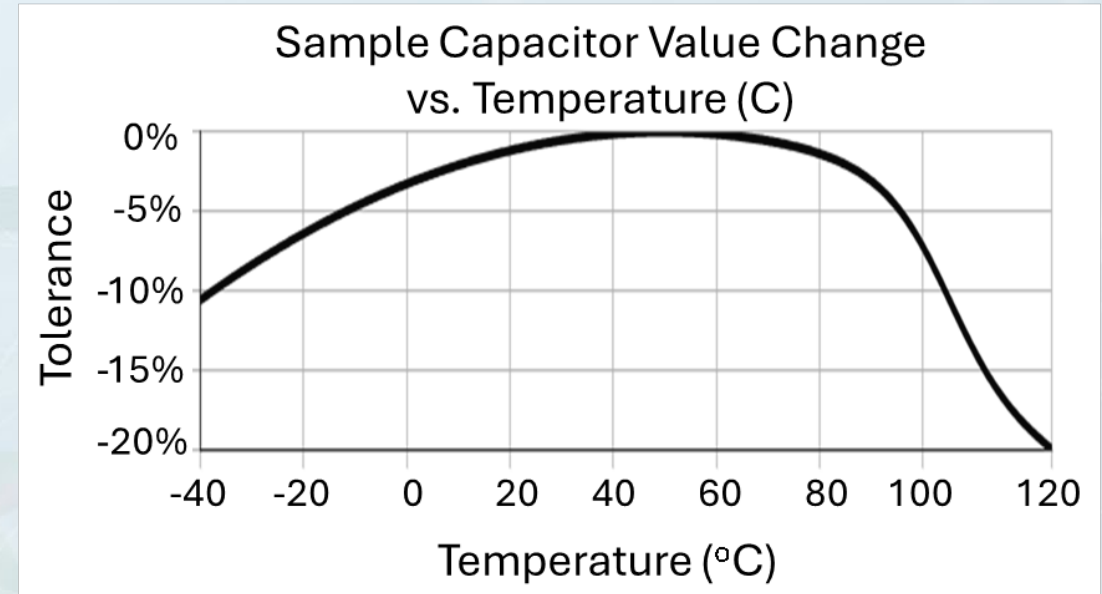
Key Factor: Test Temperature

- **Contributors:**

- Varying customer segments with different test condition requirements
- AEC-Q100: -40C to 125C

- **Implications:**

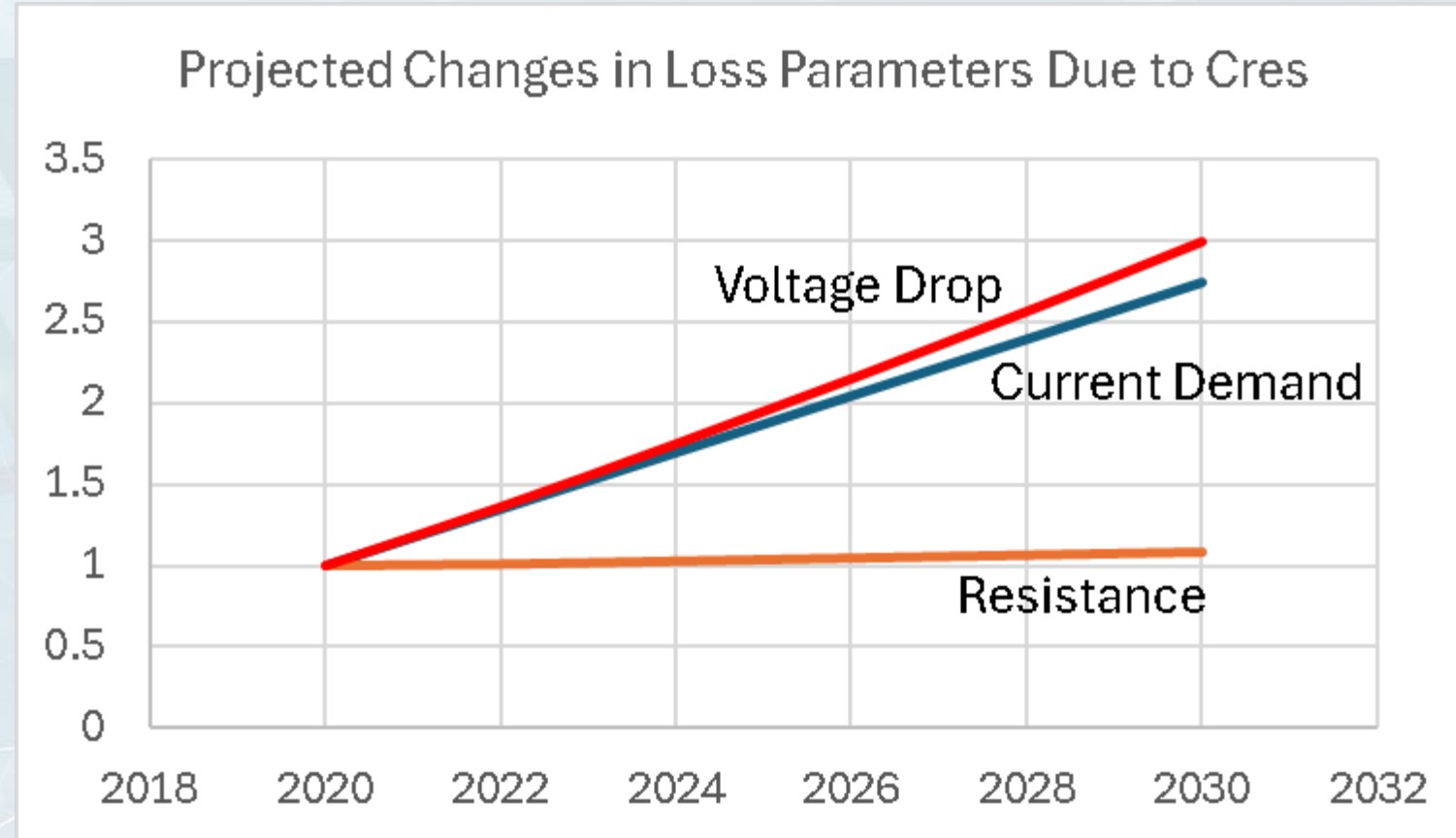
- Limits decoupling capacitor selection
 - Tolerances
 - Package size
- Electrical properties of materials



Size (SI/Metric)	Value (uF)	Temp Rating
0402 (1005)	0.047	X7R
	0.1	X7R
0603 (1608)	0.022	X7R
	0.1	X7R
	0.22	X7R
	1	X7R
	2.2	X7R

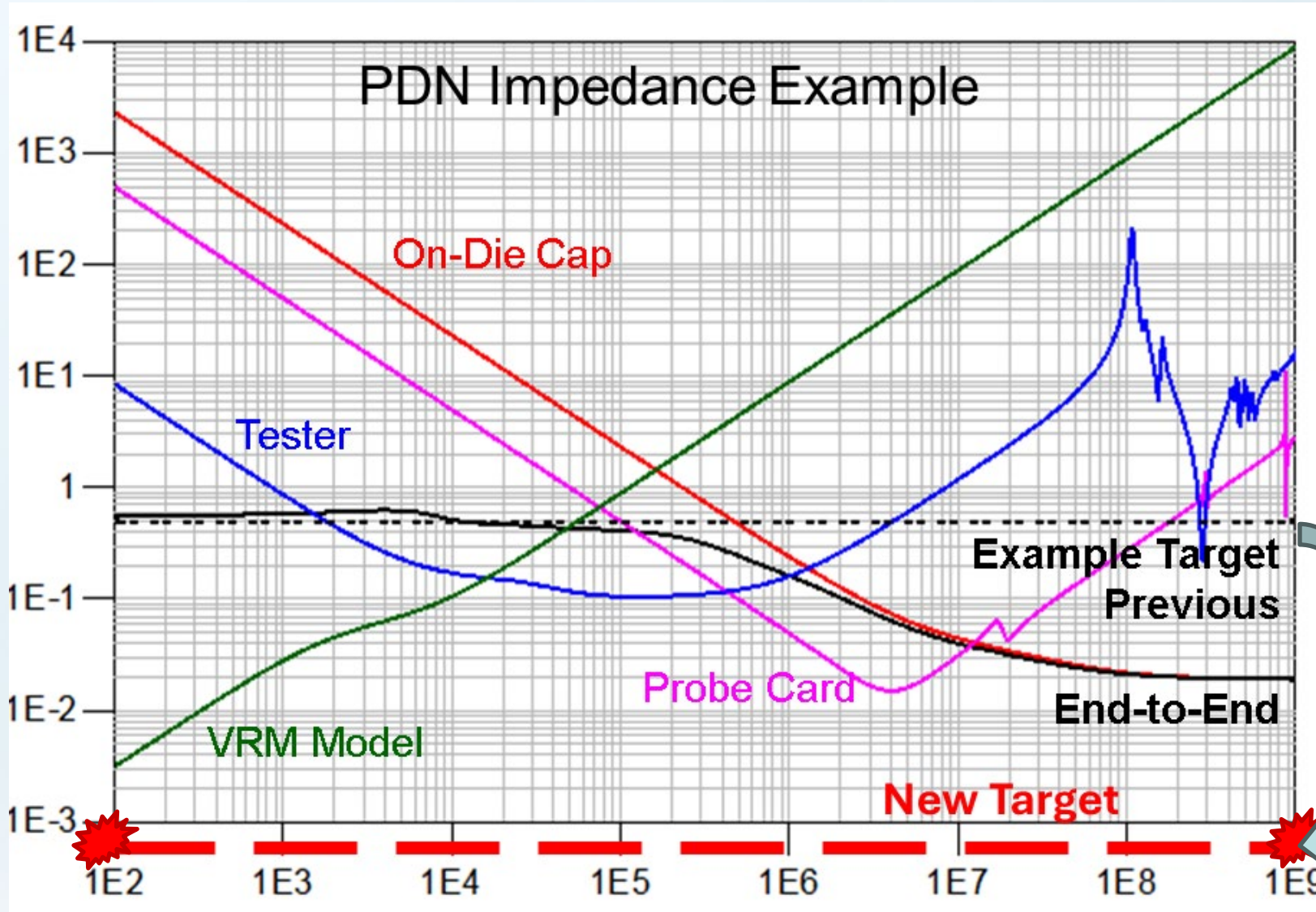
High-Current Emerging Memory

- **High current:** 1 – 2 orders of magnitude higher
- **Assumptions per two years**
 - 2x increase in Cres
 - 35% increase in current
 - No change in tester resistance
- **10-20 ns power supply response delay still present**



High-Current Emerging Memory (cont.)

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Test Requirements

Data Rate
and Current

Vdroop and
Impedance
Target

Test requirements lead
to compromised test
conditions

Industry Opportunities

- **Novel techniques reduce inductance, increase decoupling**
 - Targeting reduced PDN impedance budget
 - Increasing probe count while managing probe force
- **Measures to reduce DC resistance, mainly in probe cards**
- **Alternate methods to improve power supply reaction time while avoiding ringing/runaway**

Acknowledgements

- **Special thanks to...**
- **Kingle Wang for technical guidance and insights**
- **My coworkers and leadership for their guidance and the opportunity**
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Thanks for Joining!

Questions?

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