SWTEST 2026 CONFERENCE

35th ANNIVERSARY

Integrated Solution for HPC Testing in AI Era

tsmc®

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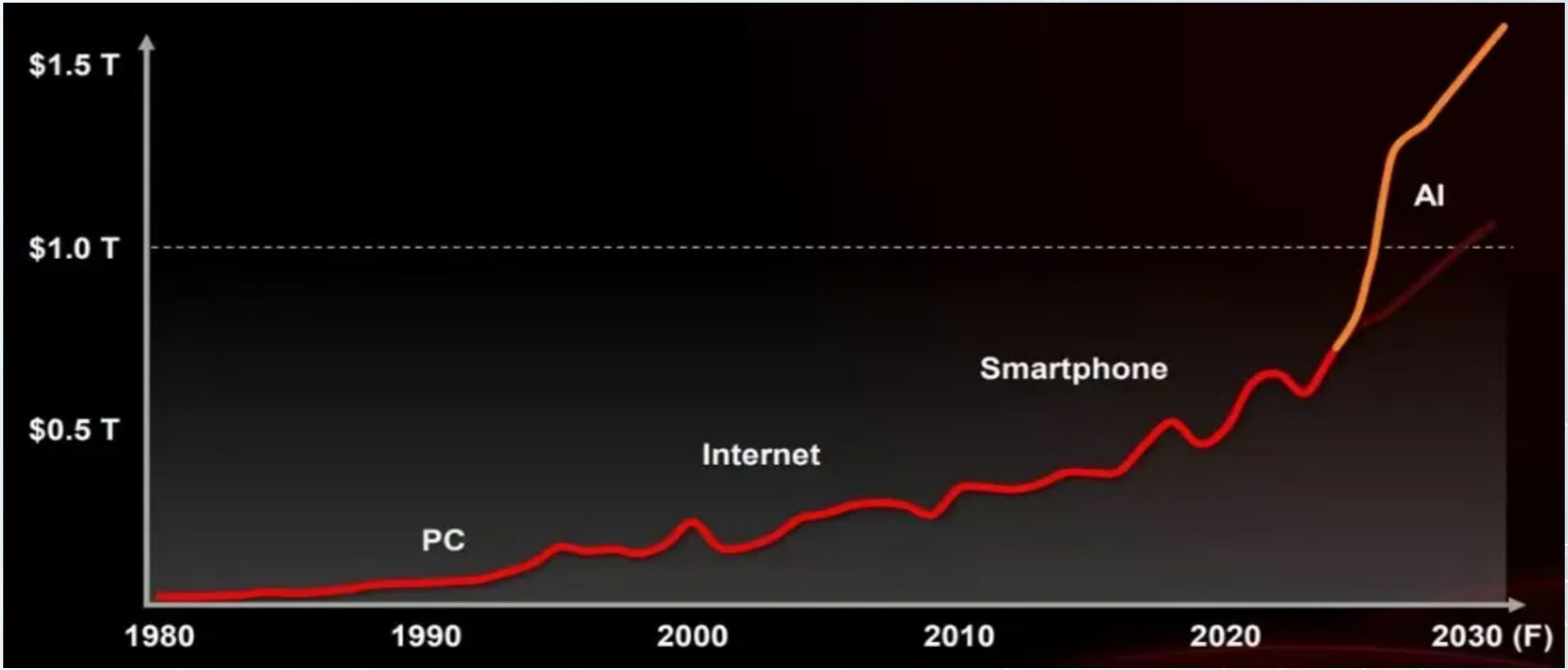
Overview

- **Introduction**
  - Product Roadmap
  - AI Technology Platform Testing and Challenging
- **Integrated Solutions for Thermal**
  - Uniform Current Distribution (UCD)
  - Thermal Dissipation Structure (TDS)
  - Active Temperature Control
- **Summary**

AI is now everywhere

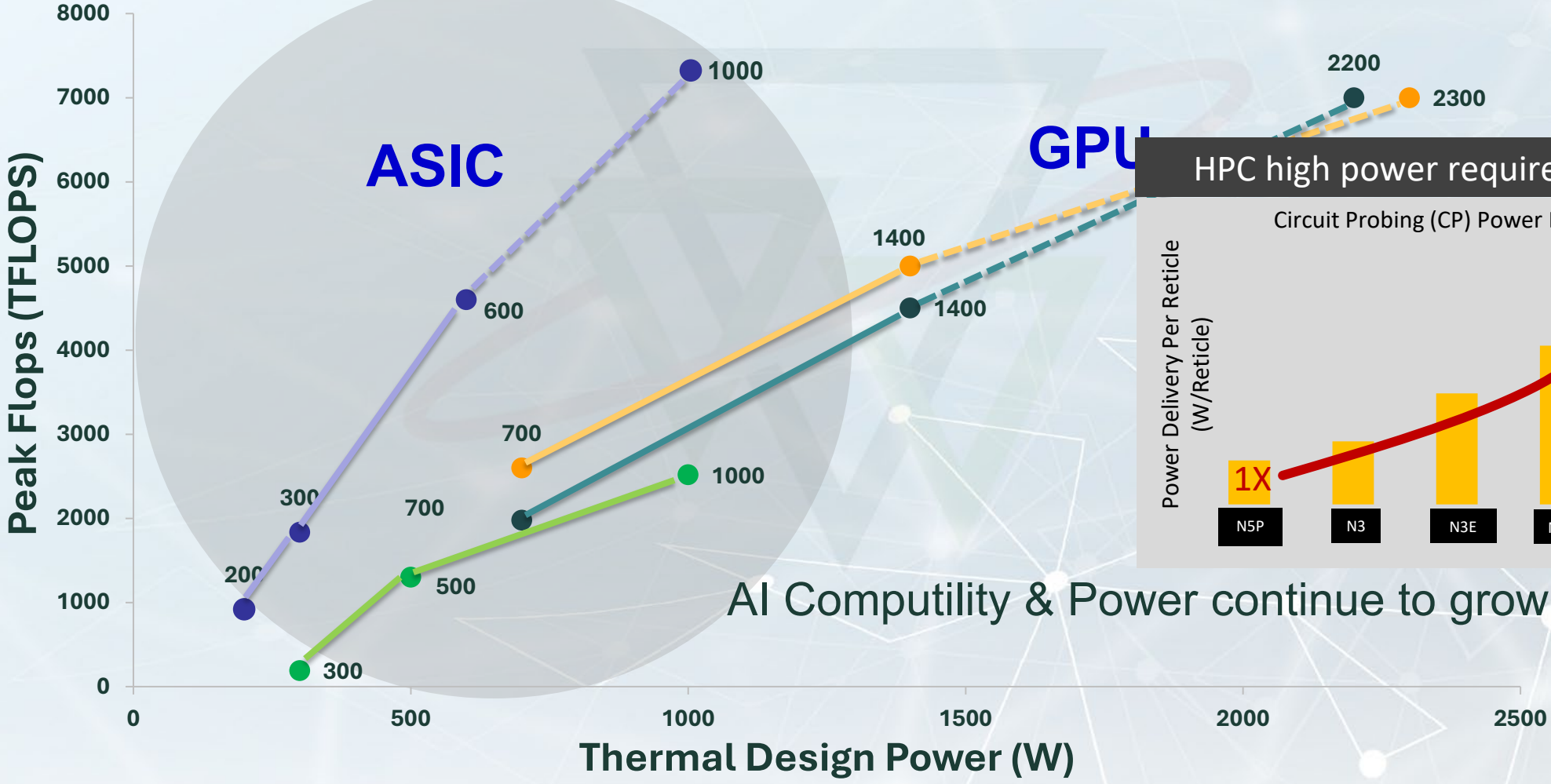
Semiconductor $1T Milestone Accelerated



Source: TSMC 2026 Symposium

HPC Power Trend

HPC Product Trend (TDP vs Peak Flops)



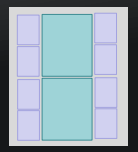
AI Computility & Power continue to grow

Packaging RoadMap

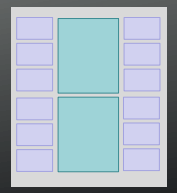
35th ANNIVERSARY

Interposer Size (-reticle)

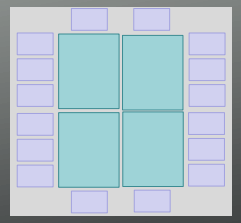
40x
14x
13x
12x
11x
10x
9x
8x
7x
6x
5x
4x
3x



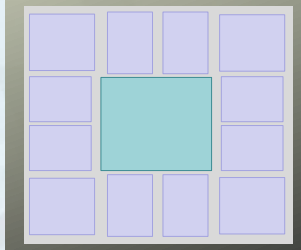
3.3-reticle
8 HBM3
75x70mm
Package size



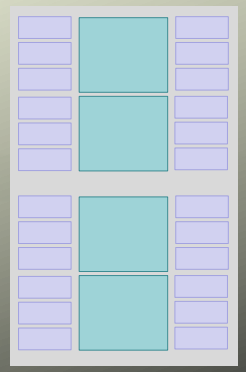
5.5-reticle
12 HBM4
85x110mm



9.5-reticle
≥12 HBM4
120x150mm

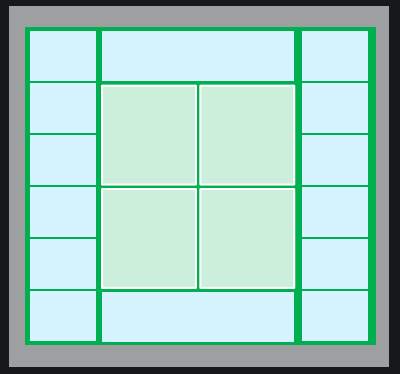


11.11-reticle
150x150mm



12 or 14-reticle
(2pcs 5x or 7x CoW)
150x230mm

>40x reticle
200x200mm

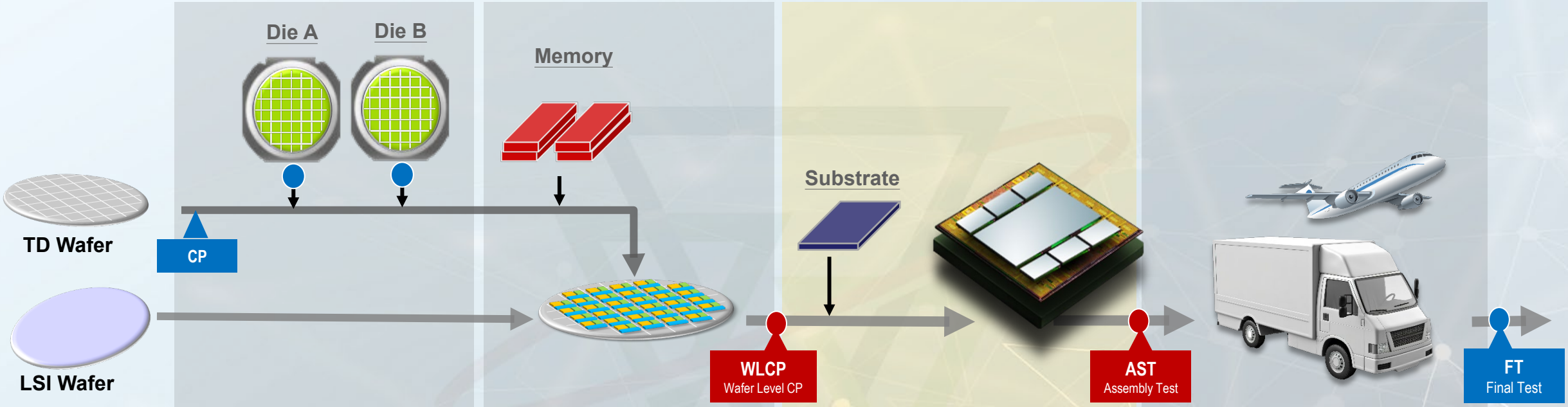


<300x300mm

CoWoS-L → ***MCM*** → ***SoW*** → ***NEW*** *(POC)*
2027

Now

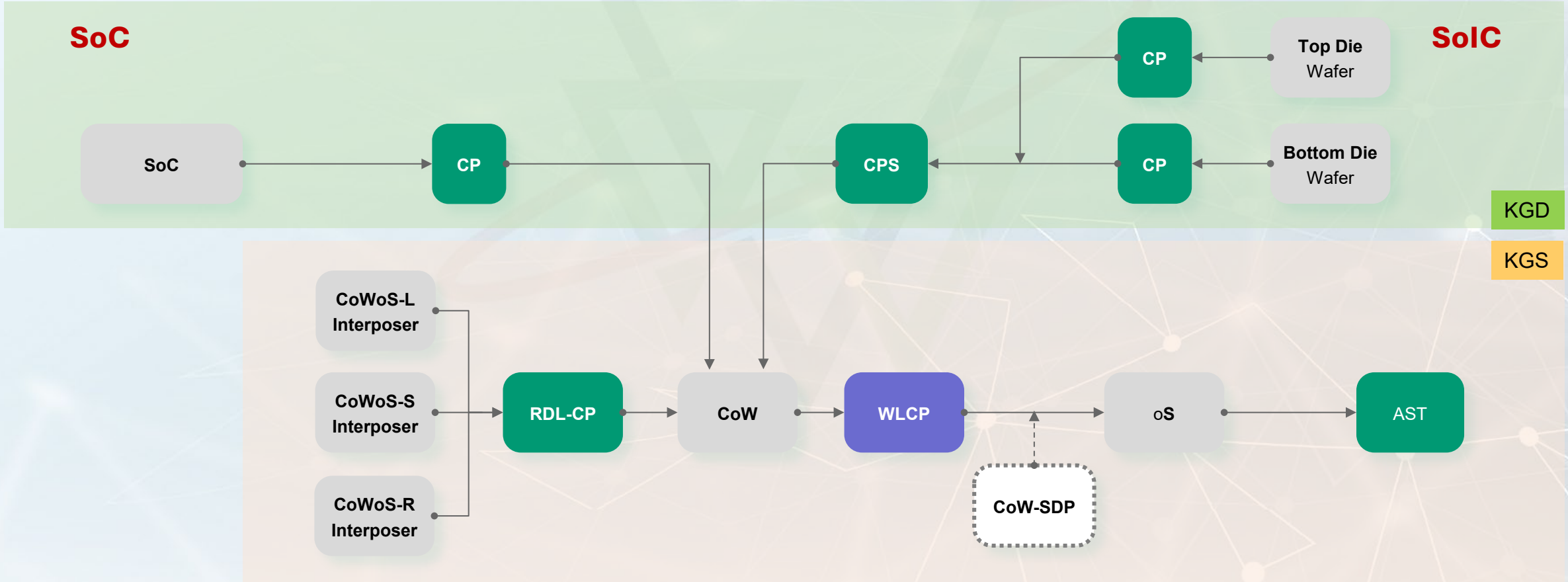
CP Testing for Early Detection



** TD: Top Die
LSI: Local Silicon Interconnect

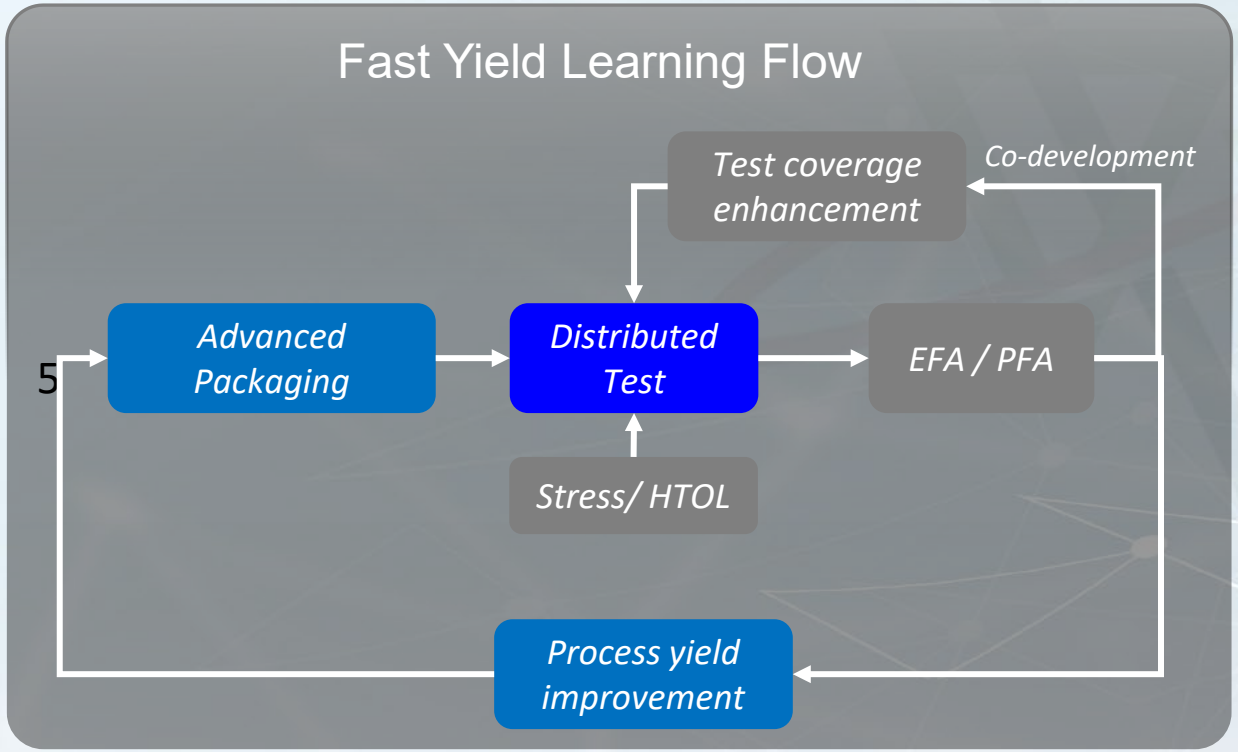
Distributed Test

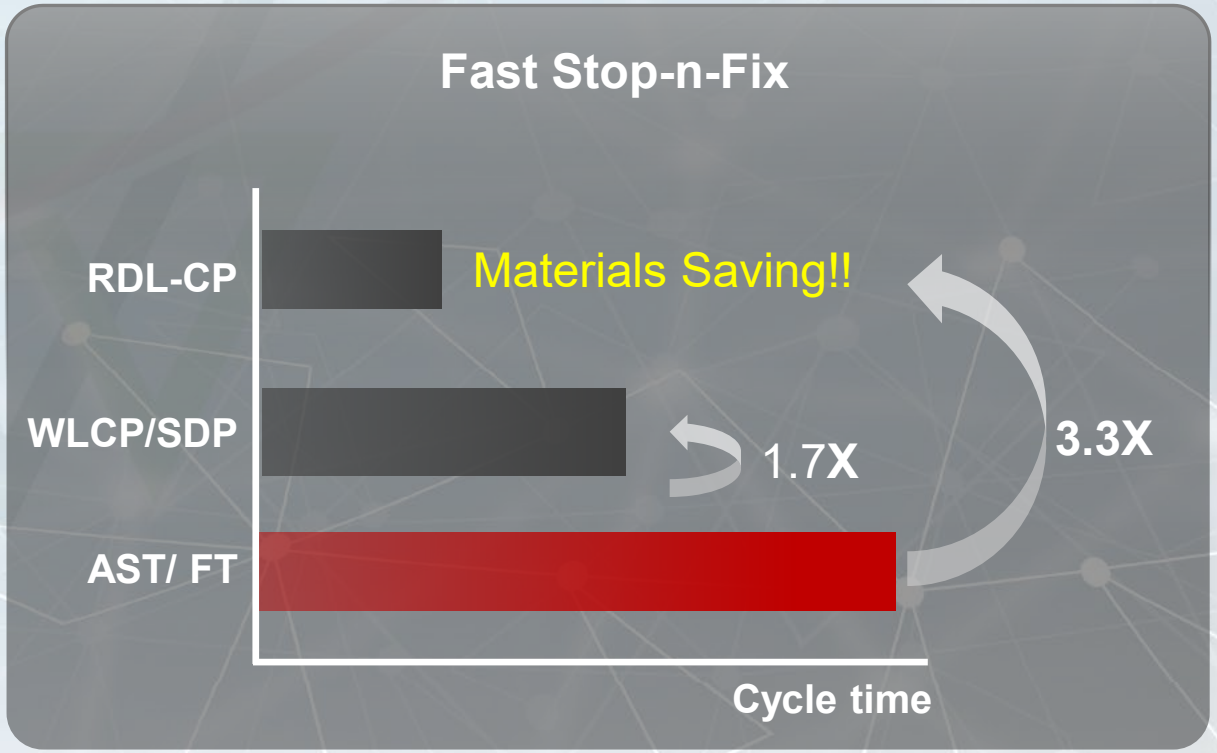
- **Boosting test coverage through distributed test architectures, including CP (CP/LSI/IVR/RDL) for KGD, CPS for KGS, AST for assembly quality**



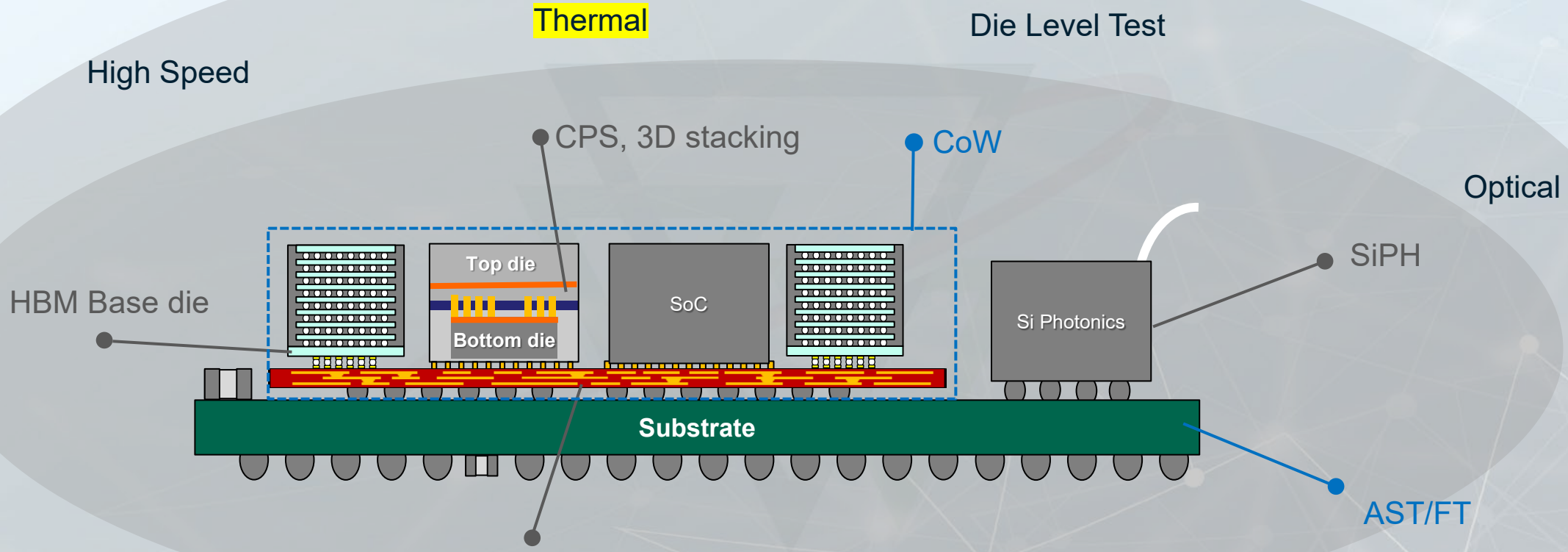
Fast and Cost-effective Testing

- Accelerate DPPM reduction by collaborating with customers and fab.
- Early process excursion detection and cost saving.



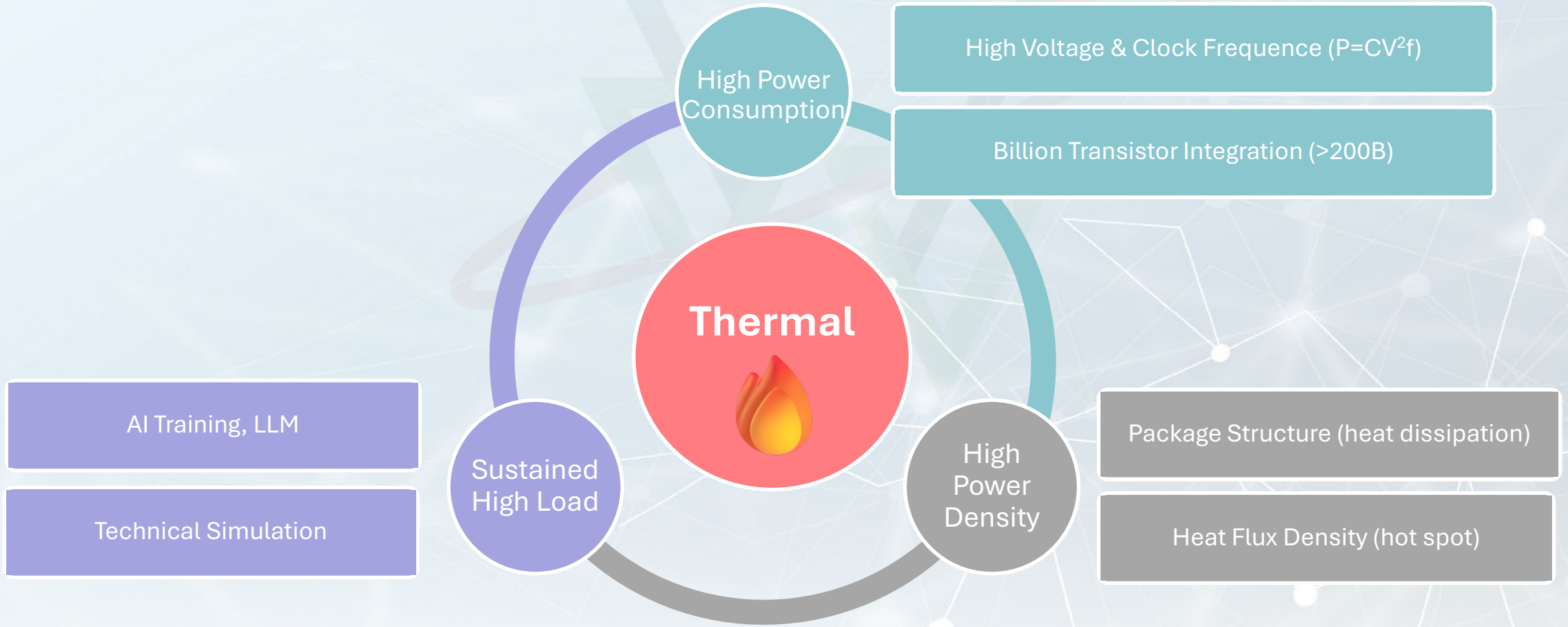


AI Technology Platform Testing



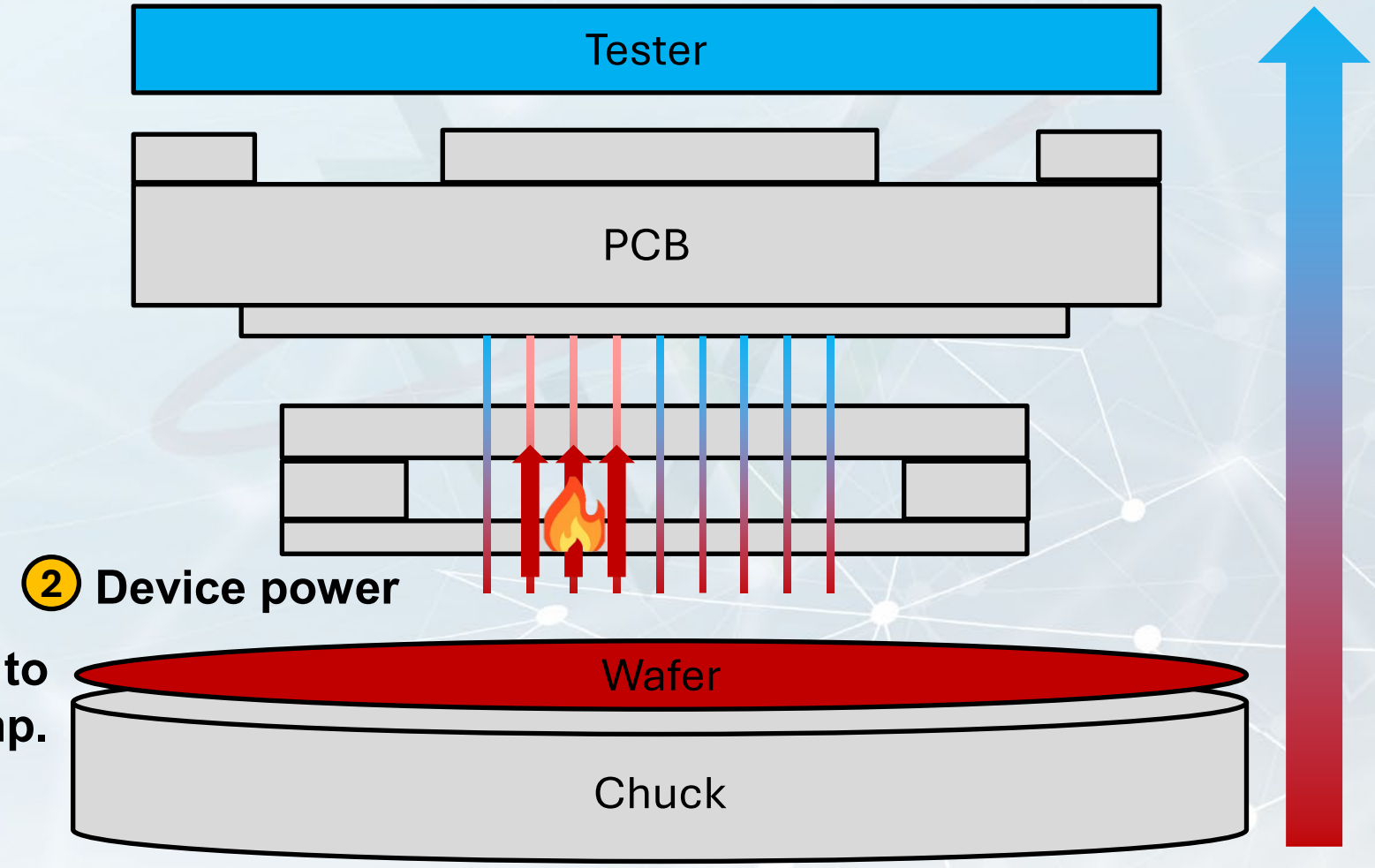
HPC Thermal Management: A Necessity

- **Extreme computational density and speed drive high power consumption and concentrated heat, presenting a major thermal challenge for HPC chips.**



Integrated Solutions for Thermal

- Heat is from (1) Chuck thermal equilibrium (2) Device power



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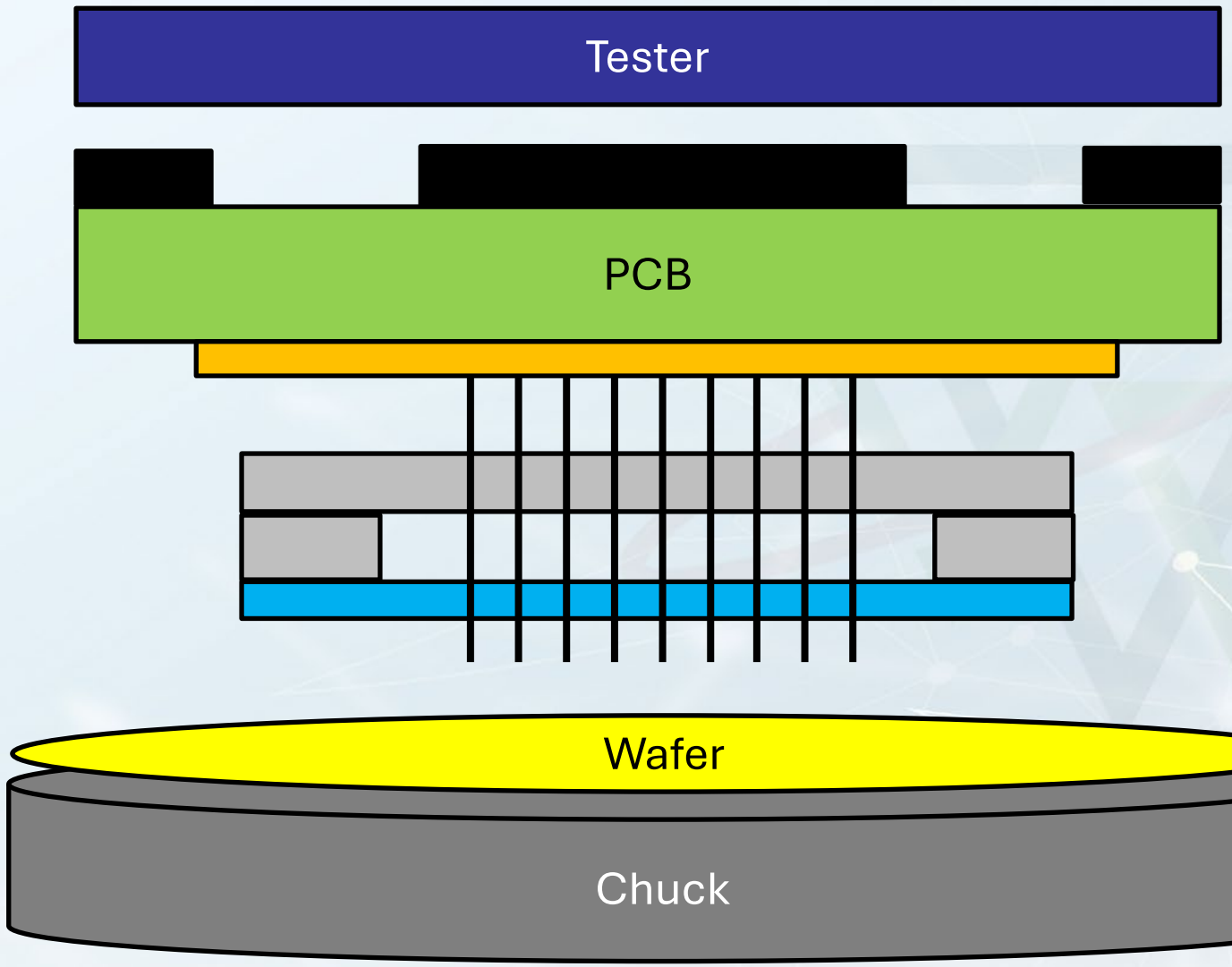


Tester

Associate with TDS (Air/ Liquid)

Probe Card

Uniform Current Distribution (UCD)

High Thermal Conductivity

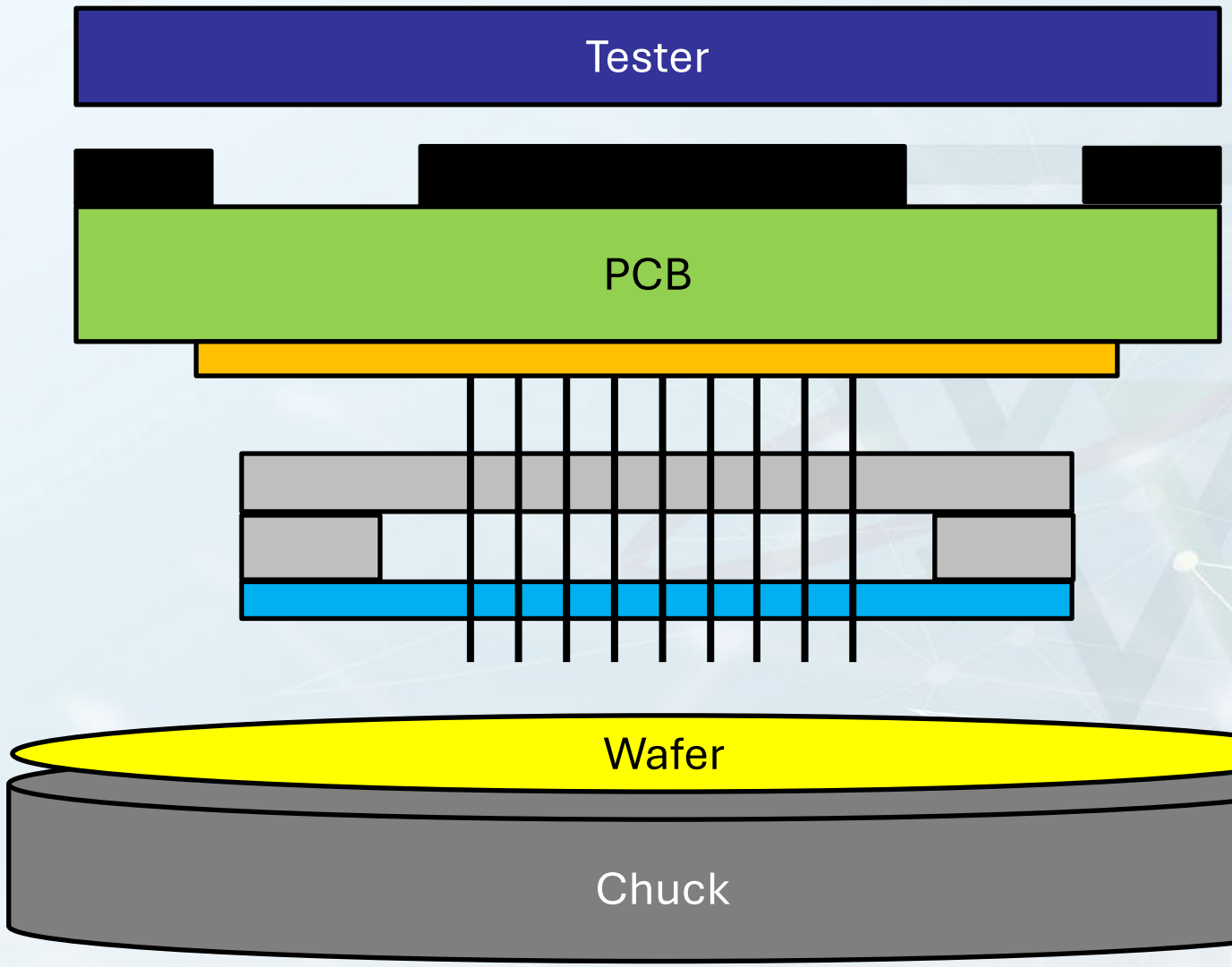
Thermal Dissipation Structure (TDS)

Wafer + Chuck

Advanced Hardware Capability

Intelligent Temperature Control

Integrated Solutions for Thermal



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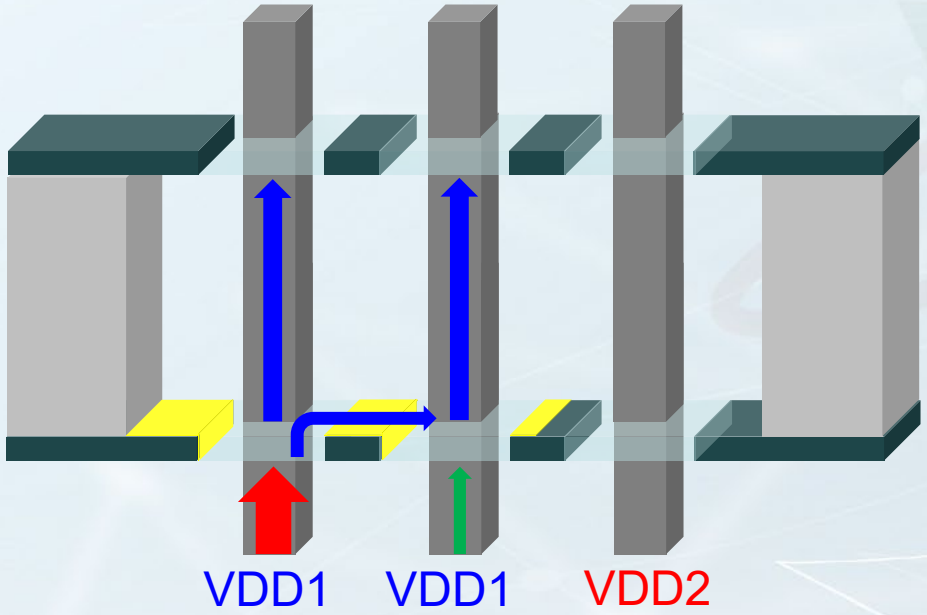
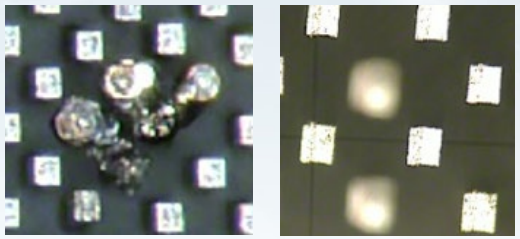
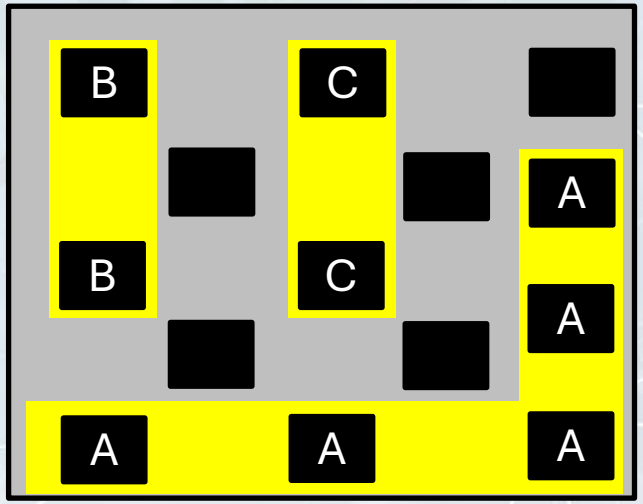
UCD (Uniform Current Distribution)

- To enhance current distribution uniformity, the metal trace is coated on PH to connect the same power rails.
- CCC could be improved > 40%.

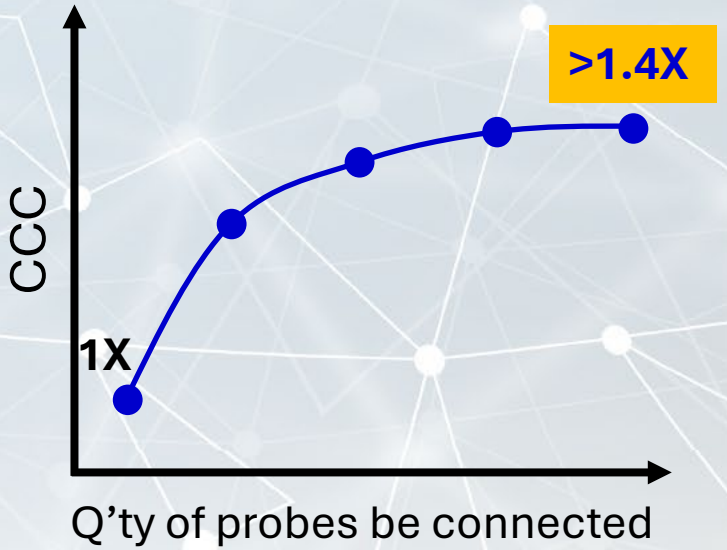




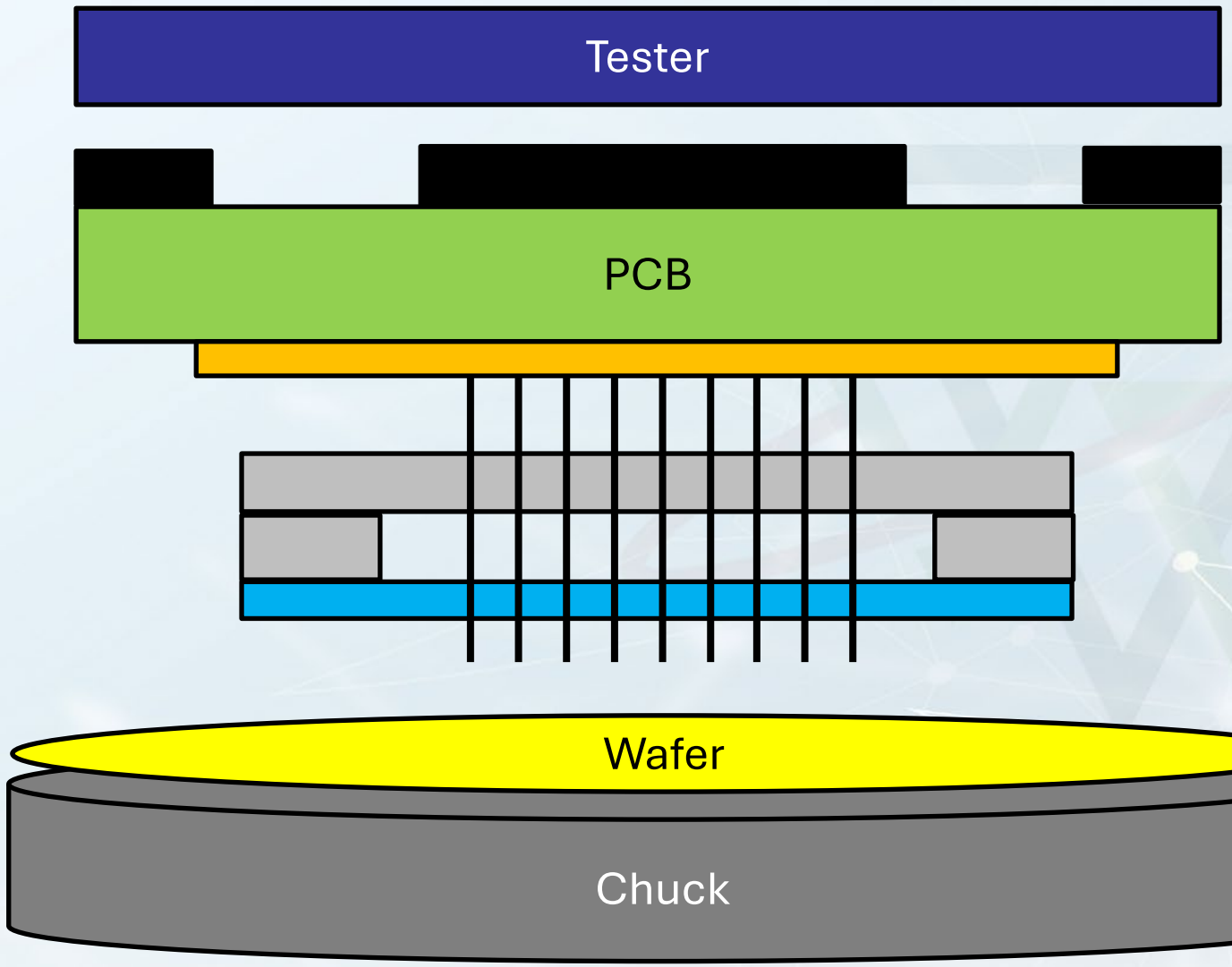


Connect the same power group

1) Improvement could > 40%
2) Saturate with connected q'ty



Integrated Solutions for Thermal



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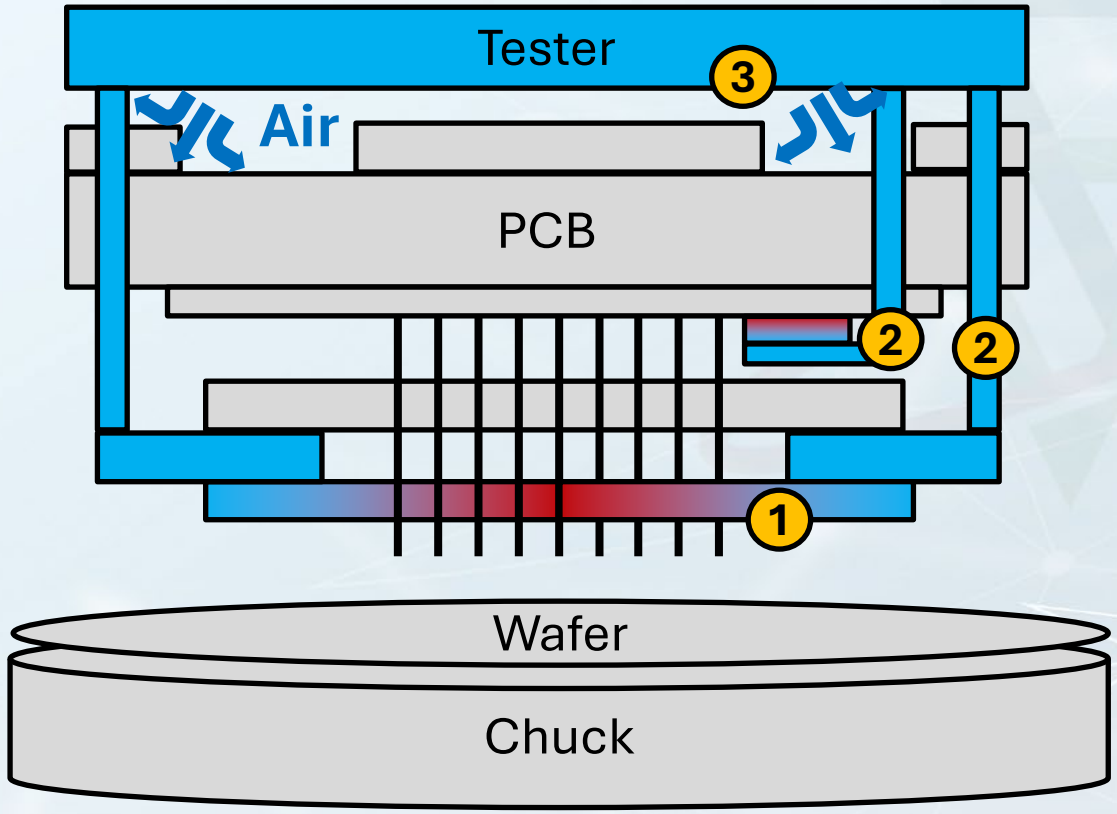
Thermal Dissipation Structure (TDS)

- To enhance the thermal dissipation, integrated structure are designed.

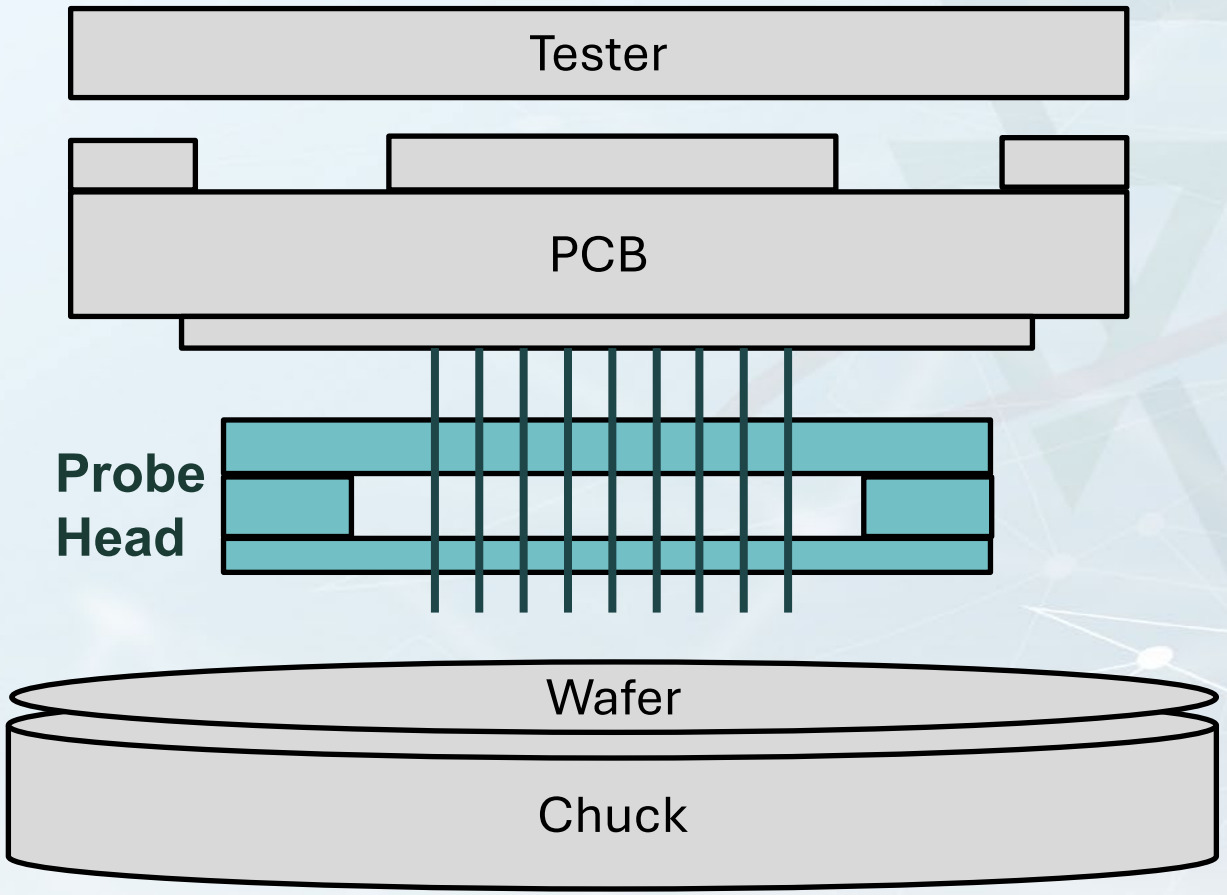


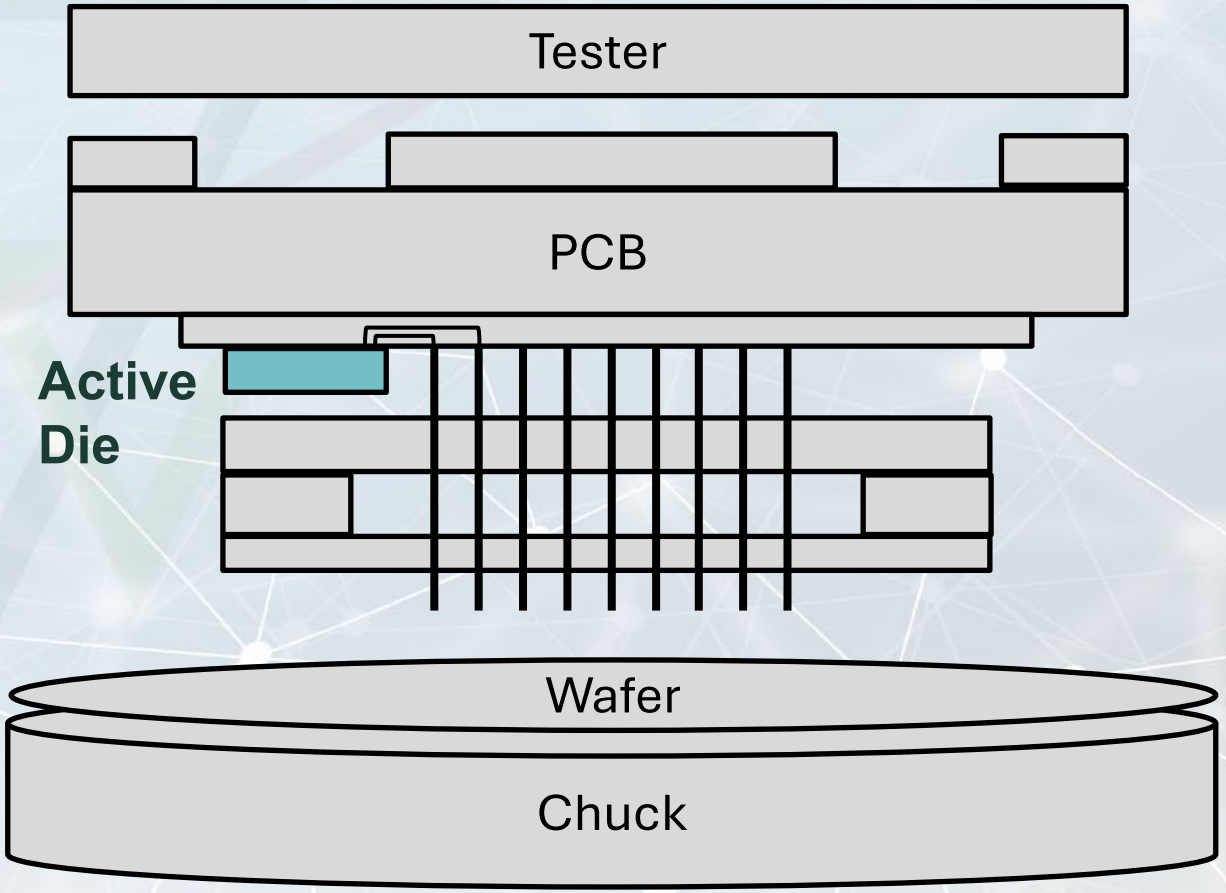
Key Structure

1. Material to improve thermal conductivity *3X*
2. Accessories to enhance thermal transfer 5X
3. Enlarge Tester air purge 4X to dissipate heat

Thermal Dissipation Structure (TDS)

- TDS Design for Key Objectives. (1) Probe Head, (2) Active Die



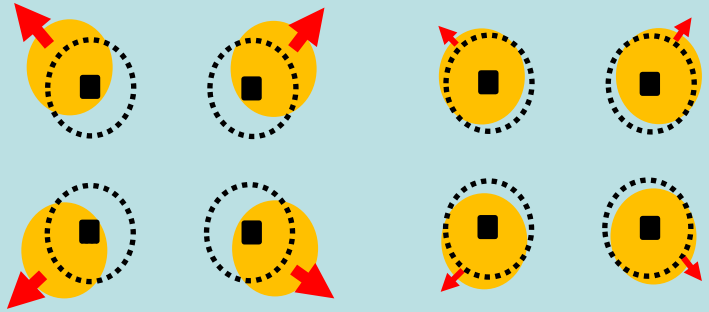


Thermal Dissipation Structure (TDS)

- **Benefits for PH Cooling.**

Decrease Equilibrium Temp

Improve Alignment due to CTE difference

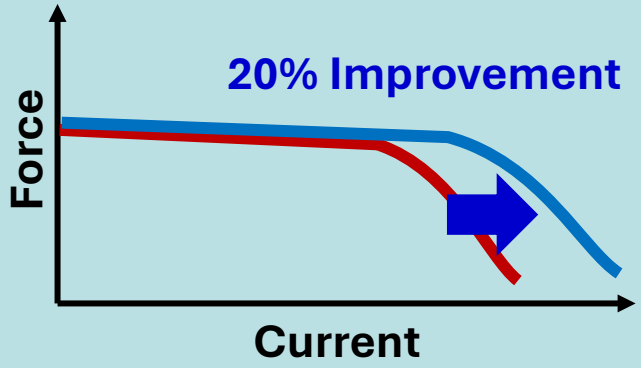


T↓, Δd ↓

(Probe to MLO pad)

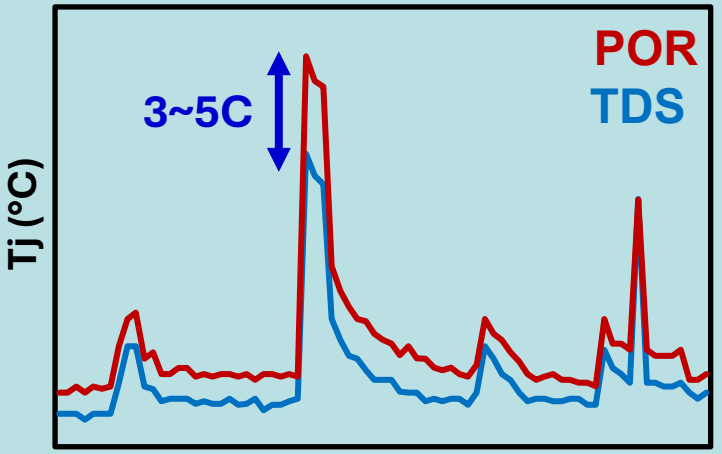
Increase Probe CCC

Avoid Tip Burnt



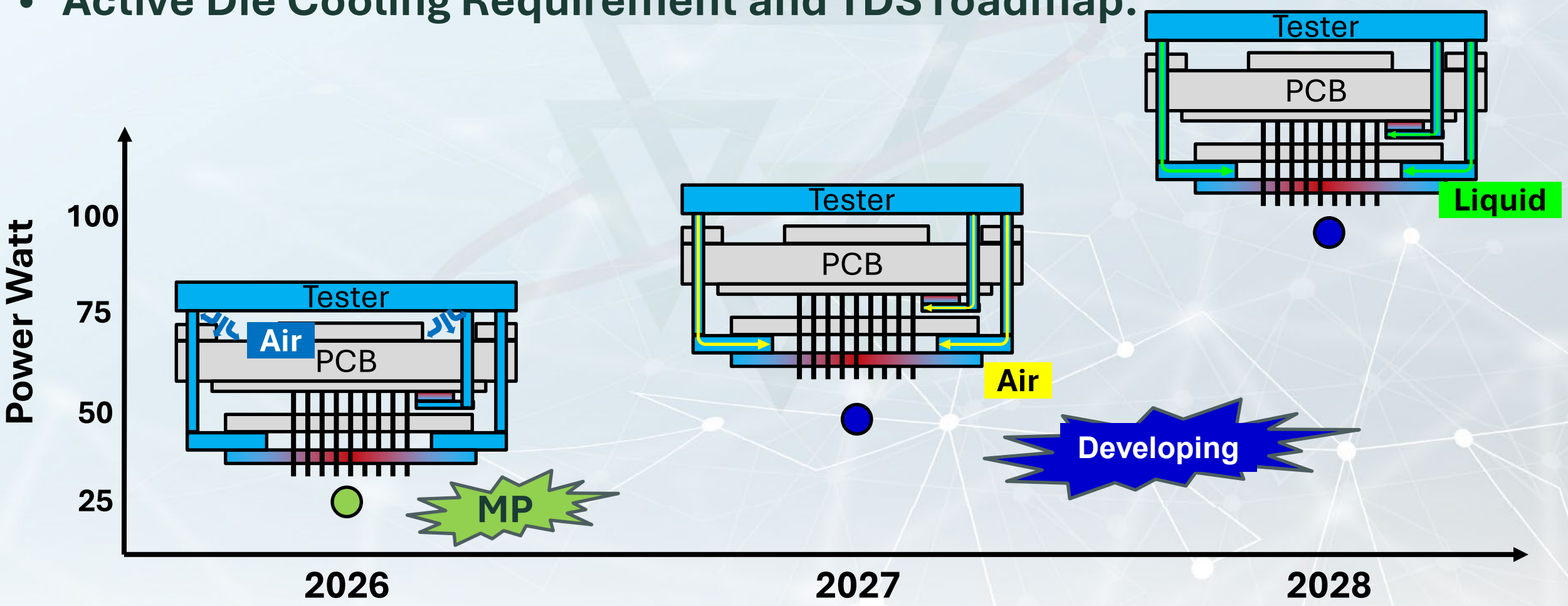
Stabilize DUT Tj

Avoid Thermal Runaway



Thermal Dissipation Structure (TDS)

- Maintain the working temperature of active die under specific temp.
- Active Die Cooling Requirement and TDS roadmap.



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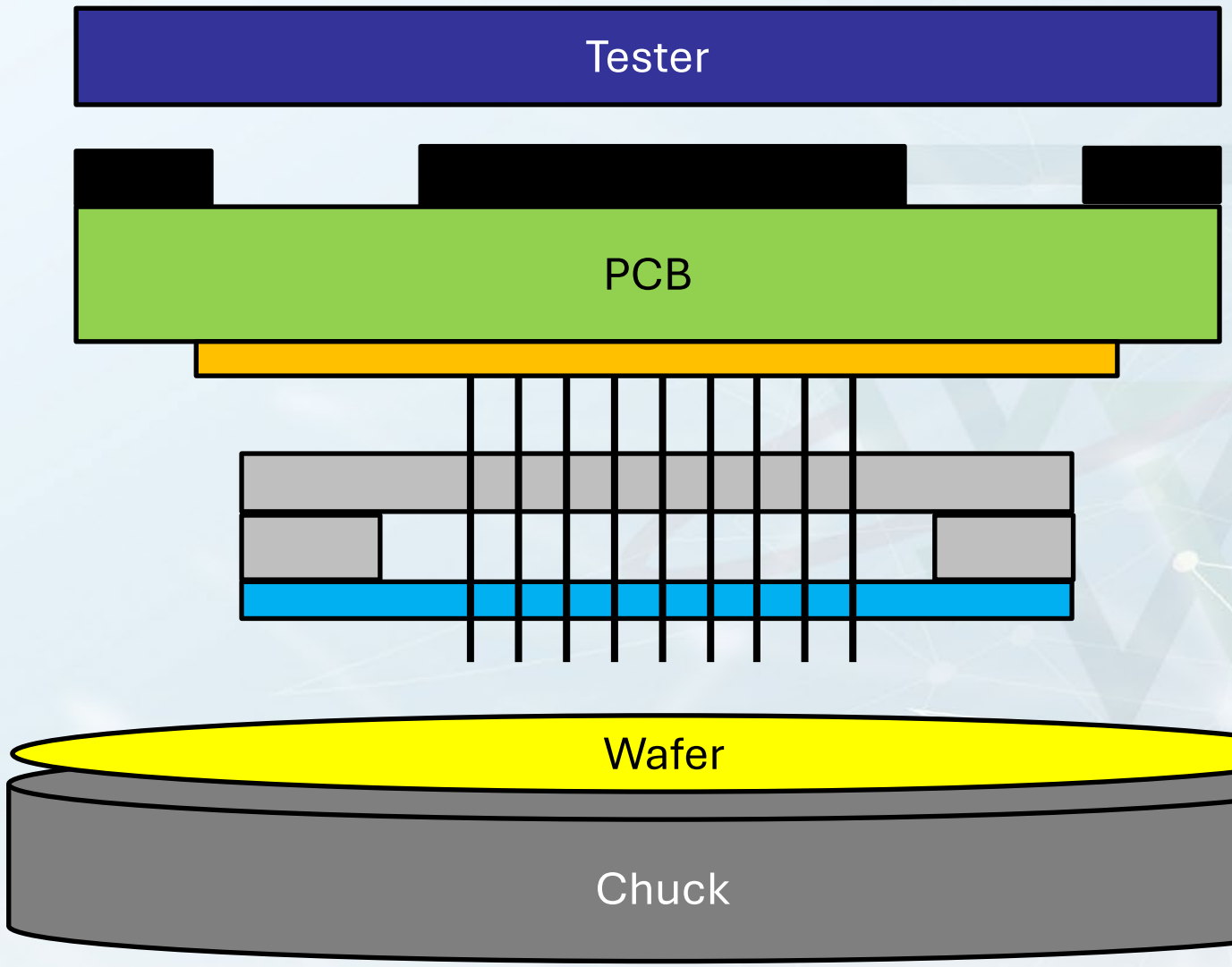

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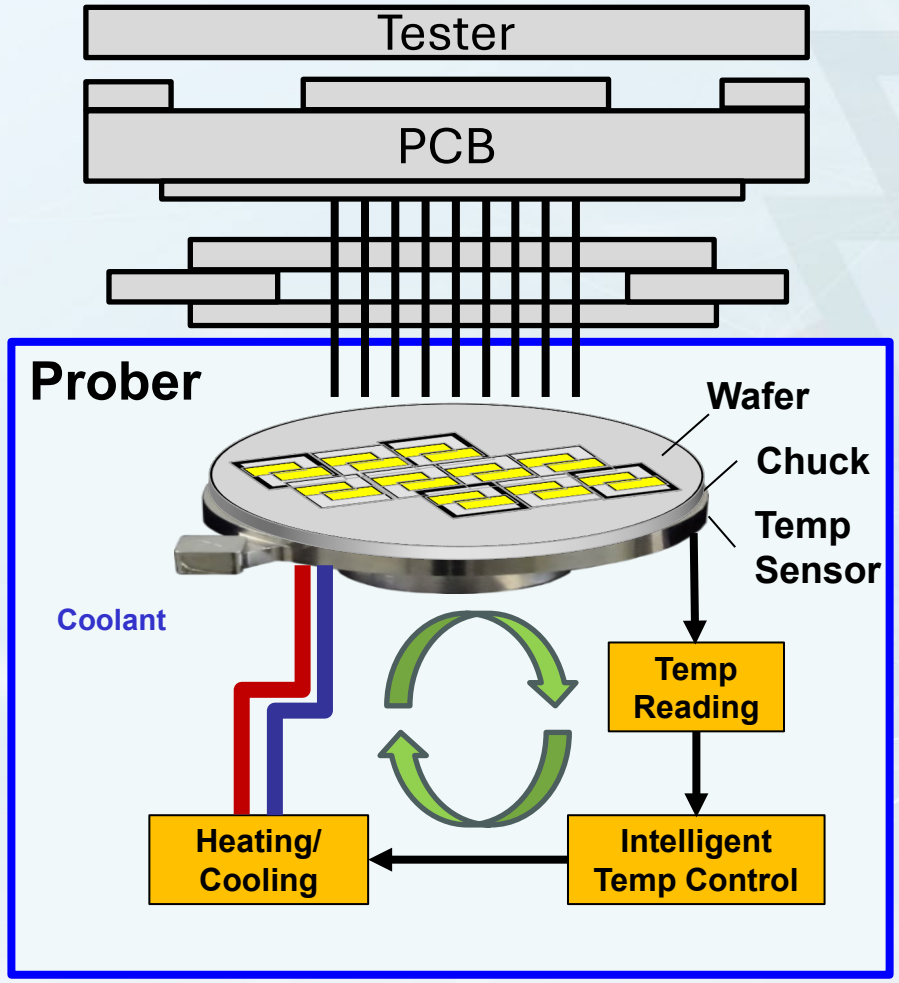
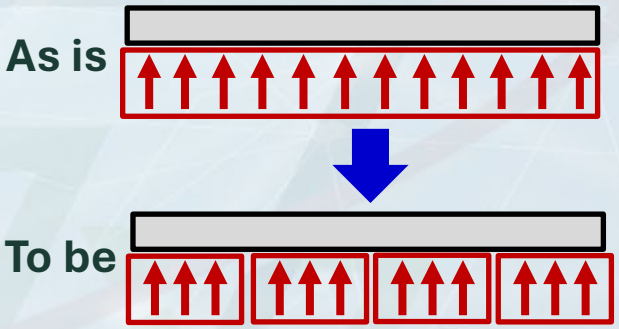
Active Temperature Control

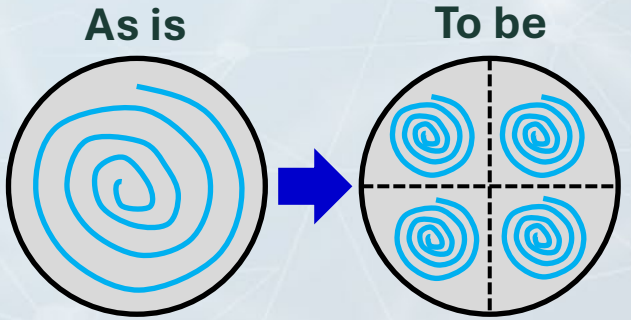
- **Integrated solution to combine H/W and S/W.**



- **Multi-Sensor and Control Zone**



Multi Heating Zone

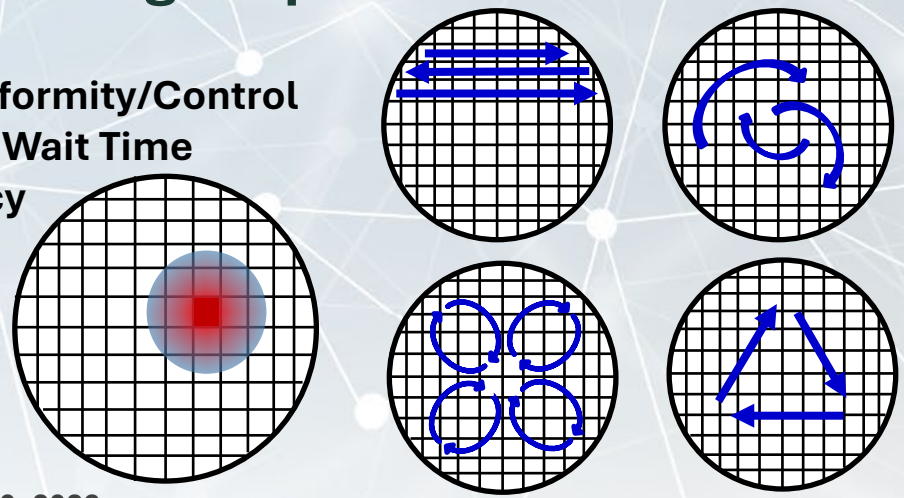


Multi Cooling Zone

- **Optimize Probing Sequence**

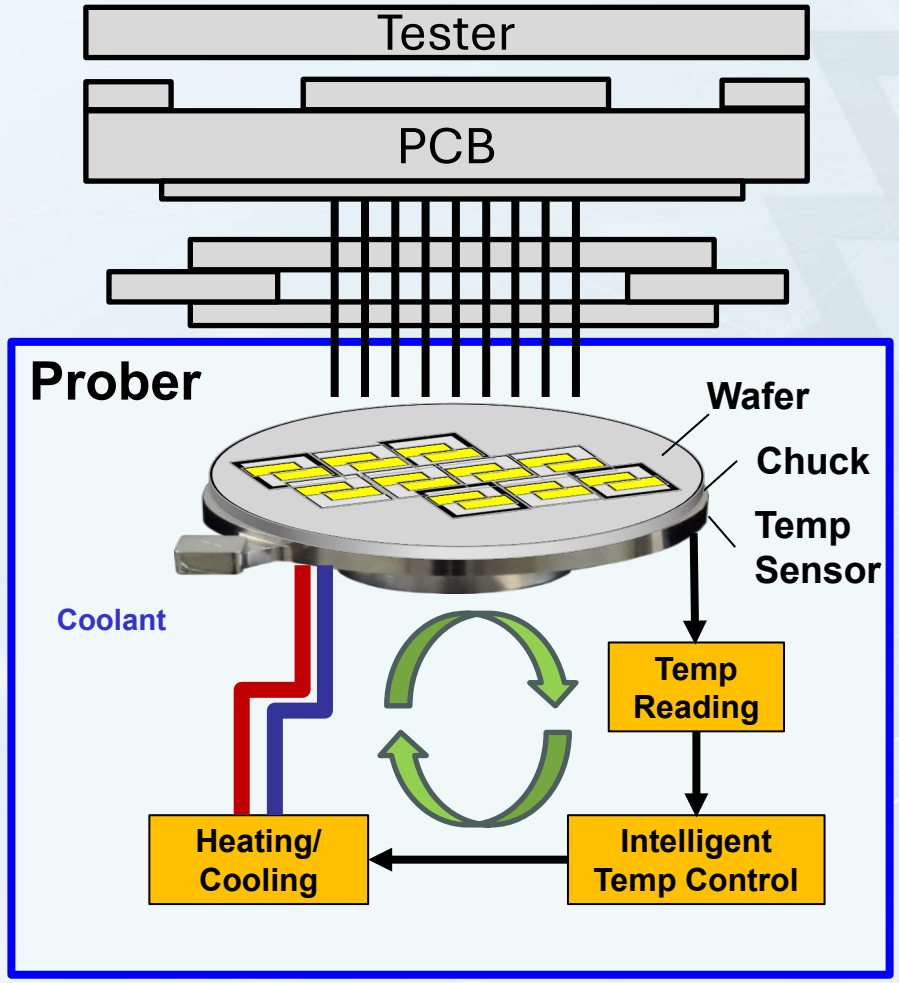
<Goal>

- Temperature Uniformity/Control
- Heating/Cooling Wait Time
- Probing Efficiency

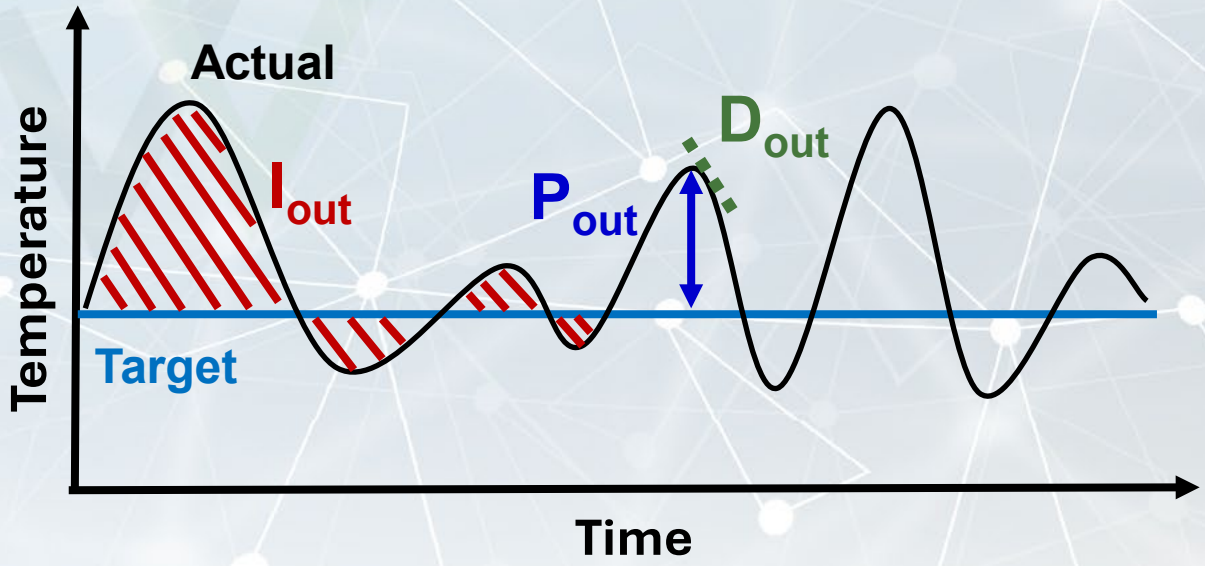


Active Temperature Control

- **Integrated solution to combine H/W and S/W.**



- **Active Temperature Control by P-I-D**
  - **Proportional (P_{out}): Adjust current error**
  - **Integral (I_{out}): Based on Past error**
  - **Derivative (D_{out}): Predict future error**



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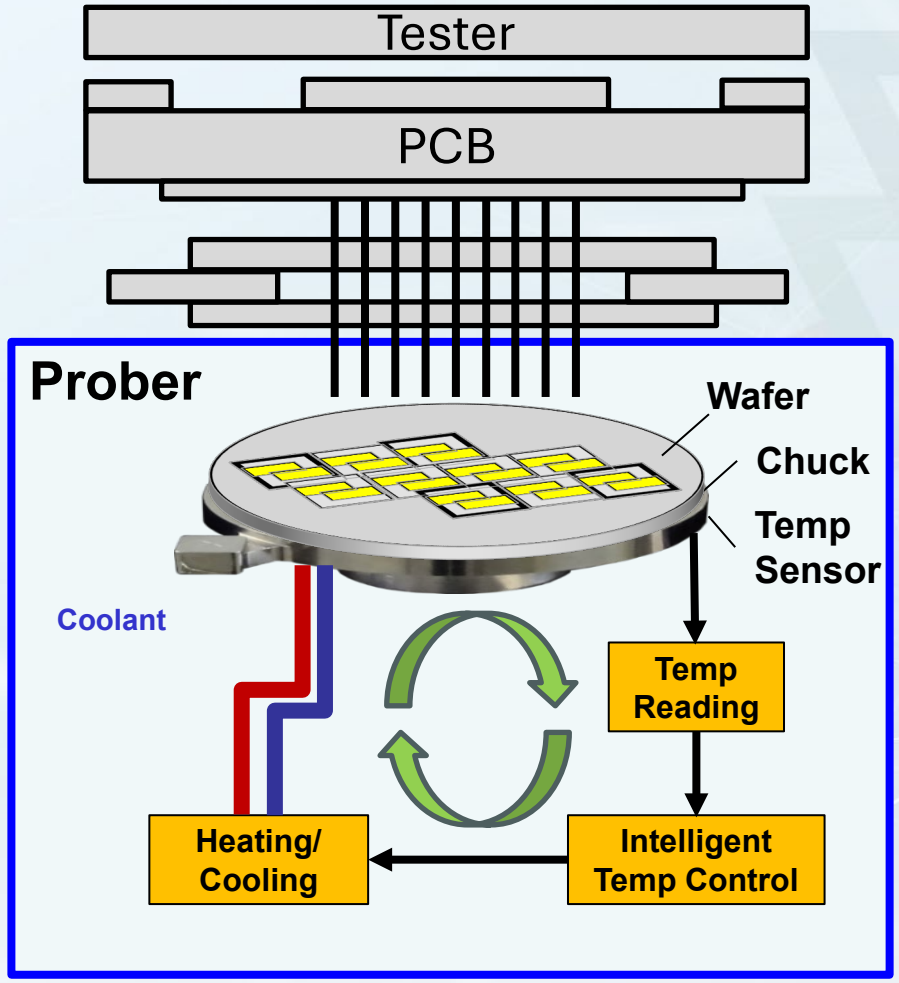

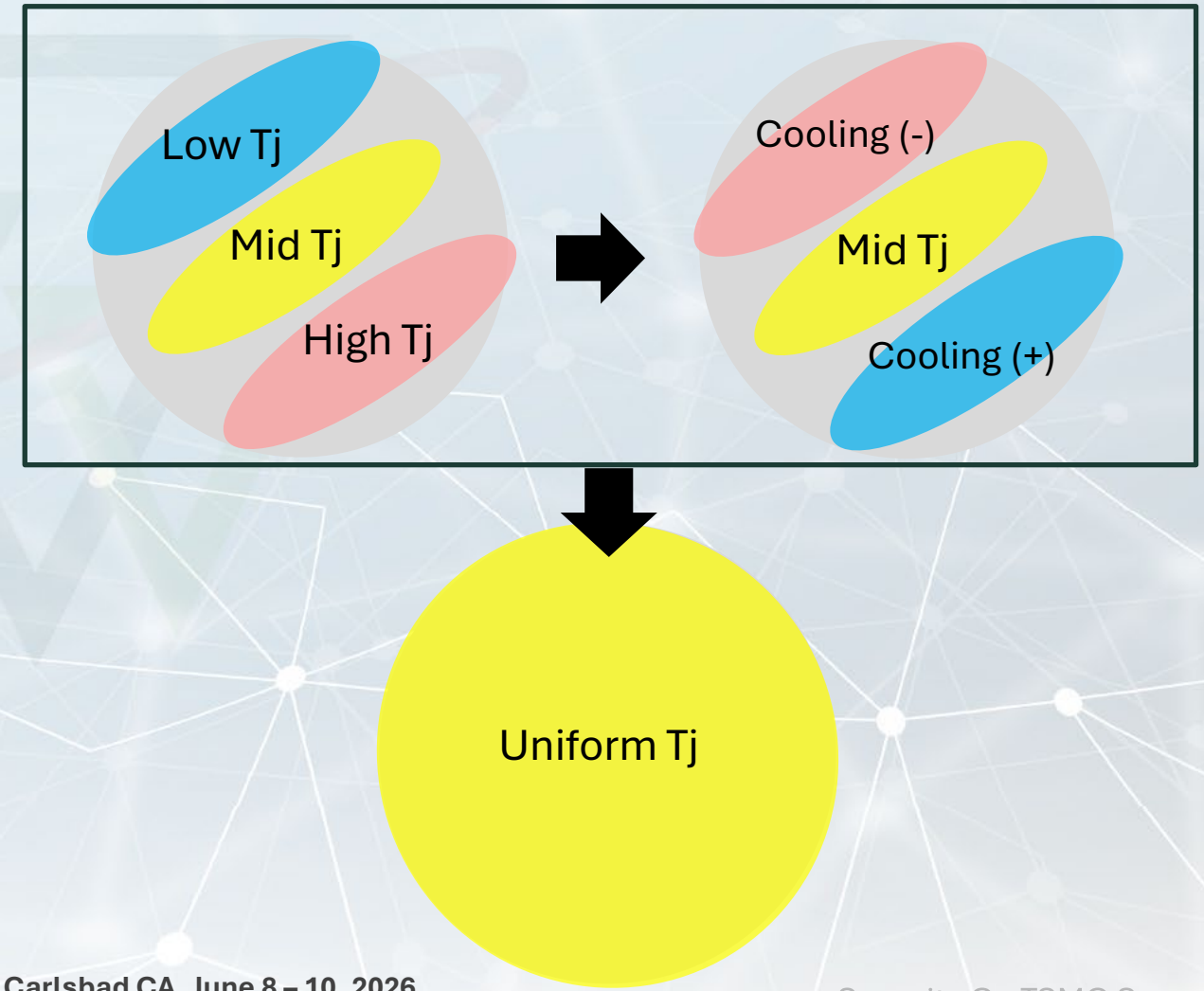

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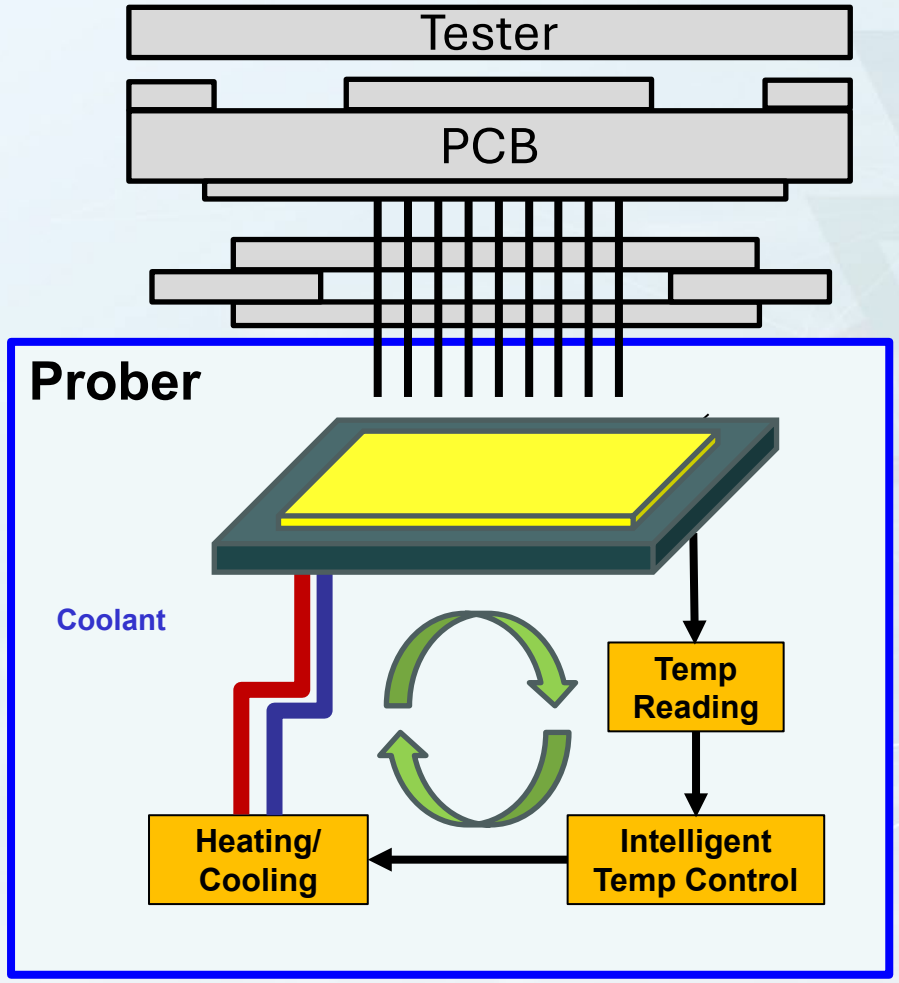

<Singulated Die Probing>

- **Chuck Capability**
  - Support Die size: ~ 100mm x 100mm
  - Multi Heating/Cooling zones
  - Power Density: >200W/cm2
- **Probing Technology**
  - Pin Count: >800K
  - Probe force control to avoid die shift

Summary

- The rapid expansion of AI technology introduces several challenges in testing, particularly in thermal management.
- To effectively manage thermal challenges, integrated solutions combining the tester, probe card, and chuck are essential.
- With successful AI chip testing, AI in turn makes us more capable and efficient.

Summary

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